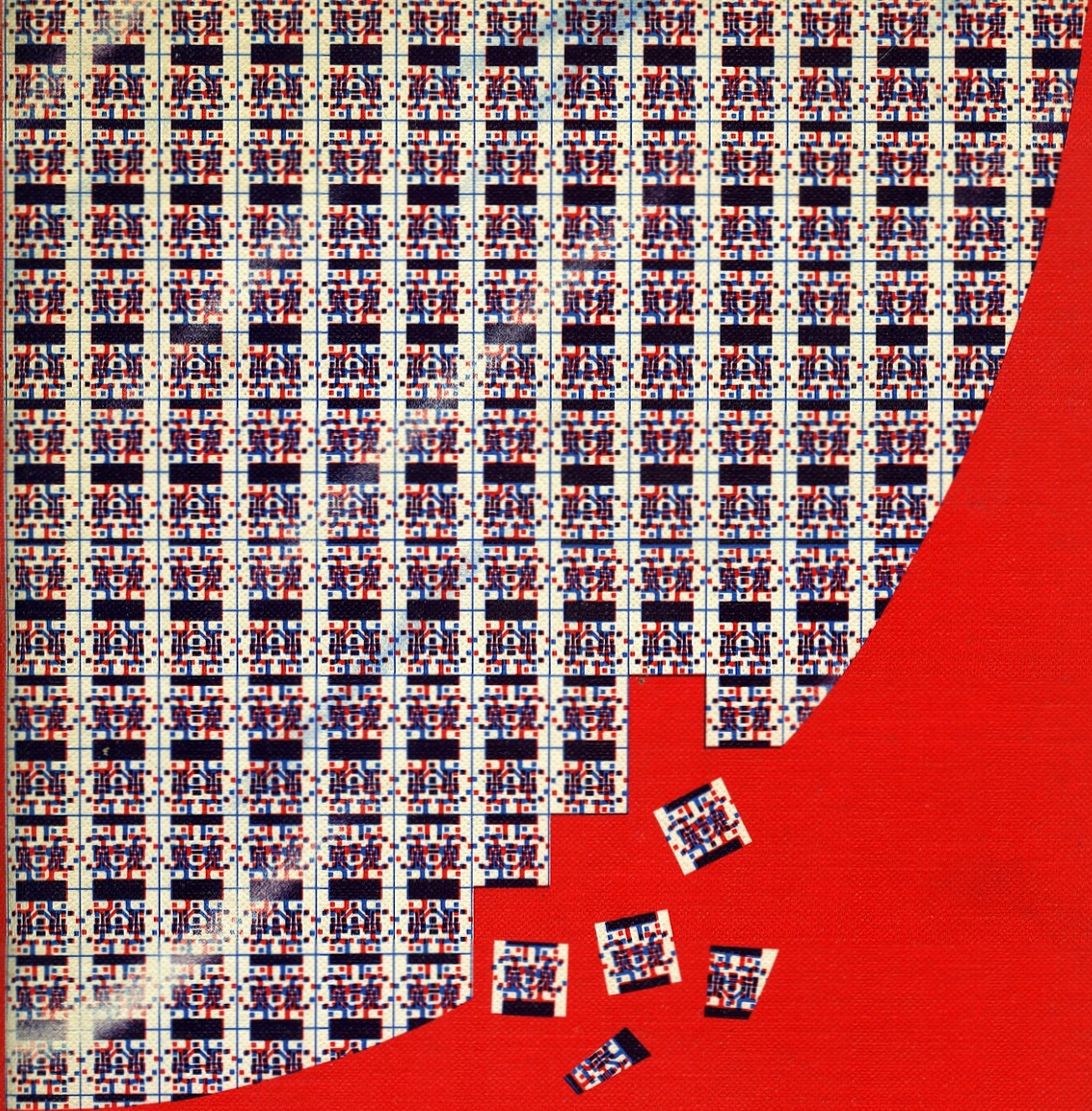


THE INTEGRATED CIRCUIT DATA BOOK

MOTOROLA Semiconductor Products Inc.

GENERAL INFORMATION

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Interchangeability Guide
Digital Circuits Applications Selector Guide

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MECL II MC1000/MC1200 Series

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COMPLEX ARRAYS

LINEAR

Application Selector Guide
Operational Amplifiers
High-Frequency Amplifiers
Power Amplifiers
Differential Amplifiers
Sense Amplifiers
Stereo Preamplifiers

APPLICATION NOTES

THE INTEGRATED CIRCUIT DATA BOOK

In the entire dynamic history of electronics, no facet of the industry has moved as rapidly from concept to implementation as has the field of integrated circuits. Already, after only 10 years of development, integrated circuits are replacing discrete-component circuits in all major computer applications and in many other digital functions as well. The linear area of applications, though somewhat lagging the digital field, is now expanding at a rate reminiscent of earlier days when new designs were emerging from the laboratories faster than they could be effectively introduced to the marketplace.

Since an integrated circuit represents a significantly larger portion of each equipment design than any single discrete component, the design engineers' cognizance of new products and their capabilities becomes increasingly vital. To the dissemination of this information, in the most useful form, the Integrated Circuit Data Book is dedicated.

This Data Book contains data sheet specifications and other applications and test data for all standard Motorola integrated circuits manufactured at the time of its publication. A complete, alpha-numeric index, page 1-1, lists and identifies all devices contained in the book and refers the reader to the proper section and page number where each device is fully characterized. Tabbed contents pages at the front and back of the book provide quick entry to the specific device section of interest.

The book covers both digital and linear integrated circuits. The digital families are subdivided as needed to group complete information for a specific logic series – data sheets and general information containing the major features and applications of that specific series. In addition, a complete "spread" of logic diagrams is included to permit quick selection of a first-order device lineup for most efficient system implementation.

The linear device section fully characterizes circuits encompassing the entire range of applications from audio to RF. A quick selection guide at the front of this section provides rapid comparison of the various circuits.

In view of the rapidly expanding technology, no book of this type can hope to remain current for any extended period of time. Therefore, the Integrated Circuit Data Book will be updated with a minimum of two supplements, as described on the following page, before the second edition of the Data Book will be published. In this way, it is hoped this effort provides a needed service that will result in significant savings of search time in the implementation of integrated circuit systems.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of semiconductor devices any license under the patent rights of any manufacturer.

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1st Edition, August 1968

DATA BOOK
UPDATING SERVICE

Because of large numbers of new integrated circuit devices introduced each year, provisions have been made to update the Integrated Circuit Data Book through the publication of Supplements. At least two supplements will be published during the year. The Supplements will contain complete data sheets for newly added Motorola devices.

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INTERCHANGEABILITY GUIDE

The following cross-reference lists integrated circuits from a number of major manufacturers, and indicates the direct replacement type. Due to the variety of packages on the market, there may be slight differences in outline dimensions.

DIGITAL INTEGRATED CIRCUITS

MECL

Part Number	Motorola Direct Replacement	Description
RCA		
CD2150F	MC1050F	Dual 4-Input OR/NOR Gate
CD2151F	MC1051F	Dual 4-Input OR/NOR Gate
CD2152F	MC1052F	Single 8-Input OR/NOR Gate
Stewart-Warner		
SW301F	MC301F	5-Input OR/NOR Gate
SW301T	MC301G	5-Input OR/NOR Gate
SW302F	MC302F	R-S Flip-Flop
SW302T	MC302G	R-S Flip-Flop
SW303F	MC303F	Half Adder
SW303T	MC303G	Half Adder
SW304F	MC304F	Bias Driver
SW304T	MC304G	Bias Driver
SW305F	MC305F	5-Input Gate Expander
SW305T	MC305G	5-Input Gate Expander
SW306F	MC306F	3-Input OR/NOR Gate
SW306T	MC306G	3-Input OR/NOR Gate
SW307F	MC307F	3-Input OR/NOR Gate
SW307T	MC307G	3-Input OR/NOR Gate
SW308F	MC308F	AC-Coupled J-K Flip-Flop
SW308T	MC308G	AC-Coupled J-K Flip-Flop
SW309F	MC309F	Dual 2-Input NOR Gate
SW309T	MC309G	Dual 2-Input NOR Gate
SW310F	MC310F	Dual 2-Input NOR Gate
SW310T	MC310G	Dual 2-Input NOR Gate
SW311F	MC311F	Dual 2-Input NOR Gate
SW311T	MC311G	Dual 2-Input NOR Gate
SW351F	MC351F	5-Input OR/NOR Gate
SW351T	MC351G	5-Input OR/NOR Gate
SW352AF	MC352AF	R-S Flip-Flop
SW352AT	MC352AG	R-S Flip-Flop
SW353F	MC353F	Half Adder
SW353T	MC353G	Half Adder
SW354F	MC354F	Bias Driver
SW354T	MC354G	Bias Driver
SW355F	MC355F	5-Input Gate Expander
SW355T	MC355G	5-Input Gate Expander
SW356F	MC356F	3-Input OR/NOR Gate
SW356T	MC356G	3-Input OR/NOR Gate
SW357F	MC357F	3-Input OR/NOR Gate
SW357T	MC357G	3-Input OR/NOR Gate
SW358AF	MC358AF	AC-Coupled J-K Flip-Flop
SW358AT	MC358AG	AC-Coupled J-K Flip-Flop
SW359F	MC359F	Dual 2-Input NOR Gate
SW359T	MC359G	Dual 2-Input NOR Gate
SW360F	MC360F	Dual 2-Input NOR Gate
SW360T	MC360G	Dual 2-Input NOR Gate
SW361F	MC361F	Dual 2-Input NOR Gate
SW361T	MC361G	Dual 2-Input NOR Gate
Westing-house		
WC377	MC1023P*	Dual 4-Input OR/NOR Clock Driver

* Not pin-for-pin replacement

MTTL

Sylvania		
SF-10-02	MC513F	R-S Flip-Flop
SF-11-02	MC563F	R-S Flip-Flop
SF-12-02	MC413F	R-S Flip-Flop
SF-13-02	MC463F	R-S Flip-Flop
SF-50-02	MC515F	AND J-K Flip-Flop
SF-51-02	MC565F	AND J-K Flip-Flop
SF-52-02	MC415F	AND J-K Flip-Flop
SF-52-P	MC415P	AND J-K Flip-Flop
SF-53-02	MC465F	AND J-K Flip-Flop
SF-53-P	MC465P	AND J-K Flip-Flop
SF-60-02	MC516F	OR J-K Flip-Flop
SF-61-02	MC566F	OR J-K Flip-Flop
SF-62-02	MC416F	OR J-K Flip-Flop
SF-62-P	MC416P	OR J-K Flip-Flop
SF-63-02	MC466F	OR J-K Flip-Flop
SF-63-P	MC466P	OR J-K Flip-Flop
SG-40-02	MC500F	Dual 4-Input NAND Gate
SG-41-02	MC550F	Dual 4-Input NAND Gate
SG-42-02	MC400F	Dual 4-Input NAND Gate
SG-42-P	MC400P	Dual 4-Input NAND Gate
SG-43-02	MC450F	Dual 4-Input NAND Gate
SG-43-P	MC450P	Dual 4-Input NAND Gate
SG-50-02	MC501F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-51-02	MC551F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-52-02	MC401F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-52-P	MC401P	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate

MTTL (cont.)

Part Number	Motorola Direct Replacement	Description
SG-53-02	MC451F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-53-P	MC451P	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-60-02	MC502F	Single 8-Input NAND Gate
SG-61-02	MC552F	Single 8-Input NAND Gate
SG-62-02	MC402F	Single 8-Input NAND Gate
SG-62-P	MC402P	Single 8-Input NAND Gate
SG-63-02	MC452F	Single 8-Input NAND Gate
SG-63-P	MC452P	Single 8-Input NAND Gate
SG-70-02	MC520F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-71-02	MC570F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-72-02	MC420F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-72-P	MC420P	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-73-02	MC470F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-73-P	MC470P	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-90-02	MC503F	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement
SG-91-02	MC553F	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement
SG-92-02	MC403F	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement
SG-93-02	MC453F	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement
SG-100-02	MC504F	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-101-02	MC554F	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-102-02	MC404F	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-102-P	MC404P	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-103-02	MC454F	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-103-P	MC454P	Expandable 3-Wide 3-Input AND-OR-INVERT Gate
SG-110-02	MC505F	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-111-02	MC555F	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-112-02	MC405F	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-112-P	MC405P	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-113-02	MC455F	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-113-P	MC455P	Expandable 2-Wide 4-Input AND-OR-INVERT Gate
SG-120-02	MC506F	Expandable 8-Input NAND Gate
SG-121-02	MC556F	Expandable 8-Input NAND Gate
SG-122-02	MC406F	Expandable 8-Input NAND Gate
SG-123-02	MC456F	Expandable 8-Input NAND Gate
SG-130-02	MC507F	Dual 4-Input Line Driver
SG-131-02	MC557F	Dual 4-Input Line Driver
SG-132-02	MC407F	Dual 4-Input Line Driver
SG-132-P	MC407P	Dual 4-Input Line Driver
SG-133-02	MC457F	Dual 4-Input Line Driver
SG-133-P	MC457P	Dual 4-Input Line Driver
SG-140-02	MC508F	Quad 2-Input NAND Gate
SG-141-02	MC558F	Quad 2-Input NAND Gate
SG-142-02	MC408F	Quad 2-Input NAND Gate
SG-142-P	MC408P	Quad 2-Input NAND Gate
SG-143-02	MC458F	Quad 2-Input NAND Gate
SG-143-P	MC458P	Quad 2-Input NAND Gate
SG-150-02	MC509F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-151-02	MC559F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-152-02	MC409F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-152-P	MC409P	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-153-02	MC459F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-153-P	MC459P	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-170-02	MC510F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-171-02	MC560F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-172-02	MC410F	Dual 4-Input Expander for AND-OR-INVERT Gates

MTTL (cont.)

Part Number	Motorola Direct Replacement	Description
SG-172-P	MC410P	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-173-02	MC460F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-173-P	MC460P	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-180-02	MC511F	Dual 4-Input Expander for NAND Gates
SG-181-02	MC561F	Dual 4-Input Expander for NAND Gates
SG-182-02	MC411F	Dual 4-Input Expander for NAND Gates
SG-183-02	MC461F	Dual 4-Input Expander for NAND Gates
SG-190-02	MC512F	Triple 3-Input NAND Gate
SG-191-02	MC562F	Triple 3-Input NAND Gate
SG-192-02	MC412F	Triple 3-Input NAND Gate
SG-192-P	MC412P	Triple 3-Input NAND Gate
SG-193-02	MC462F	Triple 3-Input NAND Gate
SG-193-P	MC462P	Triple 3-Input NAND Gate

MTTL II

Sylvania		
SF-250-02	MC2109F	AND J-K Flip-Flop
SF-251-02	MC2159F	AND J-K Flip-Flop
SF-252-02	MC2009F	AND J-K Flip-Flop
SF-253-02	MC2059F	AND J-K Flip-Flop
SF-260-02	MC2110F	OR J-K Flip-Flop
SF-261-02	MC2160F	OR J-K Flip-Flop
SF-262-02	MC2010F	OR J-K Flip-Flop
SF-263-02	MC2060F	OR J-K Flip-Flop
SG-210-02	MC2100F	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-211-02	MC2150F	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-212-02	MC2000F	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-212-P	MC2000P	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-213-02	MC2050F	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-213-P	MC2050P	Expandable 2-Wide 4-Input AND-OR INVERT Gate
SG-220-02	MC2101F	Quad 2-Input NAND Gate
SG-221-02	MC2151F	Quad 2-Input NAND Gate
SG-222-02	MC2001F	Quad 2-Input NAND Gate
SG-222-P	MC2001P	Quad 2-Input NAND Gate
SG-223-02	MC2051F	Quad 2-Input NAND Gate
SG-223-P	MC2051P	Quad 2-Input NAND Gate

Part Number	Motorola Direct Replacement	Description
SG-230-02	MC2102F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-231-02	MC2152F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-232-02	MC2002F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-232-P	MC2002P	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-233-02	MC2052F	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-233-P	MC2052P	4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates
SG-240-02	MC2103F	Dual 4-Input NAND Gate
SG-241-02	MC2153F	Dual 4-Input NAND Gate
SG-242-02	MC2003F	Dual 4-Input NAND Gate
SG-242-P	MC2003P	Dual 4-Input NAND Gate
SG-243-02	MC2053F	Dual 4-Input NAND Gate
SG-243-P	MC2053P	Dual 4-Input NAND Gate
SG-250-02	MC2104F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-251-02	MC2154F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-252-02	MC2004F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-252-P	MC2004P	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-253-02	MC2054F	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-253-P	MC2054P	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate
SG-260-02	MC2105F	Single 8-Input NAND Gate
SG-261-02	MC2155F	Single 8-Input NAND Gate
SG-262-02	MC2005F	Single 8-Input NAND Gate
SG-262-P	MC2005P	Single 8-Input NAND Gate
SG-263-02	MC2055F	Single 8-Input NAND Gate
SG-263-P	MC2055P	Single 8-Input NAND Gate
SG-270-02	MC2106F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-271-02	MC2156F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-272-02	MC2006F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-272-P	MC2006P	Dual 4-Input Expander for AND-OR-INVERT Gates

MTTL II (cont.)

Part Number	Motorola Direct Replacement	Description
SG-273-02	MC2056F	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-273-P	MC2056P	Dual 4-Input Expander for AND-OR-INVERT Gates
SG-310-02	MC2113F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-311-02	MC2163F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-312-02	MC2013F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-312-P	MC2013P	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-313-02	MC2063F	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate
SG-313-P	MC2063P	Dual Expandable 2-Wide, 2-Input AND-OR-INVERT Gate

MDTL

Fairchild		
U3I909351X	MC953F	Dual J-K Flip-Flop
U3I909359X	MC853F	Dual J-K Flip-Flop
U3I909451X	MC956F	Dual J-K Flip-Flop
U3I909459X	MC856F	Dual J-K Flip-Flop
U3I909751X	MC955F	Dual J-K Flip-Flop
U3I909759X	MC855F	Dual J-K Flip-Flop
U3I909951X	MC952F	Dual J-K Flip-Flop
U3I909959X	MC852F	Dual J-K Flip-Flop
U3I993051X	MC930F	Dual 4-Input NAND Gate
U3I993059X	MC830F	Dual 4-Input NAND Gate
U3I993151X	MC931F	Clocked Flip-Flop
U3I993159X	MC831F	Clocked Flip-Flop
U3I993251X	MC932F	Dual 4-Input Buffer
U3I993259X	MC832F	Dual 4-Input Buffer
U3I993351X	MC933F	Dual 4-Input Expander
U3I993359X	MC833F	Dual 4-Input Expander
U3I993651X	MC936F	Hex Inverter
U3I993659X	MC836F	Hex Inverter
U3I993751X	MC937F	Hex Inverter
U3I993759X	MC837F	Hex Inverter
U3I994451X	MC944F	Dual 4-Input Power NAND Gate
U3I994459X	MC844F	Dual 4-Input Power NAND Gate
U3I994551X	MC945F	Clocked Flip-Flop
U3I994559X	MC845F	Clocked Flip-Flop
U3I994651X	MC946F	Quad 2-Input NAND Gate
U3I994659X	MC846F	Quad 2-Input NAND Gate
U3I994851X	MC948F	Clocked Flip-Flop
U3I994859X	MC848F	Clocked Flip-Flop
U3I994951X	MC949F	Quad 2-Input NAND Gate with 2 k Pullup Resistor
U3I994959X	MC849F	Quad 2-Input NAND Gate with 2 k Pullup Resistor
U3I995051X	MC950F	Pulse Triggered Binary
U3I995059X	MC850F	Pulse Triggered Binary
U3I995151X	MC951F	Monostable Multivibrator
U3I995159X	MC851F	Monostable Multivibrator
U3I996151X	MC961F	Dual 4-Input NAND Gate with 2 k Pullup Resistor
U3I996159X	MC861F	Dual 4-Input NAND Gate with 2 k Pullup Resistor
U3I996251X	MC962F	Triple 3-Input NAND Gate
U3I996259X	MC862F	Triple 3-Input NAND Gate
U3I996351X	MC963F	Triple 3-Input NAND Gate with 2 k Pullup Resistor
U3I996359X	MC863F	Triple 3-Input NAND Gate with 2k Pullup Resistor
U5F993051X	MC930G	Dual 3-2 Input NAND Gate
U5F993059X	MC830G	Dual 3-2 Input NAND Gate
U5F993151X	MC931G	Clocked Flip-Flop
U5F993159X	MC831G	Clocked Flip-Flop
U5F993251X	MC932G	Dual 3-2 Input Buffer
U5F993259X	MC832G	Dual 3-2 Input Buffer
U5F993351X	MC933G	Dual 4-3 Input Expander
U5F993359X	MC833G	Dual 4-3 Input Expander
U5F994451X	MC944G	Dual 3-2 Input Power NAND Gate
U5F994459X	MC844G	Dual 3-2 Input Power NAND Gate
U5F994551X	MC945G	Clocked Flip-Flop
U5F994559X	MC845G	Clocked Flip-Flop
U5F994651X	MC946G	Quad Inverter
U5F994659X	MC846G	Quad Inverter
U5F994851X	MC948G	Clocked Flip-Flop
U5F994859X	MC848G	Clocked Flip-Flop
U5F994951X	MC949G	Quad Inverter with 2 k Pullup Resistor
U5F994959X	MC849G	Quad Inverter with 2 k Pullup Resistor
U5F995051X	MC950G	Pulse Triggered Binary
U5F995059X	MC850G	Pulse Triggered Binary
U5F995151X	MC951G	Monostable Multivibrator
U5F995159X	MC851G	Monostable Multivibrator
U5F996151X	MC961G	Dual 3-2 Input NAND Gate with 2 k Pullup Resistor
U5F996159X	MC861G	Dual 3-2 Input NAND Gate with 2 k Pullup Resistor
U5F996251X	MC962G	Dual 2-Input NAND Gate Plus Inverter
U5F996259X	MC862G	Dual 2-Input NAND Gate Plus Inverter
U5F996351X	MC963G	Dual 2-Input NAND Gate Plus Inverter
U5F996359X	MC863G	Dual 2-Input NAND Gate Plus Inverter
U6A909359X	MC853P	Dual J-K Flip-Flop
U6A909459X	MC856P	Dual J-K Flip-Flop
U6A909759X	MC855P	Dual J-K Flip-Flop
U6A909959X	MC852P	Dual J-K Flip-Flop
U6A993059X	MC830P	Dual 4-Input NAND Gate
U6A993159X	MC831P	Clocked Flip-Flop
U6A993259X	MC832P	Dual 4-Input Buffer
U6A993359X	MC833P	Dual 4-Input Gate Expander

MDTL (cont.)

Part Number	Motorola Direct Replacement	Description
U6A993659X	MC836P	Hex Inverter
U6A993759X	MC837P	Hex Inverter
U6A994459X	MC844P	Dual 4-Input Power NAND Gate
U6A994559X	MC845P	Clocked Flip-Flop
U6A994659X	MC846P	Quad 2-Input NAND Gate
U6A994859X	MC848P	Clocked Flip-Flop
U6A994959X	MC849P	Quad 2-Input NAND Gate with 2 k Pullup Resistor
U6A995059X	MC850P	Pulse Triggered Binary
U6A995159X	MC851P	Monostable Multivibrator
U6A996159X	MC861P	Dual 4-Input NAND Gate 2 k Pullup Resistor
U6A996259X	MC862P	Triple 3-Input NAND Gate
U6A996359X	MC863P	Triple 3-Input NAND Gate with 2 k Pullup Resistor
ITT		
MIC930-1B	MC930F	Dual 4-Input Gate
MIC930-1C	MC930G	Dual 3-2 Input Gate
MIC930-5B	MC830F	Dual 4-Input Gate
MIC930-5C	MC830G	Dual 3-2 Input Gate
MIC932-1B	MC932F	Dual 4-Input Buffer
MIC932-1C	MC932G	Dual 3-2 Input Buffer
MIC932-5B	MC832F	Dual 4-Input Buffer
MIC932-5C	MC832G	Dual 3-2 Input Buffer
MIC933-1B	MC933F	Dual 4-Input Expander
MIC933-1C	MC933G	Dual 4-3 Input Expander
MIC933-5B	MC833F	Dual 4-Input Expander
MIC933-5C	MC833G	Dual 4-3 Input Expander
MIC936-1B	MC936F	Hex Inverter
MIC936-5B	MC836F	Hex Inverter
MIC937-1B	MC937F	Hex Inverter
MIC937-5B	MC837F	Hex Inverter
MIC944-1B	MC944F	Dual 4-Input Power Gate
MIC944-1C	MC944G	Dual 3-2 Input Power Gate
MIC944-5B	MC844F	Dual 4-Input Power Gate
MIC944-5C	MC844G	Dual 3-2 Input Power Gate
MIC945-1B	MC945F	Clocked Flip-Flop
MIC945-1C	MC945G	Clocked Flip-Flop
MIC945-5B	MC845F	Clocked Flip-Flop
MIC945-5C	MC845G	Clocked Flip-Flop
MIC946-1B	MC946F	Quad 2-Input Gate
MIC946-5B	MC846F	Quad 2-Input Gate
MIC948-1B	MC948F	Clocked Flip-Flop
MIC948-1C	MC948G	Clocked Flip-Flop
MIC948-5B	MC848F	Clocked Flip-Flop
MIC948-5C	MC848G	Clocked Flip-Flop
MIC949-1B	MC949F	Quad 2-Input Gate
MIC949-5B	MC849F	Quad 2-Input Gate
MIC950-1B	MC950F	Pulse Triggered Binary
MIC950-1C	MC950G	Pulse Triggered Binary
MIC950-5B	MC850F	Pulse Triggered Binary
MIC950-5C	MC850G	Pulse Triggered Binary
MIC951-1B	MC951F	Monostable Multivibrator
MIC951-1C	MC951G	Monostable Multivibrator
MIC951-5B	MC851F	Monostable Multivibrator
MIC951-5C	MC851G	Monostable Multivibrator
MIC961-1B	MC961F	Dual 4-Input Gate
MIC961-1C	MC961G	Dual 3-2 Input Gate
MIC961-5B	MC861F	Dual 4-Input Gate
MIC961-5C	MC861G	Dual 3-2 Input Gate
MIC962-1B	MC962F	Triple 3-Input Gate
MIC962-5B	MC862F	Triple 3-Input Gate
MIC963-1B	MC963F	Triple 3-Input Gate
MIC963-5B	MC863F	Triple 3-Input Gate
Philco		
PE9930	MC830P	Dual 4-Input NAND Gate
PE9932	MC832P	Dual 4-Input Buffer
PE9933	MC833P	Dual 4-Input Gate Expander
PE9944	MC844P	Dual 4-Input Power NAND Gate
PE9945	MC845P	Clocked Flip-Flop
PE9946	MC846P	Quad 2-Input NAND Gate
PE9948	MC848P	Clocked Flip-Flop
PE9962	MC862P	Triple 3-Input NAND Gate
PL9930 51	MC930F	Dual 4-Input NAND Gate
PL9930 59	MC830F	Dual 4-Input NAND Gate
PL9931 51	MC931F	Clocked Flip-Flop
PL9931 59	MC831F	Clocked Flip-Flop
PL9932 51	MC932F	Dual 4-Input Buffer
PL9932 59	MC832F	Dual 4-Input Buffer
PL9933 51	MC933F	Dual 4-Input Expander
PL9933 59	MC833F	Dual 4-Input Expander
PL9936 51	MC936F	Hex Inverter
PL9936 59	MC836F	Hex Inverter
PL9944 51	MC944F	Dual 4-Input Power NAND Gate
PL9944 59	MC844F	Dual 4-Input Power NAND Gate
PL9945 51	MC945F	Clocked Flip-Flop
PL9945 59	MC845F	Clocked Flip-Flop
PL9946 51	MC946F	Quad 2-Input NAND Gate
PL9946 59	MC846F	Quad 2-Input NAND Gate
PL9948 51	MC948F	Clocked Flip-Flop
PL9948 59	MC848F	Clocked Flip-Flop
PL9950 51	MC950F	Pulse Triggered Binary
PL9950 59	MC850F	Pulse Triggered Binary
PL9951 51	MC951F	Monostable Multivibrator
PL9951 59	MC851F	Monostable Multivibrator
PL9962 51	MC962F	Triple 3-Input NAND Gate
PL9962 59	MC862F	Triple 3-Input NAND Gate
RCA		
CD2300/930	MC930F	Dual 4-Input Gate
CD2300E/830	MC830P	Dual 4-Input Gate
CD2301/961	MC961F	Dual 4-Input Gate
CD2301E/861	MC861P	Dual 4-Input Gate
CD2302/946	MC946F	Quad 2-Input Gate
CD2302E/846	MC846P	Quad 2-Input Gate
CD2303/949	MC949F	Quad 2-Input Gate

MDTL (cont.)

Part Number	Motorola Direct Replacement	Description
CD2303E/849	MC849P	Quad 2-Input Gate
CD2304/945	MC945F	Clocked Flip-Flop
CD2304E/845	MC845P	Clocked Flip-Flop
CD2305/948	MC948F	Clocked Flip-Flop
CD2305E/848	MC848P	Clocked Flip-Flop
CD2306/932	MC932F	Dual 4-Input Buffer
CD2306E/832	MC832P	Dual 4-Input Buffer
CD2307/944	MC944F	Dual 4-Input Power Gate
CD2307E/844	MC844P	Dual 4-Input Power Gate
CD2308/962	MC962F	Triple 3-Input Gate
CD2308E/862	MC862P	Triple 3-Input Gate
CD2309/963	MC963F	Triple 3-Input Gate
CD2309E/863	MC863P	Triple 3-Input Gate
CD2310/936	MC936F	Hex Inverter
CD2310E/836	MC836P	Hex Inverter
CD2311/937	MC937F	Hex Inverter
CD2311E/837	MC837P	Hex Inverter
CD2314/933	MC933F	Dual 4-Input Expander
CD2314E/833	MC833P	Dual 4-Input Expander
Raytheon		
RC930J	MC830F	Dual 4-Input NAND Gate
RC930T	MC830G	Dual 3-2 Input NAND Gate
RC932J	MC832F	Dual 4-Input Buffer
RC932T	MC832G	Dual 3-2 Input Buffer
RC933J	MC833F	Dual 4-Input Expander
RC933T	MC833G	Dual 4-3 Input Expander
RC944J	MC844F	Dual 4-Input Power NAND Gate
RC944T	MC844G	Dual 3-2 Input Power NAND Gate
RC945J	MC845F	Clocked Flip-Flop
RC945T	MC845G	Clocked Flip-Flop
RC946J	MC846F	Quad 2-Input NAND Gate
RC946T	MC846G	Quad Inverter
RC948G	MC848F	Clocked Flip-Flop
RC948T	MC848G	Clocked Flip-Flop
RC950J	MC850F	Pulse Triggered Binary
RC950T	MC850G	Pulse Triggered Binary
RC951J	MC851F	Monostable Multivibrator
RC951T	MC851G	Monostable Multivibrator
RC962J	MC862F	Triple 3-Input NAND Gate
RC962T	MC862G	Dual 2-Input NAND Gate Plus Inverter
RC993J	MC853F	Dual J-K Flip-Flop
RC994J	MC856F	Dual J-K Flip-Flop
RC997J	MC855F	Dual J-K Flip-Flop
RC999J	MC852F	Dual J-K Flip-Flop
RM930J	MC930F	Dual 4-Input NAND Gate
RM930T	MC930G	Dual 3-2 Input NAND Gate
RM932J	MC932F	Dual 4-Input Buffer
RM932T	MC932G	Dual 3-2 Input Buffer
RM933J	MC933F	Dual 4-Input Gate Expander
RM933T	MC933G	Dual 4-3 Input Expander
RM944J	MC944F	Dual 4-Input Power NAND Gate
RM944T	MC944G	Dual 3-2 Input Power NAND Gate

Part Number	Motorola Direct Replacement	Description
RM945J	MC945F	Clocked Flip-Flop
RM945T	MC945G	Clocked Flip-Flop
RM946J	MC946F	Quad 2-Input NAND Gate
RM946T	MC946G	Quad Inverter
RM948J	MC948F	Clocked Flip-Flop
RM948T	MC948G	Clocked Flip-Flop
RM950J	MC950F	Pulse Triggered Binary
RM950T	MC950G	Pulse Triggered Binary
RM951J	MC951F	Monostable Multivibrator
RM951T	MC951G	Monostable Multivibrator
RM962J	MC962F	Triple 3-Input NAND Gate
RM962T	MC962G	Dual 2-Input NAND Gate plus Inverter
RM993J	MC953F	Dual J-K Flip-Flop
RM994J	MC956F	Dual J-K Flip-Flop
RM997J	MC955F	Dual J-K Flip-Flop
RM999J	MC952F	Dual J-K Flip-Flop
Stewart Warner		
SW705-1F	MC953F	Dual J-K Flip-Flop
SW705-2F	MC853F	Dual J-K Flip-Flop
SW706-1F	MC952F	Dual J-K Flip-Flop
SW706-2F	MC852F	Dual J-K Flip-Flop
SW708-1F	MC956F	Dual J-K Flip-Flop
SW708-2F	MC856F	Dual J-K Flip-Flop
SW709-1F	MC955F	Dual J-K Flip-Flop
SW709-2F	MC855F	Dual J-K Flip-Flop
SW930-1F	MC930F	Dual 4-Input Gate
SW930-1T	MC930G	Dual 3-2 Input Gate
SW930-2F	MC830F	Dual 4-Input Gate
SW930-2T	MC830G	Dual 3-2 Input Gate
SW932-1F	MC932F	Dual 4-Input Buffer
SW932-1T	MC932G	Dual 3-2 Input Buffer
SW932-2F	MC832F	Dual 4-Input Buffer
SW932-2T	MC832G	Dual 3-2 Input Buffer
SW933-1F	MC933F	Dual 4-Input Expander
SW933-1T	MC933G	Dual 4-3 Input Expander
SW933-2F	MC833F	Dual 4-Input Expander
SW933-2T	MC833G	Dual 4-3 Input Expander
SW936-1F	MC936F	Hex Inverter
SW936-2F	MC836F	Hex Inverter
SW937-1F	MC937F	Hex Inverter
SW937-2F	MC837F	Hex Inverter
SW944-1F	MC944F	Dual 4-Input Power Gate
SW944-1T	MC944G	Dual 3-2 Input Power Gate
SW944-2F	MC844F	Dual 4-Input Power Gate
SW944-2T	MC844G	Dual 3-2 Input Power Gate
SW945-1F	MC945F	Clocked Flip-Flop
SW945-1T	MC945G	Clocked Flip-Flop
SW945-2F	MC845F	Clocked Flip-Flop
SW945-2T	MC845G	Clocked Flip-Flop
SW946-1F	MC946F	Quad 2-Input Gate
SW946-1T	MC946G	Quad Inverter
SW946-2F	MC846F	Quad 2-Input Gate
SW946-2T	MC846G	Quad Inverter
SW948-1F	MC948F	Clocked Flip-Flop
SW948-1T	MC948G	Clocked Flip-Flop

MDTL (cont.)

Part Number	Motorola Direct Replacement	Description
SW948-2F	MC848F	Clocked Flip-Flop
SW948-2T	MC848G	Clocked Flip-Flop
SW949-1F	MC949F	Quad 2-Input Gate
SW949-1T	MC949G	Quad Inverter
SW949-2F	MC849F	Quad 2-Input Gate
SW949-2T	MC849G	Quad Inverter
SW950-1F	MC950F	Pulse Triggered Binary
SW950-1T	MC950G	Pulse Triggered Binary
SW950-2F	MC850F	Pulse Triggered Binary
SW950-2T	MC850G	Pulse Triggered Binary
SW951-1F	MC951F	Monostable Multivibrator
SW951-1T	MC951G	Monostable Multivibrator
SW951-2F	MC851F	Monostable Multivibrator
SW951-2T	MC851G	Monostable Multivibrator
SW961-1F	MC961F	Dual 4-Input Gate
SW961-1T	MC961G	Dual 3-2 Input Gate
SW961-2F	MC861F	Dual 4-Input Gate
SW961-2T	MC861G	Dual 3-2 Input Gate
SW962-1F	MC962F	Triple 3-Input Gate
SW962-1T	MC962G	Dual 2-Input Gate Plus Inverter
SW962-2F	MC862F	Triple 3-Input Gate
SW962-2T	MC862G	Dual 2 Input Gate Plus Inverter
SW963-1F	MC963F	Triple 3-Input Gate
SW963-1T	MC963G	Dual 2-Input Gate Plus Inverter
SW963-2F	MC863F	Triple 3-Input Gate
SW963-2T	MC863G	Dual 2-Input Gate Plus Inverter
Sylvania		
S9301-02	MC930F	Dual 4-Input NAND Gate
S9303-02	MC830F	Dual 4-Input NAND Gate
S9311-02	MC931F	Clocked Flip-Flop
S9313-02	MC831F	Clocked Flip-Flop
S9321-02	MC932F	Dual 4-Input Buffer
S9323-02	MC832F	Dual 4-Input Buffer
S9331-02	MC933F	Dual 4-Input Expander
S9333-02	MC833F	Dual 4-Input Expander
S9441-02	MC944F	Dual 4-Input Power NAND Gate
S9443-02	MC844F	Dual 4-Input Power NAND Gate
S9451-02	MC945F	Clocked Flip-Flop
S9453-02	MC845F	Clocked Flip-Flop
S9461-02	MC946F	Quad 2-Input NAND Gate
S9463-02	MC846F	Quad 2-Input NAND Gate
S9481-02	MC948F	Clocked Flip-Flop
S9483-02	MC848F	Clocked Flip-Flop
S9621-02	MC962F	Triple 3-Input NAND Gate
S9623-02	MC862F	Triple 3-Input NAND Gate
Texas Instruments		
SN15830	MC830F	Dual 4-Input NAND Gate
SN15830N	MC830P	Dual 4-Input NAND Gate
SN15831	MC831F	Clocked Flip-Flop
SN15831N	MC831P	Clocked Flip-Flop
SN15832	MC832F	Dual 4-Input Buffer
SN15832N	MC832P	Dual 4-Input Buffer
SN15833	MC833F	Dual 4-Input Expander

Part Number	Motorola Direct Replacement	Description
SN15833N	MC833P	Dual 4-Input Expander
SN15844	MC844F	Dual 4-Input Power NAND Gate
SN15844N	MC844P	Dual 4-Input Power NAND Gate
SN15845	MC845F	Clocked Flip-Flop
SN15845N	MC845P	Clocked Flip-Flop
SN15846	MC846F	Quad 2-Input NAND Gate
SN15846N	MC846P	Quad 2-Input NAND Gate
SN15848	MC848F	Clocked Flip-Flop
SN15848N	MC848P	Clocked Flip-Flop
SN15850	MC850F	Pulse Triggered Binary
SN15850N	MC850P	Pulse Triggered Binary
SN15851	MC851F	Monostable Multivibrator
SN15851N	MC851P	Monostable Multivibrator
SN15862	MC862F	Triple 3-Input NAND Gate
SN15862N	MC862P	Triple 3-Input NAND Gate
SN15930	MC930F	Dual 4-Input NAND Gate
SN15931	MC931F	Clocked Flip-Flop
SN15932	MC932F	Dual 4-Input Buffer
SN15933	MC933F	Dual 4-Input Expander
SN15944	MC944F	Dual 4-Input Power NAND Gate
SN15945	MC945F	Clocked Flip-Flop
SN15946	MC946F	Quad 2-Input NAND Gate
SN15948	MC948F	Clocked Flip-Flop
SN15950	MC950F	Pulse Triggered Binary
SN15951	MC951F	Monostable Multivibrator
SN15962	MC962F	Triple 3-Input NAND Gate

DTL

Signetics		
CS700G	MC207F	Dual 3-2 Input NAND Gate
CS700K	MC207G	Dual 3-2 Input NAND Gate
CS701G	MC208F	Dual 3-2 Input NAND Gate
CS701K	MC208G	Dual 3-2 Input NAND Gate
CS704G	MC210F	Clocked R-S Flip-Flop
CS704K	MC210G	Clocked R-S Flip-Flop
CS705G	MC215F	Dual 3-Input AND Gate Expander
CS705K	MC215G	Dual 3-Input AND Gate Expander
CS709G	MC217F	Dual 3-Input Diode Array
CS709K	MC217G	Dual 3-Input Diode Array
NE101G	MC251F	4-Input NAND Gate
NE101K	MC251G	4-Input NAND Gate
NE102G	MC252F	3-Input NAND Gate
NE102K	MC252G	3-Input NAND Gate
NE105G	MC253F	6-Input AND Gate Expander
NE105K	MC253G	6-Input AND Gate Expander
NE110G	MC254F	3-Input Power NAND Gate
NE110K	MC254G	3-Input Power NAND Gate

DTL (cont.)

Part Number	Motorola Direct Replacement	Description
NE115G	MC256F	Dual 2-Input NAND Gate
NE115K	MC256G	Dual 2-Input NAND Gate
NE124G	MC259F	Clocked R-S Flip-Flop
NE124K	MC259G	Clocked R-S Flip-Flop
NE150G	MC255F	Line Driver
NE150K	MC255G	Line Driver
NE700G	MC257F	Dual 3-2 Input NAND Gate
NE700K	MC257G	Dual 3-2 Input NAND Gate
NE701G	MC258F	Dual 3-2 Input NAND Gate
NE701K	MC258G	Dual 3-2 Input NAND Gate
SE101G	MC201F	4-Input NAND Gate
SE101K	MC201G	4-Input NAND Gate
SE102G	MC202F	3-Input NAND Gate
SE102K	MC202G	3-Input NAND Gate
SE105G	MC203F	6-Input AND Gate Expander
SE105K	MC203G	6-Input AND Gate Expander
SE110G	MC204F	3-Input Power NAND Gate
SE110K	MC204G	3-Input Power NAND Gate
SE115G	MC206F	Dual 2-Input NAND Gate
SE115K	MC206G	Dual 2-Input NAND Gate
SE124G	MC209F	Clocked R-S Flip-Flop
SE124K	MC209G	Clocked R-S Flip-Flop
SE150G	MC205F	Line Driver
SE150K	MC205G	Line Driver

MRTL

Fairchild		
U3F990021X	MC900F	Buffer
U3F990022X	MC800F	Buffer
U3F990321X	MC903F	3-Input NOR Gate
U3F990322X	MC803F	3-Input NOR Gate
U3F990421X	MC904F	Half Adder
U3F990422X	MC804F	Half Adder
U3F990521X	MC905F	Half-Shift Register
U3F990522X	MC805F	Half-Shift Register
U3F990621X	MC906F	Half-Shift Register (w/o Inverter)
U3F990622X	MC806F	Half Shift Register (w/o Inverter)
U3F990721X	MC907F	4-Input NOR Gate
U3F990722X	MC807F	4-Input NOR Gate
U3F991421X	MC914F	Dual 2-Input NOR Gate
U3F991422X	MC814F	Dual 2-Input NOR Gate
U3F991521X	MC915F	Dual 3-Input NOR Gate
U3F991522X	MC815F	Dual 3-Input NOR Gate
U3F992621X	MC926F	J-K Flip-Flop
U3F992622X	MC826F	J-K Flip-Flop
U3F992721X	MC927F	Quad Inverter
U3F992722X	MC827F	Quad Inverter
U5B990029X	MC700G	Buffer
U5B990121X	MC901G	Counter Adapter
U5B990122X	MC801G	Counter Adapter
U5B990229X	MC702G	R-S Flip-Flop
U5B990329X	MC703G	3-Input NOR Gate
U5B990421X	MC904G	Half Adder
U5B990422X	MC804G	Half Adder
U5B990429X	MC704G	Half Adder
U5B990521X	MC905G	Half-Shift Register
U5B990522X	MC805G	Half-Shift Register
U5B990529X	MC705G	Half-Shift Register
U5B990621X	MC906G	Half-Shift Register (w/o Inverter)
U5B990622X	MC806G	Half-Shift Register (w/o Inverter)
U5B990721X	MC907G	4-Input NOR Gate
U5B990722X	MC807G	4-Input NOR Gate
U5B990729X	MC707G	4-Input NOR Gate
U5B991421X	MC914G	Dual 2-Input NOR Gate
U5B991422X	MC814G	Dual 2-Input NOR Gate
U5B991429X	MC714G	Dual 2-Input NOR Gate
U5B991621X	MC916G	J-K Flip-Flop
U5B991622X	MC816G	J-K Flip-Flop
U5B992329X	MC723G	J-K Flip-Flop
U5B997421X	MC974G	J-K Flip-Flop
U5B997422X	MC874G	J-K Flip-Flop
U5B997429X	MC774G	J-K Flip-Flop
U5C990321X	MC903G	3-Input NOR Gate
U5C990322X	MC803G	3-Input NOR Gate
U5D990021X	MC900G	Buffer
U5D990022X	MC800G	Buffer
U5D990221X	MC902G	R-S Flip-Flop
U5D990222X	MC802G	R-S Flip-Flop
U5F991521X	MC915G	Dual 3-Input NOR Gate
U5F991522X	MC815G	Dual 3-Input NOR Gate
U5F991529X	MC715G	Dual 3-Input NOR Gate
U5F992621X	MC926G	J-K Flip-Flop
U5F992622X	MC826G	J-K Flip-Flop
U5F992629X	MC726G	J-K Flip-Flop
U5F992721X	MC927G	Quad Inverter
U5F992722X	MC827G	Quad Inverter
U5F992729X	MC727G	Quad Inverter

Philco		
PL9900 21	MC900G,F	Buffer
PL9901 21	MC901G,F	Counter Adapter
PL9902 21	MC902G,F	R-S Flip-Flop
PL9903 21	MC903G,F	3-Input NOR Gate
PL9904 21	MC904G,F	Half Adder
PL9904 29	MC704G,F	Half Adder
PL9905 21	MC905G,F	Half Shift Register
PL9906 21	MC906G,F	Half-Shift Register
PL9907 21	MC907G,F	4-Input NOR Gate
PL9914 21	MC914G,F	Dual 2-Input NOR Gate
PL9915 21	MC915G,F	Dual 3-Input NOR Gate
PL9916 21	MC916G,F	J-K Flip Flop
PL9923 21	MC916G,F	J-K Flip-Flop
PL9926 21	MC926G,F	J-K Flip-Flop

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Fairchild		
U3F990821X	MC908F	Half Adder
U3F990921X	MC909F	2-Input Buffer
U3F991021X	MC910F	Dual 2-Input NOR Gate
U3F991121X	MC911F	4-Input OR/NOR Gate
U3F991221X	MC912F	Half Adder
U3F991321X	MC913F	Type "D" Flip-Flop
U3F992121X	MC921F	Dual 2-Input Gate Expander
U5B990821X	MC908G	Half Adder
U5B990829X	MC808G	Half Adder
U5B990921X	MC909G	2-Input Buffer
U5B990929X	MC809G	2-Input Buffer
U5B991021X	MC910G	Dual 2-Input NOR Gate
U5B991029X	MC710G	Dual 2-Input NOR Gate
U5B991121X	MC911G	4-Input OR/NOR Gate
U5B991129X	MC811G	4-Input OR/NOR Gate
U5B991221X	MC912G	Half Adder
U5B991229X	MC812G	Half Adder
U5B991321X	MC913G	Type "D" Flip-Flop
U5B991329X	MC813G	Type "D" Flip-Flop

mW MRTL (cont.)

Part Number	Motorola Direct Replacement	Description
U5B992121X	MC921G	Dual 2-Input Gate Expander
U5B992129X	MC721G	Dual 2-Input Gate Expander
Philco		
PL9908 21	MC908G,F	Half Adder
PL9908 23	MC808G,F	Half Adder
PL9909 21	MC909G,F	2-Input Buffer
PL9909 23	MC809G,F	2-Input Buffer
PL9910 21	MC910G,F	Dual 2-Input Gate
PL9912 23	MC810G,F	Dual 2-Input Gate
PL9911 21	MC911G,F	4-Input Gate
PL9911 23	MC811G,F	4-Input Gate
PL9912 21	MC912G,F	Half Adder
PL9913 21	MC913G,F	Type "D" Flip-Flop
PL9913 23	MC813G,F	Type "D" Flip-Flop
PL9921 21	MC921G,F	Dual 2-Input Gate Expander
PL9921 23	MC821G,F	Dual 2-Input Gate Expander
PL9939 21	MC918G,F	Dual 3-Input Gate
PL9931 23	MC818G,F	Dual 3-Input Gate

Part Number	Motorola Direct Replacement	Description
PL9940 21	*MC920G,F	J-K Flip-Flop
PL9940 29	*MC720G,F	J-K Flip-Flop

* Not pin-for-pin replacement.

Texas Instruments		
SN17 808L	MC808G	Half Adder
SN17 809L	MC809G	2-Input Buffer
SN17 810L	MC810G	Dual 2-Input Gate
SN17 811L	MC811G	4-Input Gate
SN17 812L	MC812G	Half Adder
SN17 813L	MC813G	Type "D" Flip-Flop
SN17 908L	MC908G	Half Adder
SN17 909L	MC909G	2-Input Buffer
SN17 910L	MC910G	Dual 2-Input Gate
SN17 911L	MC911G	4-Input OR/NOR Gate
SN17 912L	MC912G	Half Adder
SN17 913L	MC913G	Type "D" Flip-Flop

LINEAR INTEGRATED CIRCUITS

Operational Amplifiers

Amelco	
805 BE	MC1533G*
A13-215	MC1531G*
A13-251	MC1530G*
General Electric	
4JPA135	MC1531G*
Fairchild	
U3H771231X	MC1712F
U3H771239X	MC1712CF
U3I770929X	MC1709CF
U3I770931X	MC1709F
U5B770931X	MC1709G
U5B770939X	MC1709CG
U5B771231X	MC1712G
U5B771239X	MC1712CG
National	
LM101	MC1539G*
Philco	
PA70931	MC1709F
PA70931	MC1709G
PA70939	MC1709CF
PA70939	MC1709CG
PA71231	MC1712F
PA71231	MC1712G
PA71239	MC1712CF
PA71239	MC1712CG
RCA	
CA3008	MC1430F*
CA3010	MC1430G*
CA3015	MC1430G*
CA3016	MC1430F*
CA3022	MC1709CG*
CA3031	MC1709G*
Raytheon	
RM702	MC1712CF
RM702	MC1712CG
RM702	MC1712F
RM702	MC1712G
RM709	MC1709CF
RM709	MC1709CG
RM709	MC1709F
RM709	MC1709G
RM4709	MC1437P*
Signetics	
NE505G	MC1430F*
NE505K	MC1430G*
NE505G	MC1431F*
NE505K	MC1431G*
SE505G	MC1530F*
SE505G	MC1531F*
SE505K	MC1530G*
SE505K	MC1531G*
Texas Instruments	
SN726	MC1430F*
SN728	MC1431F*
SN52702	MC1712F
SN52702L	MC1712G
SN52709	MC1709F
SN52709L	MC1709G
SN72702	MC1712CF
SN72702L	MC1712CG
SN72709	MC1709CF
SN72709L	MC1709CG
Westinghouse	
WS161Q	MC1531F*
WS174Q	MC1709F*

High-Frequence Amplifiers

Fairchild	
SH9004	MC1110G
U5D770339X	MC1550G*
Philco	
PA713	MC1550G*
PA7601	MC1550G*
RCA	
CA3002	MC1550G*
CA3003	MC1550G*
CA3004	MC1550G*
CA3014	MC1314G*
Signetics	
SE501K	MC1552G*
Texas Instruments	
SN5510L	MC1510G
SN5510	MC1510F†
SN5510	MC1509F
Westinghouse	
WM1146T	MC1550G*

Sense Amplifiers

Fairchild	
U3H771031X	MC1710F
U3H771039X	MC1710CF
U3I771131X	MC1711F
U5B771031X	MC1710G
U5B771039X	MC1710CG
U5F771131X	MC1711G
Philco	
PA71031	MC1710F
PA71031	MC1710G
PA71039	MC1710CF
PA71039	MC1710CG
Raytheon	
RM710	MC1710CF
RM710	MC1710CG
RM710	MC1710F
RM710	MC1710G
Sylvania	
SA-10	MC1540F*
Texas Instruments	
SN5500	MC1540F*
SN52710	MC1710F
SN52710L	MC1710G
SN72710	MC1710CF
SN72710L	MC1710CG

* Nearest equivalent

†Electrically interchangeable; pin-outs different.

DIGITAL APPLICATION SELECTOR GUIDE

This table shows the various circuit functions available in each integrated circuit logic family. "F" indicates the device is available in ceramic flat package, "G" indicates metal can, and "P" indicates dual in-line plastic package.

Many of these devices have provision for expanding input capability. See individual family specifications for detail.

FUNCTION (Positive Logic)	MECL	MECL II	MHTL	MTTL	MTTL II	MTTL III	MDTL	DTL	MRTL	mW MRTL	MOS
GATES											
Quad Inverter							G		F,G		
Hex Inverter							F,P		F,P		
3-Input OR/NOR Gate	F,G										
4-Input OR/NOR Gate										F,G	
5-Input OR/NOR Gate	F,G										
6-Input OR/NOR Gate		F,P									
Dual 2-Input OR/NOR Gate	G	F,P									
Dual 4-Input OR/NOR Gate	F	F,P									
3-Input NOR Gate									F,G		
4-Input NOR Gate									F,G		
5-Input NOR Gate									F,G	F,G	
Dual 2-Input NOR Gate	F,G								F,G	F,G	
Dual 3-Input NOR Gate	F,G								F,G,P	F,G,P	
Dual 4-Input NOR Gate									F,G,P	F,P	
Triple 3-Input NOR Gate		F,P							F,P	F,P	
Quad 2-Input NOR Gate	F	F,P				F,P	F,P		F,P	F,P	
3-Input NAND Gate								F,G			
4-Input NAND Gate								F,G			
8-Input NAND Gate				F,P	F,P	F,P					
Dual 2-Input NAND Gate								F,G			
Dual 3-2 Input NAND Gate							G	F,G			
Dual 3-Input NAND Gate								F,G			
Dual 4-Input NAND Gate			P	F,P	F,P		F,P				
Dual 2-Input NAND Gate plus Inverter							G				
Triple 3-Input NAND Gate			P	F,P	F,P	F,P	F,P				
Quad 2-Input NAND Gate			P	F,P	F,P	F,P					
Quad 2-Input OR Gate						F,P					
6-Input AND Gate								F,G			
Dual 3-Input AND Gate								F,G			
Quad 2-Input AND Gate						F,P					
Quad Exclusive NOR Gate		F,P									
Quad Exclusive OR Gate		F,P							F,P		
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement				F,P							
2-Wide 4-Input AND-OR-INVERT Gate				F,P	F,P						
3-Wide 3-Input AND-OR-INVERT Gate				F,P							
4-Wide 2-2-2-3 Input AND-OR-INVERT Gate				F,P	F,P						
Dual 2-Wide 2-Input AND-OR-INVERT Gate				F,P	F,P	F,P					
GATE EXPANDERS											
5-Input Gate Expander	F,G										
6-Input Gate Expander								F,G			
Dual 2-Input Gate Expander										F,G	
Dual 3-Input Gate Expander								F,G			
Dual 3-4 Input Gate Expander							G				
Dual 4-Input Expander for NAND Gates				F,P			F,P				
Dual 4-Input Expander for AND-OR-INVERT Gates				F,P	F,P	F,P					
Dual 4-Input Gate Expander			P						F,P		
Dual 4-5 Input Gate Expander		F,P									
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates				F,P	F,P						
Quad 2-Input Gate Expander									F,P	F,P	
Hex Expander									F,P		

(continued on next page)

DIGITAL APPLICATION SELECTOR GUIDE (continued)

FUNCTION (Positive Logic)	MECL	MECL II	MHTL	MTTL	MTTL II	MTTL III	MDTL	DTL	MRTL	mW MRTL	MOS
FLIP FLOPS											
J-K Flip-Flop	F,G	F,P		F,P	F,P	F,P	F,G,P		F,G,P	F,G,P	
R-S Flip-Flop	F,G		P	F,P					G		
Clocked R-S Flip-Flop							F,G,P	F,G			
Type D Flip-Flop		F,P								F,G	
Dual J-K Flip-Flop			P			F,P	F,P		F,P	F,P	
Dual Clocked R-S Flip-Flop		F,P									
Dual Type D Flip-Flop						F,P				F,P	
DRIVERS & BUFFERS											
3-Input NAND Power Gate								F,G			
Dual 3-2 Input NAND Power Gate							G				
Dual 4-Input NAND Power Gate						F,P	F,P				
Dual 4-Input AND Power Gate						F,P					
Bias Driver	F,G										
Line Driver	F,G		P	F,P		F,P	F,G,P	F,G			
Lamp Driver	F,G						G				
Dual 2-Input Clock Driver	G										
Dual 4-Input OR/NOR Clock Driver	F	P									
Buffer Inverter									F,G		
2-Input Buffer										F,G	
Dual Buffer Inverter									F,G,P		
Dual 2-Input Buffer										F,G,P	
Dual 3-2 Input Buffer							G				
Dual 3-Input Buffer									F,P		
Dual 4-Input Buffer							F,P				
MISCELLANEOUS											
Half Adder	F,G								F,G	F,G	
Dual Half Adder									F,P		
Full Adder		F,P							F,G	F,G	
Dual Full Adder									F,P		
Full Subtractor		F,P									
Dual Full Subtractor									F,P		
Half-Shift Register									F,G		
Half-Shift Register (without inverter)									F,G		
Dual Half-Shift Register									F,P		
Dual Half-Shift Register (without inverter)									F,P		
Monostable Multivibrator							F,G,P				
Level Translator	F,G	F,P									
Quad Line Receiver		F,P									
1 J-K FF, 1 Expander, 2 Buffers									P		
1 J-K FF, 1 Inverter, 2 Buffers									P		
Dual 3-Input Diode Array								F,G			
Counter Adapter									G		
Decade Counter							F,P				
Binary Up Counter (Divide by 16)							F,P				
Data Distributor		F,P									
Dual Keyer Gate											P
Frequency Divider											P
16-Bit Memory		P									

MECL

INTEGRATED CIRCUITS
MC300/MC350 SERIES

MECL

INTEGRATED CIRCUITS

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MC300 Series

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GATES		
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NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C

Function	Type ①	DC Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Case	Page No.
5-Input OR/NOR Gate	MC301	25	7.5	37	71, 72	2-12
R-S Flip-Flop	MC302	↓	11	42	↓	2-20
Half-Adder	MC303	↓	7.5	63	↓	2-26
Bias Driver	MC304	↓	–	18	↓	2-29
5-Input Gate Expander	MC305	–	4.5	–	↓	2-28
3-Input OR/NOR Gate	MC306	25	7.5	37	↓	2-9
3-Input OR/NOR Gate	MC307	↓	7.5	15	↓	2-9
AC-Coupled J-K Flip-Flop	MC308	↓	8.5	87	↓	2-22
Dual 2-Input NOR Gate	MC309	↓	7.0	54	↓	2-14
Dual 2-Input NOR Gate	MC310	↓	7.0	54	↓	2-14
Dual 2-Input NOR Gate	MC311	↓	7.0	41	↓	2-14
Dual 3-Input NOR Gate (With Internal Bias)	MC312A	↓	7.5	70	↓	2-16
Quad 2-Input NOR Gate	MC313F	↓	7.0	125	83	2-18
AC-Coupled J-K Flip-Flop	MC314	↓	12	118	71, 72	2-24
Line Driver	MC315	–	14	180 ②	↓	2-30
Lamp Driver	MC316	–	–	135	↓	2-31
Level Translator – MECL to Saturated Logic	MC317	7 (DTL)	27.5	63	↓	2-32
Level Translator – Saturated Logic to MECL	MC318	25 (MECL)	17	105	71, 72	2-33

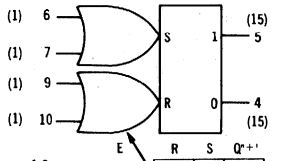
① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC301G = Metal Can, MC301F = Flat Package.)
② With 93-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC300 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC304, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are given on page 2—29.

MC302 — R-S FLIP-FLOP

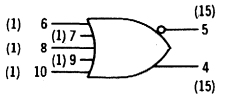


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

t_{dr} = 10.5 ns
P_D = 42 mW

DC Set-Reset flip-flop with expandable input and buffered outputs.

MC301 — 5-INPUT GATE



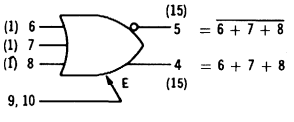
$5 = \overline{6 + 7 + 8 + 9 + 10}$

$4 = 6 + 7 + 8 + 9 + 10$

t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC306 — 3-INPUT GATE



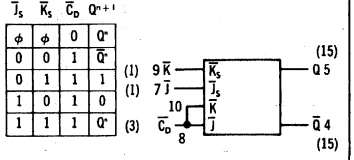
t_{dl} = 6.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC308 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

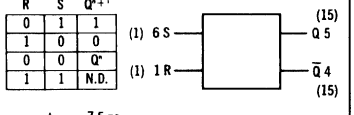
$\overline{J}_s$	$\overline{K}_s$	$\overline{C}_D$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}_s$ and $\overline{K}_s$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}_s$ and $\overline{K}_s$ inputs would be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

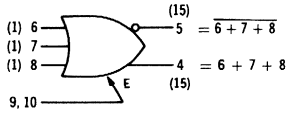
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC307 — 3-INPUT GATE



t_{dl} = 6.0 ns
P_D = 15 mW

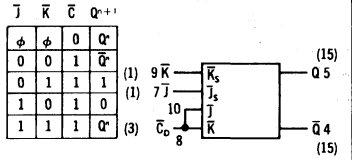
*No pull-down resistors

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC306, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on page 2-9)

MC314 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

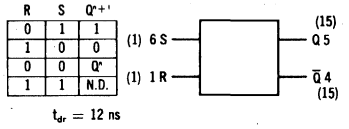
$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

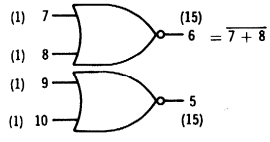
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

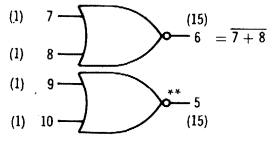
MC309 — DUAL 2-INPUT GATE



t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

MC310 — DUAL 2-INPUT GATE

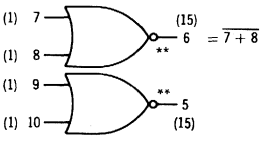


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

t_{dl} = 6.5 ns P_D = 27 mW/gate

Provides the positive logic "NOR" function. Same as MC309 with one output pull-down resistor optional (see schematic diagram on page 2-14).

MC311 — DUAL 2-INPUT GATE

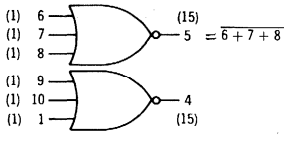


**Optional pull-down resistor If resistor is desired, connect pin 4 to pin 5 or pin 6.

t_{dl} = 6.5 ns P_D = 21 mW/gate

Provides the positive logic "NOR" function. Same as MC309 with one output pull-down resistor omitted and the second optional (see schematic diagram on page 2-14).

MC312A — DUAL 3-INPUT GATE

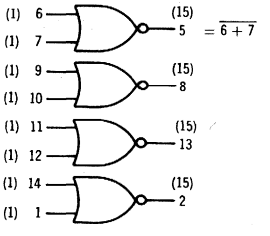


t_{dl} = 6.5 ns

P_D = 35 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver. This gate without the bias driver is available as the MC312.

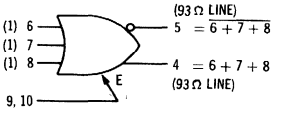
MC313F — QUAD 2-INPUT GATE



t_{dl} = 6.5 ns P_D = 31 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC315 — LINE DRIVER

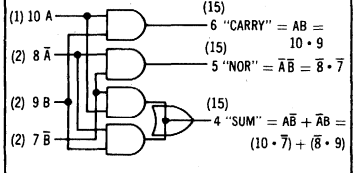


t_{dl} = 14 ns

P_D = 180 mW (with 93 Ω load)

Drives lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC303 — HALF-ADDER

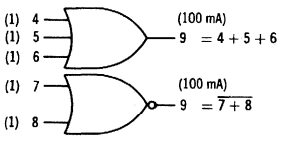


t_{dl} = 7 ns

P_D = 63 mW

Provides the "SUM", "CARRY", and "NOR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

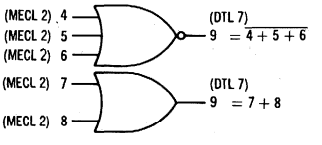
MC316 — LAMP DRIVER



P_D = 135 mW

Capable of driving 6-volt lamps. Positive "NOR" function is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC317 — LEVEL TRANSLATOR

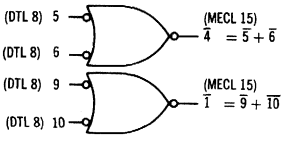


t_{dr} = 30 ns

P_D = 63 mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NOR" function is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC318 — LEVEL TRANSLATOR

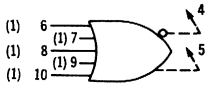


t_{dl} = 17 ns

P_D = 105 mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC305 — 5-INPUT EXPANDER



t_{dl} = 5 ns

For use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

Note:

Any unused input should be connected to V_{EE}.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

"0" = −1.55 V
"1" = −0.75 V
} typical

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

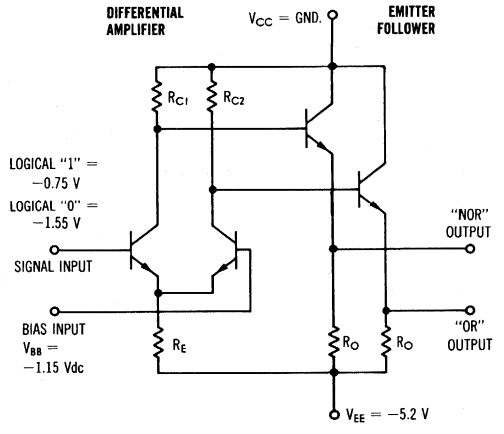
A bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE} drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE} drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC304. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V

FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

DEFINITIONS

e_{in} AC signal applied to the input

e_{out} AC signal at the output

I_C Amount of current drawn from the positive power supply by the test unit

I_{CEX} Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential

I_E Amount of current drawn from the test unit by the negative power supply

I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input

I_L Current drawn from a node when that node is at ground potential

t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge

t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge

t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge

t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge

t_f Time required for the output pulse to go more negative from its 90% point to its 10% point

t_r Time required for the output pulse to go more positive from its 10% point to its 90% point

V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input

V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input

V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero

V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input

V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input

V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of change in the input voltage approaches infinity

V_H Logical "1" input voltage

V_L Logical "0" input voltage

V_{OH} High-level output voltage when the saturated logic circuit output is in an "off" condition

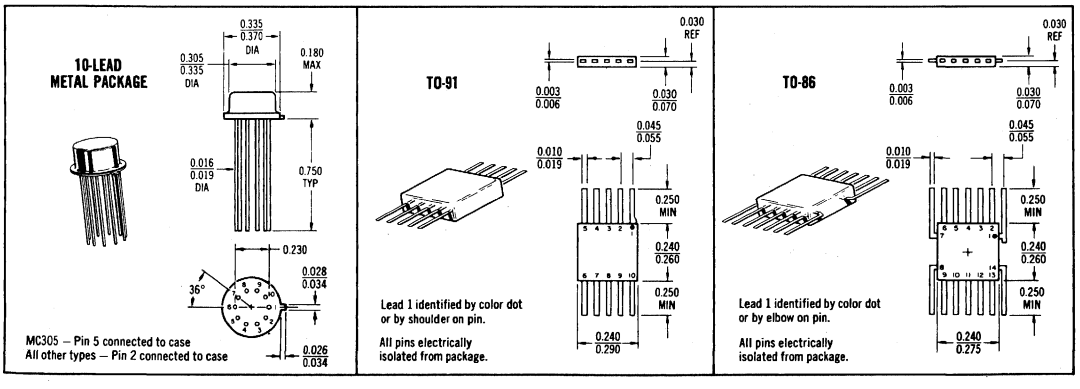
V_{OL} Low-level output voltage when the saturated logic output circuit is in an "on" condition

ΔV_1, ΔV_5 Change in the "1" level output voltage as the load is varied from no load to full load

PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

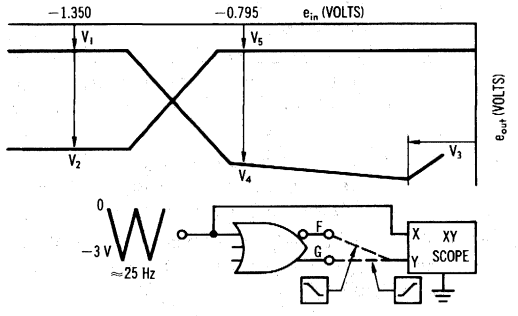
Exception: Type MC313F is available only in the TO-86, 14-lead flat package.

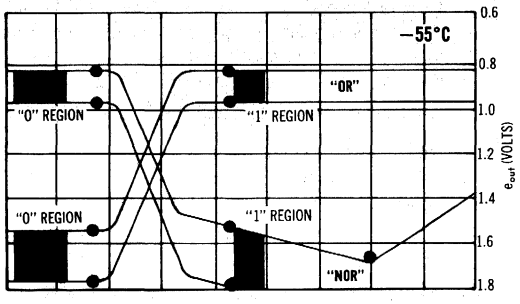


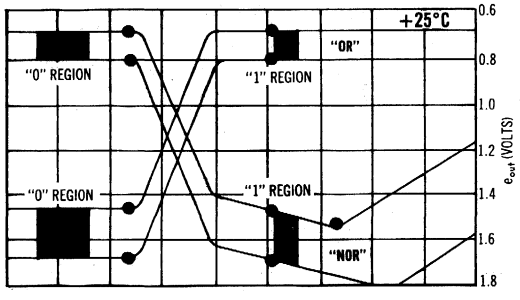
WORST-CASE TRANSFER CHARACTERISTICS

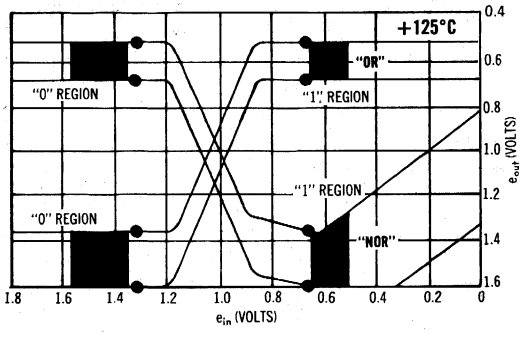
The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS









MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0 Vdc)	V_{EE}	−10	Vdc
Base Input Voltage (V_{CC} = 0 Vdc)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	−55 to +125	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

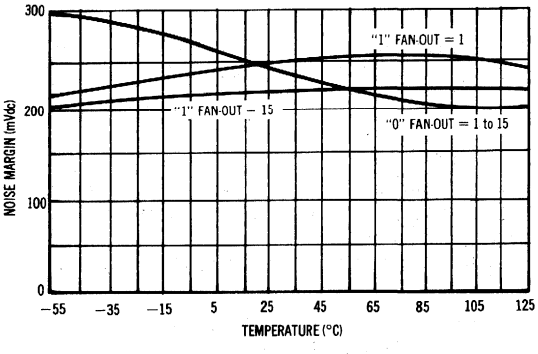
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

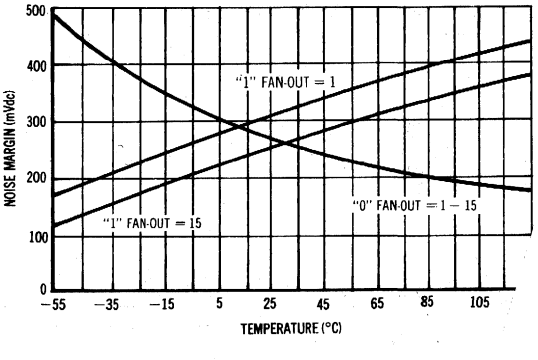
The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC304 bias driver, as compared with non-compensated fixed bias source, bottom.

Note: Any unused input should be connected to V_{EE}.

USING MC304

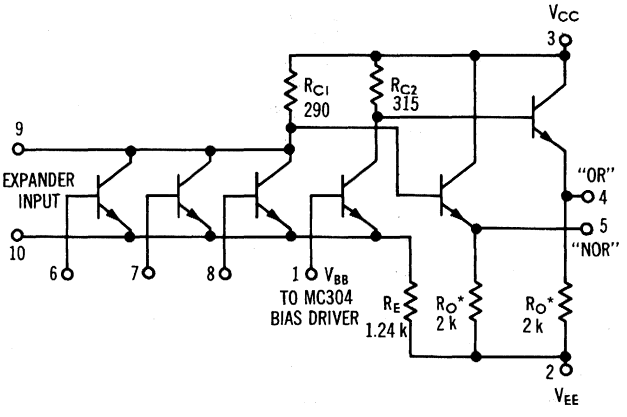


USING FIXED V_{BB} of −1.15 V



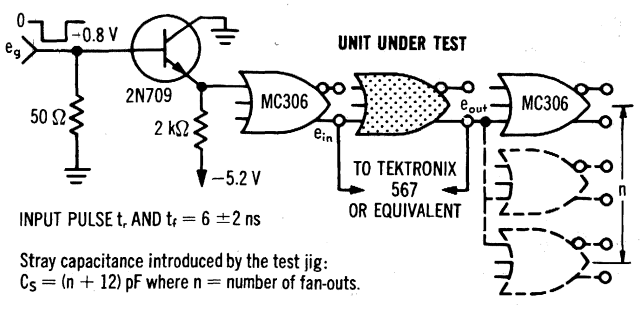
MC306 · MC307

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC307 omits output pull-down resistors, permitting reduction of power dissipation.



*Resistors R_O are omitted in MC307 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

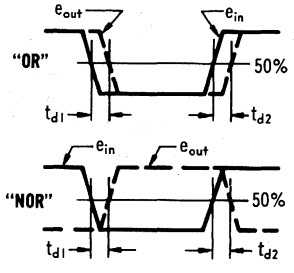
SWITCHING TIME TEST CIRCUIT



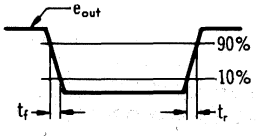
INPUT PULSE t_r AND $t_f = 6 \pm 2$ ns

Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

PROPAGATION DELAY

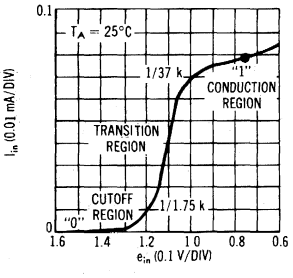


RISE AND FALL TIME

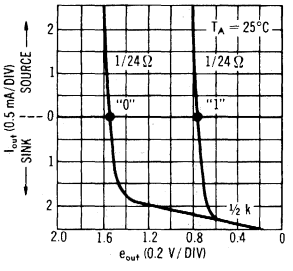


Fan-in obtained with MC305 input expanders; all but driven input connected to −5.2 V.

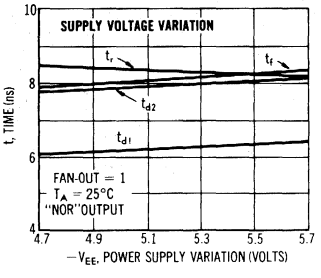
TYPICAL INPUT CHARACTERISTICS

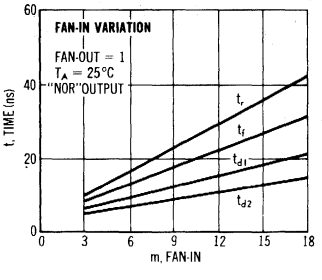


TYPICAL OUTPUT CHARACTERISTICS

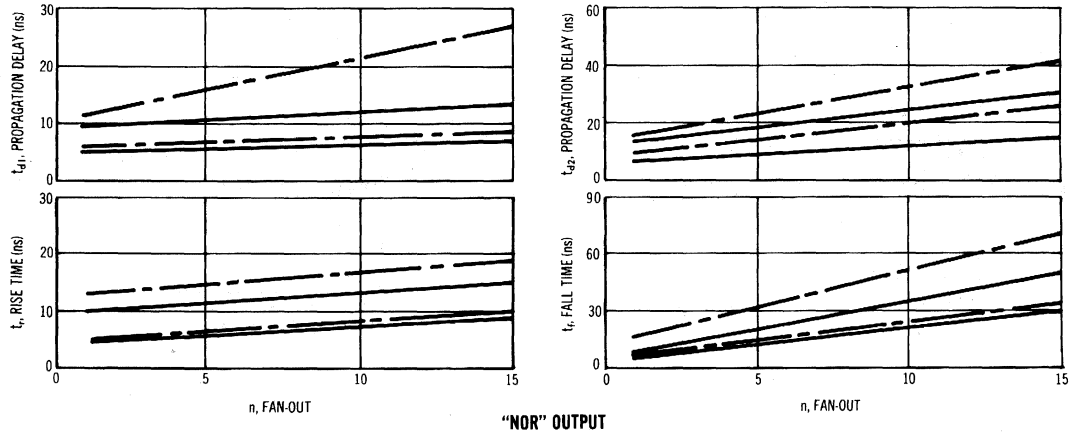


TYPICAL SWITCHING TIME VARIATIONS MC306





SWITCHING CHARACTERISTICS (10% to 90% distribution)



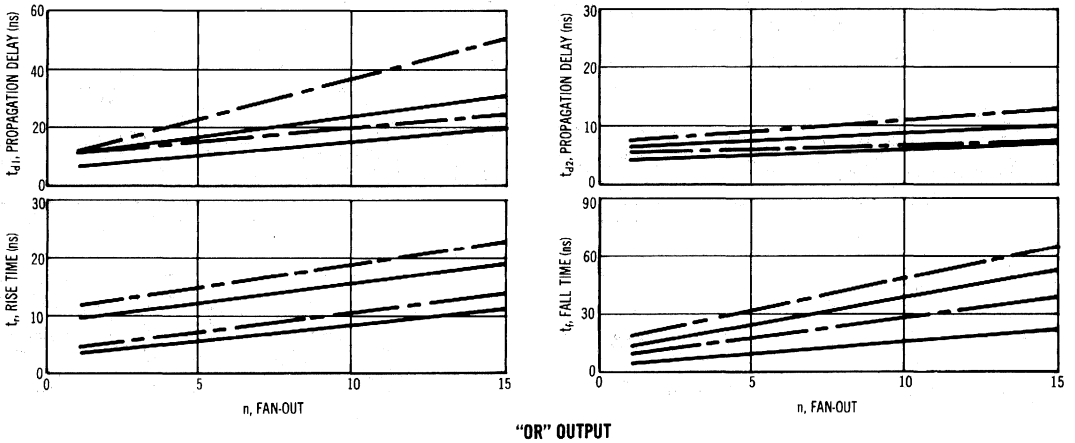
ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ±1%				
@ Test Temperature	−55°C	—	−0.945	−1.450	−5.20	−1.25
	+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
	+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply MC306	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	8.85	—	8.85	—	8.15	mAdc
Drain Current MC307	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	3.6	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,8	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	2,6,8	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,8	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	7	—	2,6,8	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,6,8	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8	1	—	5③	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8	1	—	4③	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8	1	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,6,8	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8	1	—	—	3	t_{d1} (4)	7.0	11.0	7.0	11.5	9.5	14.5	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	5.5	10.0	5.5	10.5	7.0	12.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	5.5	10.0	5.5	11.0	7.0	12.5	↓
	6	5	—	2,7,8	1	—	—	3	t_{d2} (5)	7.0	10.5	7.0	11.0	9.5	14.5	↓
Rise Time	6	4	—	2,7,8	1	—	—	3	t_r (4)	6.0	8.5	6.0	10.0	8.0	13.0	↓
	6	5	—	2,7,8	1	—	—	3	t_r (5)	7.5	11.5	7.5	12.5	9.5	15.0	↓
Fall Time	6	4	—	2,7,8	1	—	—	3	t_f (4)	6.5	10.5	6.5	12.0	9.0	15.0	↓
	6	5	—	2,7,8	1	—	—	3	t_f (5)	6.5	12.0	6.5	12.5	9.0	15.0	↓

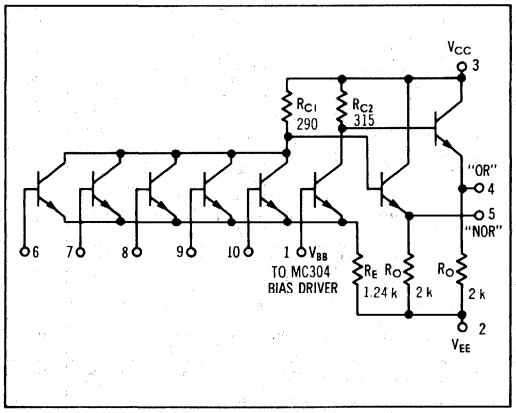
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR / $dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

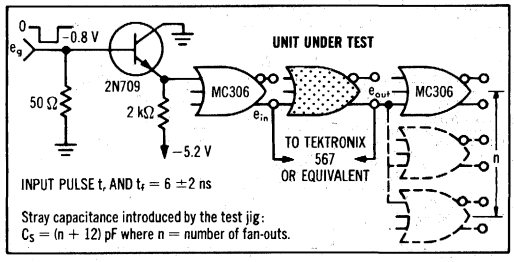


MC301

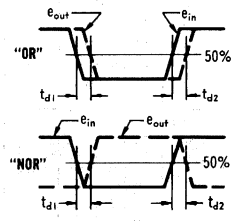
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



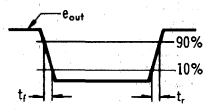
SWITCHING TIME TEST CIRCUIT



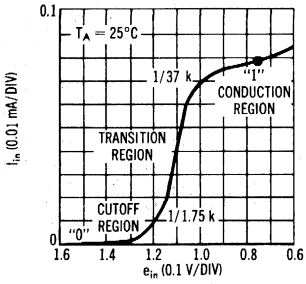
PROPAGATION DELAY



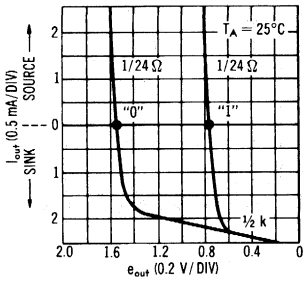
RISE AND FALL TIME



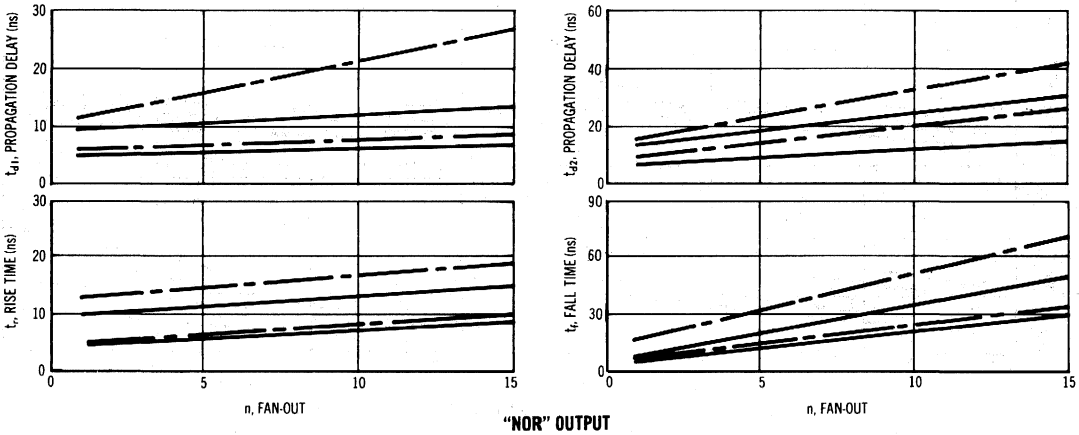
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" OUTPUT

——— −55°C and +25°C

— — — +125°C

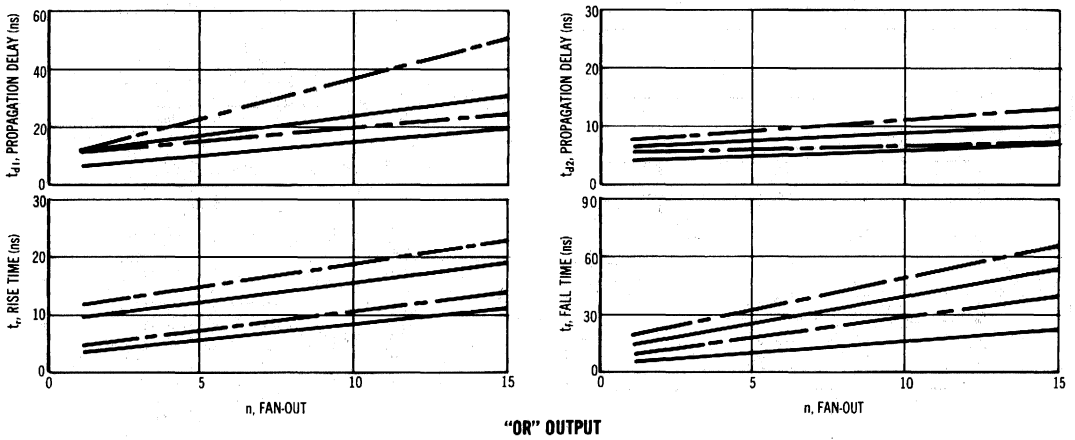
ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
	Test Conditions Vdc ±1%															
−55°C	—	−0.945	−1.450	−5.20	−1.25											
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15											
+125°C	—	−0.655	−1.300	−5.20	−1.00											
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	8.85	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_4 (5)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_2 (4)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5⑤	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4⑤	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9	1	10①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	8.0	12.0	8.5	12.5	10.0	15.5	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	6.5	10.0	6.5	11.0	7.5	14.0	↓
	6	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	5.5	9.0	6.0	10.0	8.0	12.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	7.5	11.0	8.0	12.5	10.0	15.5	
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	6.5	9.0	7.0	10.0	10.5	15.5	
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	8.5	14.0	9.0	14.5	11.0	17.5	
Fall Time	6	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	7.0	11.5	7.5	13.0	10.0	16.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	7.0	12.0	7.5	12.5	10.0	15.5	↓

Pins not listed are left open

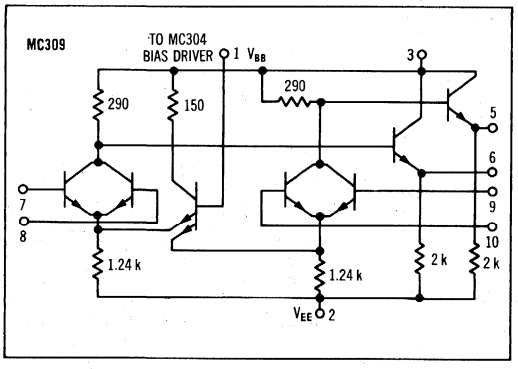
① Input voltage is adjusted to obtain dV "NOR / dV_{in} = "0".

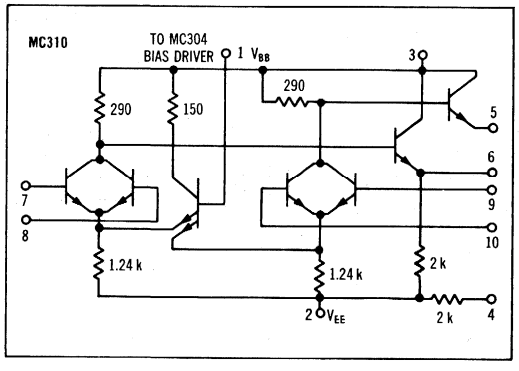
⑤ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

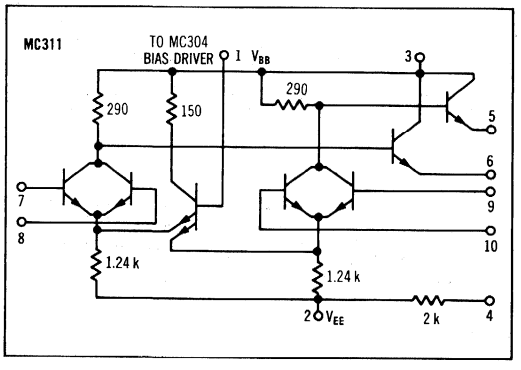


MC309 · MC310 · MC311

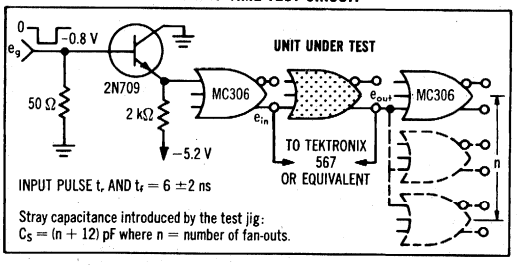
Dual 2-input gates that provide the positive logic "NOR" function. MC309 has two output pull-down resistors; MC310 has one of the output pull-down resistors optional; MC311 omits one output pull-down resistor and has the second optional.



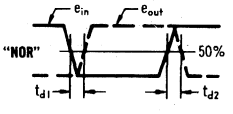




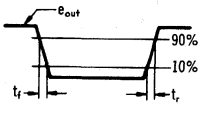
SWITCHING TIME TEST CIRCUIT



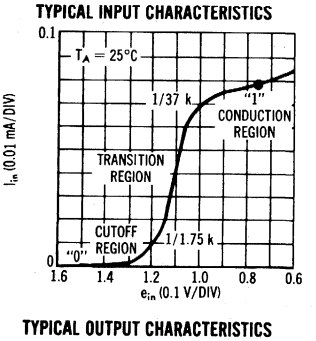
PROPAGATION DELAY



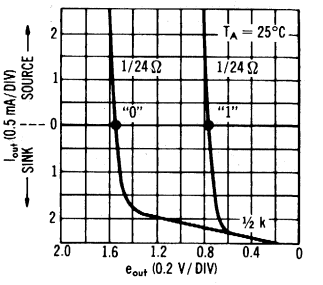
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



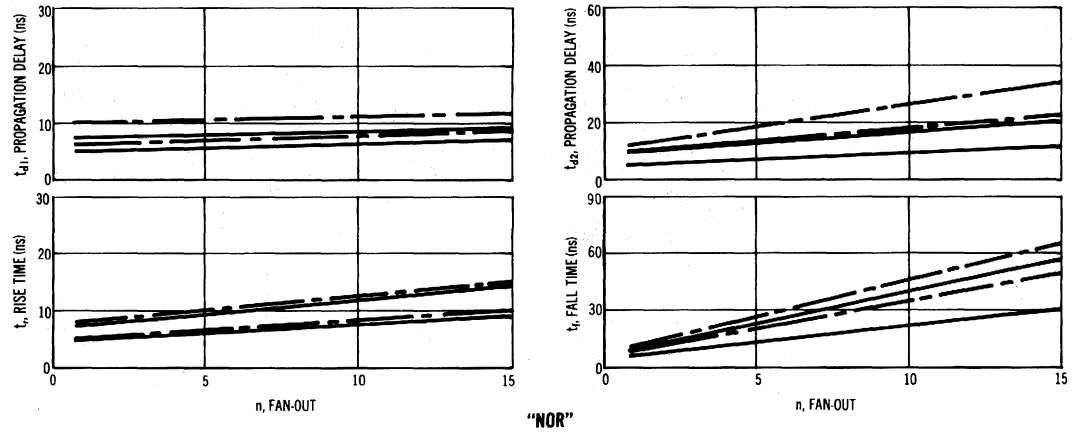
ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%				
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply MC309, MC310	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.0	—	13.0	—	12.0	mAdc
Drain Current MC311	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	10.1	—	10.1	—	9.3	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	—	2,7,8,9,10	1	—	6②	3	$\triangle V_1$ (6)	—	−0.055	—	−0.055	—	−0.060	Vdc
(No load to full load)	—	—	—	2,7,8,9,10	1	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Vdc
"NOR" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,7,9,10	1	8①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	6	—	2,8,9,10	1	—	—	3	t_{d1} (6)	5.5	10.0	6.0	11.0	7.0	12.0	ns
	10	5	—	2,7,8,9	1	—	—	3	t_{d1} (5)	5.5	10.0	6.0	11.0	7.0	12.0	↓
	7	6	—	2,8,9,10	1	—	—	3	t_{d2} (6)	6.5	13.0	7.0	13.5	9.5	15.0	↓
	10	5	—	2,7,8,9	1	—	—	3	t_{d2} (5)	6.5	13.0	7.0	13.5	9.5	15.0	↓
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	6.0	12.0	6.0	12.0	7.0	13.5	↓
	10	5	—	2,7,8,9	1	—	—	3	t_r (5)	6.0	12.0	6.0	12.0	7.0	13.5	↓
Fall Time	7	6	—	2,8,9,10	1	—	—	3	t_f (6)	7.0	13.0	7.5	14.0	9.5	17.0	↓
	10	5	—	2,7,8,9	1	—	—	3	t_f (5)	7.0	13.0	7.5	14.0	9.5	17.0	↓

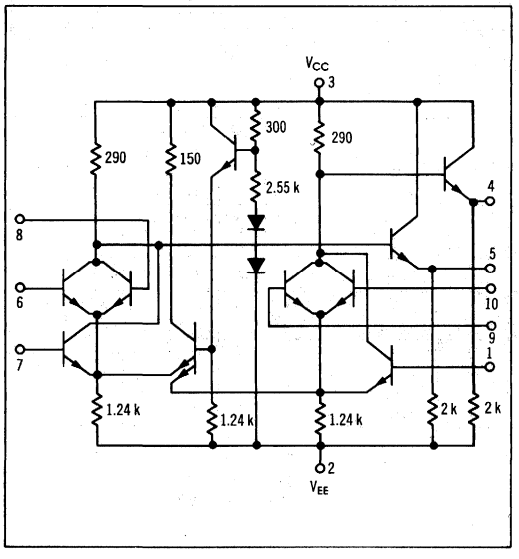
Pins not listed are left open For MC310, connect pin 4 to pin 5 for all tests ①Input voltage is adjusted to obtain dV "NOR"/dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

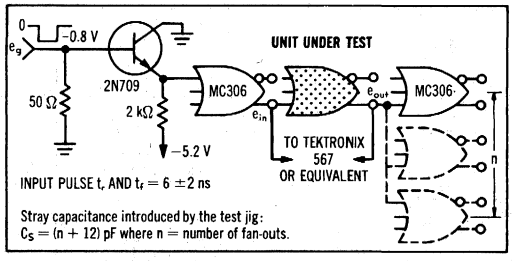


MC312A

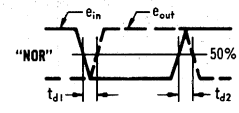
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC312.



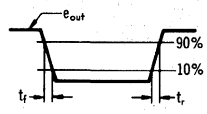
SWITCHING TIME TEST CIRCUIT



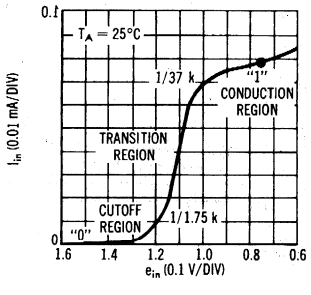
PROPAGATION DELAY



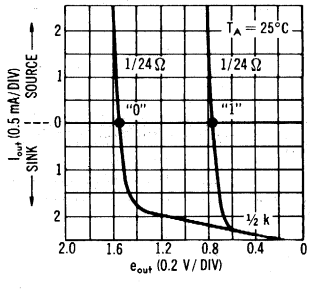
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



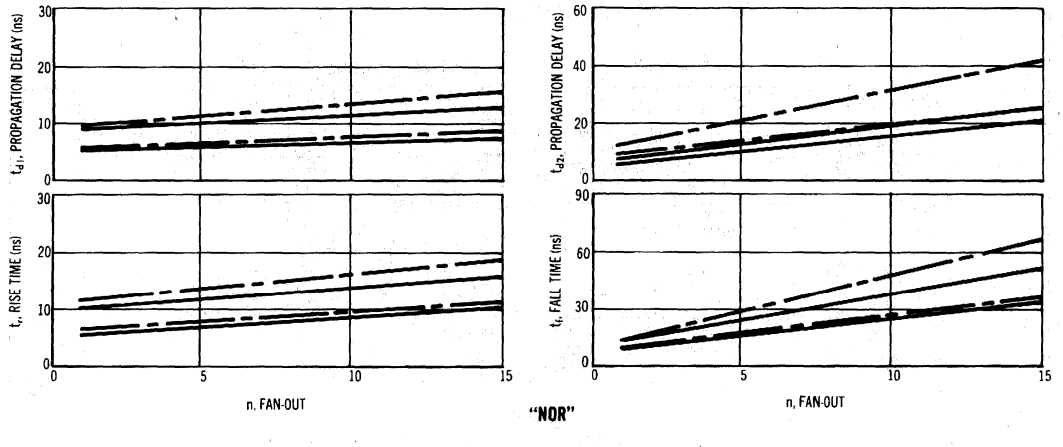
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_{IH} Pin No	$V_{I\,max}$ Pin No	V_{IL} Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5③	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	1	2,6,7,8,9,10	—	4③	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—	↓	—	↓	—	↓	
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

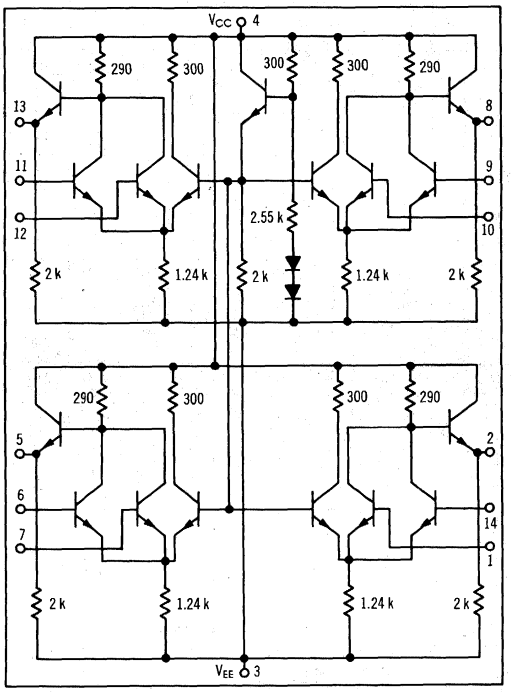
Pins not listed are left open.
①Input voltage is adjusted to obtain dv "NOR"/dV_{in} = 0. ③Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

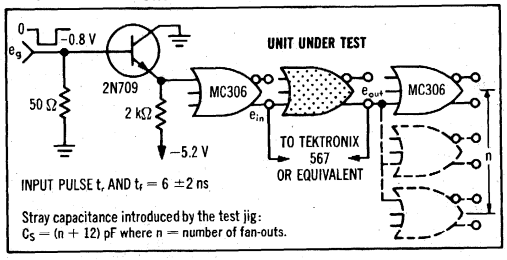


MC313F

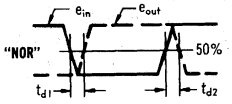
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



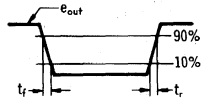
SWITCHING TIME TEST CIRCUIT



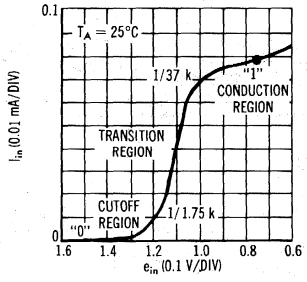
PROPAGATION DELAY



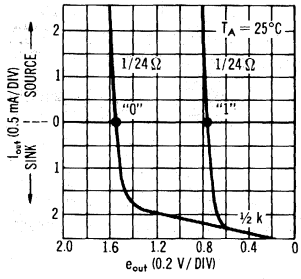
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



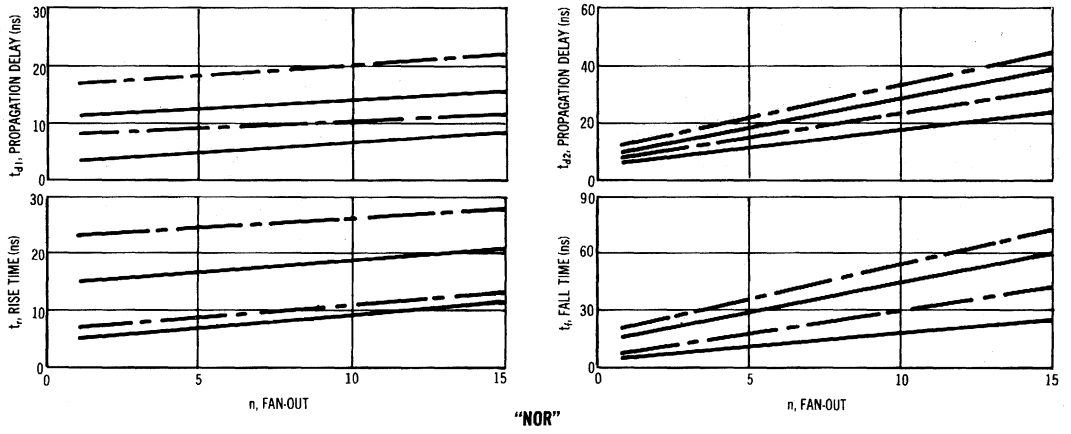
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,3,6,7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—	↓	—	—	↓
	11	—	—	1,3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—	↓	—	—	↓
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—	↓	—	—	↓
	14	—	—	1,3,6,7,9,10,11,12	—	—	4	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_I (2)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_I (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6,9,10,11,12,14	—	—	4	V_I (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_I (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_I (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_I (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_I (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_I (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	6	—	1,3,7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,3,6,7,10,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2⑤	4	$\triangle V_I$ (2)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5⑤	4	$\triangle V_I$ (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8⑤	4	$\triangle V_I$ (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	13⑤	4	$\triangle V_I$ (13)	—	↓	—	↓	—	↓	↓
"NOR" Saturation Breakpoint Voltage	—	—	—	1,3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,3,6,7,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	10①	—	4	V_3 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	12①	—	4	V_3 (13)	—	↓	—	↓	—	↓	↓
Switching Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d1} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)	↓	↓	↓	↓	↓	↓	↓
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)	↓	↓	↓	↓	↓	↓	
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_r (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)	↓	↓	↓	↓	↓	↓	
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)	↓	↓	↓	↓	↓	↓	

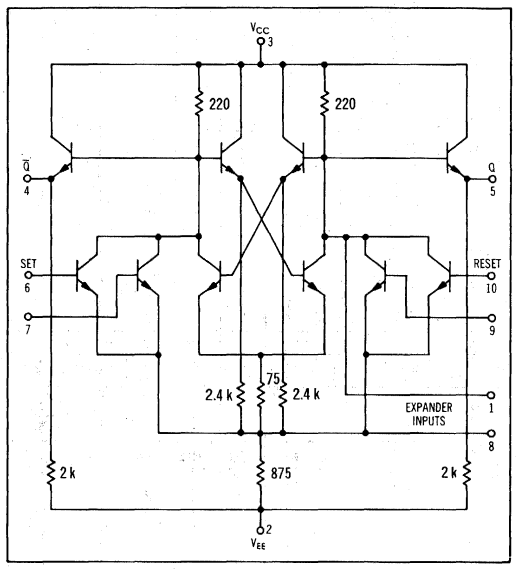
Pins not listed are left open ①Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$. ⑤Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

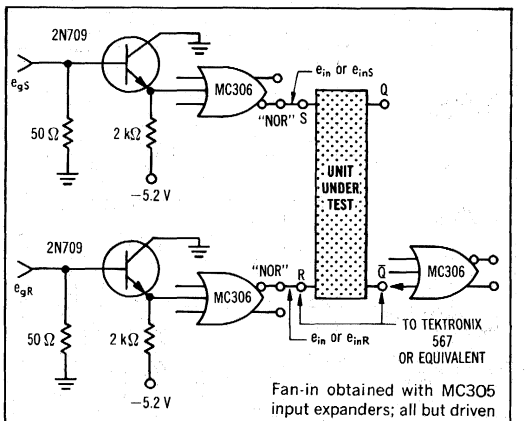


MC302

DC Set-Reset flip-flop with an expandable input and buffered outputs.



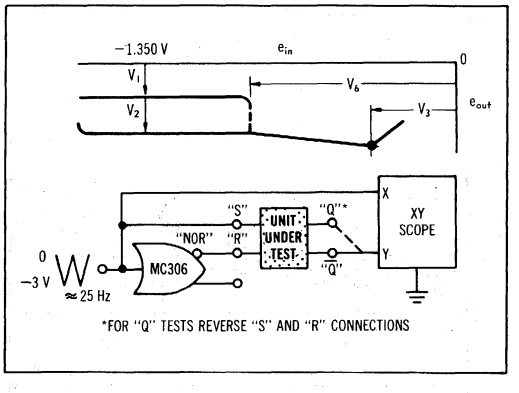
SWITCHING TIME TEST CIRCUIT



Fan-in obtained with MC305 input expanders; all but driven input connected to −5.2 V.

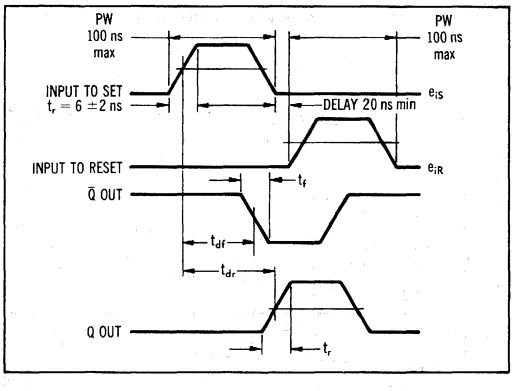
Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

SWITCHING TIME WAVEFORMS



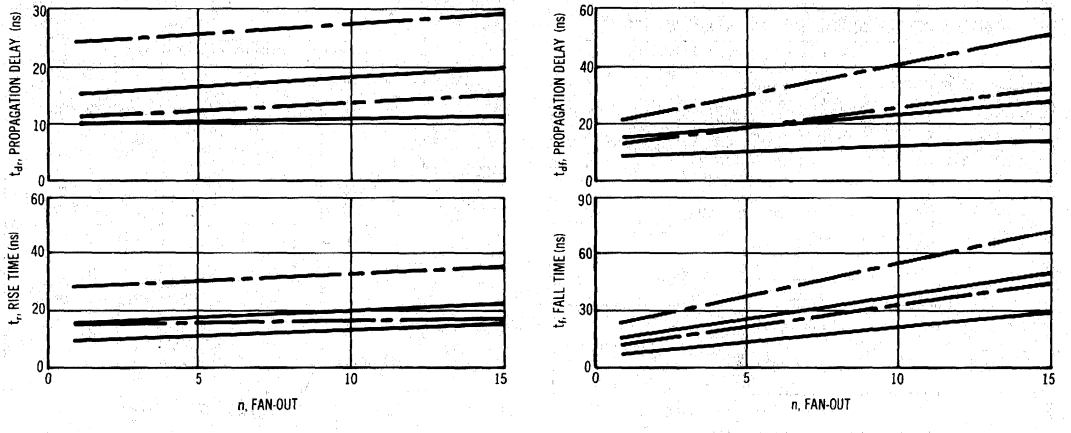
ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%			
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{i\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_E (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,9	6,10④	—	3	V_4 (6,10)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	9.0	14.0	10.5	16.0	22.0	29.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	8.5	14.0	11.5	19.5	16.0	24.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	9.0	15.0	11.5	19.0	23.0	31.0	
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	7.0	13.0	12.5	19.5	18.0	29.0	

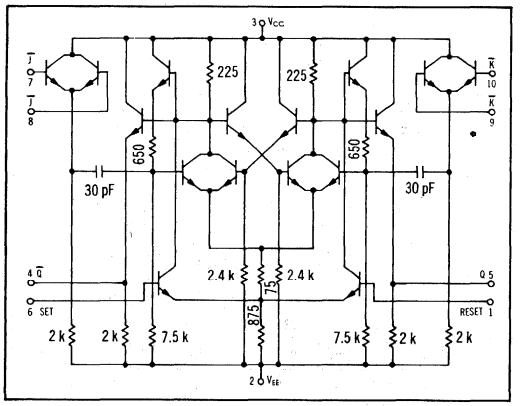
Pins not listed are left open. ①Input voltage is adjusted to obtain dV "$\overline{Q}$"$/dV_{in} = 0$; dV "Q"$/dV_{in} = 0$. ②Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③Apply momentary $V_{i\,max}$ to set output, then V_L for measurement. ④Input voltage is adjusted to obtain $dV_1/dV_{in} \approx \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC308

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS

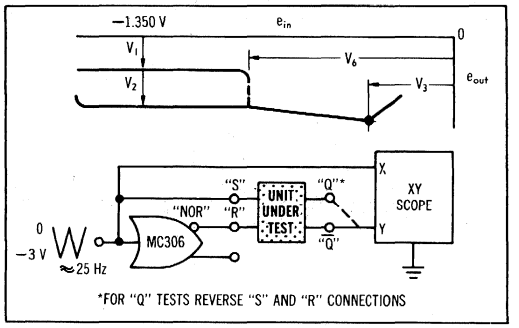


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

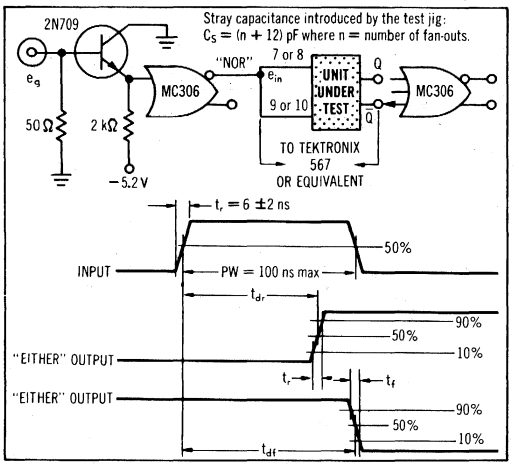


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

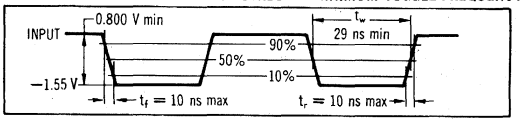


FIGURE 3 – SENSITIVITY (NO TOGGLE)

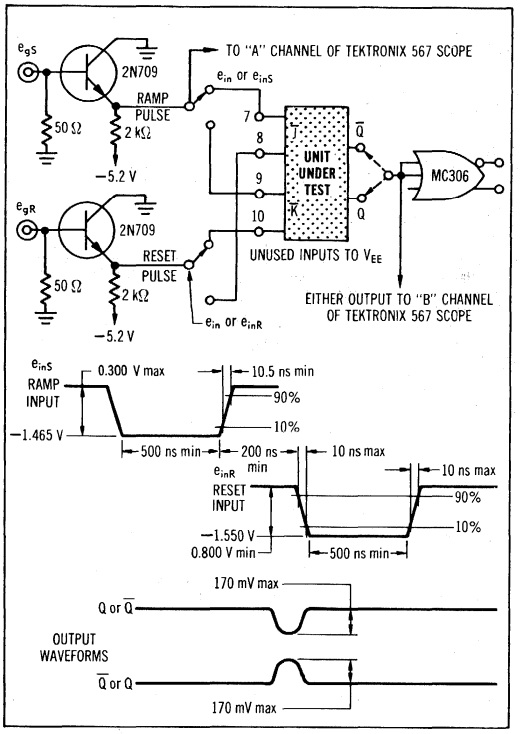
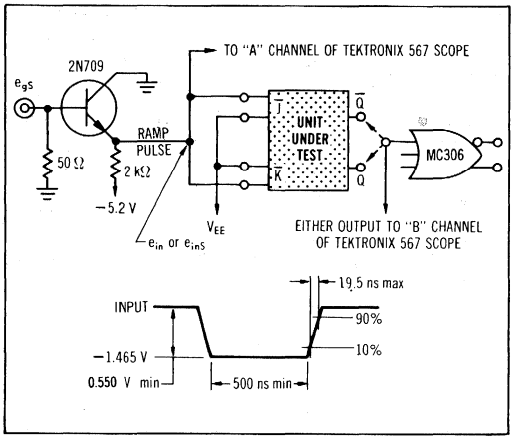


FIGURE 4 – SENSITIVITY (TOGGLE)



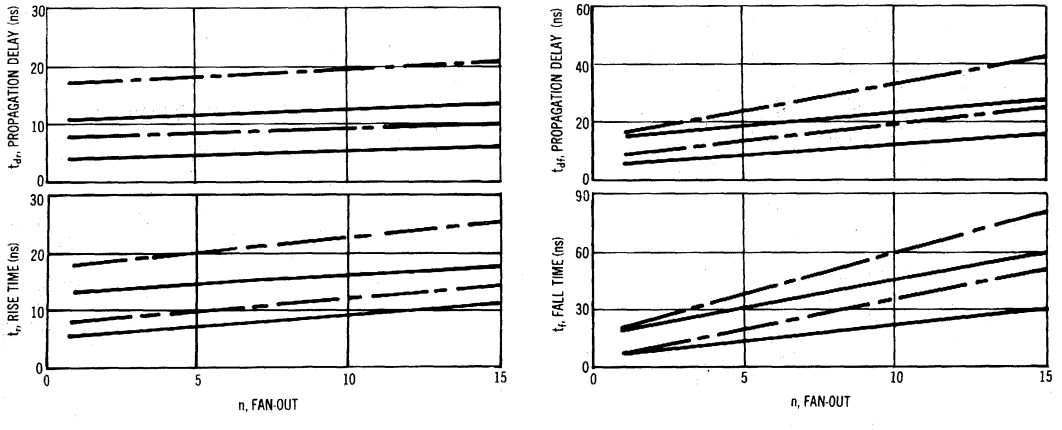
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4②	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6③	—	3	V_8 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{Tog}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5		1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	7,10	4,5		1,2,6,8,9	—	—	3	t_{dr} (4,5)	7.0	11.5	7.0	12.5	9.5	18.5	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	8.5	14.0	8.5	14.5	10.0	16.5	↓
Rise Time	7,10	4,5		1,2,6,8,9	—	—	3	t_r (4,5)	6.5	13.0	6.5	13.0	10.0	18.5	
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	7.5	14.5	8.5	15.5	11.5	20.0	

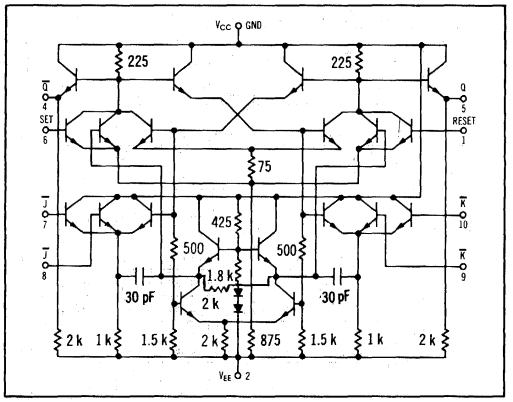
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ③ Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
② Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_I / dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

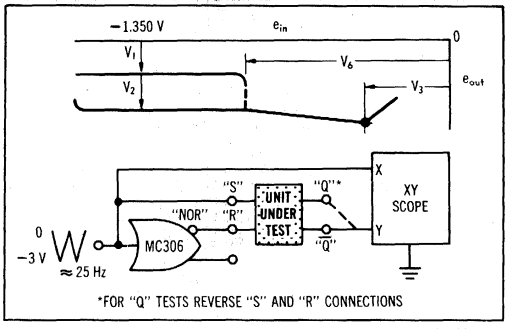


MC314

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

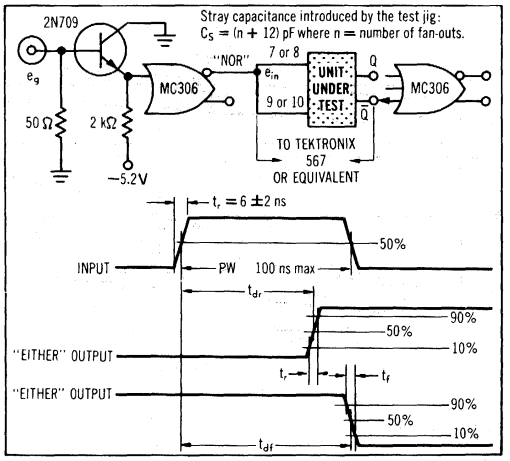


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

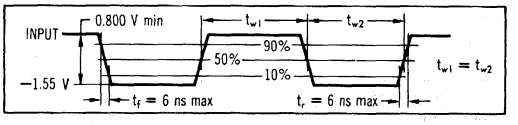


FIGURE 3 – SENSITIVITY (NO TOGGLE)

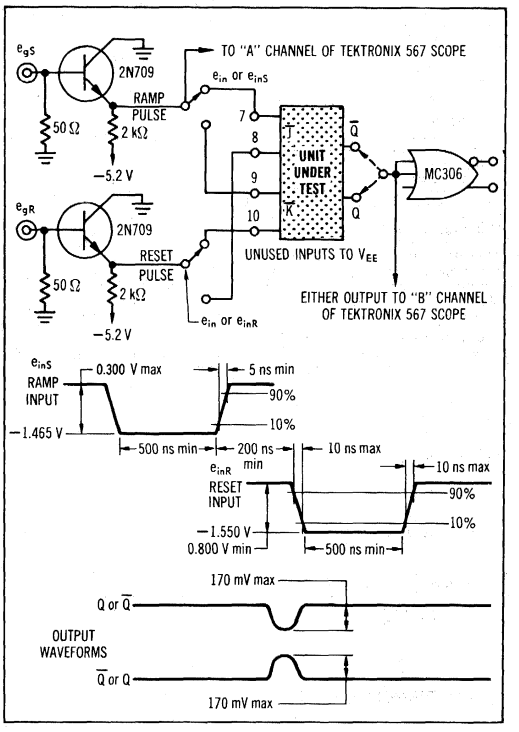
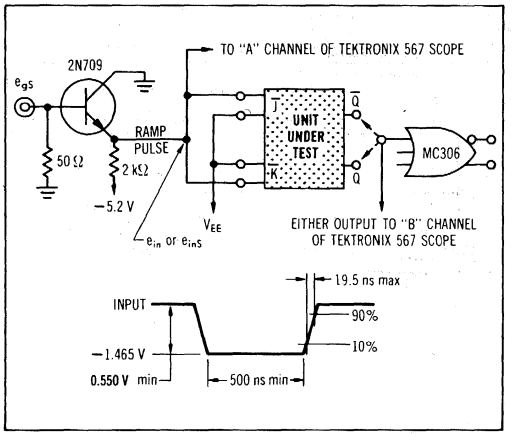


FIGURE 4 – SENSITIVITY (TOGGLE)



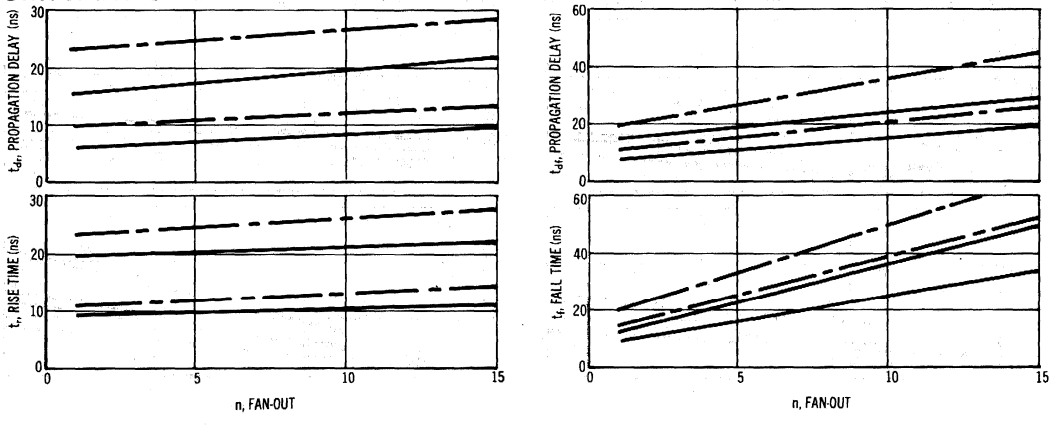
ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%			
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	28.5	—	28.5	—	27.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1④	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5⑤	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\bar{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4②	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6①	—	3	V_6 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5	—	1,2,6,9	—	—	3	f_{Tog}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5	—	1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{dr} (4,5)	11.0	16.0	12.0	16.0	14.0	24.0	ns
	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{df} (4,5)	12.0	16.0	13.0	16.0	15.0	24.0	↓
Rise Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_r (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	
Fall Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	

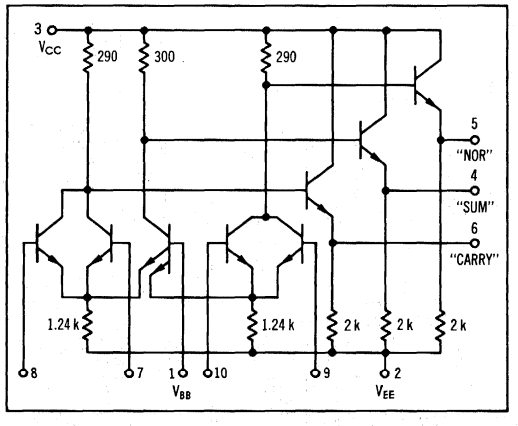
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
② Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_I/dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

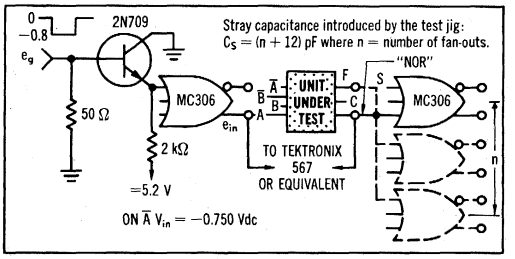


MC303

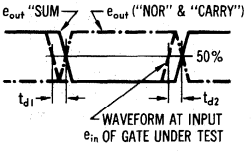
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



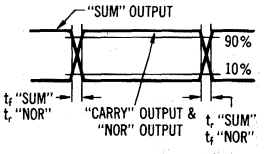
SWITCHING TIMES TEST CIRCUIT



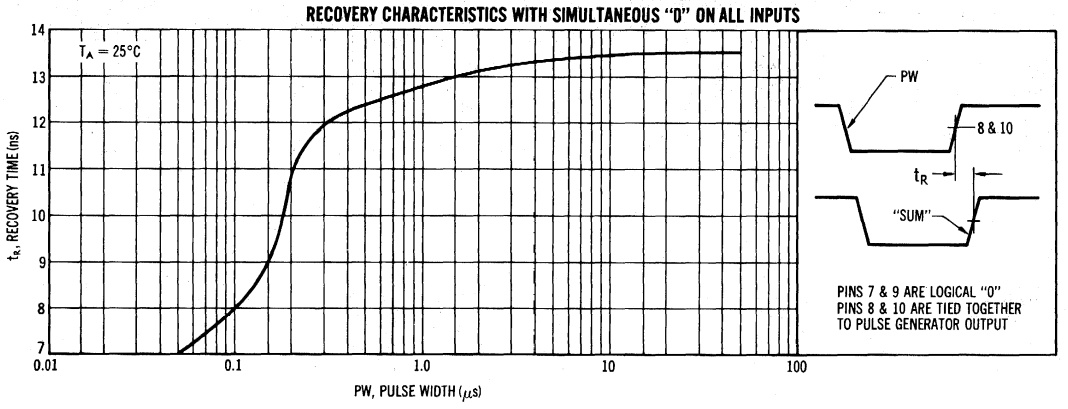
PROPAGATION DELAY



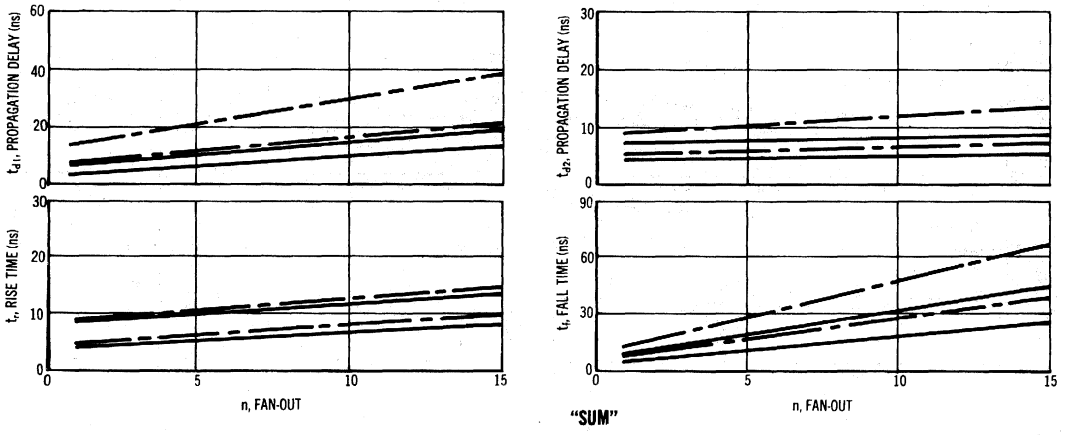
RISE AND FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



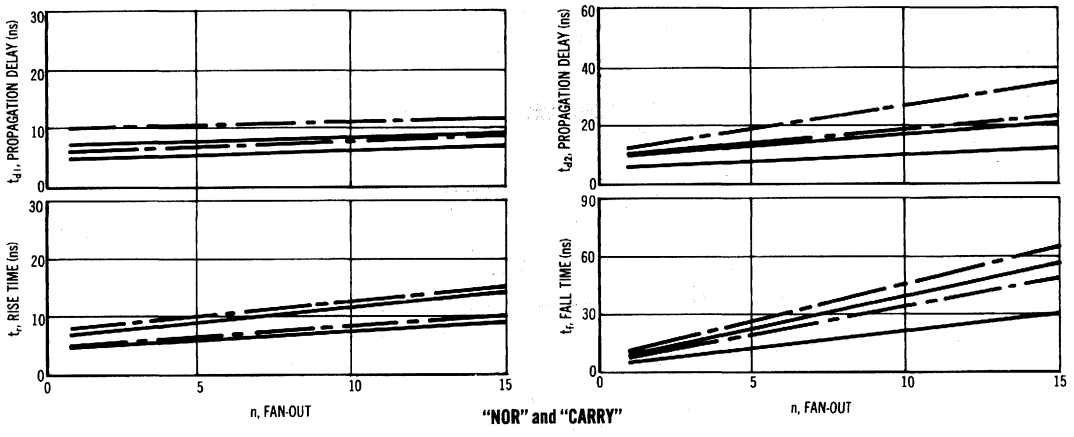
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{RB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.3	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)							
	—	10	7	2,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6②	3	$\triangle V_1$ (6)	—	−0.055	—	−0.055	—	−0.060	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4②	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.65	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.40	—	−0.55	—	−0.65	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.0	10.0	6.0	11.0	7.5	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.0	10.0	6.0	11.0	7.5	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.0	12.0	8.0	12.0	10.5	17.0	
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	7.5	10.5	7.5	11.0	10.0	15.0	
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	7.5	10.5	7.5	11.0	10.0	15.0	
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	5.5	8.0	5.5	8.5	7.5	12.0	
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	6.0	11.5	6.5	12.0	7.5	14.0	
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	6.0	11.5	6.5	12.0	7.5	14.0	
	—	7	—	2,8,9	1	10	4	3	t_r (4)	6.0	10.0	6.5	11.0	10.0	16.0	
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	7.5	12.0	8.0	13.5	10.5	16.5	
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	7.5	12.0	8.0	13.5	10.5	16.5	
	—	7	—	2,8,9	1	10	4	3	t_f (4)	8.0	12.5	8.5	13.5	11.0	18.0	↓

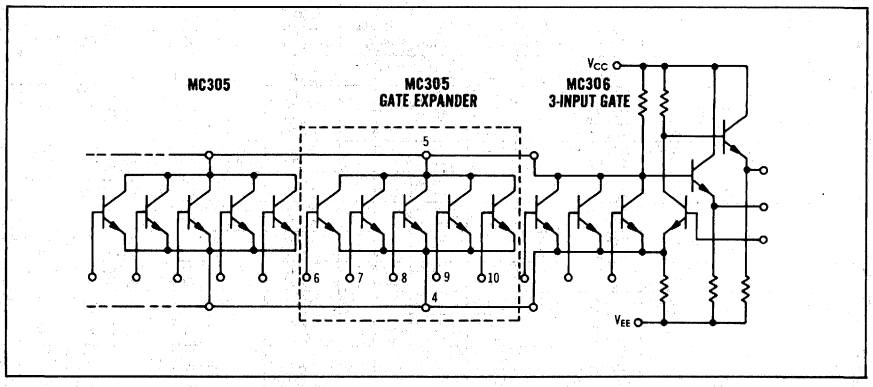
Pins not listed are left open. ① Input voltage is adjusted to obtain dV"NOR"/dV_{in} = 0 or dV "CARRY"/dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC305

A 5-input expander for use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five.



ELECTRICAL CHARACTERISTICS

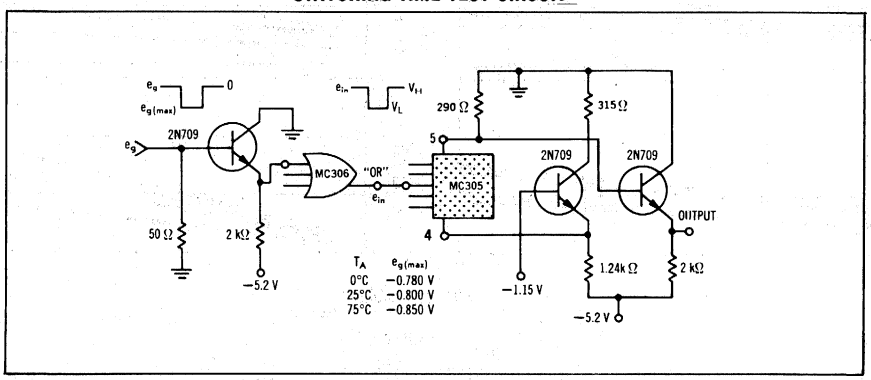
		Test Conditions					
		Vdc ±1%					mAdc
@ Test Temperature	−55°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
	+25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
	+125°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CB} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	μAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—		—		—		
	4	9	—	—	—	—	5	I_{BL} (9)	—		—		—		
	4	10	—	—	—	—	5	I_{BL} (10)	—		—		—		
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	100.0	μAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	−0.810	−0.880	−0.680	−0.730	−0.490	−0.540	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)							
	—	—	—	5	—	4	9	V_{BE} (4)							
	—	—	—	5	—	4	10	V_{BE} (4)							

Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	①	—	—	—	—	—	—	t_{d1}	5.0	8.0	5.0	8.5	5.5	9.5	ns
	8	①	—	—	—	—	—	—	t_{d2}	4.0	8.0	4.0	8.0	4.5	10.0	↓
Rise Time	8	①	—	—	—	—	—	—	t_r	8.0	10.5	8.5	11.5	6.5	13.0	
Fall Time	8	①	—	—	—	—	—	—	t_f	3.0	8.5	3.5	8.5	4.5	9.5	

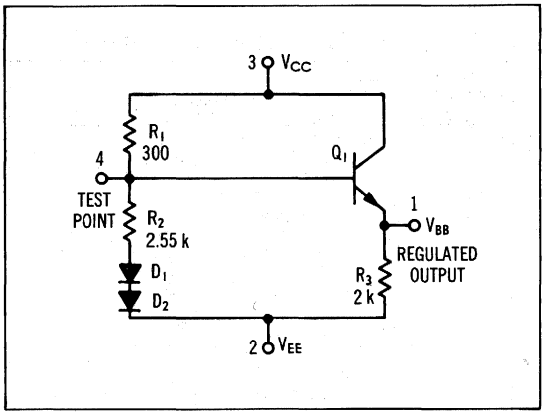
Pins not listed are left open. ①See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



MC304

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ± 1%
@ Test Temperature	−55°C	−5.20
	+25°C	−5.20
	+125°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	2	—	3	I_E(2)	—	4.4	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.19	−1.32	−1.09	−1.22	−0.95	−1.08	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of −55 to +125°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

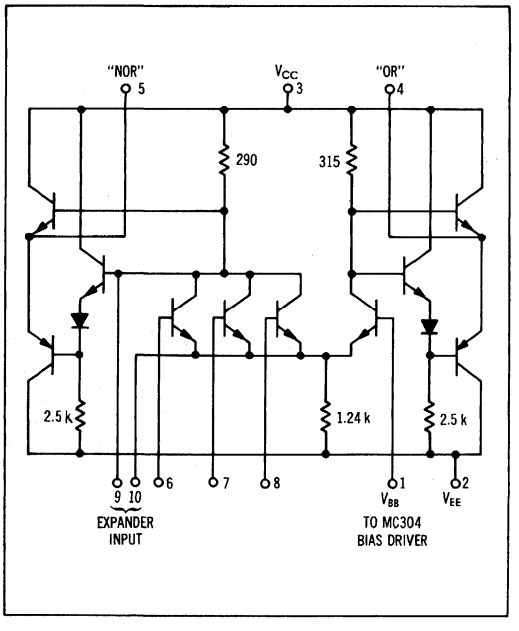
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

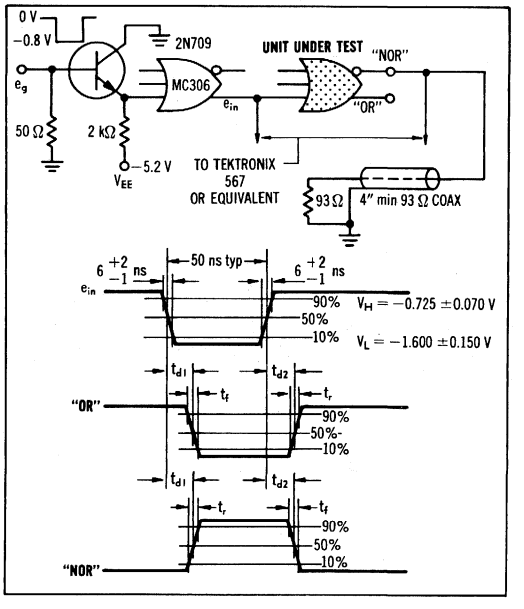
$V_{BB} = -1.15$ nominal output voltage at 25°C

MC315

Line driver for driving lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

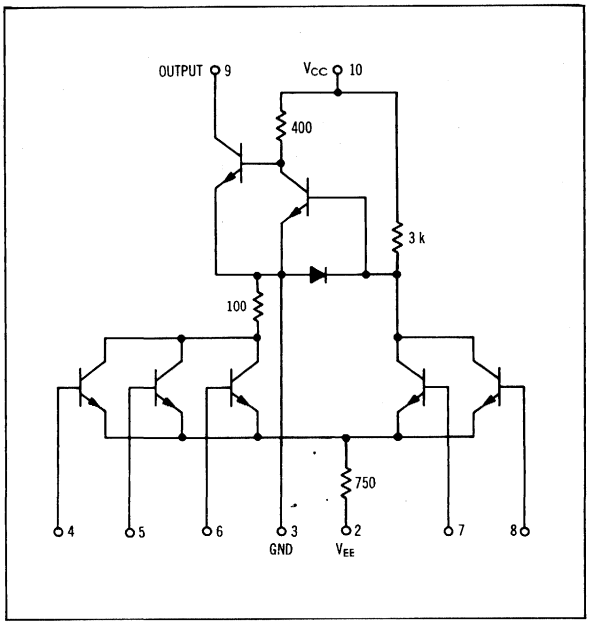
		Test Conditions Vdc ±1%				
@ Test Temperature	−55°C	—	−0.945	−1.450	−5.20	−1.25
	+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
	+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L ① Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8	1	4,5	3	I_E (2)	—	45	—	45	—	45	mAdc
Input Current	6	—	—	2,7,8	1	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_1 (6)	−0.805	−0.945	−0.670	−0.795	−0.505	−0.655	Vdc
	—	—	7	2,6,8	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_4 (6)	−1.540	−1.850	−1.450	−1.750	−1.320	−1.675	Vdc
	—	7	—	2,6,8	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_5 (6)	−0.805	−0.945	−0.670	−0.795	−0.505	−0.655	Vdc
	—	7	—	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_5 (8)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_2 (6)	−1.540	−1.850	−1.450	−1.750	−1.320	−1.675	Vdc
	—	—	7	2,6,8	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_2 (8)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	10.0	20.0	10.0	20.0	15.0	30.0	ns
	6	4	—	2,7,8	1	—	3	t_{d1} (4)	12.0	25.0	12.0	25.0	17.0	34.0	↓
	6	5	—	2,7,8	1	—	3	t_{d2} (5)	12.0	25.0	12.0	25.0	13.0	30.0	↓
	6	4	—	2,7,8	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	25.0	↓
Rise Time	6	5	—	2,7,8	1	—	3	t_r (5)	13.0	25.0	13.0	25.0	16.0	31.0	↓
	6	4	—	2,7,8	1	—	3	t_r (4)	10.0	20.0	10.0	20.0	14.5	26.0	↓
Fall Time	6	5	—	2,7,8	1	—	3	t_f (5)	15.0	35.0	15.0	35.0	20.0	40.0	↓
	6	4	—	2,7,8	1	—	3	t_f (4)	15.0	35.0	15.0	35.0	20.0	40.0	↓

Pins not listed are left open. ①Output is loaded with a 93-ohm resistor.

MC316

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6 V lamps.



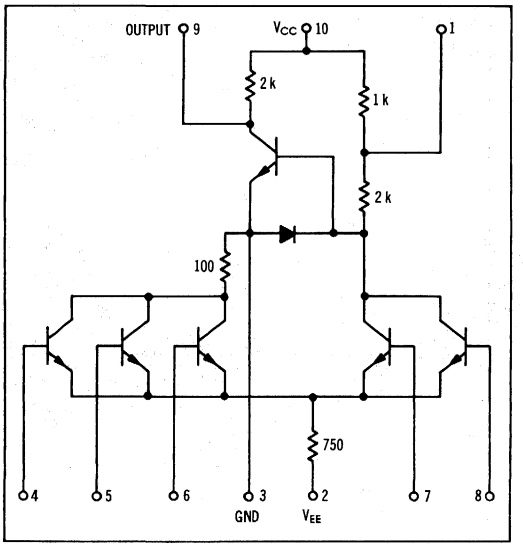
ELECTRICAL CHARACTERISTICS

	Test Conditions										Test Limits						
	Vdc ±1%						mAdc				−55°C		+25°C		+125°C		
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L ② Pin No	Ground Pin No	Symbol Pin No in ( )	Min	Max	Min	Max	Min	Max	Unit
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	100										
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100										
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	50										
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	21.0	—	21.0	—	20.5		
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.0	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—		—	—	
Output Voltage, Low	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	10,9①	—	3	V_{OH} (5)	—	—	—	↓	—		↓
	—	6	—	2,4,5,7	8	10,9①	—	3	V_{OH} (6)	—	—	—		—		
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—		—		

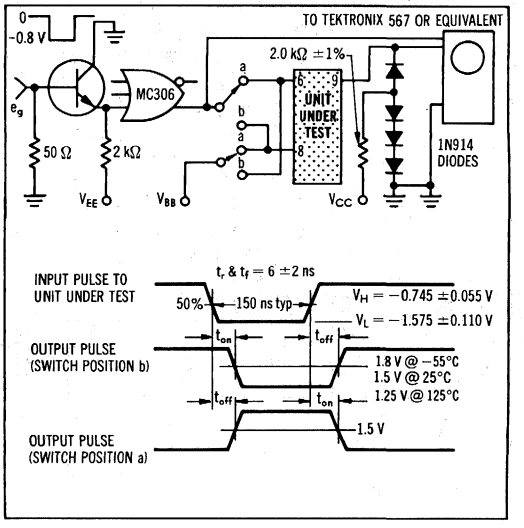
Pins not listed are left open. ①Pin 9 is connected to V_{CC} through a 10 k-ohm resistor.
②I_L specified for ambient temperature conditions. I_L = 100 mAdc at T_C = +125°C is acceptable, requiring a heat sink.

MC317

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS

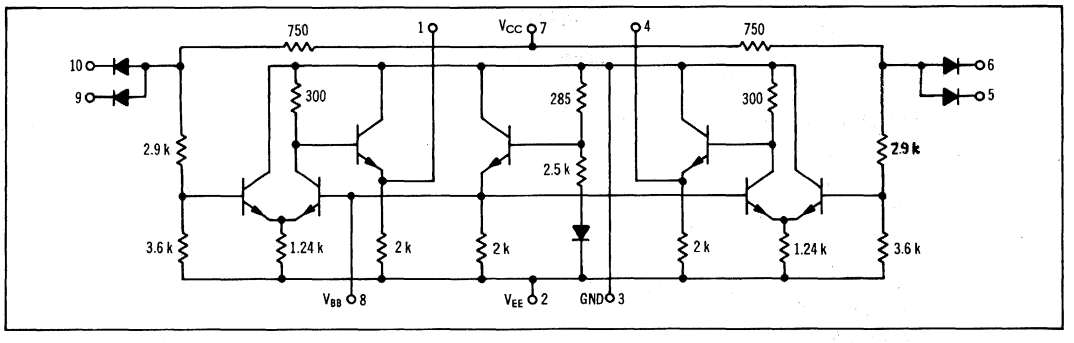


ELECTRICAL CHARACTERISTICS

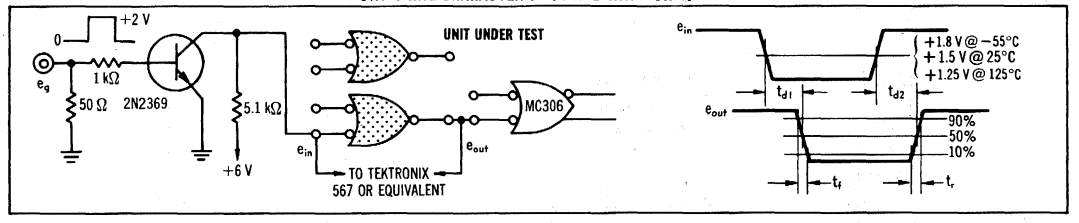
@ Test Temperature	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions																
	Vdc ±1%						mAdc									
−55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	10									
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15	+6.0	10									
+125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	10									
Characteristic																
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.0	—	7.0	—	6.8	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.0	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,8	6	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,6,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,8	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	8	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓
	8	9	—	2,4,5,7	6	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓

MC318

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%			
@ Test Temperature −55°C	+0.45	+5.0	−5.20	+6.0
@ Test Temperature +25°C	+0.45	+5.0	−5.20	+6.0
@ Test Temperature +125°C	+0.45	+5.0	−5.20	+6.0

Characteristic	V Pin No	V Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	2	7	3	I_C (7)	—	4.0	—	4.0	—	3.9	mAdc
	—	—	2	7	3	I_E (2)	—	24.0	—	24.0	—	23.3	mAdc
Input Load Current	—	—	2	7	3,5	I_L (5)	—	—	—	8.0	—	—	mAdc
	—	—	2	7	3,6	I_L (6)	—	—	—	↓	—	—	↓
	—	—	2	7	3,9	I_L (9)	—	—	—		—	—	
	—	—	2	7	3,10	I_L (10)	—	—	—		—	—	
Input Reverse Current	—	—	2	5,7	3,6	I_R (5)	—	—	—	0.5	—	2.0	μAdc
	—	—	2	6,7	3,5	I_R (6)	—	—	—	↓	—	↓	↓
	—	—	2	7,9	3,10	I_R (9)	—	—	—		—		
	—	—	2	7,10	3,9	I_R (10)	—	—	—		—		
"OR" Logical "1" Output Voltage	—	5	2	7	3	V_S (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	6	2	7	3	V_S (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	2	7	3	V_S (1)							
	—	10	2	7	3	V_S (1)							
"OR" Logical "0" Output Voltage	5	—	2	7	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	6	—	2	7	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	9	—	2	7	3	V_2 (1)							
	10	—	2	7	3	V_2 (1)							
Bias Voltage Output Current	—	—	2	7	3	V_{BB} (8)	−1.19	−1.32	−1.09	−1.22	−0.95	−1.08	Vdc
							↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5	4	2	7	3	t_{d1} (4)	16.5	27.0	15.0	23.0	19.0	28.0	ns
	9	1	2	7	3	t_{d1} (1)	16.5	27.0	15.0	23.0	19.0	28.0	↓
	5	4	2	7	3	t_{d2} (4)	13.0	20.0	15.5	23.0	20.0	31.0	
	9	1	2	7	3	t_{d2} (1)	13.0	20.0	15.5	23.0	20.0	31.0	
Rise Time	5	4	2	7	3	t_r (4)	8.0	15.0	7.0	13.0	9.5	16.0	
	9	1	2	7	3	t_r (1)	8.0	15.0	7.0	13.0	9.5	16.0	
Fall Time	5	4	2	7	3	t_f (4)	8.0	14.0	7.5	13.0	10.0	17.0	
	9	1	2	7	3	t_f (1)	8.0	14.0	7.5	13.0	10.0	17.0	↓

Pins not listed are left open.

MECL

INTEGRATED CIRCUITS

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NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C

Function	Type ①	DC Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Case	Page No.
5-Input OR/NOR Gate	MC351	25	7.5	37	71, 72	2-44
R-S Flip-Flop	MC352A	↓	11	42	↓	2-52
Half-Adder	MC353	↓	7.5	63	↓	2-58
Bias Driver	MC354	↓	–	18	↓	2-61
5-Input Gate Expander	MC355	–	4.5	–	↓	2-60
3-Input OR/NOR Gate	MC356	25	7.5	37	↓	2-41
3-Input OR/NOR Gate	MC357	↓	7.5	15	↓	2-41
AC-Coupled J-K Flip-Flop	MC358A	↓	8.5	87	↓	2-54
Dual 2-Input NOR Gate	MC359	↓	7.0	54	↓	2-46
Dual 2-Input NOR Gate	MC360	↓	7.0	54	↓	2-46
Dual 2-Input NOR Gate	MC361	↓	7.0	41	↓	2-46
Dual 3-Input NOR Gate (With Internal Bias)	MC362A	↓	7.5	70	↓	2-48
Quad 2-Input NOR Gate	MC363F	↓	7.0	125	83	2-50
AC-Coupled J-K Flip-Flop	MC364	↓	12	118	71, 72	2-56
Line Driver	MC365	–	14	270 ②	↓	2-62
Lamp Driver	MC366	–	–	135	↓	2-67
Level Translator – MECL to Saturated Logic	MC367	7 (DTL)	27.5	63	↓	2-68
Level Translator – Saturated Logic to MECL	MC368	25 (MECL)	17	105	71, 72	2-69
Dual 4-Input Clock Driver/High-Speed Gate	MC369F	100	3.0	250	83	2-65
Dual 2-Input Clock Driver/High-Speed Gate	MC369G	100	3.0	250	71	2-63

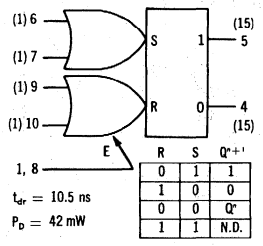
① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC351G = Metal Can, MC351F = Flat Package.)
② With 50-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC350 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC354, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are given on page 2—61

MC352A — R-S FLIP-FLOP

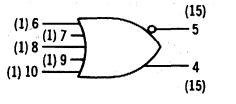


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

t_{dr} = 10.5 ns
P_D = 42 mW

DC Set-Reset flip-flop with expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

MC351 — 5-INPUT GATE



$5 = \overline{6 + 7 + 8 + 9 + 10}$

$4 = 6 + 7 + 8 + 9 + 10$

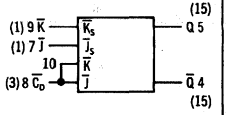
t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC358A — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

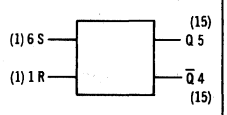
$\overline{J}_s$	$\overline{K}_s$	$\overline{C}_D$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}_s$ and $\overline{K}_s$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}_s$ and $\overline{K}_s$ inputs would be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



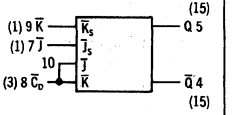
t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC364 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

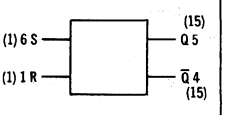
$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

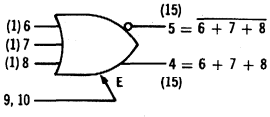
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

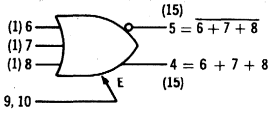
MC356 — 3-INPUT GATE



t_{dl} = 7.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC357 — 3-INPUT GATE

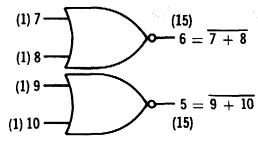


t_{dl} = 7.0 ns
P_D = 15 mW

*No pull-down resistors

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC356, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on page 2-41).

MC359 — DUAL 2-INPUT GATE

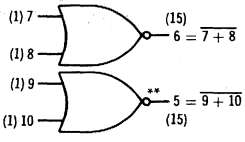


t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

LOGIC DESCRIPTION (continued)

MC360 — DUAL 2-INPUT GATE

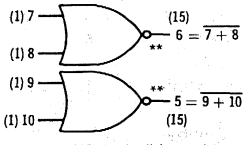


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

t_{pl} = 6.5 ns P_D = 27 mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor optional (see schematic diagram on page 2-46).

MC361 — DUAL 2-INPUT GATE

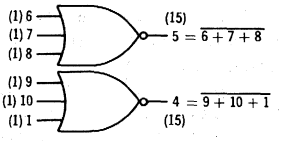


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5 or pin 6.

t_{pl} = 6.5 ns P_D = 21 mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor omitted and the second optional (see schematic diagram on page 2-46).

MC362A — DUAL 3-INPUT GATE

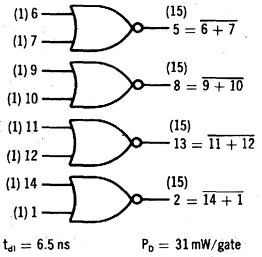


t_{pl} = 7.5 ns

P_D = 35 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver. This gate without the bias driver is available as the MC362.

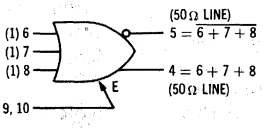
MC363F — QUAD 2-INPUT GATE



t_{pl} = 6.5 ns P_D = 31 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC365 — LINE DRIVER

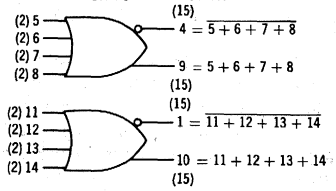


t_{pl} = 14 ns

P_D = 270 mW (with 50 Ω load)

Drives lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC369F — HIGH-SPEED CLOCK DRIVER OR DUAL 4-INPUT GATE

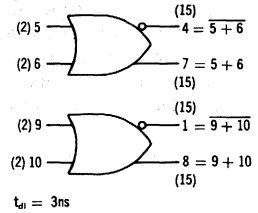


t_{pl} = 3 ns

P_D = 125 mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC369G — HIGH-SPEED CLOCK DRIVER OR DUAL 2-INPUT GATE

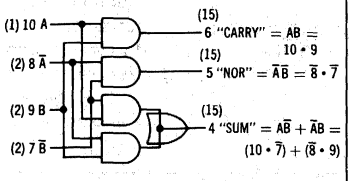


t_{pl} = 3ns

P_D = 125 mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC353 — HALF-ADDER

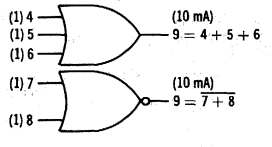


t_{pl} = 7 ns

P_D = 63 mW

Provides the "SUM", "CARRY", and "NOR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

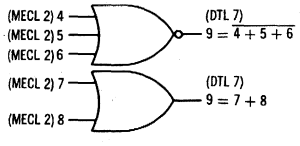
MC366 — LAMP DRIVER



P_D = 135 mW

Capable of driving 6-volt lamps. Positive "NOR" function is obtained by applying V_{ss} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "OR" is obtained by applying V_{ss} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC367 — LEVEL TRANSLATOR

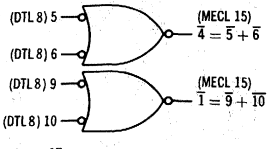


t_{dr} = 30 ns

P_D = 63 mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NOR" function is obtained by applying V_{ss} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "OR" is obtained by applying V_{ss} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC368 — LEVEL TRANSLATOR

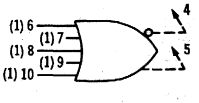


t_{df} = 17 ns

P_D = 105 mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC355 — 5-INPUT EXPANDER



t_{pl} = 5 ns

For use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

"0" = −1.55 V
"1" = −0.75 V
} typical

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

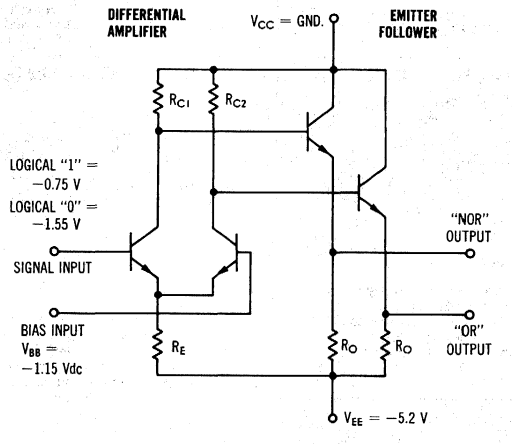
A fixed bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE} drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE} drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC354. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V
FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

DEFINITIONS

e_{in} AC signal applied to the input

e_{out} AC signal at the output

I_C Amount of current drawn from the positive power supply by the test unit

I_{CEX} Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential

I_E Amount of current drawn from the test unit by the negative power supply

I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input

I_L Current drawn from a node when that node is at ground potential

t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge

t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge

t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge

t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge

t_f Time required for the output pulse to go more negative from its 90% point to its 10% point

t_r Time required for the output pulse to go more positive from its 10% point to its 90% point

V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input

V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input

V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero

V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input

V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input

V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity

V_H Logical "1" input voltage

V_L Logical "0" input voltage

V_{OH} High-level output voltage when the saturated logic circuit output is in an "off" condition

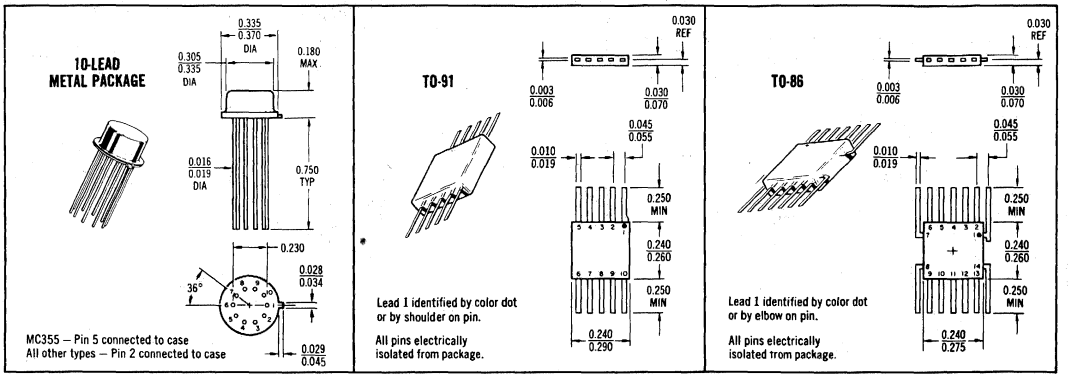
V_{OL} Low-level output voltage when the saturated logic output circuit is in an "on" condition

ΔV_1 Change in the "1" level output voltage as the
ΔV_5 load is varied from no load to full load

PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

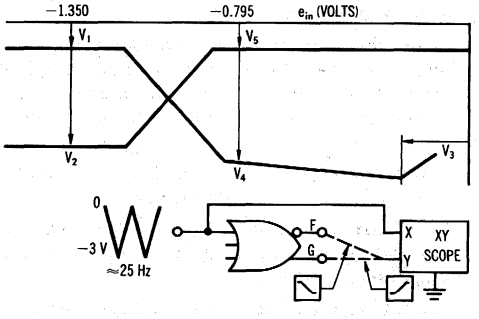
Exceptions: Types MC363F and MC369F are available only in the TO-86, 14-lead flat package; type MC369G is available only in the metal package.

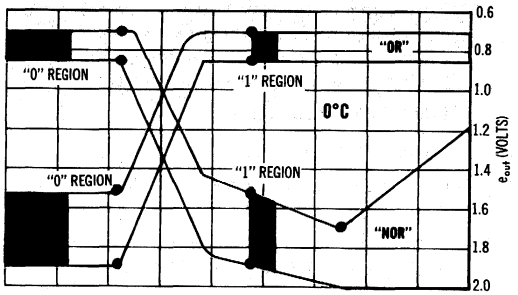


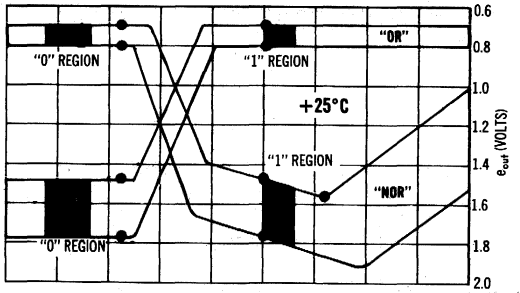
WORST-CASE TRANSFER CHARACTERISTICS

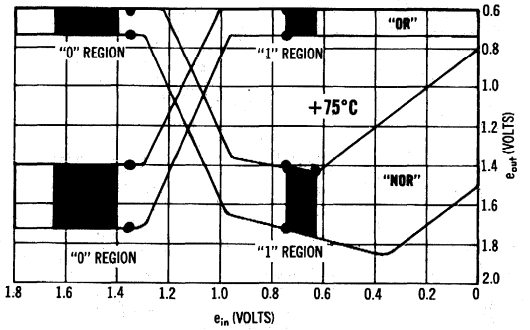
The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS









MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−10	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

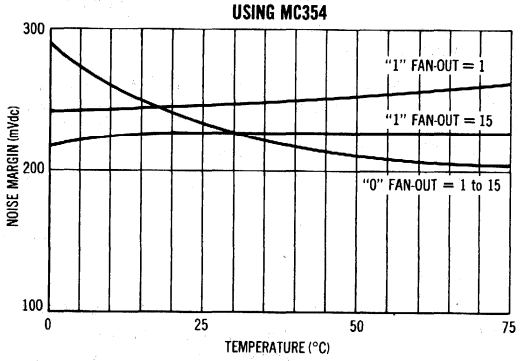
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

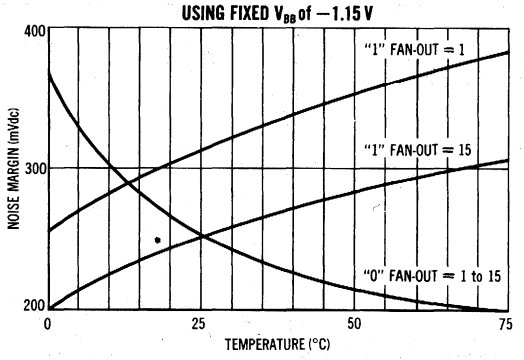
The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC354 bias driver, as compared with non-compensated fixed bias source, bottom.

Note: Any unused input should be connected to V_{EE}.

USING MC354

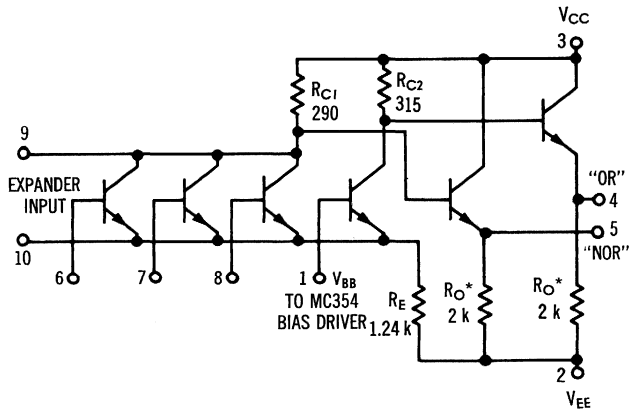


USING FIXED V_{BB} of −1.15 V



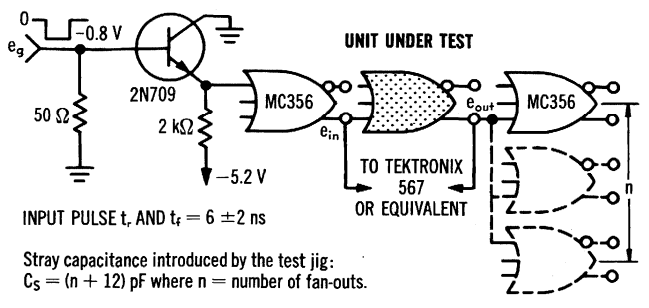
MC356 • MC357

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC357 omits output pull-down resistors, permitting reduction of power dissipation.

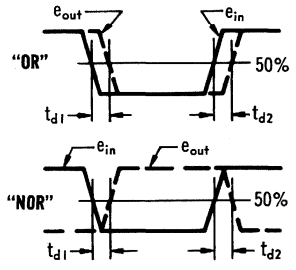


*Resistors R_O are omitted in MC357 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

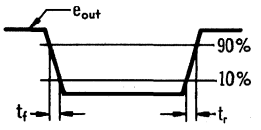
SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY

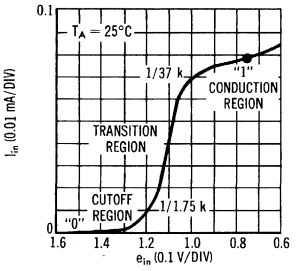


RISE AND FALL TIME

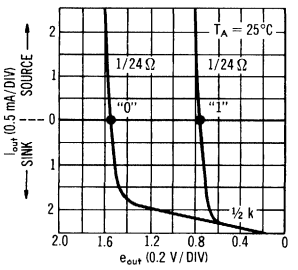


Fan-in obtained with MC355 input expanders; all but driven input connected to −5.2 V.

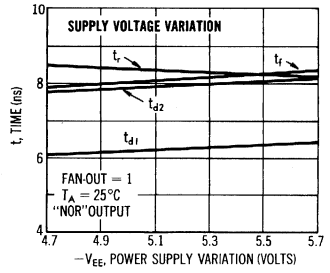
TYPICAL INPUT CHARACTERISTICS

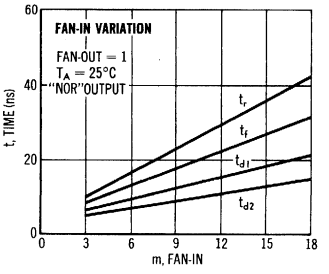


TYPICAL OUTPUT CHARACTERISTICS

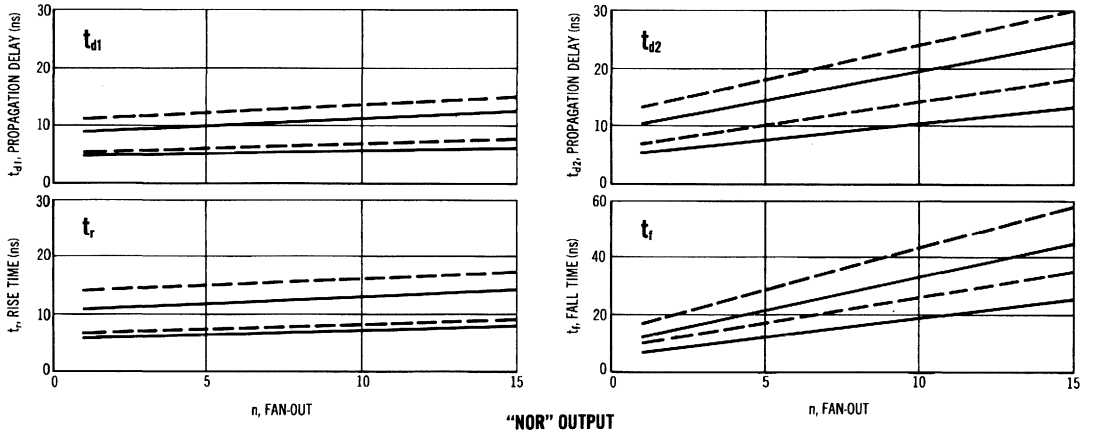


TYPICAL SWITCHING TIME VARIATIONS MC356





SWITCHING CHARACTERISTICS (10% to 90% distribution)



ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%				
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08

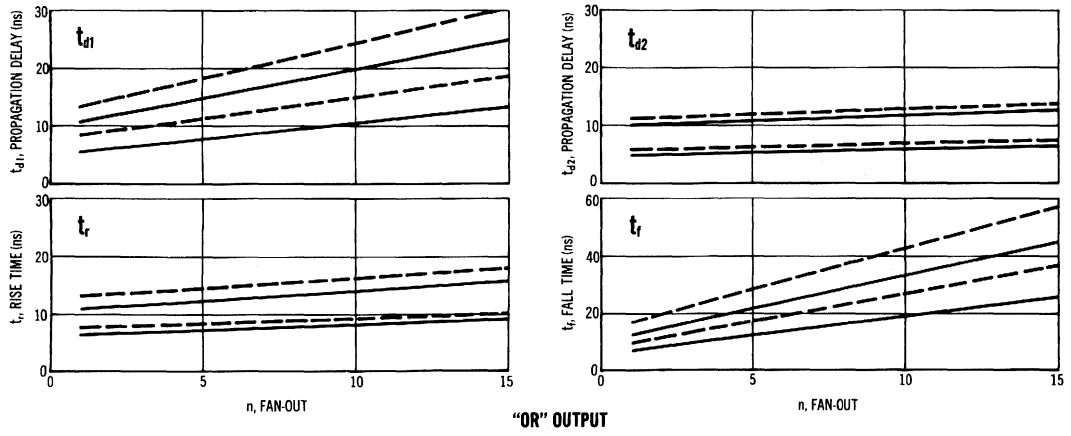
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current MC356	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	9.25	—	8.85	—	8.15	mAdc
MC357	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	3.8	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,8	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,8	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,8	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8	1	—	5⑤	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8	1	—	4⑤	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8	1	6①	—	3	V_3 (5)	—	− 0.51	—	− 0.55	—	− 0.63	Vdc
	—	—	—	2,6,8	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8	1	—	—	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	
	6	5	—	2,7,8	1	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	4	—	2,7,8	1	—	—	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	
	6	5	—	2,7,8	1	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	4	—	2,7,8	1	—	—	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	
	6	5	—	2,7,8	1	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	↓

Pins not listed are left open

① Input voltage is adjusted to obtain dV "NOR / dV_{in} = 0.

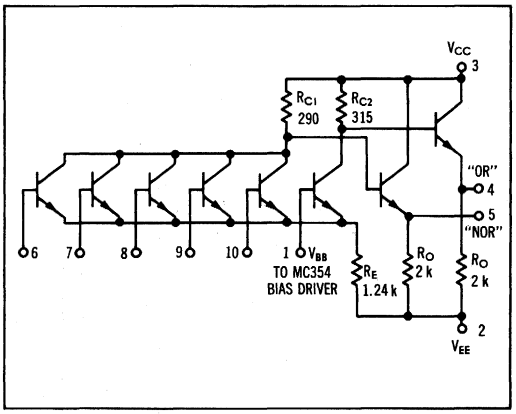
⑤ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

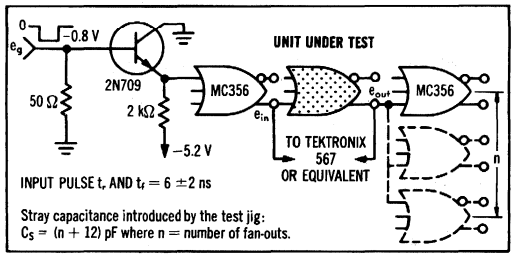


MC351

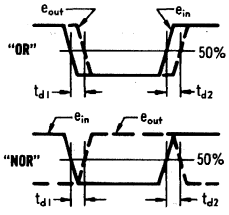
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



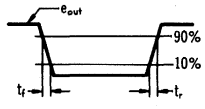
SWITCHING TIME TEST CIRCUIT



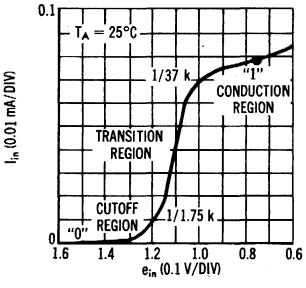
PROPAGATION DELAY



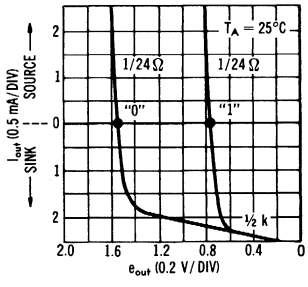
RISE AND FALL TIME



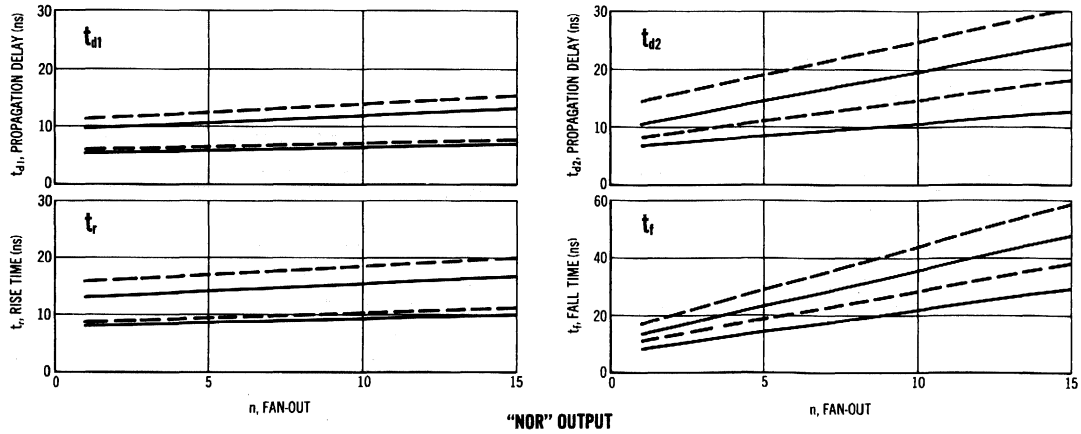
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



ELECTRICAL CHARACTERISTICS

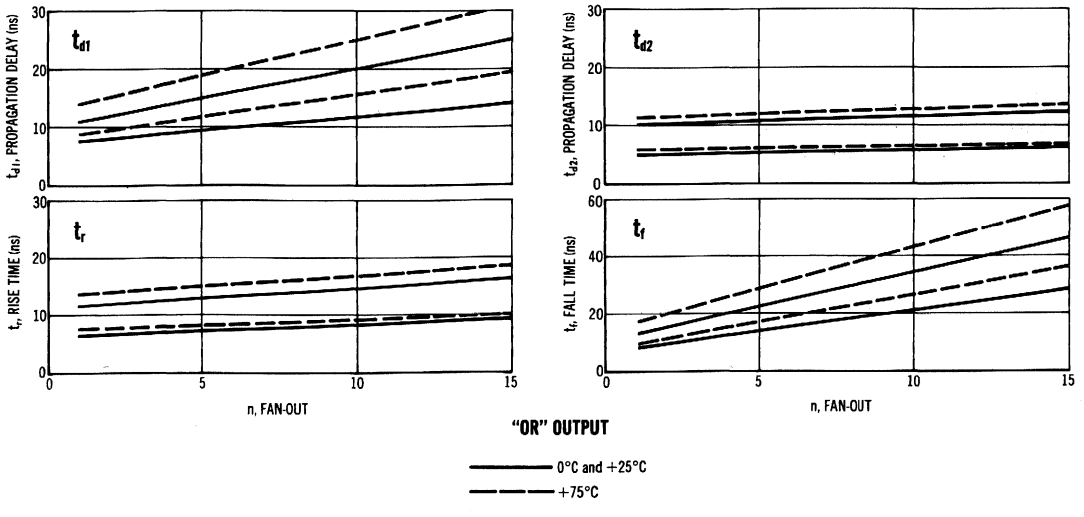
	Test Conditions Vdc ±1%				
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	9.25	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,6,7,8,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5⑤	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4⑤	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	− 0.51	—	− 0.55	—	− 0.63	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	9.0	12.5	9.0	12.5	9.5	16.0	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	7.0	11.0	7.0	11.0	7.5	13.0	↓
	6	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	6.5	11.0	6.5	11.0	7.5	13.0	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	8.5	12.5	8.5	12.5	10.0	16.0	↓
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	8.0	12.0	8.0	12.0	9.5	15.5	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	9.5	14.5	10.0	14.5	11.0	17.0	↓
Fall Time	6	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	9.5	15.0	10.0	15.0	11.0	17.5	↓
	6	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	9.0	15.0	9.5	15.0	10.5	17.5	↓

Pins not listed are left open

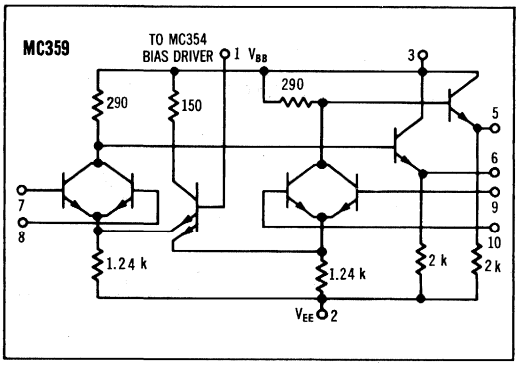
① Input voltage is adjusted to obtain dV "NOR / dV_{in} = "0".

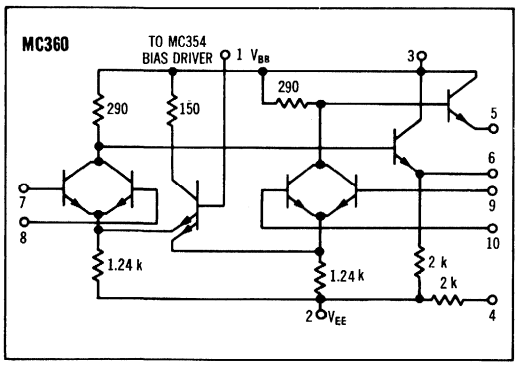
⑤ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

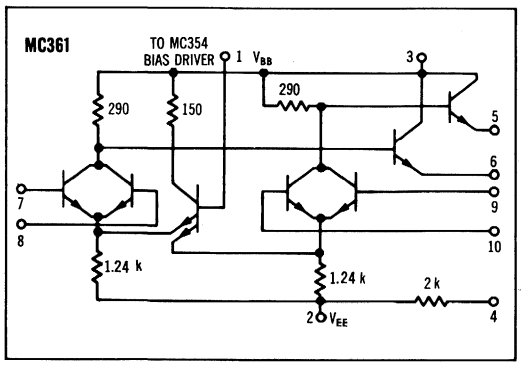


MC359 • MC360 • MC361

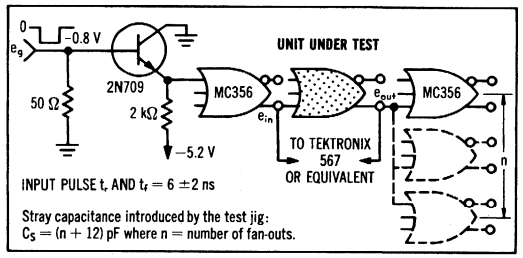
Dual 2-input gates that provide the positive logic "NOR" function. MC359 has two output pull-down resistors; MC360 has one of the output pull-down resistors optional; MC361 omits one output pull-down resistor and has the second optional.



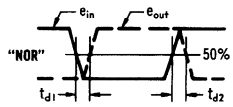




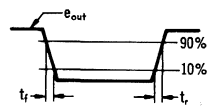
SWITCHING TIME TEST CIRCUIT



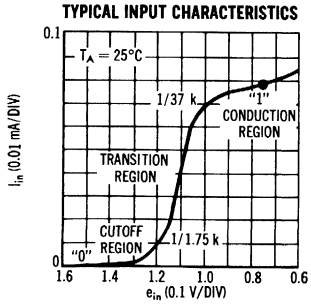
PROPAGATION DELAY



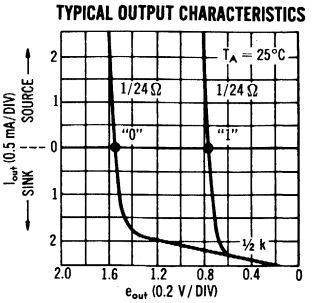
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



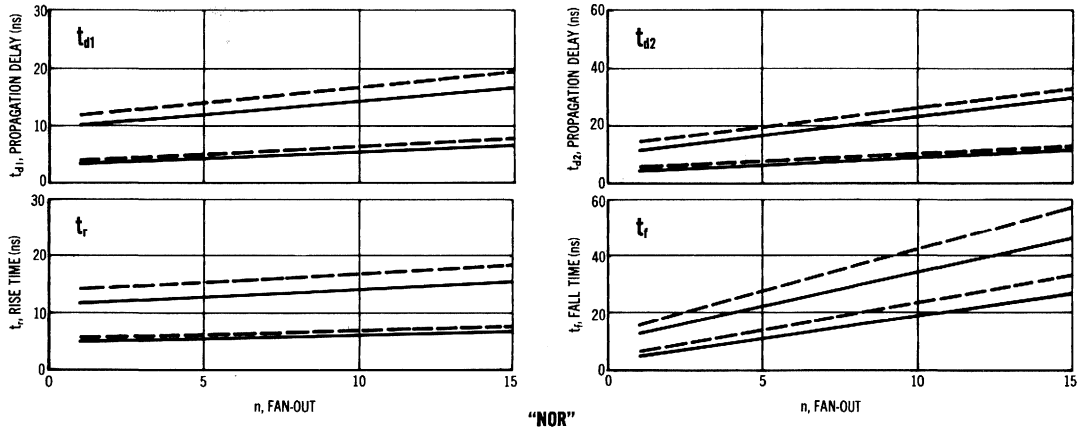
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply MC359, MC360	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.55	—	13.0	—	12.0	mAdc
Drain Current MC361	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	10.5	—	10.1	—	9.2	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	
"NOR" Logical "1"	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
Output Voltage	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0"	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
Output Voltage	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)							
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	—	2,7,8,9,10	1	—	6②	3	$\triangle V_1$ (6)	—	−0.055	—	−0.055	—	−0.065	Vdc
(No load to full load)	—	—	—	2,7,8,9,10	1	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.065	Vdc
"NOR" Saturation	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.51	—	−0.55	—	−0.63	Vdc
Breakpoint Voltage	—	—	—	2,7,9,10	1	8①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	6	—	2,8,9,10	1	—	—	3	t_{d1} (6)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	10	5	—	2,7,8,9	1	—	—	3	t_{d1} (5)	6.5	11.0	6.5	11.0	8.0	14.5	↓
	7	6	—	2,8,9,10	1	—	—	3	t_{d2} (6)	8.5	13.5	8.5	13.5	10.0	16.0	
	10	5	—	2,7,8,9	1	—	—	3	t_{d2} (5)	8.5	13.5	8.5	13.5	10.0	16.0	
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	8.5	12.5	9.0	12.5	11.0	15.5	
	10	5	—	2,7,8,9	1	—	—	3	t_r (5)	8.5	12.5	9.0	12.5	11.0	15.5	
Fall Time	7	6	—	2,8,9,10	1	—	—	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	
	10	5	—	2,7,8,9	1	—	—	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	↓

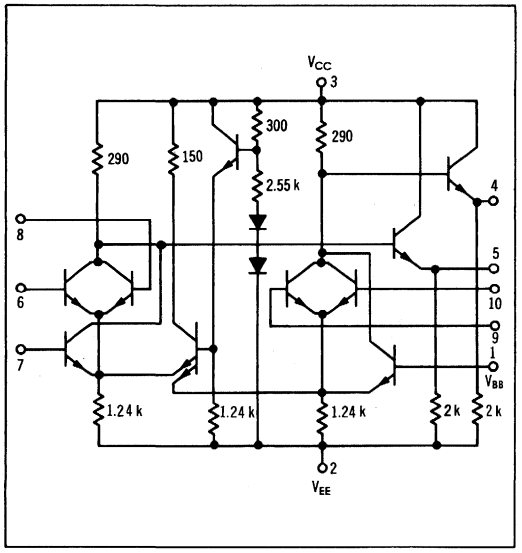
Pins not listed are left open For MC360, connect pin 4 to pin 5 for all tests ① Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

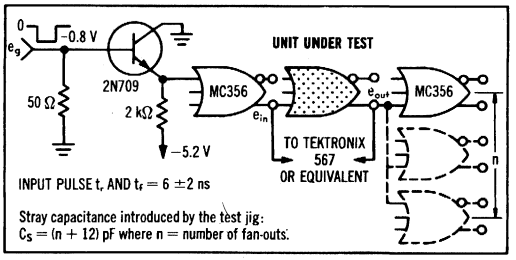


MC362A

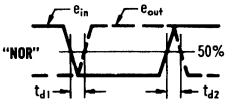
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC362.



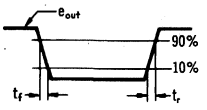
SWITCHING TIME TEST CIRCUIT



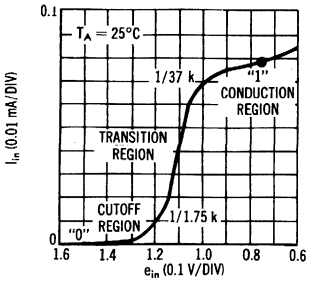
PROPAGATION DELAY



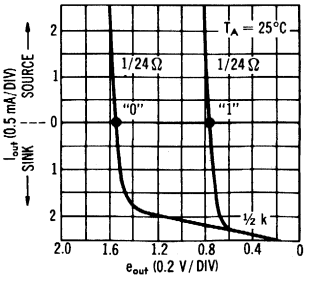
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



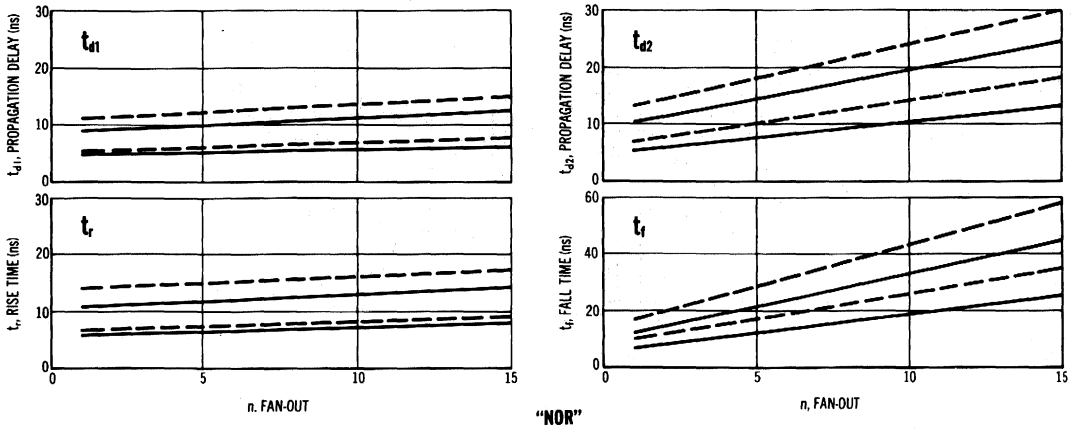
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5⑤	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	1	2,6,7,8,9,10	—	4⑤	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—		—		—		
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

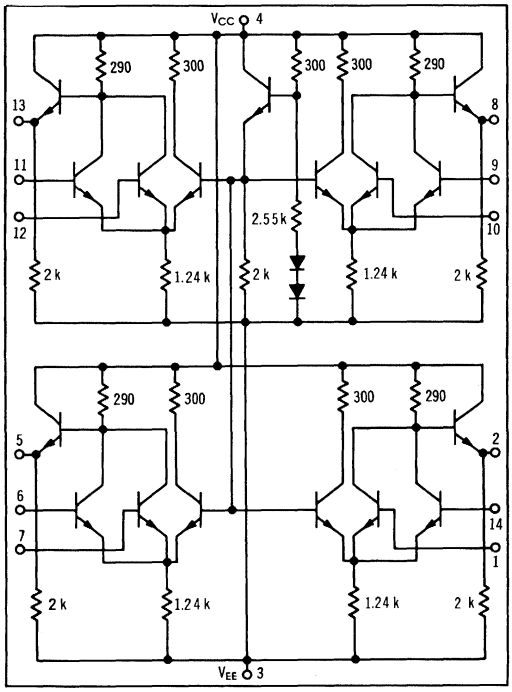
Pins not listed are left open.
①Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ⑤Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

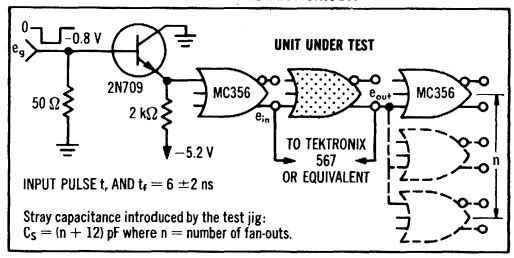


MC363F

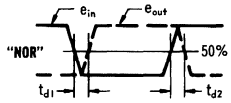
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



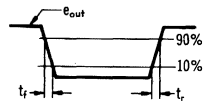
SWITCHING TIME TEST CIRCUIT



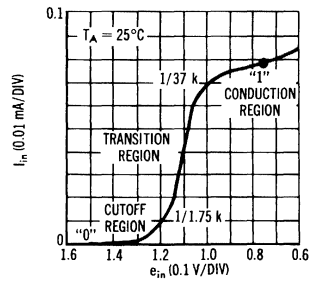
PROPAGATION DELAY



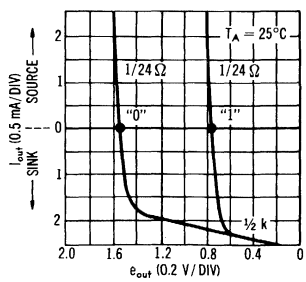
RISE AND FALL TIME



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL INPUT CHARACTERISTICS



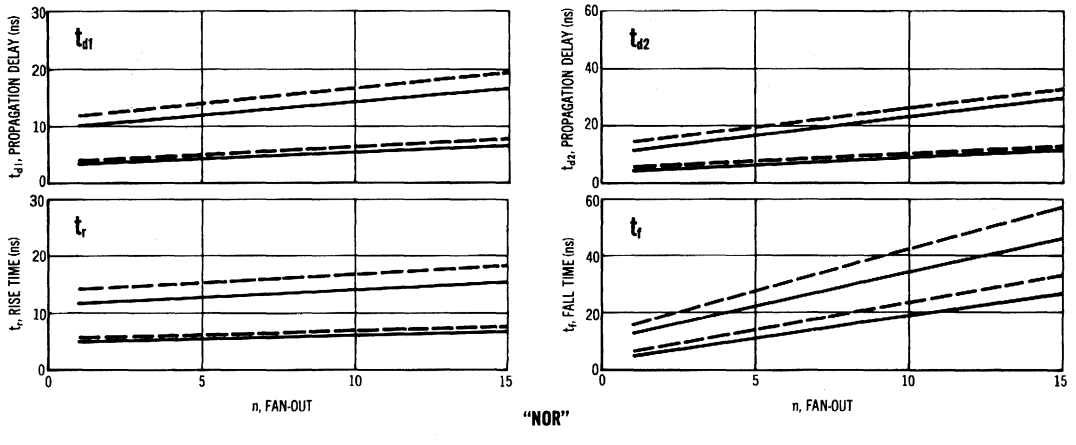
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,3,6,7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—	↓	—	—	↓
	11	—	—	1,3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—	↓	—	—	↓
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—	↓	—	—	↓
	14	—	—	1,3,6,7,9,10,11,12	—	—	4	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_1 (2)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_1 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	6	—	1,3,7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,3,6,7,10,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2②	4	$\triangle V_1$ (2)	—	0.055	—	0.055	—	0.065	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5②	4	$\triangle V_1$ (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8②	4	$\triangle V_1$ (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	13②	4	$\triangle V_1$ (13)	—	↓	—	↓	—	↓	↓
"NOR" Saturation Breakpoint Voltage	—	—	—	3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	0.51	—	0.55	—	0.63	Vdc
	—	—	—	1,3,6,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,11,12,14	10①	—	4	V_3 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,14	12①	—	4	V_3 (13)	—	↓	—	↓	—	↓	↓
Switching Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d1} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)	↓	↓	↓	↓	↓	↓	↓
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)	↓	↓	↓	↓	↓	↓	
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_r (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)	↓	↓	↓	↓	↓	↓	
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)	↓	↓	↓	↓	↓	↓	

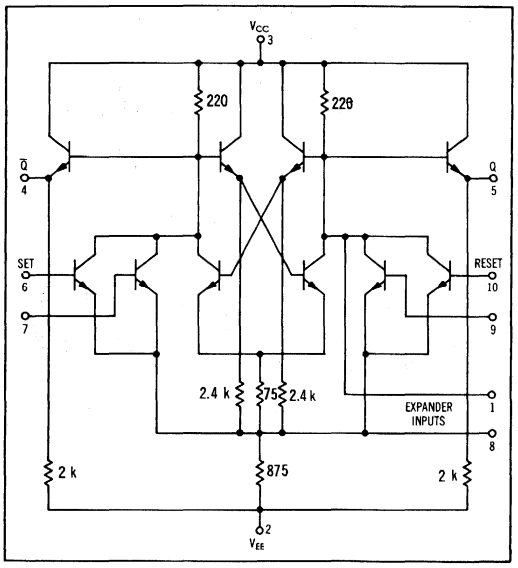
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

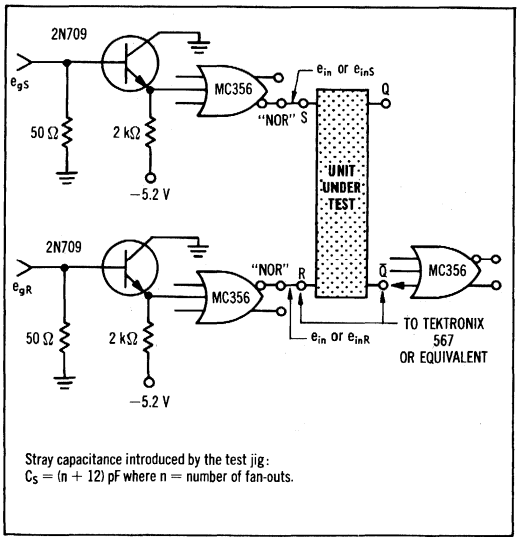


MC352A

DC Set-Reset flip-flop with an expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

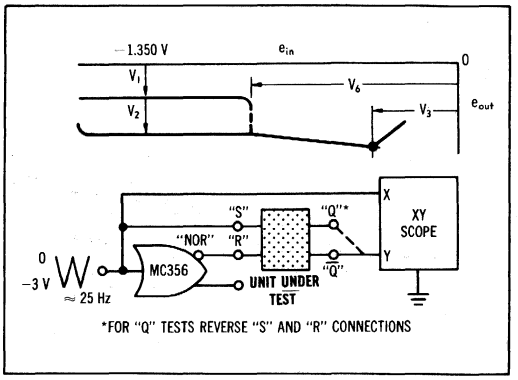


SWITCHING TIME TEST CIRCUIT



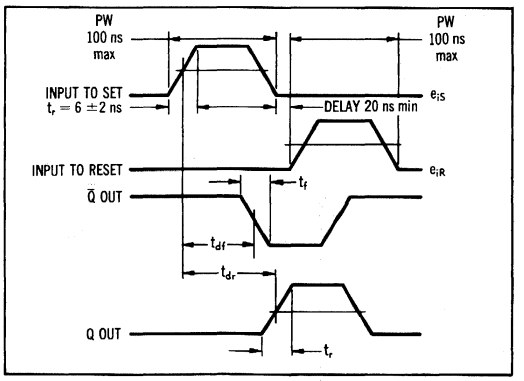
Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

SWITCHING TIME WAVEFORMS

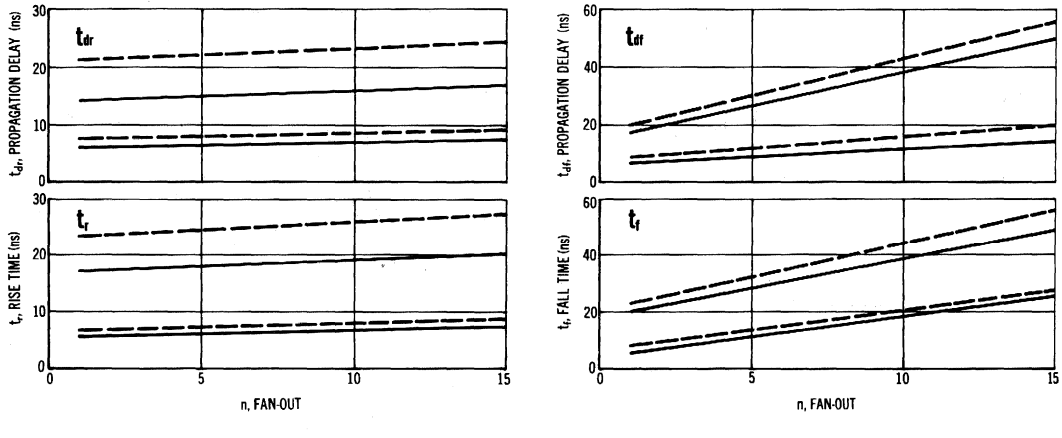


ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_H Pin No	$V_{i\,max}$ Pin No	V_L ② Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
	Test Conditions Vdc ±1%														
0°C	—	−0.850	−1.350	−5.20											
+25°C	−0.670	−0.795	−1.350	−5.20											
+75°C	—	−0.725	−1.350	−5.20											
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_E (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"Q" Logical "1" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	10	2,6,7,9	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,6,7,9	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5③	3	ΔV_1 (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\bar{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4③	3	ΔV_1 (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.61	—	−0.65	—	−0.73	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.61	—	−0.65	—	−0.73	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,9	6,10④	—	3	V_4 (6,10)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	10.0	16.0	10.5	16.0	13.5	22.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	11.0	19.5	11.5	19.5	14.0	22.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	11.0	19.0	11.5	19.0	13.5	26.0	↓
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	12.0	19.5	12.5	19.5	14.0	26.0	↓

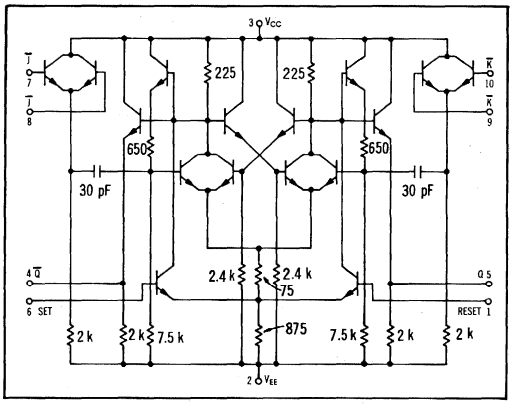
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "Q" / dV_{in} = 0; dV "$\bar{Q}$" / dV_{in} = 0. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
② Apply momentary $V_{i\,max}$ to set output, then V_L for measurement. ④ Input voltage is adjusted to obtain $dV_1 / dV_{in} \approx \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC358A

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS

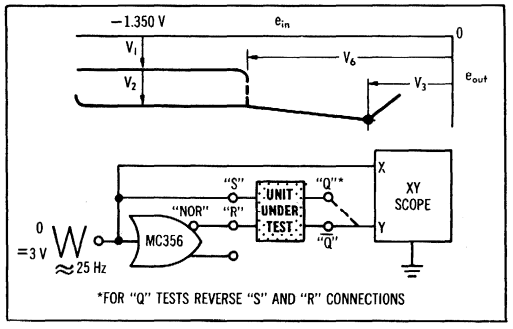


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

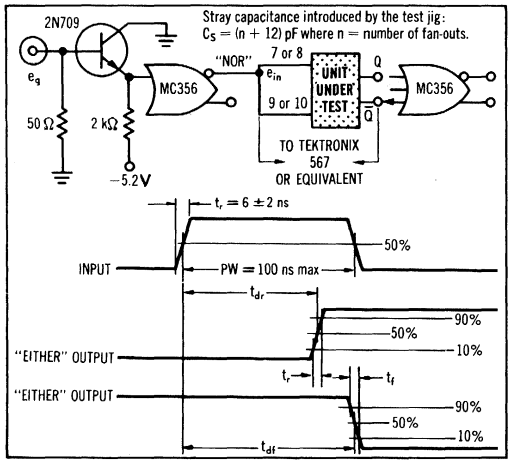


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

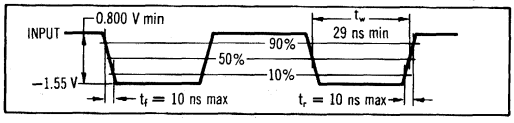


FIGURE 3 — SENSITIVITY (NO TOGGLE)

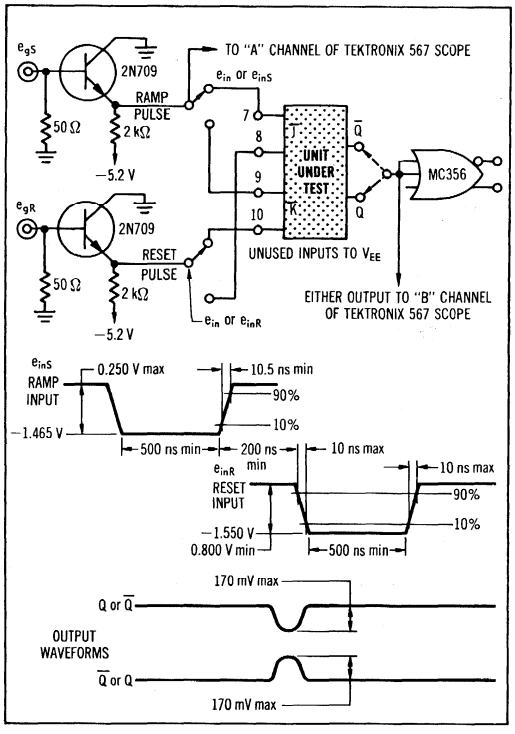
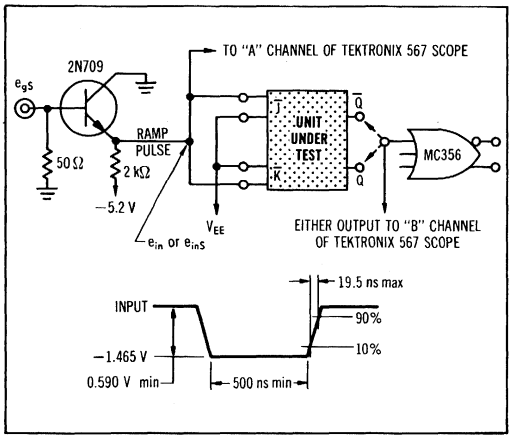


FIGURE 4 — SENSITIVITY (TOGGLE)



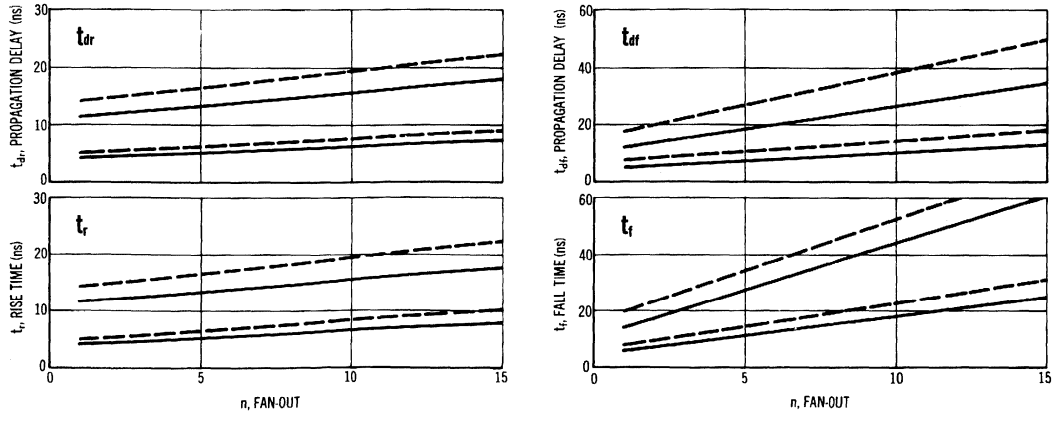
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L ② Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.6	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5③	3	$\triangle V_1$ (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4③	3	$\triangle V_1$ (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	− 0.61	—	− 0.65	—	− 0.73	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	− 0.61	—	− 0.65	—	− 0.73	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	− 1.11	− 1.25	− 1.09	− 1.21	−1.02	− 1.14	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{tog}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5		1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	7,10	4,5		1,2,6,8,9	—	—	3	t_{dr} (4,5)	7.5	13.0	7.5	13.0	8.0	16.0	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	10.0	14.5	10.0	15.0	11.0	20.0	↓
Rise Time	7,10	4,5		1,2,6,8,9	—	—	3	t_r (4,5)	8.0	13.0	8.0	13.0	8.5	16.0	
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	10.5	15.5	11.0	15.5	12.5	22.0	

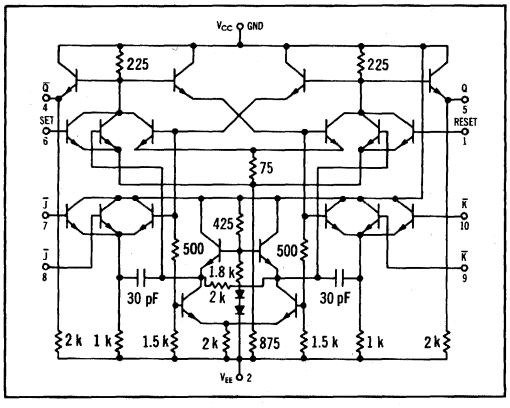
Pins not listed are left open. ① Input voltage is adjusted to obtain dV_{out}/dV_{in} = "0". ③ Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_I/dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

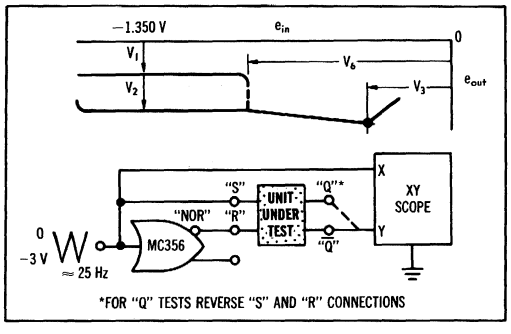


MC364

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

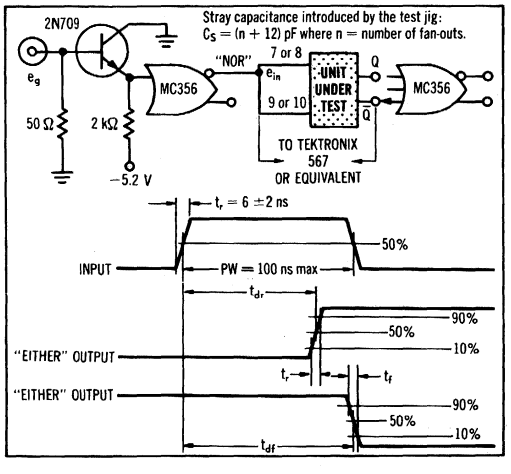


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

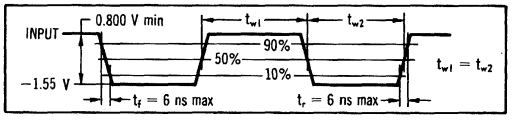


FIGURE 3 — SENSITIVITY (NO TOGGLE)

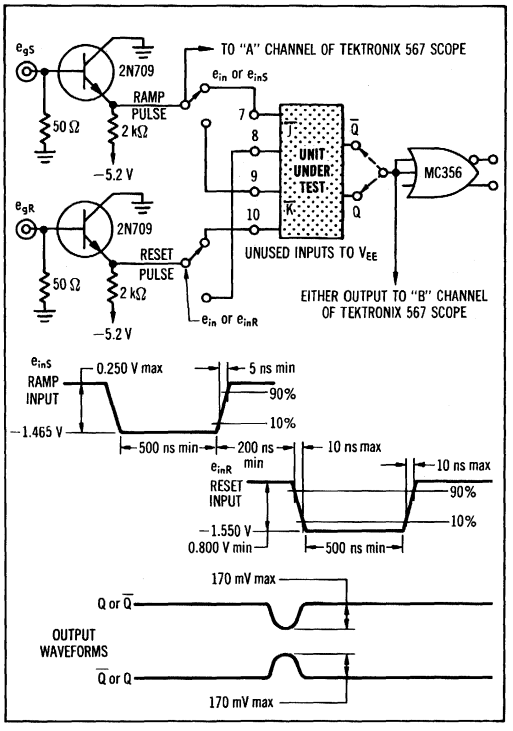
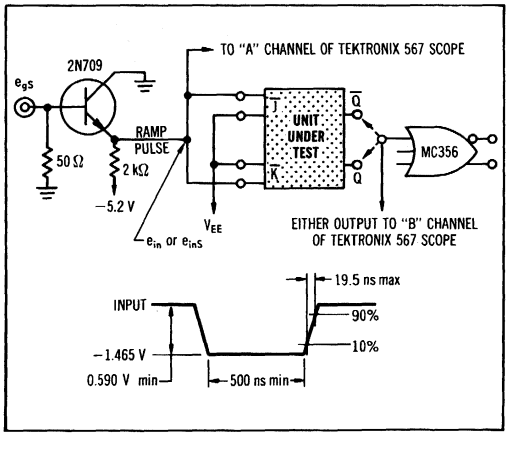


FIGURE 4 — SENSITIVITY (TOGGLE)



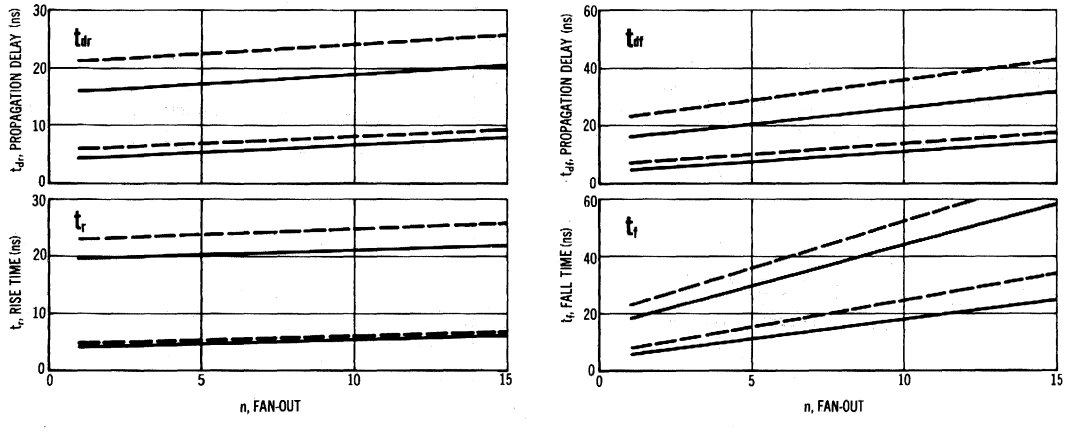
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	30.0	—	28.5	—	28.0	mAdc
Input Current	7	—	—	1,2,6.8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1⑤	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6⑤	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5⑤	3	$\triangle V_1$ (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4⑤	3	$\triangle V_1$ (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.61	—	−0.65	—	−0.73	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.61	—	−0.65	—	−0.73	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5	—	1,2,6,9	—	—	3	f_{tog}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5	—	1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{dr} (4,5)	11.0	18.0	12.0	18.0	14.0	24.0	ns
	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{df} (4,5)	12.0	18.0	13.0	18.0	15.0	24.0	↓
Rise Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_r (4,5)	11.5	20.0	12.5	21.0	15.0	26.0	
Fall Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	18.0	12.5	21.0	15.0	26.0	

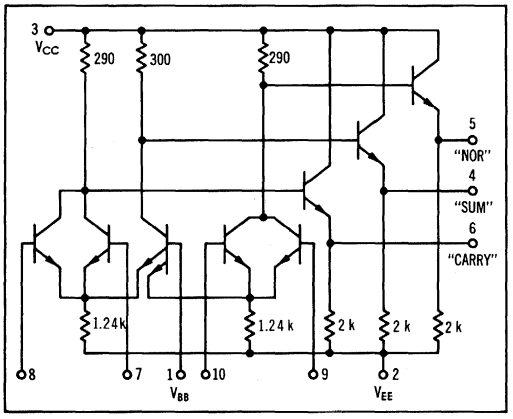
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

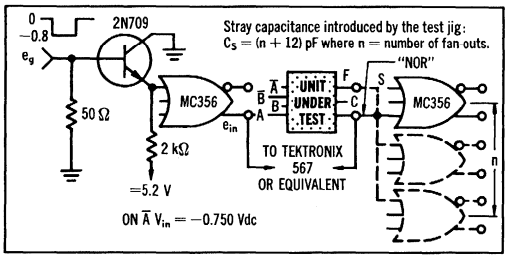


MC353

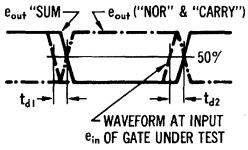
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



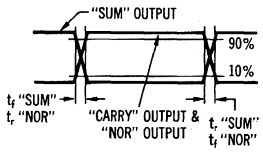
SWITCHING TIMES TEST CIRCUIT



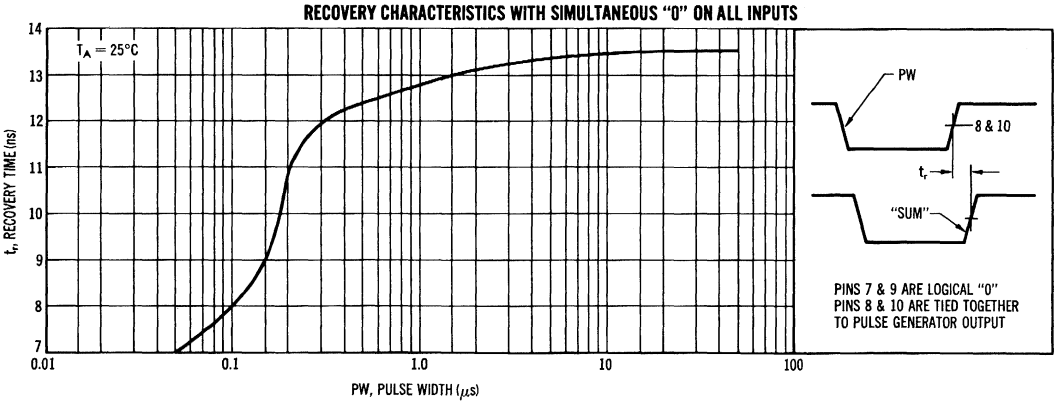
PROPAGATION DELAY



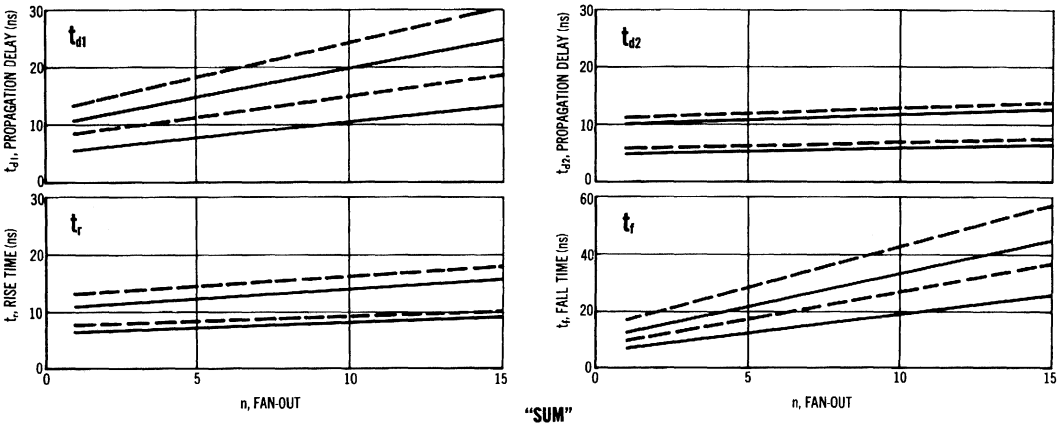
RISE AND FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



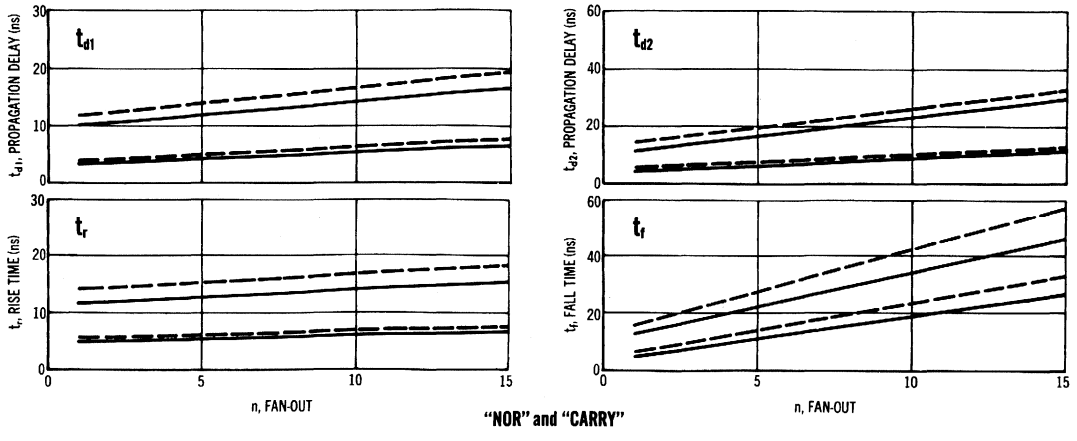
ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ±1%				
@ Test Temperature	0°C	—	−0.850	−1.350	−5.20	−1.18
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
	+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.9	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)							
	—	10	7	2,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5③	3	ΔV_1 (5)	—	0.055	—	0.055	—	0.065	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6③	3	ΔV_1 (6)	—	0.055	—	0.055	—	0.065	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4③	3	ΔV_5 (4)	—	0.055	—	0.055	—	0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	0.510	—	0.550	—	0.630	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	0.510	—	0.550	—	0.630	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.5	11.0	6.5	11.0	7.0	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.5	11.0	6.5	11.0	7.0	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	8.5	13.5	8.5	13.5	10.0	16.0	
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	8.5	13.5	8.5	13.5	10.0	16.0	
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	9.0	12.5	9.0	12.5	11.0	15.5	
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	9.0	12.5	9.0	12.5	11.0	15.5	
	—	7	—	2,8,9	1	10	4	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	
	—	7	—	2,8,9	1	10	4	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	↓

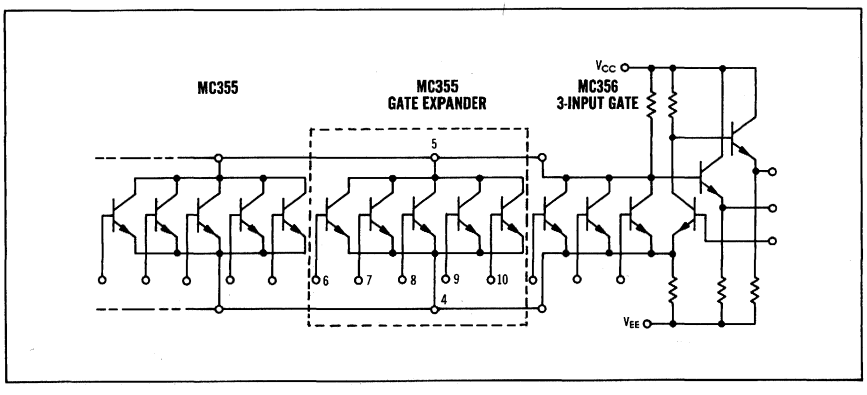
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{"NOR"}/dV_{in} = 0$ or $dV_{"CARRY"}/dV_{in} = 0$.
③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC355

A 5-input expander for use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five.



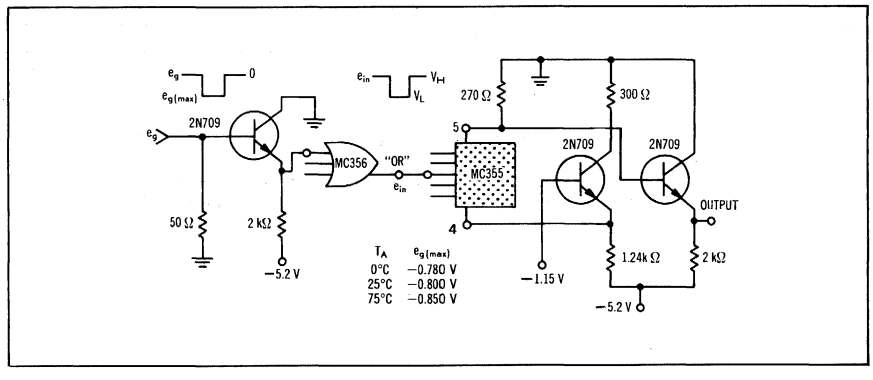
ELECTRICAL CHARACTERISTICS

	Test Conditions					
	Vdc ±1%					mAdc
@ Test Temperature 0°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +75°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CB} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	μAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—	↓	—	↓	—	↓	↓
	4	9	—	—	—	—	5	I_{BL} (9)	—	↓	—	↓	—	↓	↓
	4	10	—	—	—	—	5	I_{BL} (10)	—	↓	—	↓	—	↓	↓
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	15.0	μAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	0.730	0.780	0.680	0.730	0.580	0.630	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	9	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	10	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	①	—	—	—	—	—	—	t_{d1} 4.5	9.5	4.5	9.5	5.5	13.0	ns
	8	①	—	—	—	—	—	—	t_{d2} 4.0	9.0	4.0	9.0	4.5	12.0	↓
Rise Time	8	①	—	—	—	—	—	—	t_r 8.5	13.0	8.5	13.0	9.0	15.0	↓
Fall Time	8	①	—	—	—	—	—	—	t_f 3.5	10.5	3.5	10.5	4.0	11.5	↓

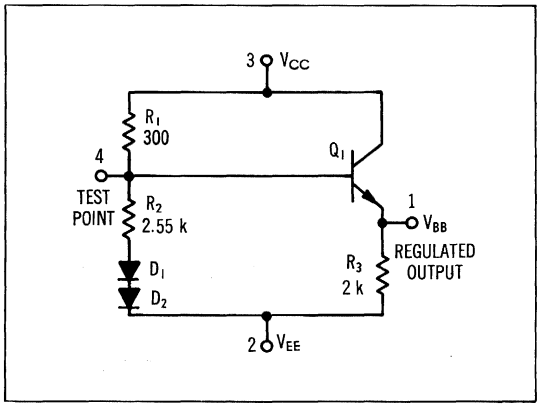
Pins not listed are left open. ①See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



MC354

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ±1%
@ Test Temperature	0°C	−5.20
	+25°C	−5.20
	+75°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	2	—	3	I_E (2)	—	4.6	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of 0 to +75°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

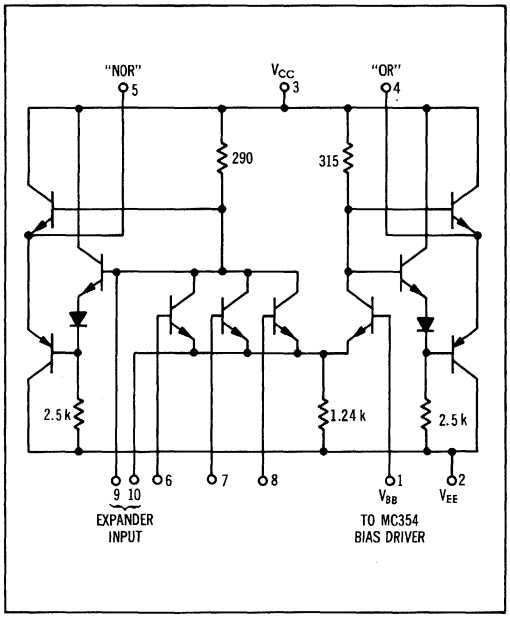
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

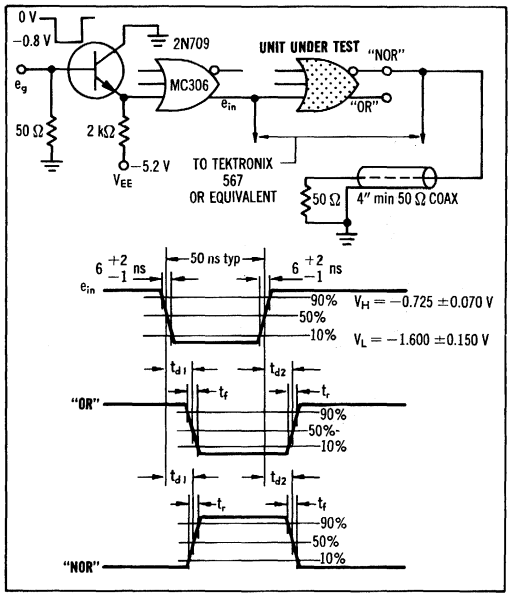
$V_{BB} = -1.15$ nominal output voltage at 25°C

MC365

Line driver for driving lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

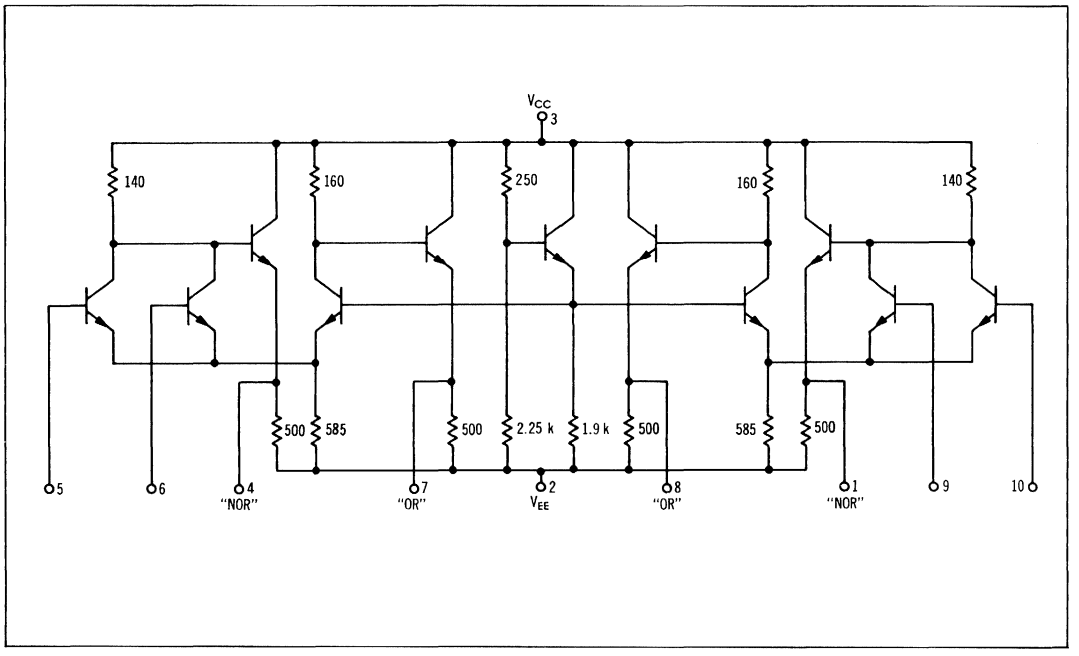
		Test Conditions Vdc ±1%				
@ Test Temperature	0°C	—	−0.850	−1.350	−5.20	−1.18
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
	+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L① Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8	1	4,5	3	I_E (2)	—	68	—	65	—	63	mAdc
Input Current	6	—	—	2,7,8	1	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_1 (6)	−0.695	−0.850	−0.650	−0.795	−0.570	−0.725	Vdc
	—	—	7	2,6,8	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_4 (6)	−1.495	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_2 (6)	−0.695	−0.850	−0.650	−0.795	−0.570	−0.725	Vdc
	—	7	—	2,6,8	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_2 (8)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_5 (6)	−1.495	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_5 (8)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
-Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	12.0	20.0	12.0	20.0	13.5	25.0	ns
	6	4	—	2,7,8	1	—	3	t_{d1} (4)	16.0	25.0	16.0	25.0	18.5	30.0	↓
	6	5	—	2,7,8	1	—	3	t_{d2} (5)	14.0	25.0	14.0	25.0	16.0	30.0	
	6	4	—	2,7,8	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	23.0	
Rise Time	6	5	—	2,7,8	1	—	3	t_r (5)	16.5	25.0	16.0	25.0	19.0	30.0	
	6	4	—	2,7,8	1	—	3	t_r (4)	13.0	20.0	13.0	20.0	15.5	25.0	
Fall Time	6	5	—	2,7,8	1	—	3	t_f (5)	20.5	35.0	20.5	35.0	26.0	47.0	
	6	4	—	2,7,8	1	—	3	t_f (4)	20.0	35.0	20.0	35.0	23.0	47.0	↓

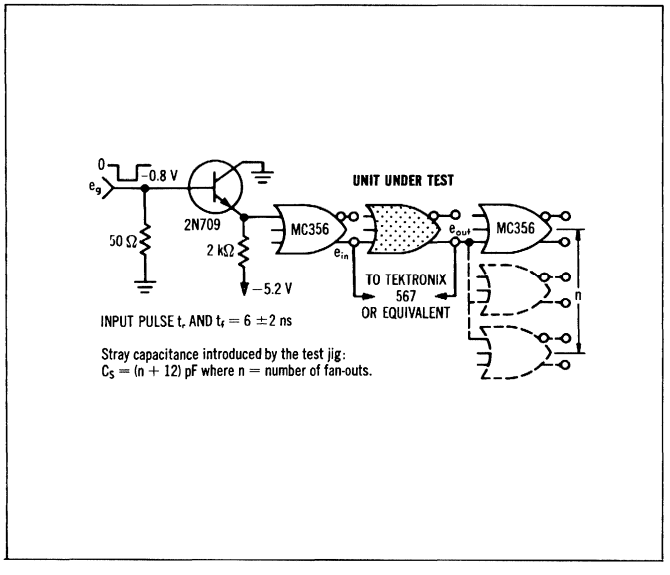
Pins not listed are left open. ①Output is loaded with a 50-ohm resistor.

MC369G

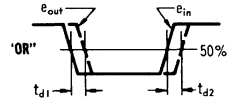
High-speed clock driver or dual 2-input gate that provides the positive logic "NOR" function and its complement simultaneously.

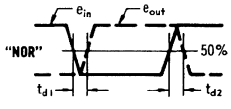


SWITCHING TIME TEST CIRCUIT

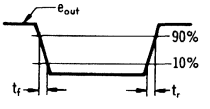


PROPAGATION DELAY





RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

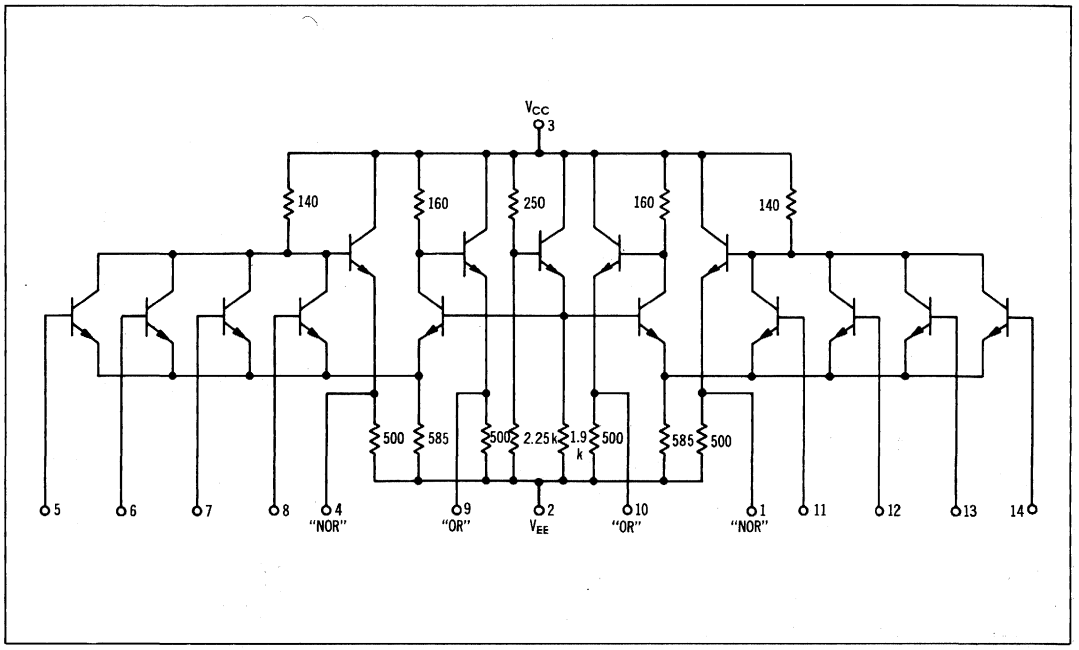
@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.510	−5.20
+25°C	−0.670	−0.795	−1.465	−5.20
+75°C	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,5,6,9,10	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,9,10	—	—	3	I_{in} (5)	—	—	—	200	—	—	μAdc
	6	—	—	2,5,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	9	—	—	2,5,6,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,5,6,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	5	2,6,9,10	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	—	6	2,5,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_1 (1)							
	—	—	10	2,5,6,9	—	—	3	V_1 (1)							
"NOR" Logical "0" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_4 (4)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	6	—	2,5,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_4 (1)							
	—	10	—	2,5,6,9	—	—	3	V_4 (1)							
"OR" Logical "1" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_5 (7)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,9,10	—	—	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_5 (8)							
	—	10	—	2,5,6,9	—	—	3	V_5 (8)							
"OR" Logical "0" Output Voltage	—	—	5	2,6,9,10	—	—	3	V_2 (7)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	—	6	2,5,9,10	—	—	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_2 (8)							
	—	—	10	2,5,6,9	—	—	3	V_2 (8)							
"NOR" Output Voltage Change	—	—	5	2,6,9,10	—	4②	3	$\triangle V_1$ (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	9	2,5,6,10	—	1②	3	$\triangle V_1$ (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" Output Voltage Change	—	5	—	2,6,9,10	—	7②	3	$\triangle V_5$ (7)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	9	—	2,5,6,10	—	8②	3	$\triangle V_5$ (8)	—	−0.100	—	−0.100	—	−0.130	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,9,10	5①	—	3	V_3 (4)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,5,9,10	6①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	2,5,6,10	9①	—	3	V_3 (1)	—		—		—		
	—	—	—	2,5,6,9	10①	—	3	V_3 (1)	—		—		—		
Switching Times Propagation Delay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	↓	6	↓	6	↓	7	↓
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)		5		5		6	
	9	8	—	2,5,6,10	—	—	3	t_{d1} (8)		6		6		7	
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	3	6	3	6	4	7	
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	↓	5	↓	5	↓	6	
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)		6		6		7	
	9	8	—	2,5,6,10	—	—	3	t_{d2} (8)		5		5		6	
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	4	7	4	7	5	8	
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	5	10	5	10	6	11	
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)	4	7	4	7	5	8	
	9	8	—	2,5,6,10	—	—	3	t_{d1} (8)	5	10	5	10	6	11	
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	5	10	5	10	6	11	
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	4	7	4	7	5	8	
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)	5	10	5	10	6	11	
	9	8	—	2,5,6,10	—	—	3	t_{d2} (8)	4	7	4	7	5	8	
Rise Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	7	4	7	5	9	
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	6	↓	6	↓	8	↓
	9	1	—	2,5,6,10	—	—	3	t_r (1)		7		7		9	
	9	8	—	2,5,6,10	—	—	3	t_r (8)		6		6		8	
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	9	4	9	5	10	
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_r (1)							
	9	8	—	2,5,6,10	—	—	3	t_r (8)							
Fall Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_f (4)	4	6	4	6	5	7	
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_f (1)							
	9	8	—	2,5,6,10	—	—	3	t_f (8)							
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_f (4)	6	11	6	11	7	12	
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_f (1)							
	9	8	—	2,5,6,10	—	—	3	t_f (8)							

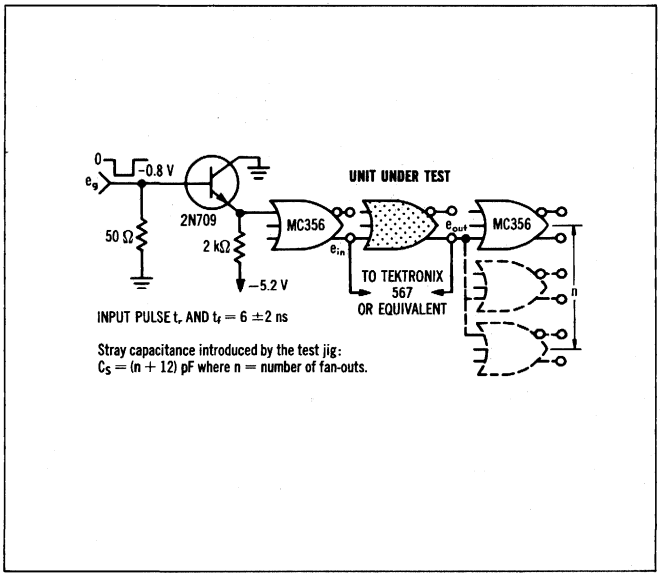
Pins not listed are left open. ①Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ②Current test conditions: no load = 0; full load = −10 mAdc ±5%.

MC369F

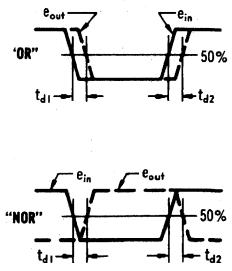
High-speed clock driver or dual 4-input gate that provides the positive logic "NOR" function and its complement simultaneously.



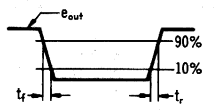
SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY



RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

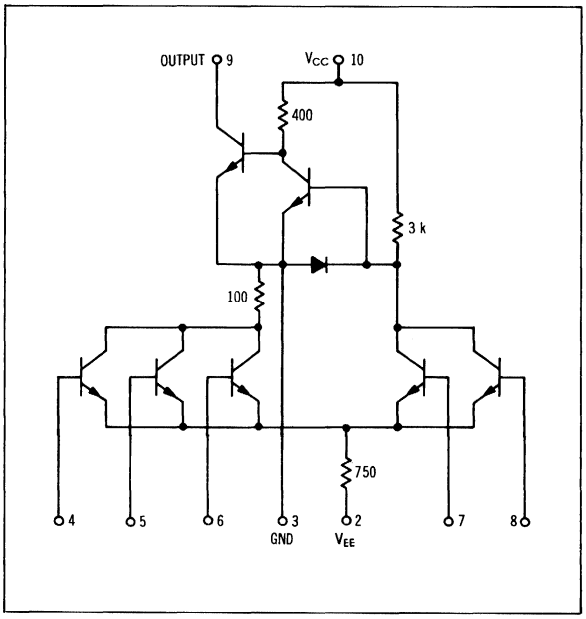
@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.510	−5.20
+25°C	−0.670	−0.795	−1.465	−5.20
+75°C	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,5,6,7,8,11,12,13,14	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,7,8,11,12,13,14	—	—	3	I_{in} (5)	—	—	—	200	—	—	μAdc
	6	—	—	2,5,7,8,11,12,13,14	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,5,6,8,11,12,13,14	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,5,6,7,11,12,13,14	—	—	3	I_{in} (8)	—	—	—		—	—	
	11	—	—	2,5,6,7,8,12,13,14	—	—	3	I_{in} (11)	—	—	—		—	—	
	12	—	—	2,5,6,7,8,11,13,14	—	—	3	I_{in} (12)	—	—	—		—	—	
	13	—	—	2,5,6,7,8,11,12,14	—	—	3	I_{in} (13)	—	—	—		—	—	
	14	—	—	2,5,6,7,8,11,12,13	—	—	3	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	—	6	2,5,7,8,11,12,13,14	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_1 (4)							
	—	—	8	2,5,6,7,11,12,13,14	—	—	3	V_1 (4)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_1 (1)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_1 (1)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_1 (1)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_1 (1)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_4 (4)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_4 (4)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_4 (4)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_4 (1)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_4 (1)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_4 (1)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_4 (1)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "1" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_5 (9)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_5 (9)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_5 (9)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_5 (9)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_5 (10)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_5 (10)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_5 (10)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_5 (10)	↓	↓	↓	↓	↓	↓	↓
"OR" Logical "0" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_2 (9)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	—	6	2,5,7,8,11,12,13,14	—	—	3	V_2 (9)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_2 (9)							
	—	—	8	2,5,6,7,11,12,13,14	—	—	3	V_2 (9)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_2 (10)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_2 (10)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_2 (10)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_2 (10)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	5	2,6,7,8,11,12,13,14	—	4③	3	$\triangle V_1$ (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	11	2,5,6,7,8,12,13,14	—	1③	3	$\triangle V_1$ (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" Output Voltage Change	—	5	—	2,6,7,8,11,12,13,14	—	9③	3	$\triangle V_5$ (9)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	11	—	2,5,6,7,8,12,13,14	—	10③	3	$\triangle V_5$ (10)	—	−0.100	—	−0.100	—	−0.130	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,11,12,13,14	5①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2 5,7,8,11,12,13,14	6①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2 5,6,8,11,12,13,14	7①	—	3	V_3 (7)	—		—		—		
	—	—	—	2,5,6,7,11,12,13,14	8①	—	3	V_3 (8)	—		—		—		
	—	—	—	2,5,6,7,8,12,13,14	11①	—	3	V_3 (11)	—		—		—		
	—	—	—	2,5,6,7,8,11,13,14	12①	—	3	V_3 (12)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,14	13①	—	3	V_3 (13)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,13	14①	—	3	V_3 (14)	—	↓	—	↓	—	↓	↓
Switching Times Propagation Delay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d1} (9)	↓	6	↓	6	↓	7	↓
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)		5		5		6	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (10)		6		6		7	
	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	3	6	3	6	4	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (9)	↓	5	↓	5	↓	6	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)		6		6		7	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)		5		5		6	
Fan-Out = 10	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	4	7	4	7	5	8	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (9)	5	10	5	10	6	11	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)	4	7	4	7	5	8	
	11	10	—	2,5,6 7,8,12,13,14	—	—	3	t_{d1} (10)	5	10	5	10	6	11	
	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	5	10	5	10	6	11	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (9)	4	7	4	7	5	8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)	5	10	5	10	6	11	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)	4	7	4	7	5	8	
Rise Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	7	4	7	5	9	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_r (9)	↓	6	↓	6	↓	8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)		7		7		9	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)		6		6		8	
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	9	4	9	5	10	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_r (9)	↓	↓	↓	↓	↓	↓	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)							
Fall Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	4	6	4	6	5	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)	↓	↓	↓	↓	↓	↓	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)							
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	6	11	6	11	7	12	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)	↓	↓	↓	↓	↓	↓	↓
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)							

Pins not listed are left open. ①Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ③Current test conditions: no load = 0; full load = −10 mAdc ±5%.

MC366

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6V lamps.



ELECTRICAL CHARACTERISTICS

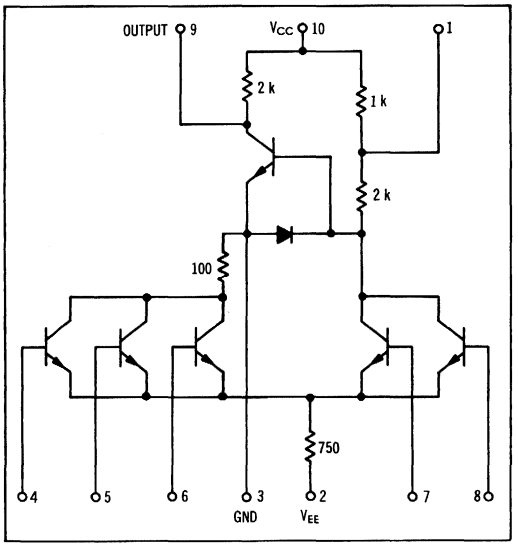
	Test Conditions						
	Vdc ±1%						mAdc
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	100
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	100

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	22.5	—	21.5	—	20.7	mAdc
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.4	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—		—	—	
Output Voltage, Low	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	10,9①	—	3	V_{OH} (5)	—	—	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10,9①	—	3	V_{OH} (6)	—	—	—		—		
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—		—		

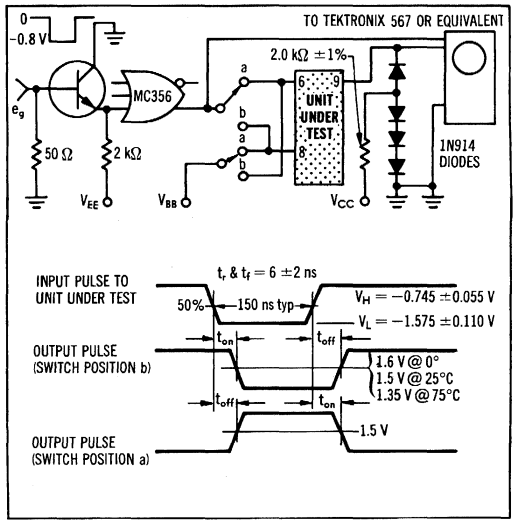
Pins not listed are left open. ①Pin 9 is connected to V_{CC} through a 10k-ohm resistor.

MC367

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS



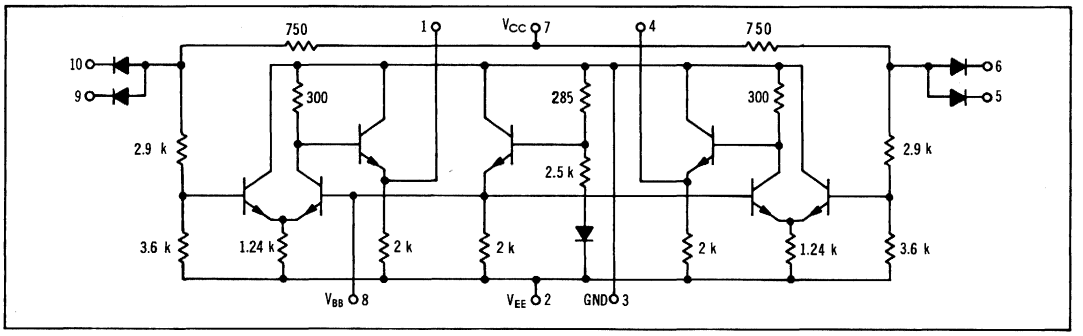
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%						mAdc
0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	10
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	10
+75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	10

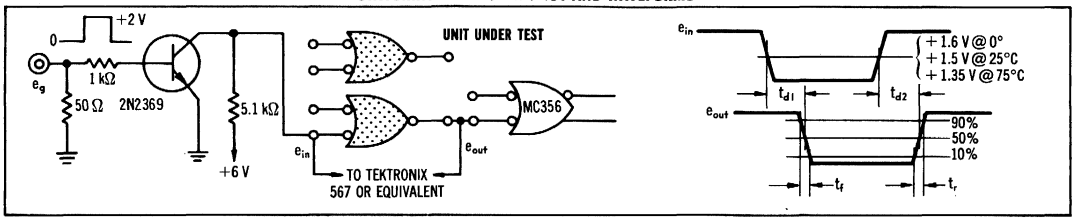
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.3	—	7.0	—	6.8	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.3	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,8	6	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,6,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—		—		—		
	—	6	—	2,4,5,8	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	8	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	
	8	9	—	2,4,5,7	6	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	↓

MC368

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_{IL} Pin No	V_{IH} Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No
	Test Conditions Vdc ±1%				
0°C	+0.45	+5.0	−5.20	+6.0	
+25°C	+0.45	+5.0	−5.20	+6.0	
+75°C	+0.50	+5.0	−5.20	+6.0	

Characteristic	V_{IL} Pin No	V_{IH} Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	2	7	3	I_C (7)	—	4.2	—	4.0	—	3.9	mAdc
	—	—	2	7	3	I_E (2)	—	21.9	—	21.0	—	20.2	mAdc
Input Load Current	—	—	2	7	3,5	I_L (5)	—	—	—	8.5	—	—	mAdc
	—	—	2	7	3,6	I_L (6)	—	—	—	↓	—	—	↓
	—	—	2	7	3,9	I_L (9)	—	—	—		—	—	
	—	—	2	7	3,10	I_L (10)	—	—	—		—	—	
Input Reverse Current	—	—	2	5,7	3,6	I_R (5)	—	—	—	0.5	—	2.0	μAdc
	—	—	2	6,7	3,5	I_R (6)	—	—	—	↓	—	↓	↓
	—	—	2	7,9	3,10	I_R (9)	—	—	—		—		
	—	—	2	7,10	3,9	I_R (10)	—	—	—		—		
"OR" Logical "1" Output Voltage	—	5	2	7	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.570	−0.725	Vdc
	—	6	2	7	3	V_6 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	2	7	3	V_5 (1)							
	—	10	2	7	3	V_6 (1)							
"OR" Logical "0" Output Voltage	5	—	2	7	3	V_2 (4)	−1.510	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	6	—	2	7	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	9	—	2	7	3	V_2 (1)							
	10	—	2	7	3	V_2 (1)							
Bias Voltage Output	—	—	2	7	3	V_{BB} (8)	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc

Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5	4	2	7	3	t_{d1} (4)	14.5	24.0	15.0	24.0	19.0	28.0	ns
	9	1	2	7	3	t_{d1} (1)	14.5	24.0	15.0	24.0	19.0	28.0	↓
	5	4	2	7	3	t_{d2} (4)	15.5	23.0	15.5	23.0	19.0	28.0	
	9	1	2	7	3	t_{d2} (1)	15.5	23.0	15.5	23.0	19.0	28.0	
Rise Time	5	4	2	7	3	t_r (4)	6.5	13.0	7.0	13.0	8.0	14.0	
	9	1	2	7	3	t_r (1)	6.5	13.0	7.0	13.0	8.0	14.0	
Fall Time	5	4	2	7	3	t_f (4)	7.0	13.0	7.5	13.0	8.0	14.0	
	9	1	2	7	3	t_f (1)	7.0	13.0	7.5	13.0	8.0	14.0	

Pins not listed are left open.

MECL II

INTEGRATED CIRCUITS
MC1000/MC1200 SERIES

MECL II

INTEGRATED CIRCUITS

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NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C

Function	Type: Case 83 −55 to +125°C	Type: Case 93 0 to +75°C	DC Output Loading Factor each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ	Page No.
Single 6-Input Gate, 3 "OR" Outputs w Pulldowns 3 "NOR" Outputs w Pulldowns	MC1201F	MC1001P	25	4.0	115	2-89
Single 6-Input Gate, 3 "OR" Outputs w Pulldowns 3 "NOR" Outputs w/o Pulldowns	MC1202F	MC1002P			80	
Single 6-Input Gate, 3 "OR" Outputs w/o Pulldowns 3 "NOR" Outputs w/o Pulldowns	MC1203F	MC1003P			40	
Dual 4-Input Gate, 2 "OR" Outputs w Pulldowns 2 "NOR" Outputs w Pulldowns	MC1204F	MC1004P			95	2-99
Dual 4-Input Gate, 2 "OR" Outputs w Pulldowns 2 "NOR" Outputs w/o Pulldowns	MC1205F	MC1005P			65	
Dual 4-Input Gate, 2 "OR" Outputs w/o Pulldowns 2 "NOR" Outputs w/o Pulldowns	MC1206F	MC1006P			45	
Triple 3-Input Gate, 3 "NOR" Outputs w Pulldowns	MC1207F	MC1007P			110	2-103
Triple 3-Input Gate, 1 "NOR" Output w Pulldowns 2 "NOR" Outputs w/o Pulldowns	MC1208F	MC1008P			75	
Triple 3-Input Gate, 3 "NOR" Outputs w/o Pulldowns	MC1209F	MC1009P			60	
Quad 2-Input Gate, 4 "NOR" Outputs w Pulldowns	MC1210F	MC1010P			115	2-107
Quad 2-Input Gate, 2 "NOR" Output w Pulldowns 2 "NOR" Output w/o Pulldowns	MC1211F	MC1011P			95	
Quad 2-Input Gate, 4 "NOR" Outputs w/o Pulldowns	MC1212F	MC1012P			65	
85 MHz AC Coupled J-K Flip-Flop	MC1213F	MC1013P		6.0	125	2-119
Dual R-S Flip-Flop (Positive Clock)	MC1214F	MC1014P			140	2-133
Dual R-S Flip-Flop (Negative Clock)	MC1215F	MC1015P			140	2-137
Dual R-S Flip-Flop (Single Rail, Positive Clock)	MC1216F	MC1016P			140	2-141
Level Translator (Sat. Logic to MECL)	MC1217F	MC1017P	25 (MECL)	15	105	2-157
Level Translator (MECL to Sat. Logic)	MC1218F	MC1018P	7 (DTL)	20	70	2-161
Full Adder	MC1219F	MC1019P	25	4.0	110	2-173
Quad Line Receiver	MC1220F	MC1020P			115	2-165
Full Subtractor	MC1221F	MC1021P			110	2-177
Type "D" Flip-Flops	**MC1222F**	**MC1022P**		**8.0**	**110**	2-153
Dual 4-Input "OR/NOR" Clock Driver	–	MC1023P		2.0	250	2-185
Dual 2-Input Expandable Gate	MC1224F	MC1024P		4.0	95	2-93
Dual 4 and 5 Input Expander	MC1225F	MC1025P	–	–	–	2-97
120 MHz AC Coupled J-K Flip-Flop	–	MC1027P	25	4.0	250	2-127
Data Distributor	MC1229F	MC1029P		4.0	160	2-181
Quad Exclusive OR Gate	MC1230F	MC1030P		5.0	130	2-111
Quad Exclusive NOR Gate	MC1231F	MC1031P		5.0	130	2-115
Dual R-S Flip-Flop (Single Rail, Negative Clock)	MC1233F	MC1033P		6.0	140	2-147
16-Bit Coincident Memory	–	MC1036P	5	17	250	2-169
16-Bit Coincident Memory w/o Pulldowns	–	MC1037P	5	17	250	2-169

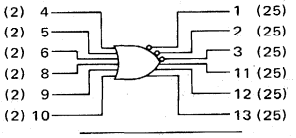
The logic diagrams shown describe the circuits of the MECL II line and permit quick selection of those circuits required to implement a particular logic system. Pertinent information, such as logic equations, truth tables, typical propagation delay time (t_{pd}), and typical power dissipation per package (P_D) is provided to show line compatibility. Package pin numbers and dc loading factors for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate dc loading factors at each terminal.

MECL II circuits contain internal bias networks, insuring that the transistion point is always in the center of the transfer characteristic curves over the temerature range.

(V_{CC} = PIN 14, V_{EE} = PIN 7)

GATES

MC1001P, MC1002P, MC1003P MC1201F, MC1202F, MC1203F
6-Input Gate



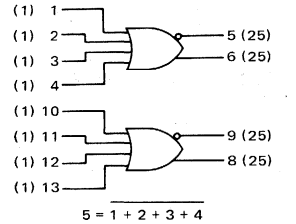
$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$

$11 = 4 + 5 + 6 + 8 + 9 + 10$

t_{pd} = 4.0 ns

P_D = MC1001/MC1201 – 115 mW
MC1002/MC1202 – 80 mW
MC1003/MC1203 – 40 mW

MC1004P, MC1005P, MC1006P MC1204F, MC1205F, MC1206F
Dual 4-Input Gate



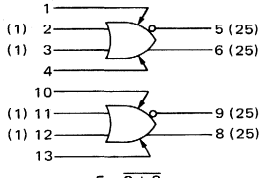
$5 = \overline{1 + 2 + 3 + 4}$

$6 = 1 + 2 + 3 + 4$

t_{pd} = 4.0 ns

P_D = MC1004/MC1204 – 95 mW
MC1005/MC1205 – 65 mW
MC1006/MC1206 – 45 mW

MC1024P, MC1224F
Dual 2-Input Expandable Gate



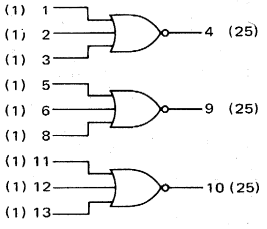
$5 = \overline{2 + 3}$

$6 = 2 + 3$

t_{pd} = 4.0 ns

P_D = 95 mW

MC1007P, MC1008P, MC1009P MC1207F, MC1208F, MC1209F
Triple 3-Input Gate

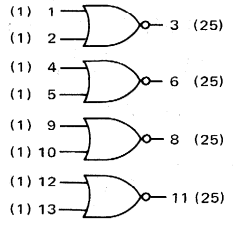


$4 = \overline{1 + 2 + 3}$

t_{pd} = 4.0 ns

P_D = MC1007/MC1207 – 110 mW
MC1008/MC1208 – 75 mW
MC1009/MC1209 – 60 mW

MC1010P, MC1011P, MC1012P MC1210F, MC1211F, MC1212F
Quad 2-Input Gate

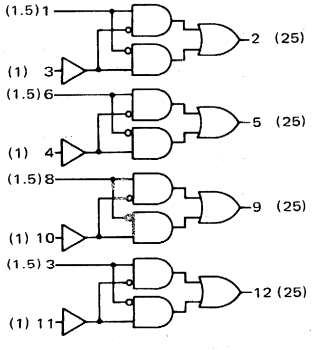


$3 = \overline{1 + 2}$

t_{pd} = 4.0 ns

P_D = MC1010/MC1210 – 115 mW
MC1011/MC1211 – 95 mW
MC1012/MC1212 – 65 mW

MC1030P, MC1230F
Quad Exclusive OR Gate

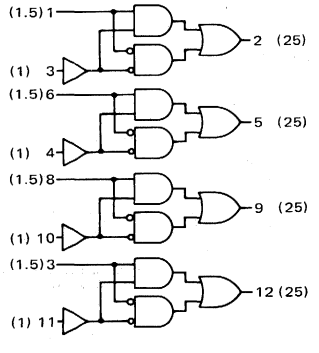


$2 = 1 \cdot \overline{3} + \overline{1} \cdot 3$

t_{pd} = 5.0 ns

P_D = 130 mW

MC1031P, MC1231F
Quad Exclusive NOR Gate



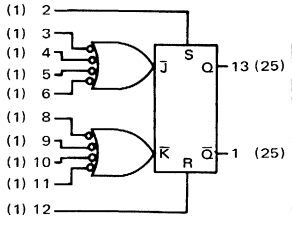
$2 = 1 \cdot 3 + \overline{1} \cdot \overline{3}$

t_{pd} = 5.0 ns

P_D = 130 mW

FLIP-FLOPS

MC1013P, MC1213F
85 MHz AC-Coupled J-K Flip Flop



t_{pd} = 6.0 ns
P_D = 125 mW

CLOCKED J-K OPERATION

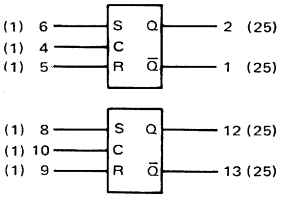
$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
◊	◊	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} – 0.6 V.) Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R-S OPERATION

R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

MC1014P, MC1214F
MC1015P, MC1215F
Dual Clocked R-S Flip-Flop



t_{pd} = 6.0 ns
P_D = 140 mW

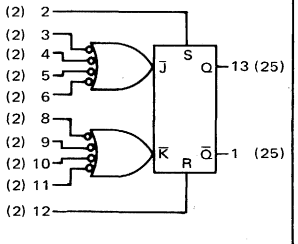
MC1014/1214

C	R	S	Q^{n+1}
1	0	0	Q^n
1	0	1	1
1	1	0	0
1	1	1	ND
0	◊	◊	Q^n

MC1015/1215

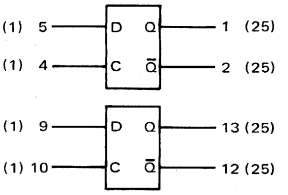
C	R	S	Q^{n+1}
0	0	0	Q^n
0	0	1	1
0	1	0	0
0	1	1	ND
1	◊	◊	Q^n

MC1027P
120 MHz AC-Coupled J-K Flip-Flop



t_{pd} = 4.0 ns
P_D = 250 mW

MC1016P, MC1216F
MC1033P, MC1233F
Dual Clocked Single Rail R-S Flip-Flop



t_{pd} = 6.0 ns
P_D = 140 mW

MC1016/1216

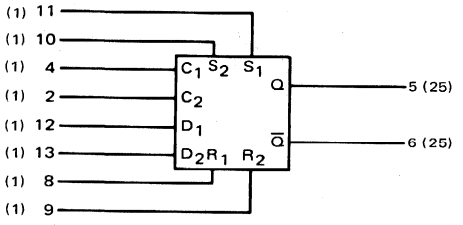
C	D	Q^{n+1}
0	0	Q^n
0	1	Q^n
1	0	0
1	1	1

MC1033/1233

C	D	Q^{n+1}
1	0	Q^n
1	1	Q^n
0	0	0
0	1	1

MC1022P, MC1222F
Type "D" Flip-Flop

POSITIVE LOGIC



t_{pd} = 8.0 ns
P_D = 110 mW

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}	$\bar{Q}^{n+1}$
	8 or 9	10 or 11	5	6
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

N.D. = Not Defined

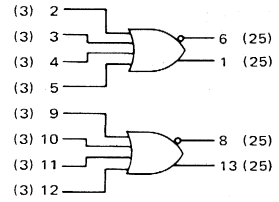
CLOCKED TRUTH TABLE

Pin No.	D	C	Q^{n+1}	$\bar{Q}^{n+1}$
	12 or 13	2 or 4	5	6
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low input to a high input.

DRIVER

MC1023P
Dual 4-Input Clock Driver

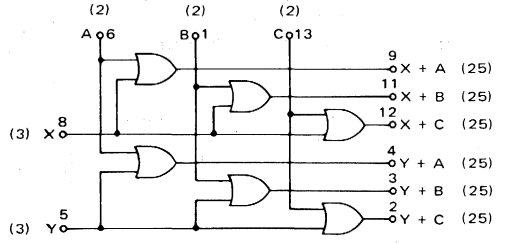


$6 = \overline{2 + 2 + 4 + 5}$
$1 = 2 + 3 + 4 + 5$

t_{pd} = 2.0 ns
P_D = 250 mW

DATA DISTRIBUTOR

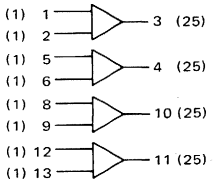
MC1029P, MC1229F
2 X 3 Data Distributor



t_{pd} = 4.0 ns
P_D = 160 mW

RECEIVER

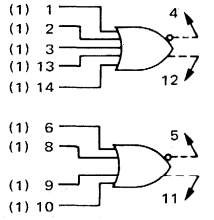
MC1020P, MC1220F
Quad Line Receiver



t_{pd} = 4.0 ns
P_D = 115 mW

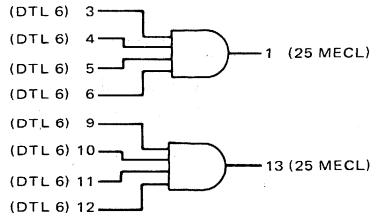
EXPANDER

MC1025P, MC1225F
Dual 4-5 Input Expander



TRANSLATORS

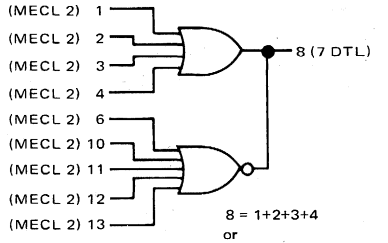
MC1017P, MC1217F
Level Translator



$1 = 3 \bullet 4 \bullet 5 \bullet 6$

t_{pd} = 15 ns
P_D = 105 mW

MC1018P, MC1218F
Level Translator

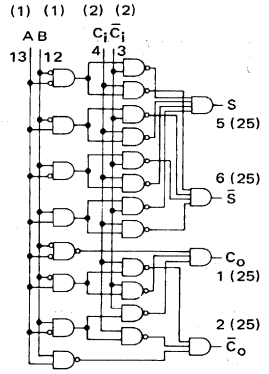


$8 = 1+2+3+4$
or
$8 = \overline{6+10+11+12+13}$

t_{pd} = 20 ns
P_D = 70 mW

FULL ADDER

MC1019P, MC1219F
Full Adder

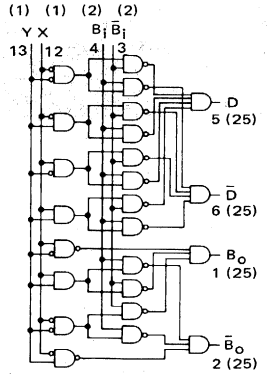


$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$
$\bar{S} = \bar{A}\bar{B}\bar{C}_i + \bar{A}BC_i + A\bar{B}C_i + ABC_i$
$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$
$\bar{C}_o = \bar{A}\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + A\bar{B}\bar{C}_i + \bar{A}\bar{B}C_i$

t_{pd} = 4.0 ns P_D = 110 mW

SUBTRACTOR

MC1021P, MC1221F
Full Subtractor

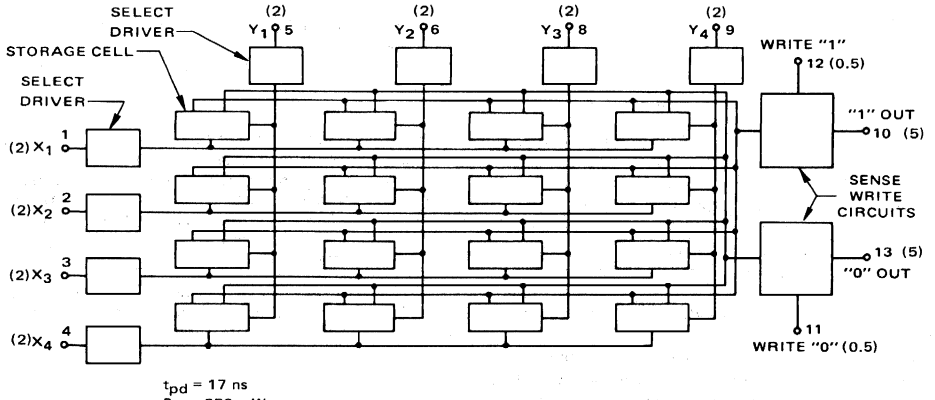


$D = YXB_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$
$\bar{D} = \bar{Y}\bar{X}\bar{B}_i + YX\bar{B}_i + Y\bar{X}B_i + \bar{Y}XB_i$
$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + YXB_i$
$\bar{B}_o = \bar{Y}\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + Y\bar{X}B_i + YX\bar{B}_i$

t_{pd} = 4.0 ns P_D = 110 mW

MEMORY

MC1036P, MC1037P
16-Bit Coincident Memory



t_{pd} = 17 ns
P_D = 250 mW

Maximum Power Supply Variation = ±10%

MECL II

GENERAL INFORMATION SECTION

INTRODUCTION

The MECL II family of Emitter-coupled Logic (current mode logic) was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL II circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower outputs to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifiers and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

MECL II devices are specified over two temperature ranges: 0 to 75°C (MC1000 Series) and −55 to 125°C (MC1200 Series). The MC1000 Series is available in the dual in-line plastic package (add suffix "P" to basic type number) and the MC1200 Series in the TO-86 ceramic flat package (suffix "F").

Family characteristics are:

- 4.0 ns propagation delay
- DC fan-out of 25 minimum
- High-frequency operation, if required
- Excellent speed-power product
- Constant current drain regardless of logic state or operating frequency
- ±20% power supply tolerance

System features include:

- Minimized cross-talk
- Reduced power dissipation and can count through Wired-OR and the series gating design techniques
- Guaranteed worst-case noise margin
- Single power supply
- Ease of designing parallel rather than serial logic

MECL II DESIGN PHILOSOPHY

The following goals have been met by MECL II, resulting in the most economical form of logic for system design:

I. Availability has been maximized through:
   A. Non-stringent processing requirements
   B. Optimized chip and device size
   C. Specifications determined by distribution data, on parts produced in volume, analyzed for system design requirements.
   D. Internal specification guard-bands set to minimize correlation problems.

II. Rise and fall times of basic family are kept slow enough to be compatible with conventional layout techniques such as two-sided printed circuit boards and point-to-point backplane wiring.

III. MECL II is compatible with the original MECL (MC300 and MC350 Series).

IV. Logic has been maximized for 14-pin packages by using complex functions wherever economical.

During design, the cost to run a problem or to do a specified amount of work on a system should be considered. To run a problem on a system, the costs decrease with increasing circuit speeds due to shorter running times. An increase in costs is experienced when using logic faster than 4.0 ns, and is caused by the required switch to stripline and ground-plane techniques. This will result in added expense in packaging and layout.

The enclosed individual device specifications show that MECL II is optimized for economy when computer operating time is compared with packaging and layout costs.

SYSTEM CHARACTERISTICS

MECL II provides several important systems features. A noise immunity-power dissipation trade-off is possible by varying the supply voltage of the system. Figures 1 and 2 show the OR and NOR transfer characteristics of typical MECL II gates as the supply voltage is varied. For example, noise immunity may be increased by 0.100 V by increasing the supply voltage to −6.0 V, which increases power dissipation by 35%.

Figures 3 through 7 illustrate the typical characteristics of MECL II versus temperature and supply voltage changes. There is minimal change in system operating characteristics for ±10% supply variation. The largest change is observed at 125°C and elevated supply voltages, where the gates will be operating into the saturation region which significantly reduces operating speeds.

For driving long lines with MECL II, or interfacing between systems that have a large difference in operating temperature, balanced twisted-pair lines are recommended. The differential output of a MECL gate drives the line. The far end is terminated in the characteristic impedance of the line and received by a differential amplifier. (See the discussion with MC1020/MC1220 Quad Line Receiver.) This method yields 1.0 V or better noise immunity at a very low impedance.

A significant feature of MECL II is its low generated noise and cross-talk in a system. The output rise and fall times are approximately the same as the propagation delay times, minimizing capacitive cross-talk. The noise immunity as a percentage of logic swing is also larger than standard saturated logic. The very low logic currents switched in the lines also appreciably reduce inductive cross-talk. If line lengths are kept short with respect to the fastest rise or fall time of noise, then the line is effectively clamped to the 15-ohm output impedance of the gate. This then requires considerable energy to overcome the voltage noise immunity of the gate. MECL II also shows a significant improvement over saturated logic rejection of noise and voltage variations due to poor regulation on the supply line.

FIGURE 1 - TYPICAL "OR" TRANSFER CHARACTERISTICS

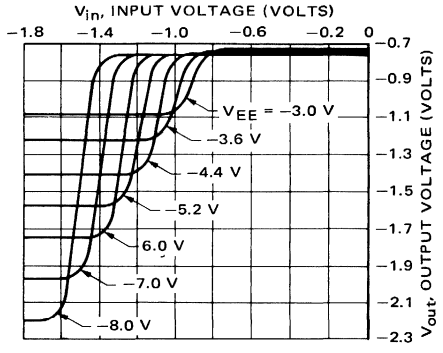


FIGURE 2 - TYPICAL "NOR" TRANSFER CHARACTERISTICS

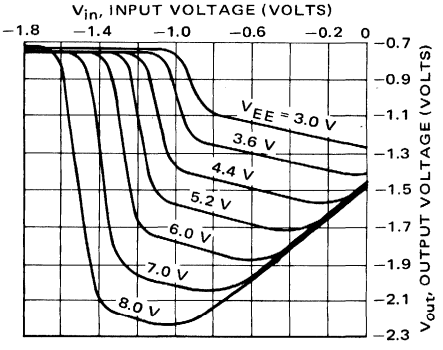


FIGURE 3 - RISE TIME versus TEMPERATURE AND SUPPLY VOLTAGE

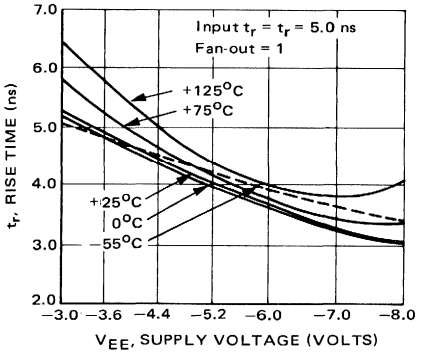


FIGURE 4 - FALL TIME versus TEMPERATURE AND SUPPLY VOLTAGE

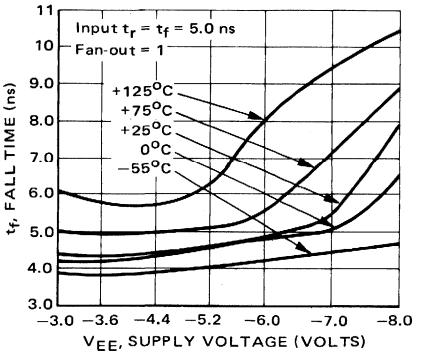


FIGURE 5 - PROPAGATION DELAY t_{pd+} versus TEMPERATURE AND SUPPLY VOLTAGE

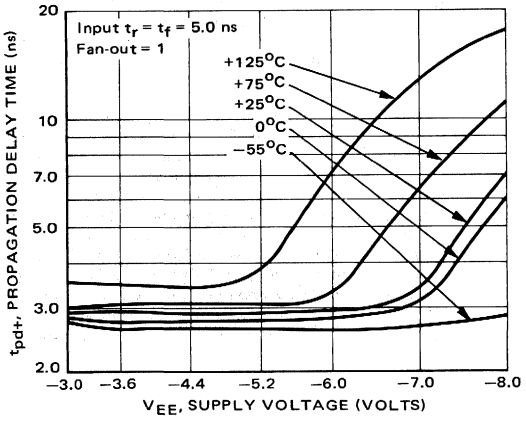


FIGURE 6 - PROPAGATION DELAY t_{pd-} versus TEMPERATURE AND SUPPLY VOLTAGE

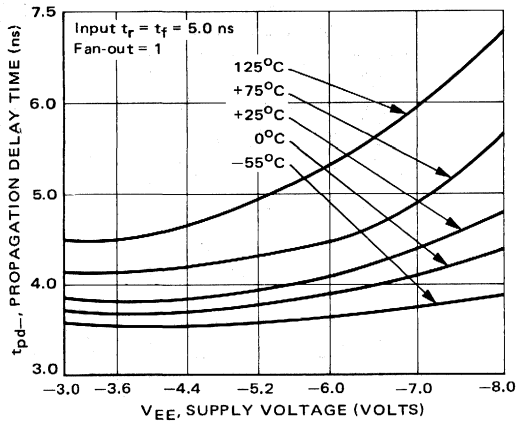
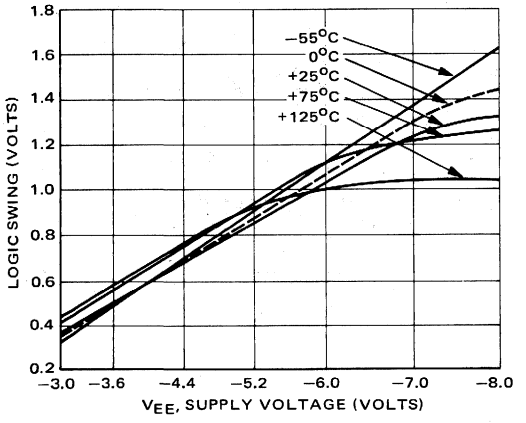


FIGURE 7 - LOGIC SWING versus TEMPERATURE AND SUPPLY VOLTAGE

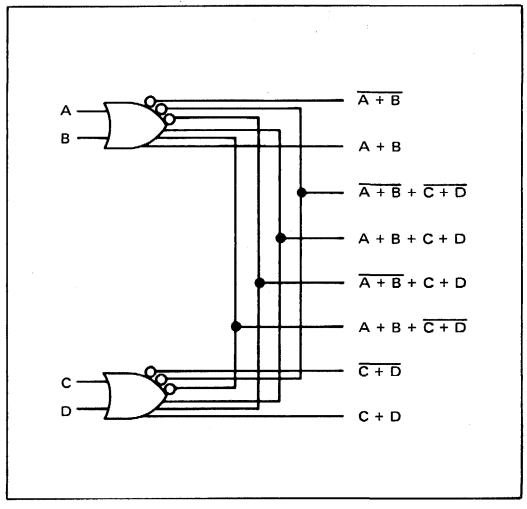


GENERAL DESIGN AND SYSTEM LAYOUT RULES

"OR"ING FEATURES

The outputs of several gates may be tied together to perform the Wired-OR function. A recommended maximum of 15 outputs should be ORed together if high-speed operation is desired. If speed is not a system requirement, a greater number of outputs may be ORed together. One pulldown resistor per Wired-OR function is recommended as a power saving feature. Two pulldowns result in appreciably better fall times with high capacitance loads. The high logic level noise immunity is reduced by a negligible amount. Three pulldown resistors reduce noise immunity typically by 50 mV and therefore are not generally recommended. As separate gates drive the Wired-OR output to the high level, approximately 3.0 mA current will be switched through the interconnecting leads with a rise time as short as 3.0 ns. To maintain the very low crosstalk advantages of MECL, it is not recommended that Wired-OR be employed on a computer back-plane but be restricted to printed circuit cards.

FIGURE 8 - EXAMPLE OF MULTIPLE OUTPUT GATE INTERCONNECTIONS



UNUSED INPUTS

All unused inputs must be tied to V_{EE} for reliable system operation. As seen from the gate input characteristics (Figure 11), the input impedance of a gate is very high when at a low-level voltage. Any leakage to the input capacitance of the gate will gradually build up a voltage on the input lead. This may affect noise imunity of the gate or hinder switching characteristics at low repetition rates. Returning the unused inputs to V_{EE} insures no build-up of voltage, and a noise immunity dependent only upon the inputs used. The emitter-base breakdown voltage of the transistors used is in excess of −6.5 V and will not start to clamp the voltage across the differential pair current source until a V_{EE} greater than −8.0 V is applied to a gate, nor will device failure occur since base current is limited internally. For most evaluation and breadboarding purposes, unused inputs may be left open with negligible difference in results.

FAN-IN

A maximum fan-in of 20 is recommended for high-speed operation. Greater fan-in may be employed if fast propagation delay, rise, and fall times are not required. Further discussion is found on the data sheets for the MC1024/MC1224 Dual 2-Input Gates and the MC1025/MC1225 Dual Expanders.

V_{BB} SUPPLY

None of the MECL II devices require an external V_{BB} or reference supply, however V_{BB} has been brought out externally on the MC1017/MC1217 and MC1018/MC1218 translators for those who may require it. To maintain noise margin levels on MECL II, the maximum recommended load current for V_{BB} is 1.0 mA.

SYSTEM LAYOUT

As rise and fall times decrease, more restrictions are required on system layout. Standard MECL II exhibits typical rise, fall, and propagation delay times of 4.0 ns, but due to process and layout variations these may go as low as 3.0 ns. MECL II has been designed to be as fast as practical without requiring non-standard layout techniques such as ground planes on printed circuit boards. Two-sided printed circuit cards are still satisfactory for 3.0 ns rise times, especially since MECL draws constant current from the power supply.

Reflections that occur on high-impedance unterminated lines are a function of logic rise and/or fall times. For example, reflections can be a problem with 1.0 ns rise time and high-impedance wire lengths greater than three inches. For MECL II, maximum wire length of 12 inches is recommended. Wire length of 36 inches or more may be driven if a small ferrite bead is slipped over the wire. The ferrite bead attenuates the high-frequency components of the fast rise or fall times and therefore damps out overshoot, ringing, and reflections. Also if a wire is run adjacent to a ground plane, effective inductance per unit length may be reduced by one-half that observed when the wire is a couple of inches above the ground plane. When long wires are being driven, a recommended fan-in of one should be employed at the receiving end. Higher fan-in increases the mismatch of high impedance wires. See the discussion in Application Note AN-277 which gives methods of reducing overshoot to acceptable levels where both long leads and high fan-in are employed. Long leads and high fan-out and fan-in are less of a problem on a printed circuit board where high width-to-thickness ratios of the printed leads greatly reduce inductance. High-speed clock drivers (2.0 ns) can be used satisfactorily on two-sided printed circuit boards if the layout is designed properly.

CLOCK DISTRIBUTION

Clock distribution is one of the largest system problems. Where large high-speed clock networks are required, a balanced twisted pair line is recommended for clock distribution. A gate such as the MC1001/MC1201 and the MC1020/MC1220 Quad Line Receiver make an excellent combination for distributing the clock throughout a system at frequencies to 50 MHz. (See the MC1020/MC1220 data sheet for further detail.) This method allows control of clock skew time and offers 1.0 V or better noise immunity regardless of line length.

DEFINITIONS

e_g	Generator inputs to test circuit.
I_{BL}	Base leakage current of a MECL expander input when at V_{EE}.
I_C	Total power supply current drawn from the positive supply by the test unit.
I_{CEX}	Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential.
I_E	Total power supply current drawn from the test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current drawn by the input of the test unit when a maximum logical "1" ($V_{IH\ max}$) is applied at that input.
I_L	Load current that is applied through a MECL circuit output when measuring the output "1" level voltage.
I_{OH}	Load current that is applied through a saturating output of a translator when measuring the output "1" level.
I_{OL}	Load current that is applied through a saturating output of a translator when measuring the output "0" level.
I_{out}	Output current.
I_R	Reverse current drawn from a transistor input of the test unit when V_{EE} is applied at that input.
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential.
t_f	Time required for the output pulse to go more negative from its 90% point to its 10% point.
t_{pd}, $t_{x\pm y\pm}$	Propagation delay time from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +).
t_r	Time required for the output pulse to go more positive from its 10% point to its 90% point.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
V_{BB}	Bias reference supply voltage (–1.175 V nominal at 25°C).
V_{BE}	Base-to-emitter voltage drop of a transistor.
V_{CB}	Collector-to-base voltage drop of a transistor.
V_{CC}	Most positive power supply voltage for a circuit.
V_{EE}	Most negative power supply voltage for a circuit.
V_{in}	Input voltage.
$V_{IH\ max}$	Maximum input logical "1" level voltage.
$V_{IH\ min}$	Minimum input logical "1" level (threshold) voltage.
$V_{IL\ max}$	Maximum input logical "0" level (threshold) voltage.
$V_{IL\ min}$	Minimum input logical "0" level voltage.
V_L	Latch voltage of a dc flip-flop.
$V_{OH\ max}$	Maximum output "1" or high-level voltage.
$V_{OH\ min}$	Minimum output "1" or high-level voltage.
$V_{OL\ max}$	Maximum output "0" or low-level voltage.
$V_{OL\ min}$	Minimum output "0" or low-level voltage.
V_{out}	Output voltage.
V_{max}	Maximum positive supply voltage.

THE BASIC MECL II LOGIC GATE

Each digital integrated circuit family is built around a basic circuit which determines the general characteristics of the family. The basic MECL II gate is evaluated in terms of circuit operation, transfer characteristics, noise margin, speed, component tolerances, and logic flexibility.

CIRCUIT OPERATION

Figure 9 illustrates a 4-input OR-NOR MECL II gate; Figure 10 depicts MECL II transfer characteristics and specification points. Typical operating voltages are V_{CC} = ground and V_{EE} = −5.2 V. The internal bias (V_{BB}) is designed for a nominal −1.175 V in reference to V_{CC}. When the gate inputs are all at a low level ($V_{in} \leq V_{IL\ max}$) the input transistors will not be conducting current and the V_{BB} transistor will act as an emitter follower. At 25°C the V_{BE}-drop of a silicon integrated transistor averages around 0.750 V for base currents within the nominal operating region. Therefore the voltage at point 3 in Figure 9 is V_{BB} − 0.750 V or −1.925 V. This potential establishes an I_E of 2.77 mA through the 1.18 k-ohm emitter resistor. I_E also causes a drop of 0.830 V across the 300-ohm collector resistor. The OR output is then obtained through an emitter follower which drops the output voltage to a nominal −1.580 V, which is a logic "0" or low logic level. The base of the NOR output transistor is essentially at 0 V, yielding an output of −0.750 V or the nominal "1" logic level.

If one or more of the gate inputs is switched to a high level ($V_{in} \geq V_{IH\ min}$), the current from point 2 to point 3 will switch from point 1 to point 3. Point 3 is now at −1.500 V resulting in an I_E of 3.14 mA which causes a drop of 0.900 V across the 290-ohm resistor. The nominal NOR output voltage is then −1.650 V or 0.070 V lower than the OR output. The reasons for this are seen from the transfer characteristics shown in Figure 10. Observing the NOR transfer characteristics as V_I increases from $V_{IL\ min}$ to $V_{IL\ max}$, it is seen that the output remains at a high level. For V_I increasing from $V_{IL\ max}$ to $V_{IH\ min}$, the NOR output will switch to a low level. Then as the input continues more positive than $V_{IH\ min}$, the output will continue more negative with a slope of about −0.24. This is caused by the input collector node going more negative as V_I goes more positive. If the input is increased above $V_{IH\ max}$, saturation will be reached at an input of about −0.40 V. Beyond this point, the base-collector junction is forward biased and the collector voltage will increase with an increasing input level. The nominal NOR low-level output is designed to be more negative than the nominal OR low-level output, to assure that at an input of $V_{IH\ min}$ the output is still more negative than $V_{OL\ max}$. Thus equal noise margins may be guaranteed for OR and NOR outputs.

The transfer characteristics (Figure10) show that MECL II operating levels are well below the point at which the gate starts to saturate. The saturation temperature for MECL II devices is nominally 140°C ambient. Since the transistors stay out of the saturation region, current mode is inherently the fastest form of logic obtainable. Typically gates exhibit an average propagation delay of 4.0 ns when wired into a system.

The differential input of the MECL gate offers several advantages. Input impedance is high due to the emitter follower inputs. A worst-case current of 100 μA is guaranteed. (See Figure 11 for input characteristics.) The voltage gain and transfer characteristics are practically independent of transistor parameters. The input thresholds are determined effectively by the internal V_{BB} due to the V_{BE} match of integrated circuit transistors. The collectors of the differential amplifier provide the complementary outputs at essentially the same propagation delay time. The differential input is also responsible for common mode rejection of power supply variations.

FIGURE 9 - BASIC MECL II GATE

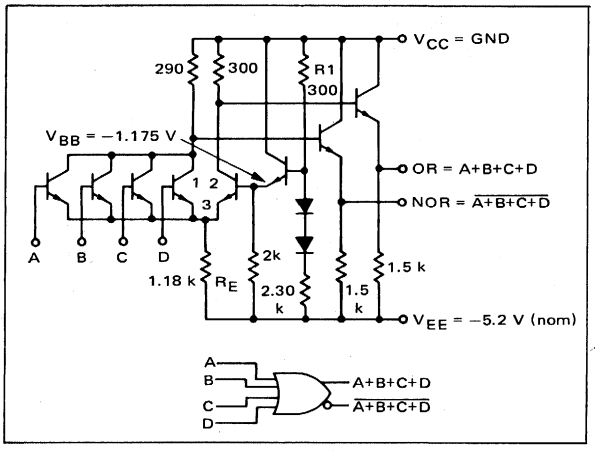


FIGURE 10 - MECL II TRANSFER CHARACTERISTICS AND SPECIFICATION POINTS

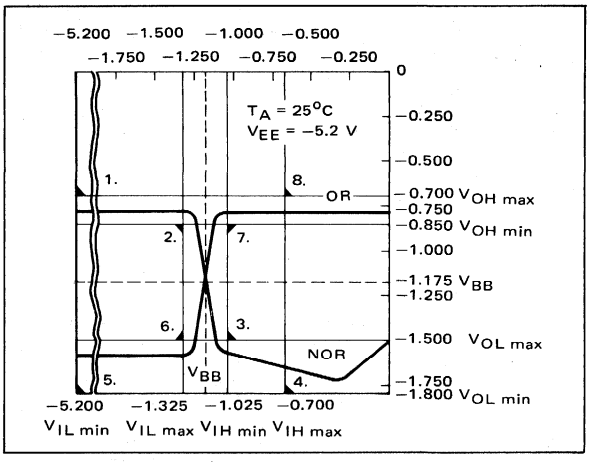
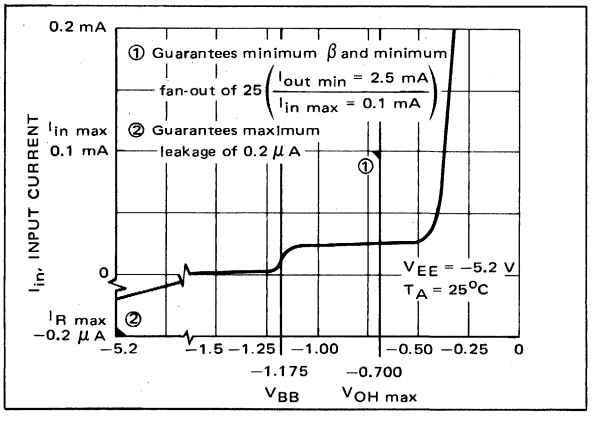


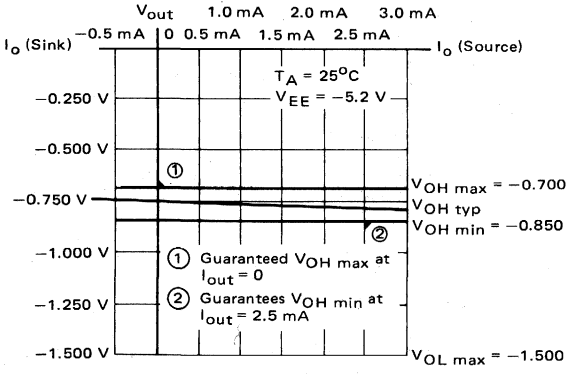
FIGURE 11 - TYPICAL INPUT VOLTAGE versus INPUT CURRENT



The emitter follower outputs offer low output impedance. Typically 15 ohms or less is measured, while a worst-case impedance of 20 ohms should be considered for any design requirements. See Figure 12 for output characteristics and specification points. The emitter follower outputs also permit the positive Wired-OR function to be obtained by tying outputs together.

Logic "0" levels in the MECL II gate are determined by resistor ratios rather than absolute values of resistance. Ratios can be held to within ±5% while absolute values can vary by ±20%. This is a significant advantage in MECL processing. The transistors used in MECL II gates have a typical β of 150. Circuit restrictions on β are much wider than normal processing variations which yields another processing advantage. One processing step – that of gold-doping – is eliminated since the transistors operate in the non-saturating mode.

FIGURE 12 - TYPICAL OUTPUT VOLTAGE versus OUTPUT CURRENT



NOISE MARGIN

Noise margin may be defined as the difference between a worst-case logic level and the worst-case threshold closest to that logic level. The threshold point is sometimes defined as the point on a transfer characteristic curve where the slope is 1/1 indicating unity gain. For MECL II a more conservative threshold is defined as the worst-case input voltage ($V_{IH\ min}$ or $V_{IL\ max}$) for which the output is still within specified limits. Another method of testing noise immunity is obtained by cascading worst-case gates and testing to the minimum "noise" input that will just propagate through the gates. This method is more indicative of actual system operation, and is often referred to as "system noise immunity". The method corresponds to driving the gate into the active region until the output reaches a worst-case V_{BB} level which could then propagate through another gate. This method yields at least 0.040 V greater worst-case noise margin than the test methods employed, but it is very difficult to implement. Typical propagation noise immunity is 0.350 V for MECL II.

Figure 13 lists the worst-case limits for the basic MECL II family. Noise margin is easily obtained by subtracting $V_{IH\ min}$ from $V_{OH\ min}$ for high-level noise margin, and $V_{OL\ max}$ from $V_{IL\ max}$ for low-level noise margin. As seen from Figure 13, 0.175 V worst-case noise margin is guaranteed at all temperatures. Gates with higher guaranteed noise margin can be obtained by selection or special order. All noise specifications are also internally guard-banded to minimize correlation problems (a factor which also adds to actual system noise immunity). The worst-case "system noise immunity" (for noise to propagate through two or more worst-case gates) that can be measured with MECL II is 0.050 V greater than that specified in the brochure. For example, it will take more than 0.225 V of "noise" to propagate through MECL II gates specified at 0.175 V noise margin. The question often arises as to system noise margin with gates of different temperatures and power supply voltages driving one another. Figure 13 also lists the worst-case change in logic levels and threshold levels with a change in supply voltage. It is seen that the "1" logic levels are effectively independent of power supply voltage, the threshold level variance is less than 1/8 the change in V_{EE}, and the worst-case "0" logic level change is 1/4 of the V_{EE} change. These changes illustrate the common-mode rejection of power supply variations exhibited by MECL II. It may be shown that a MECL II system will operate with a ±30% variation in supply voltage, but it is recommended that a maximum variation of ±20% from the design nominal of −5.2 V be allowed. Supply variations of ±10% show negligible effect on system performance.

Figure 14 illustrates two worst-case system noise margin calculations with the data from Figure 13. It is seen that a system with a ±5% change in power supply voltage and 100°C temperature differential will still operate with worst-case devices.

Noise immunity is specified only for logic inputs. In system applications noise at both the V_{CC} and the V_{EE} nodes must be considered. The logical "1" levels in MECL II are one diode drop more negative than V_{CC}. Therefore V_{CC} noise immunity is basically the same as logic input noise immunity. In actual measurements, V_{CC} noise immunity is about 0.030 V higher than if the noise were imposed directly on a logic input. V_{EE} noise immunity is typically greater than 1.5 V due to the common-mode rejection of the basic gate.

POWER SUPPLY CONNECTIONS

Ground is usually the most stable and lowest impedance source in a system. For this reason, V_{CC} is usually at ground potential in a MECL system while V_{EE} is the supply voltage. Another advantage of having V_{CC} as ground is that an output may be shorted to ground without drawing high current. If an output is accidentally shorted to V_{EE}, no permanent damage will result. If an output remains shorted for long periods of time (especially with values of V_{EE} greater than −5.2 V), permanent degradation may result due to excessive chip temperatures. The output of high-speed MECL II devices such as the clock driver should not be shorted to V_{EE} due to its very low output impedance.

Nominal power dissipation of the MECL II circuit is 15 mW for the basic gate, 14 mW for each emitter follower pull-down resistor, and 18 mW for the built-in bias driver. Since MECL II devices are built of various combinations of the above, power dissipation per package and logic function can vary widely. For example, a single gate with six output pull-down resistors and a bias driver dissipates 120 mW, while a quad 2-input gate without pull-

FIGURE 13 - MECL II WORST-CASE LEVELS

VOLTAGE LEVEL	AMBIENT TEMPERATURE 125°C	75°C	25°C	0°C	−55°C
$V_{IH\ max}$	−0.535	−0.600	−0.700	−0.735	−0.825
$V_{OH\ max}$	−0.535	−0.600	−0.700	−0.735	−0.825
$V_{OH\ min}$	−0.700	−0.775	−0.850	−0.895	−0.990
$V_{IH\ min}$	−0.875	−0.950	−1.025	−1.070	−1.165
$V_{IL\ max}$	−1.205	−1.260	−1.325	−1.350	−1.405
$V_{OL\ max}$	−1.380	−1.440	−1.500	−1.525	−1.580
$V_{OL\ min}$	−1.720	−1.760	−1.800	−1.830	−1.890
$V_{IL\ min}$	< V_{EE}	< V_{EE}	< V_{EE}	< V_{EE}	< V_{EE}

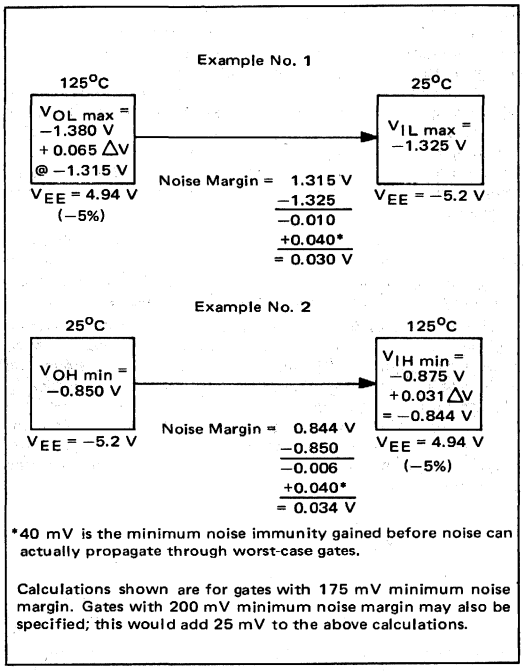
$$\frac{\Delta V_{OH}}{\Delta V_{EE}} = 0.015 \text{ max}$$

$$\frac{\Delta(V_{IH\ min},\ V_{IL\ max})}{\Delta V_{EE}} = \begin{matrix}0.110 \text{ min} \\ 0.115 \text{ nom} \\ 0.120 \text{ max}\end{matrix}$$

$$\frac{\Delta(V_{OL\ max},\ V_{OL\ min})}{\Delta V_{EE}} = \begin{matrix}0.210 \text{ min} \\ 0.230 \text{ nom} \\ 0.250 \text{ max}\end{matrix}$$

down resistors and with a single bias driver dissipates only 20 mW per gate. Normalized power dissipation curves versus temperature and supply voltages are shown in Figure 15. Power dissipation for system design should be 80% of the value calculated from the I_E maximum values specified on the various data sheets. Nominal power dissipation is lower (75% of the maximum value specified).

FIGURE 14 - EXAMPLES OF WORST CASE NOISE MARGINS IN A MECL II SYSTEM



*40 mV is the minimum noise immunity gained before noise can actually propagate through worst-case gates.

Calculations shown are for gates with 175 mV minimum noise margin. Gates with 200 mV minimum noise margin may also be specified; this would add 25 mV to the above calculations.

DC LOADING CONSIDERATIONS

Worst-case fan-out specifications are obtained from Figures 11 and 12. With a worst-case input current of 100 μA and a minimum output current of 2.5 mA for a $V_{OH\ min}$ level, a fan-out of 25 is guaranteed. Figure 16 illustrates the typical input characteristics of a MECL II gate versus temperature and a wide excursion of input voltage. The output dc loading characteristics of MECL II are shown in Figure 17 for loads that greatly exceed normal operation. It may be observed from the curves that one MECL II gate could typically drive more than a thousand other gates before noise immunity dropped below 0.100 V. It is obvious that loading restrictions are normally ac rather than dc. The heaviest loading occurs under Wired-OR conditions. If only one pull-down resistor is used (recommended as a power saving feature), the dc loading is the same as for normal conditions. If two pull-down resistors are employed, an additional current of 3.6 mA maximum is drawn at V_{EE} = −5.2 V and T_A = 25°C. $V_{OH\ min}$ is specified at 2.5 mA load current, but the worst-case pull-down resistor draws an additional 1.1 mA. A worst-case output impedance of 20 ohms would then give an additional drop of 0.022 V. If the Wired-OR also drives a nominal fan-out, the output may drop 0.025 V below $V_{OH\ min}$ which subtracts 0.025 V from the worst-case noise margin. For this reason a maximum of two pull-down resistors is recommended for worst-case system design. It should be noted that two pull-down resistors appreciably decrease fall time under high capacitance loading. Typically three pull-down resistors (an additional load of 6.0 mA) would give a V_{OH} of 0.850 V, which is $V_{OH\ min}$.

AC LOADING CONSIDERATIONS

The input capacitance of a MECL II gate averages 3.3 pF. Since in any system stray capacitance is also present, a typical value of 5.0 pF per fan-out should be used for design purposes. A fan-out of 15 MECL II gates is than roughly equivalent to 75 pF, while a fan-out of 20 gates would be approximately 100 pF. These figures may be easily decreased with careful layout techniques.

FIGURE 15 - NORMALIZED POWER DISSIPATION versus TEMPERATURE AND SUPPLY VOLTAGE

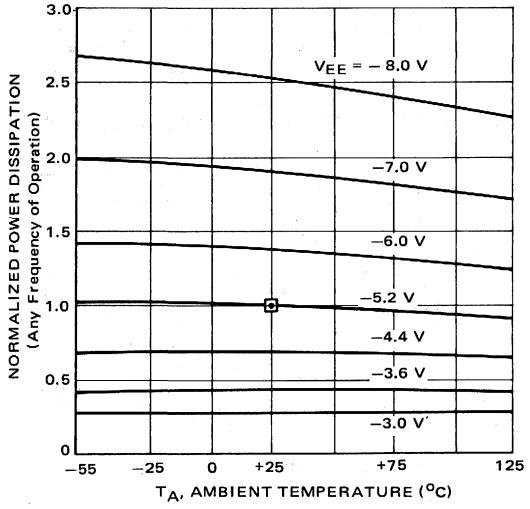


FIGURE 16 - INPUT CURRENT versus INPUT VOLTAGE AND TEMPERATURE

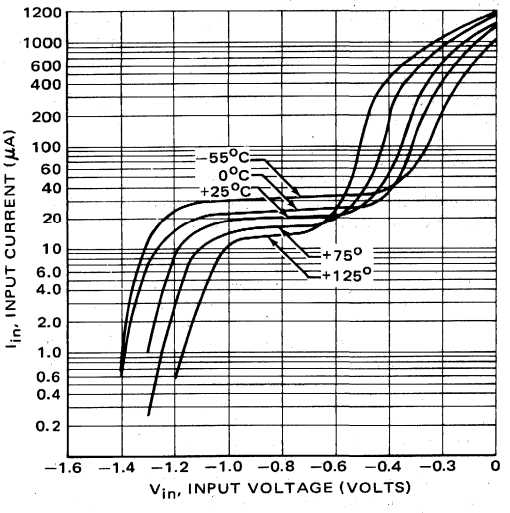
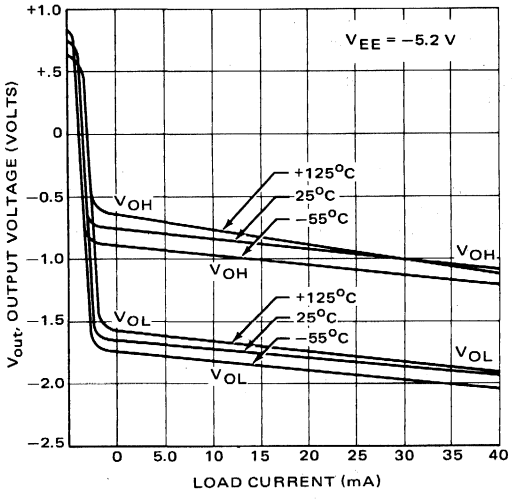
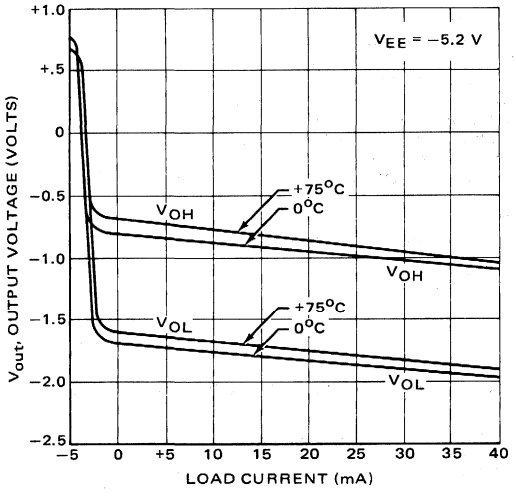


FIGURE 17 - TYPICAL OUTPUT VOLTAGES versus LOAD CURRENT
(Ambient Temperature)





SWITCHING TIMES

Figures 18 through 21 give typical rise, fall, and propagation delay times versus loading and temperature. The slow fall times and t_{pd-} are caused by the relatively long R-C time constant of the emitter pull-down resistor and the load capacitance. The fall time, t_f, may be calculated as 0.2 RC, where R is the value of the pull-down resistor (in kΩ) and C is the external load capacitance (in pF). For example, with a 100 pF load and a 1.5 k-ohm internal resistor, the fall time is approximately 30 ns. The increase in t_{pd-} over the delay at no load is very closely obtained by 0.1 RC. At no load, t_{pd-} is approximately 3.5 ns, and 0.1 RC with a 100 pF load is 15 ns, giving a total of 18.5 ns for t_{pd-}. The RC time constant of the load may be reduced significantly (for high capacitance) by paralleling an external resistance with the load to V_{EE}.

FIGURE 18 - RISE TIME versus LOADING AND TEMPERATURE

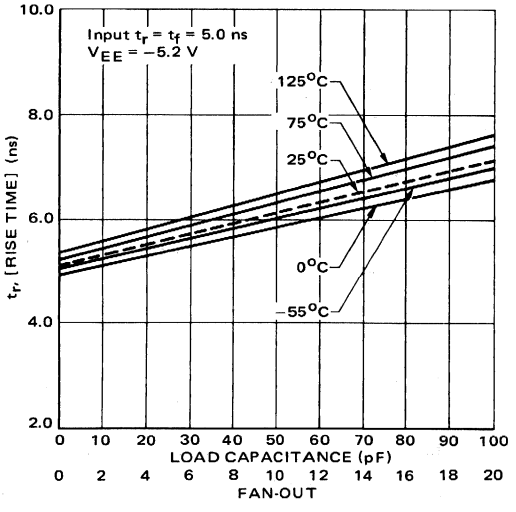
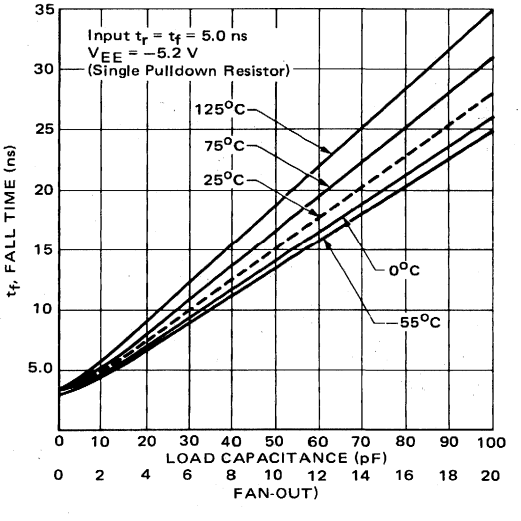


FIGURE 19 - FALL TIME versus LOADING AND TEMPERATURE
(Single Pulldown Resistor)



THERMAL CHARACTERISTICS

The junction temperature of the integrated circuit is closely related to its long term operational characteristics; therefore, an accurate estimate of the junction temperature of the various circuit components must be made before the circuit designer can predict the expected reliability of his system. Motorola is including sufficient information in this section to permit the user of MECL II to estimate worst-case junction temperatures if he can estimate accurately the ambient or case temperatures and the operating circuit's power drain.

The average temperature at the junction region is a function of the systems ability to remove the heat generated in the circuit from the junction regions to the ambient or equivalent heat sink. The basic formula for converting calculated power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$$

or

$$T_J = T_A + P_D (\theta_{JA})$$

where

T_A = ambient temperature
P_D = calculated power dissipation
θ_{JC} = thermal resistance, junction to case
θ_{CA} = thermal resistance, case to ambient
θ_{JA} = thermal resistance, junction to ambient.

The worst-case rated thermal resistance values for Motorola's integrated circuit packages are found in Table 1. Figures 22, 23, and 24 are variations of the same derating curve. Figure 22, for instance, plots the maximum permissible package power handling capability as a function of ambient temperature when the maximum permissible junction is at 150°C (plastic package) and 175°C (ceramic flat package). Figure 23 plots worst-case junction temperature as a function of power dissipated for the two ambient temperatures, 75°C and 125°C. Figure 24 plots the junction temperature as a function of power drain when the case temperature is held constant. These figures have been developed using the worst-case thermal resistance values found in Table 1.

FIGURE 20 - PROPAGATION DELAY t_{pd+} versus LOADING AND TEMPERATURE

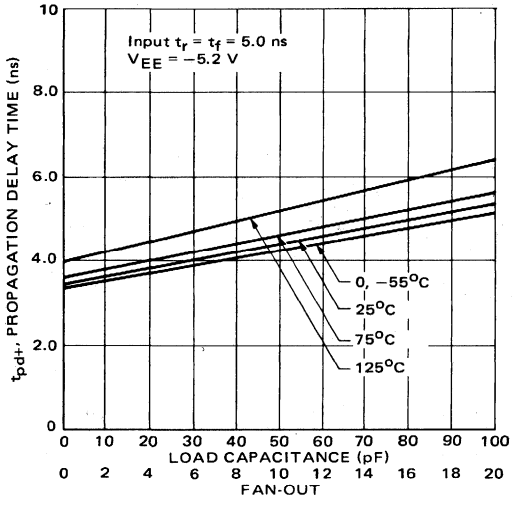


FIGURE 21 - PROPAGATION DELAY t_{pd-} versus LOADING AND TEMPERATURE

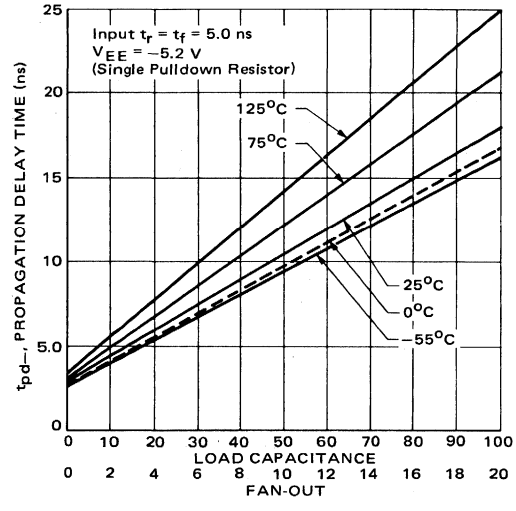


FIGURE 22 - AMBIENT TEMPERATURE DERATING CURVE

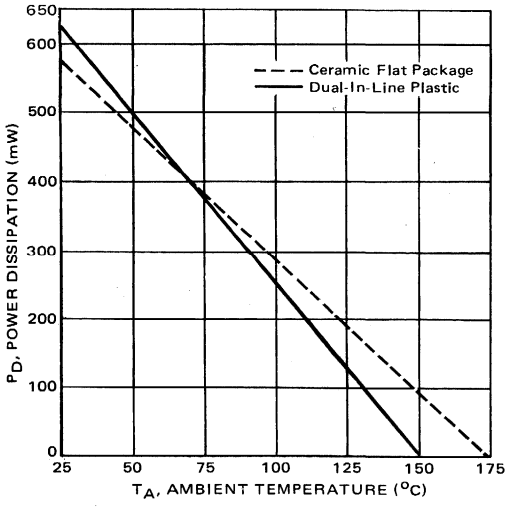


FIGURE 23 - JUNCTION TEMPERATURE DERATING CURVE USING AMBIENT TEMPERATURE

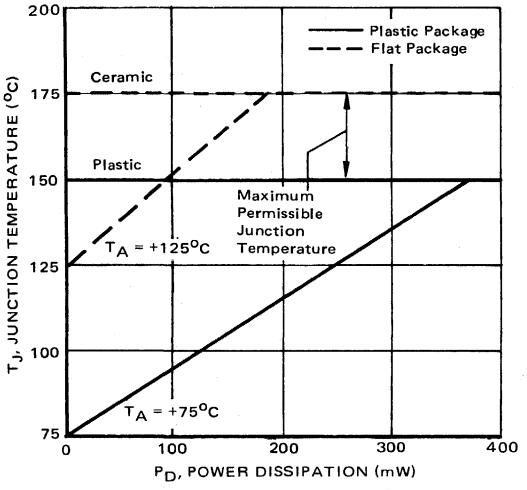


FIGURE 24 - JUNCTION TEMPERATURE DERATING CURVE USING CASE TEMPERATURE

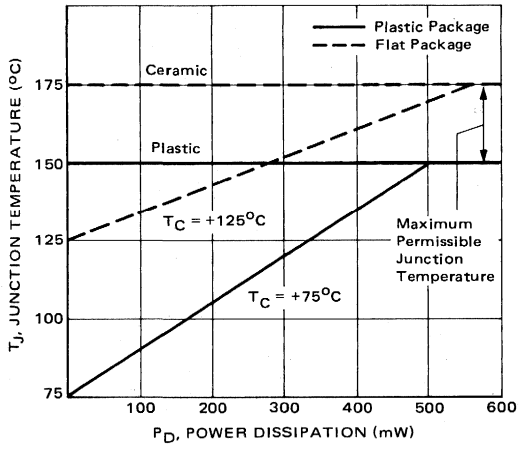


TABLE 1 - WORST-CASE THERMAL RESISTANCE OF INTEGRATED CIRCUIT PACKAGES

PACKAGE	θ_{JA} JUNCTION TO AMBIENT	θ_{JC} JUNCTION TO CASE
Ceramic Flat Package 14 lead ¼ x ¼ inch	0.26°C/mW	0.090°C/mW
Plastic 14 lead dual-in-line	0.20°C/mW	0.15°C/mW

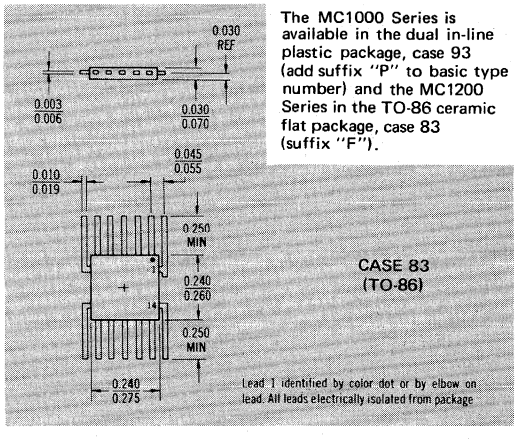
MAXIMUM RATINGS

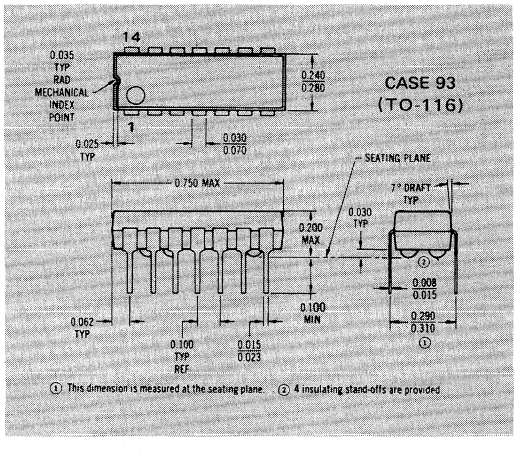
Characteristic		Symbol	Rating	Unit
Ratings above which device life may be impaired:				
Power Supply Voltage (V_{CC} = 0)		V_{EE}	−10	Vdc
Input Voltage (V_{CC} = 0)		V_{in}	0 to V_{EE}	Vdc
Output Source Current		Io	20	mAdc
Storage Temperature Range	MC1000 MC1200	T_{stg}	−55 to +125 −65 to +175	°C
Recommended maximum ratings above which performance may be degraded:				
Operating Temperature Range	MC1000 MC1200	T_A	0 to +75 −55 to +125	°C
AC Fan-In (Expandable Gates)		m	20	—
AC Fan-Out* (Gates and Flip-Flops)		n	15	—

*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

PACKAGING

The MC1000 Series is available in the dual in-line plastic package, case 93 (add suffix "P" to basic type number) and the MC1200 Series in the TO-86 ceramic flat package, case 83 (suffix "F").



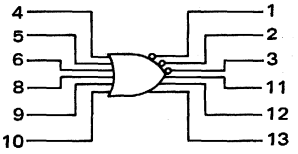


MC1001 thru MC1003
MC1201 thru MC1203

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

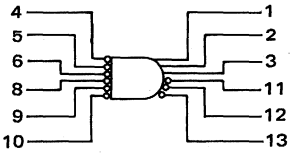
POSITIVE LOGIC



$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$

$11 = 4 + 5 + 6 + 8 + 9 + 10$

NEGATIVE LOGIC



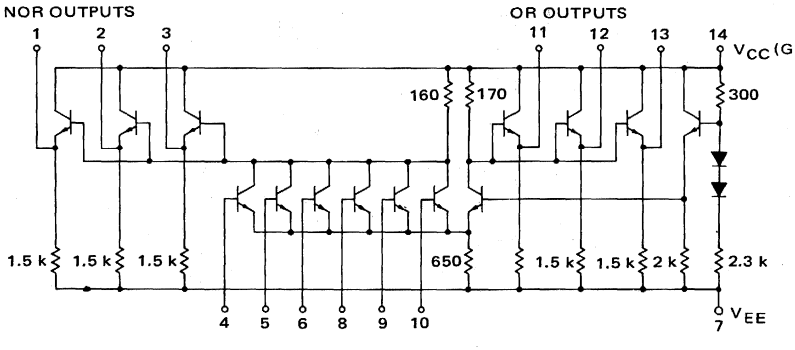
$1 = \overline{4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10}$

$11 = 4 \cdot 5 \cdot 6 \cdot 8 \cdot 9 \cdot 10$

DC Input Loading Factor = 2
DC Output Loading Factor = 25

Power Dissipation = MC1001/MC1201 — 115 mW typical
MC1002/MC1202 — 80 mW typical
MC1003/MC1203 — 40 mW typical

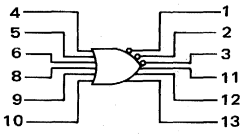
MC1001/MC1201 CIRCUIT SCHEMATIC



MC1002/MC1202
Omit NOR output pulldown resistors

MC1003/MC1203
Omit all output pulldown resistors

Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

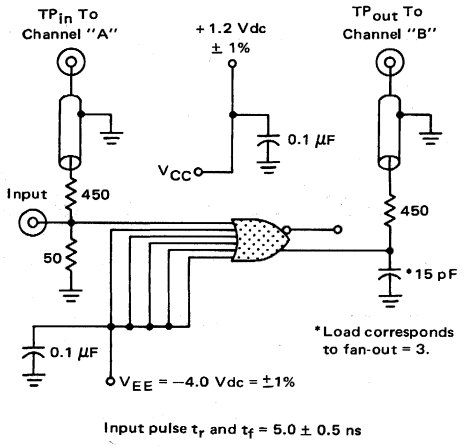
Characteristic	Symbol	Pin Under Test	MC1201-1203 Test Limits							MC1001-1003 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7														
MC1201/MC1001			-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1202/MC1002			-	-	-	22	-	-		-	-	-	22	-	-	
MC1203/MC1003			-	-	-	11	-	-		-	-	-	11	-	-	
Input Current	I_{in}	4	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
		5	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{4+1-}	1	4.0	7.5	4.0	7.0	6.0	9.0	ns	4.0	7.0	4.0	7.0	5.0	8.0	ns
	t_{4-1+}	1					6.0	9.0								
	t_{4+11+}	11					5.0	9.0								
	t_{4-11-}	11					6.0	9.0								
(Fan-Out = 15)	t_{4+1-}	1	18	-	18	-	22	-		18	-	18	-	20	-	
	t_4-1+	1	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_4+11+	11	4.0	-	4.0	-	6.0	-		4.0	-	4.0	-	5.0	-	
	t_{4-11-}	11	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{1+}	1	5.0	8.0	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.5	8.0	
	t_{11+}	11	4.0	7.0	4.0	6.5	5.0	8.0		4.0	6.5	4.0	6.5	4.5	7.0	
Fall Time (Fan-Out = 3)	t_{1-}	1	6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	
	t_{11-}	11	6.0	8.0	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	

*Individually test each input using the pin connections shown.
†Individually test each output listed using the pin connections shown.
‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.

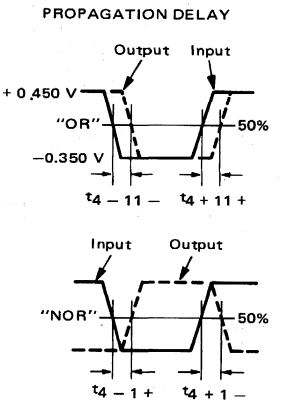
@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1201-1203	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1001-1003	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

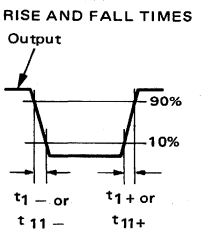
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1201/MC1001			-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
MC1202/MC1002			-	-	-	↓	-	↓
MC1203/MC1003			-	-	-		-	
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	14
		5	-	-	5	4, 6, 7, 8, 9, 10	-	
		6	-	-	6	4, 5, 7, 8, 9, 10	-	
		8	-	-	8	4, 5, 6, 7, 9, 10	-	
		9	-	-	9	4, 5, 6, 7, 8, 10	-	
		10	-	-	10	4, 5, 6, 7, 8, 9		
Input Leakage Current	I_R	Inputs*	-	-	-	4, 5, 6, 7, 8, 9, 10	-	14
"NOR" Logical "1" Output Voltage	V_{OH}‡	1, 2, 3†	4	-	-	5, 6, 7, 8, 9, 10	‡	14
			5	-	-	4, 6, 7, 8, 9, 10		
			6	-	-	4, 5, 7, 8, 9, 10		
			8	-	-	4, 5, 6, 7, 9, 10		
			9	-	-	4, 5, 6, 7, 8, 10		
			10	-	-	4, 5, 6, 7, 8, 9		
"NOR" Logical "0" Output Voltage	V_{OL}	1, 2, 3†	-	4	-	5, 6, 7, 8, 9, 10	-	14
			-	5	-	4, 6, 7, 8, 9, 10	-	
			-	6	-	4, 5, 7, 8, 9, 10	-	
			-	8	-	4, 5, 6, 7, 9, 10	-	
			-	9	-	4, 5, 6, 7, 8, 10	-	
			-	10	-	4, 5, 6, 7, 8, 9	-	
"OR" Logical "1" Output Voltage‡	V_{OH}‡	11, 12, 13†	-	4	-	5, 6, 7, 8, 9, 10	‡	14
			-	5	-	4, 6, 7, 8, 9, 10		
			-	6	-	4, 5, 7, 8, 9, 10		
			-	8	-	4, 5, 6, 7, 9, 10		
			-	9	-	4, 5, 6, 7, 8, 10		
			-	10	-	4, 5, 6, 7, 8, 9		
"OR" Logical "0" Output Voltage	V_{OL}	11, 12, 13†	4	-	-	5, 6, 7, 8, 9, 10	-	14
			5	-	-	4, 6, 7, 8, 9, 10	-	
			6	-	-	4, 5, 7, 8, 9, 10	-	
			8	-	-	4, 5, 6, 7, 9, 10	-	
			9	-	-	4, 5, 6, 7, 8, 10	-	
			10	-	-	4, 5, 6, 7, 8, 9	-	
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Propagation Delay (Fan-Out = 3)	t_{4+1-}	1	4	1	-	5, 6, 7, 8, 9, 10	-	14
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
(Fan-Out = 15)	t_{4+1-}	1		1	-		-	
	t_{4-1+}	1		1	-		-	
	t_{4+11+}	11		11	-		-	
	t_{4-11-}	11		11	-		-	
Rise Time (Fan-Out = 3)	t_{1+}	1		1	-		-	
	t_{11+}	11		11	-		-	
Fall Time (Fan-Out = 3)	t_{1-}	1		1	-		-	
	t_{11-}	11	↓	11	-	↓	-	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input pulse t_r and t_f = 5.0 ± 0.5 ns





Switching waveforms shown for pulse in on pin 4 and pulse out on pins 1 and 11, however all other input-output combinations will meet the limits specified.

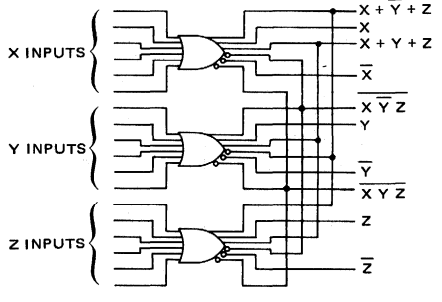
APPLICATIONS INFORMATION

The MC1001-1003/MC1201-1203 6-input OR/NOR gates are extremely useful in generating multiple wired-OR logic functions since six independent outputs are provided. (An example is shown in Figure 1.) The gate performs well as a clock driver with the multiple outputs which result in three times the normal fan-out for a given clock waveform. If twisted pair lines are being used for clock distribution in a system, the gate will drive three independent twisted pair lines, each with the same clock waveform.

An output impedance of about 2 ohms is obtained if three OR or NOR outputs are tied together. This provides an excellent 50-ohm driving capability. The 50-ohm line or coax should be terminated in its characteristic impedance to a nominal −2.0 V. This prevents excessively high output current that would pull the logic "1" level below nominal (see Figure 2).

FIGURE 1 - MECL II "WIRED OR" FEATURE

EXAMPLE SHOWN FOR ONE POSSIBLE COMBINATION OF OUTPUTS



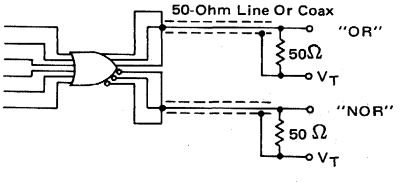
WHERE:
X = f (Six Variables)
Y = f (Six Variables)
Z = f (Six Variables)

t_{pd} Average = 4.0 ns
Total Power = 200 mW

NOTE:
All Outputs That Are Used Require An Internal or External Pulldown Resistor.

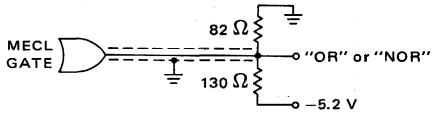
FIGURE 2 - MC1003/MC1203 AS A 50-OHM DRIVER WITH NOMINAL MECL LOGIC LEVELS

50-OHM TERMINATION TO SEPARATE NEGATIVE VOLTAGE



$V_T \approx -2.0$ V Well Bypassed To Ground

50 OHM TERMINATION TO MECL POWER SUPPLY



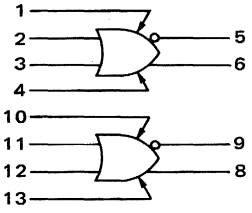
Output Logic Swing ≈ 0.8 V
Typical Gate Propagation Delay = 4.0 ns
Typical Rise Time At 50-Ohm Load = 7.0 ns
Typical Fall Time At 50-Ohm Load = 7.0 ns

MC1024
MC1224

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

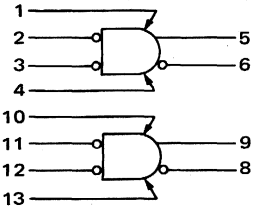
Expandable inputs are available on pins 1, 4 and 10, 13 as shown in the circuit schematic.

POSITIVE LOGIC



$5 = \overline{2 + 3}$
$6 = 2 + 3$

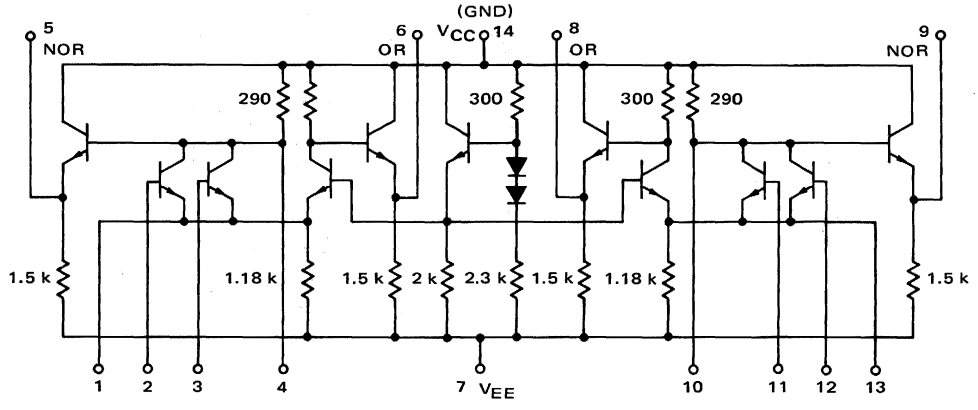
NEGATIVE LOGIC



$5 = \overline{2 \cdot 3}$
$6 = 2 \cdot 3$

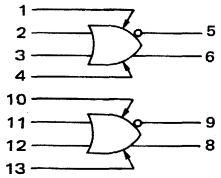
DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 95 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

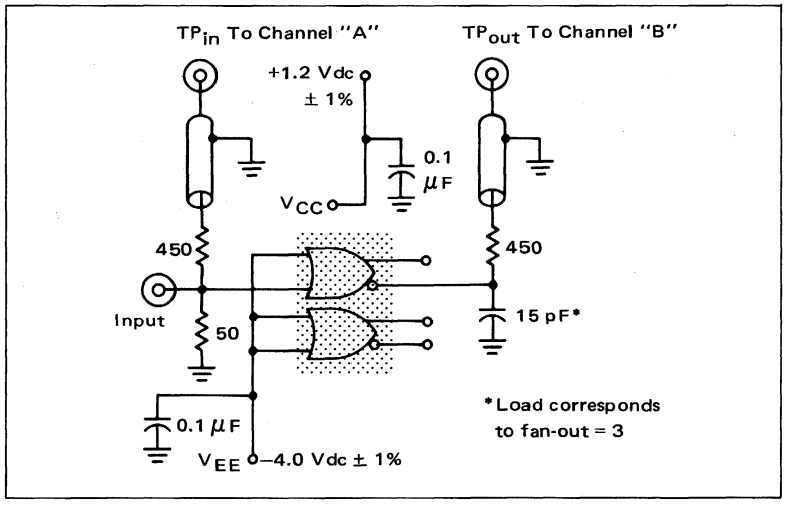


Test procedures are shown for only one gate.
The other gate is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1224 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	26	-	-	mAdc	-	-	-	26	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		3	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times Propagation Delay			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
(Fan-Out = 3)	t_{2+5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns
	t_{2-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0		4.0	7.5	4.0	7.5	5.0	8.5	
	t_{2+6+}	6	4.0	7.5	4.0	7.0	5.5	8.5		4.0	7.0	4.0	7.0	5.0	8.0	
	t_{2-6-}	6	4.0	7.0	4.0	7.0	5.5	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{2+5-}	5	14	-	14	-	18	-		14	-	14	-	16	-	
	t_{2-5+}	5	5.0	-	5.0	-	7.0	-		5.0	-	5.0	-	6.0	-	
	t_{2+6+}	6	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_{2-6-}	6	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.0	8.0	
	t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0		4.0	6.5	4.0	6.5	5.0	7.0	
Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0	10		5.0	8.0	5.0	8.0	5.5	9.0	
	t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10		5.0	8.0	5.0	8.0	6.0	9.0	

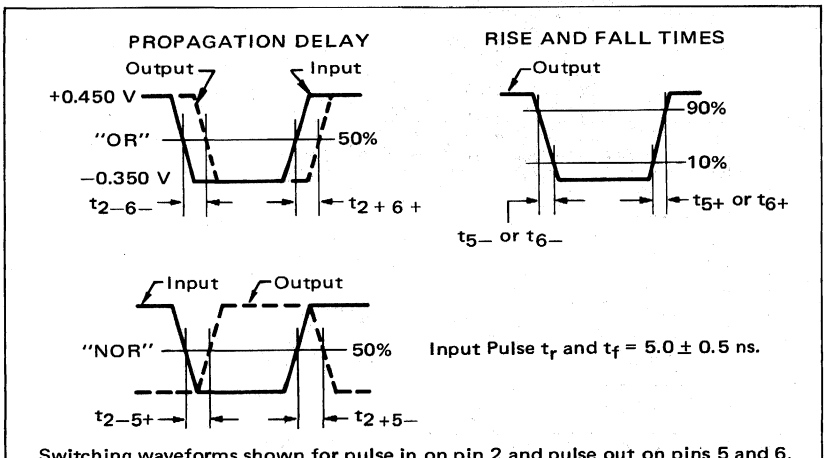
*Individually test each input using the pin connections shown. ‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1224	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1024	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 7, 11, 12	-	14
Input Current	I_{in}	2	-	-	2	3, 7, 11, 12	-	14
		3	-	-	3	2, 7, 11, 12	-	14
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 7, 11, 12	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	2	-	-	3, 7, 11, 12	5	14
		5	3	-	-	2, 7, 11, 12	5	14
"NOR" Logical "0" Output Voltage	V_{OL}	5	-	2	-	3, 7, 11, 12	-	14
		5	-	3	-	2, 7, 11, 12	-	14
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-	2	-	3, 7, 11, 12	6	14
		6	-	3	-	2, 7, 11, 12	6	14
"OR" Logical "0" Output Voltage	V_{OL}	6	2	-	-	3, 7, 11, 12	-	14
		6	3	-	-	2, 7, 11, 12	-	14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay (Fan-Out = 3)	t_{2+5-}	5	2	5	-	3, 7, 11, 12	-	14
	t_{2-5+}	5		5	-		-	
	t_{2+6+}	6		6	-		-	
	t_{2-6-}	6		6	-		-	
(Fan-Out = 15)	t_{2+5-}	5		5	-		-	
	t_{2-5+}	5		5	-		-	
	t_{2+6+}	6		6	-		-	
	t_{2-6-}	6		6	-		-	
Rise Time (Fan-Out = 3)	t_{5+}	5		5	-		-	
	t_{6+}	6		6	-		-	
Fall Time (Fan-Out = 3)	t_{5-}	5		5	-		-	
	t_{6-}	6		6	-		-	



Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

SWITCHING TIME WAVEFORMS

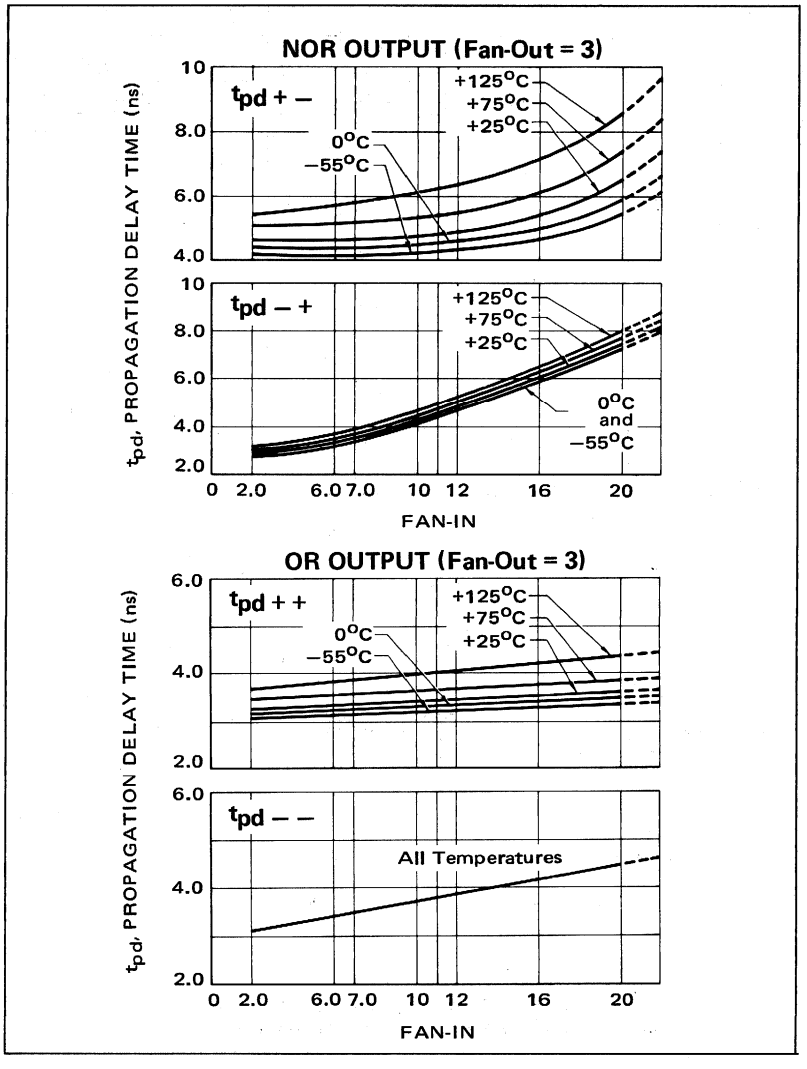
Switching waveforms shown for pulse in on pin 2 and pulse out on pins 5 and 6, however all other input-output combinations will meet the limits specified.

APPLICATIONS INFORMATION

The MC1024/MC1224 dual 2-input expandable OR/NOR gate provides the capability of increasing fan-in by making available the collector and emitter nodes of the standard gate. Note that complementary outputs are available, lending to circuit flexibility. By using the MC1025/MC1225 expander 6, 7, 10, 11, 12, 15, 16, or 20 gate inputs may be obtained with one or two expanders per gate. Note that as fan-in is increased, capacitance is added to the input collector node and propagation delays through the gate will increase. A maximum fan-in of 20 is recommended for high-speed operation. If high speed is not required, larger fan-ins may be utilized.

The expandable inputs allow a large fan-in NOR or NAND gate to be obtained, where power dissipation is decreased at the expense of propagation delay. The OR propagation delay times vary little with increasing fan-in since capacitance is not being added to the OR collector node. At a fan-in of 20, NOR output rise and fall times approach 20 ns, while OR output rise and fall times remain about 4.0 ns. For minimal added capacitance at the NOR collector node, lead lengths should be kept short and the circuits wired in directly rather than using sockets. Typical propagation delay curves versus fan-in and temperature are shown below.

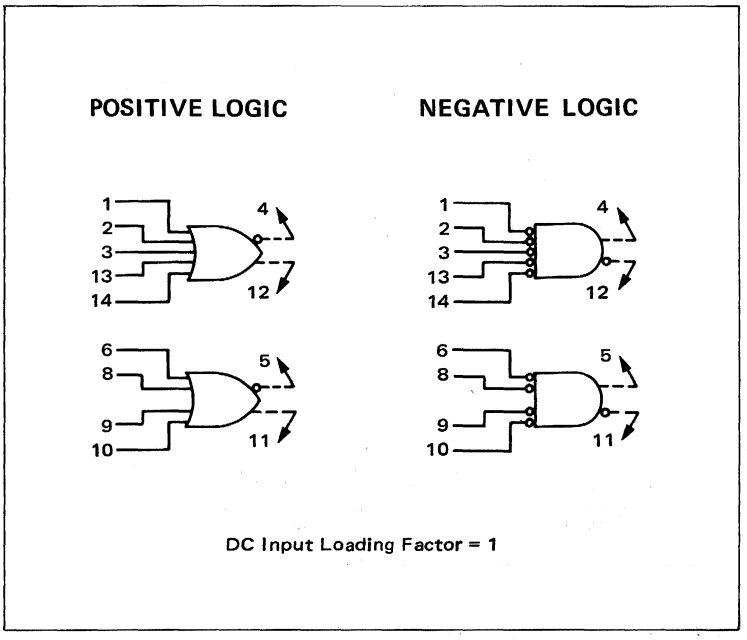
TYPICAL PROPAGATION DELAY TIMES



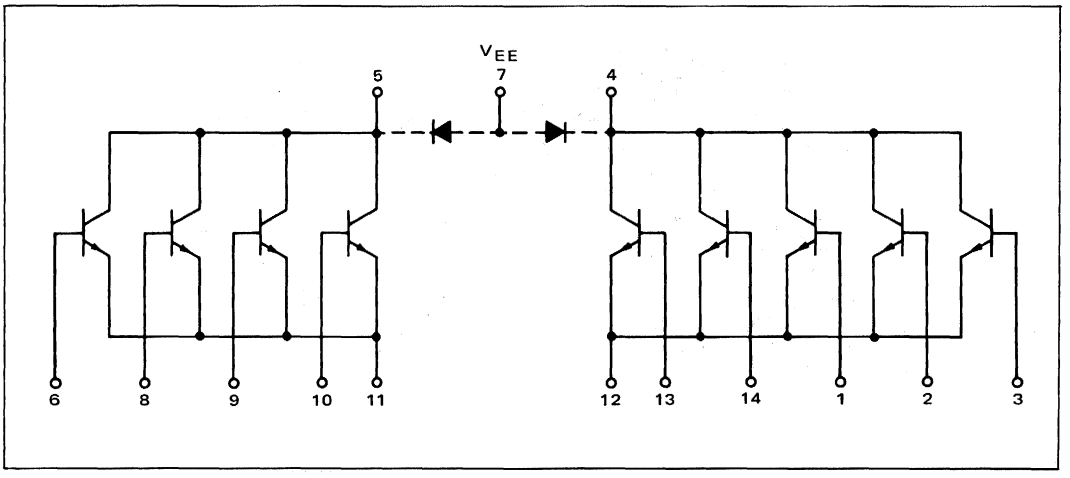
MC1025
MC1225

Dual expander arrays, with a 4-transistor array isolated from a 5-transistor array. The collectors and emitters from both arrays may be connected to form a 9-transistor array. With each base available, a 4, 5, or 9-input expander may be obtained.

Designed specifically for use with MC1024/MC1224 Dual 2-Input Gates.

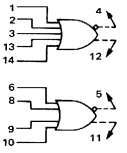


CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander.
The other expander is tested in the same manner.



@ All Temperatures

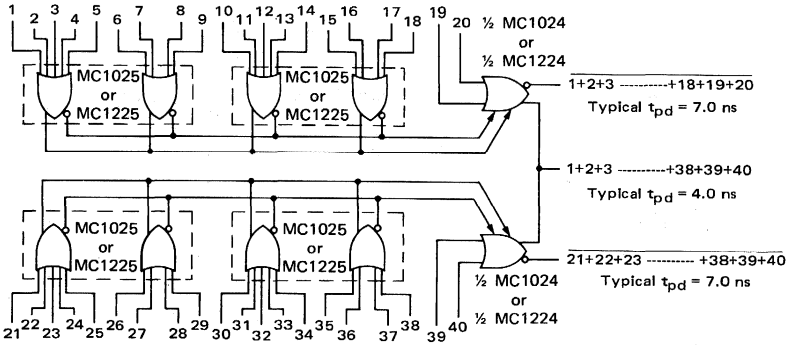
TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					mAdc
V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E
-2.0	+2.0	-5.2	+0.7	+0.3	-1.33

Characteristic	Symbol	Pin Under Test	MC1225 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1025 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{EE}	V_{CC}	V_{BB}	V_{CB}	V_{BE}	I_E	Gnd
Base Leakage Current	I_{BL}	1	-	0.5	-	0.5	-	2.0	μAdc	-	0.5	-	0.5	-	2.0	μAdc	11,12	-	1	-	-	-	4,5,7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	↓	-	2	-	-	-	↓
		3	-		-		-			-		-		-				-	3	-	-	-	
		13	-		-		-			-		-		-				-	13	-	-	-	
		14	-		-		-			-		-		-				-	14	-	-	-	
Collector Leakage Current	I_{CEX}	1	-	1.0	-	1.0	-	100	μAdc	-	1.0	-	1.0	-	15.0	μAdc	-	4,5,7	-	-	1	-	11,12
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	-	2	-	↓
		3	-		-		-			-		-		-			-		-	-	3	-	
		13	-		-		-			-		-		-			-		-	-	13	-	
		14	-		-		-			-		-		-			-		-	-	14	-	
Input Voltage	V_{BE}	12	-0.860	-0.910	-0.710	-0.760	-0.520	-0.570	Vdc	-0.760	-0.810	-0.710	-0.760	-0.610	-0.660	Vdc	-	-	-	4,5	-	12	1
			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-	-	-		-		2
																	-	-	-		-		3
																	-	-	-		-		13
																	-	-	-		-		14

APPLICATIONS INFORMATION

The MC1025/MC1225 dual 4-5 input expander is designed to work with the MC1024/MC1224 expandable gate. The transistors are manufactured with the same buried layer process used on all MECL II devices and are typical of MECL II gate transistors. BV_{CEO} is 12 V or greater, $f_T \approx 600$ MHz, and β is typically from 100 to 150. An example of two 20-input NOR gates and a 40-input OR gate made from an MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders is shown.

Two 20-input NOR gates and one 40-input OR gate generated using one MC1024/MC1224 expandable gate and four MC1025/MC1225 expanders.



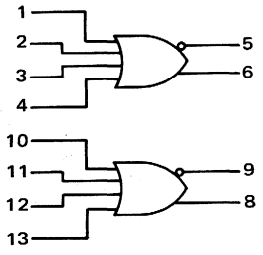
Power Dissipation = 100 mW

MC1004 thru MC1006
MC1204 thru MC1206

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

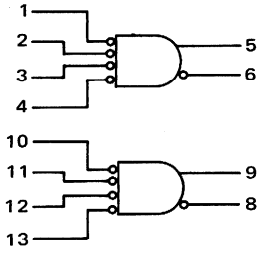
POSITIVE LOGIC



$5 = \overline{1 + 2 + 3 + 4}$

$6 = 1 + 2 + 3 + 4$

NEGATIVE LOGIC



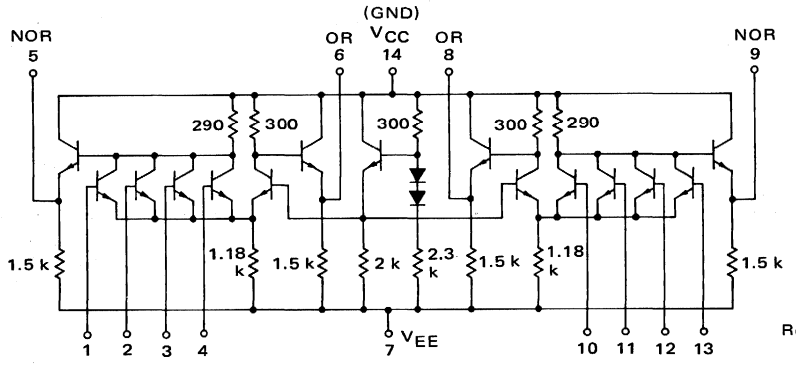
$5 = \overline{1 \cdot 2 \cdot 3 \cdot 4}$

$6 = 1 \cdot 2 \cdot 3 \cdot 4$

DC Input Loading Factor = 1
DC Output Loading Factor = 25

Power Dissipation = MC1004/MC1204 — 95 mW typical
MC1005/MC1205 — 65 mW typical
MC1006/MC1206 — 45 mW typical

MC1004/MC1204 CIRCUIT SCHEMATIC



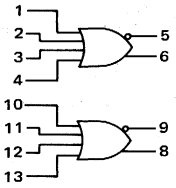
MC1005/MC1205
Omit NOR output pulldown resistors.

MC1006/MC1206
Omit all output pulldown resistors.

Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 kΩ resistor to V_{EE}.



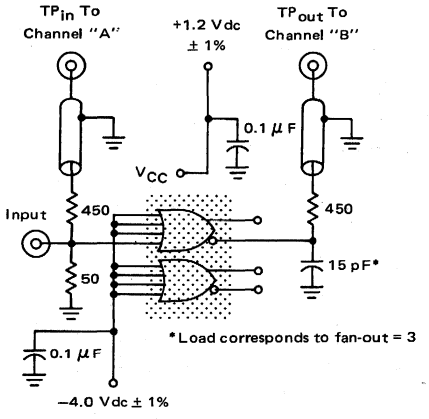
Characteristic	Symbol	Pin Under Test	MC1204-1206 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1004-1006 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1204/MC1004			-	-	-	26	-	-	mAdc	-	-	-	26	-	-	mAdc
MC1205/MC1005			-	-	-	18	-	-		-	-	-	18	-	-	
MC1206/MC1006			-	-	-	12	-	-		-	-	-	12	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-		-	-		-	-	-		-	-	
		3	-	-	-		-	-		-	-	-		-	-	
		4	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns
	t_{1-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0		4.0	7.5	4.0	7.5	5.0	8.5	
	t_{1+6+}	6	4.0	7.5	4.0	7.0	5.5	8.5		4.0	7.0	4.0	7.0	5.0	8.0	
	t_{1-6-}	6	4.0	7.0	4.0	7.0	5.5	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{1+5-}	5	14	-	14	-	18	-		14	-	14	-	16	-	
	t_{1-5+}	5	5.0	-	5.0	-	7.0	-		5.0	-	5.0	-	6.0	-	
	t_{1+6+}	6	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_{1-6-}	6	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.0	8.0	
	t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0		4.0	6.5	4.0	6.5	5.0	7.0	
Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0	10		5.0	8.0	5.0	8.0	5.5	9.0	
	t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10		5.0	8.0	5.0	8.0	6.0	9.0	

* Individually test each input using the pin connections shown. ‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

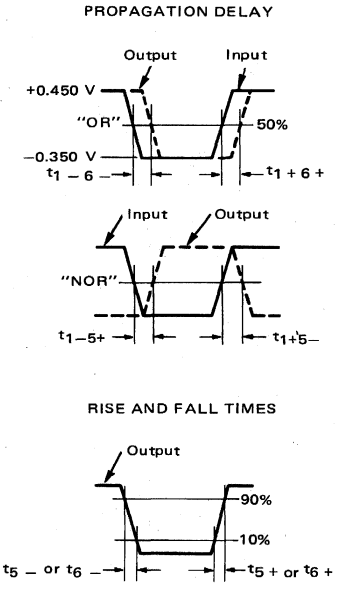
@Test Temperature		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L
MC1204-1206	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1004-1006	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1204/MC1004			-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13	-	14
MC1205/MC1005			-	-	-	↓	-	↓
MC1206/MC1006			-	-	-		-	
Input Current	I_{in}	1	-	-	1	2, 3, 4, 7, 10, 11, 12, 13	-	14
		2	-	-	2	1, 3, 4, 7, 10, 11, 12, 13	-	↓
		3	-	-	3	1, 2, 4, 7, 10, 11, 12, 13	-	
		4	-	-	4	1, 2, 3, 7, 10, 11, 12, 13	-	
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	5	14
		↓	2	-	-	1, 3, 4, 7, 10, 11, 12, 13	↓	↓
			3	-	-	1, 2, 4, 7, 10, 11, 12, 13		
			4	-	-	1, 2, 3, 7, 10, 11, 12, 13		
"NOR" Logical "0" Output Voltage	V_{OL}	5	-	1	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
		↓	-	2	-	1, 3, 4, 7, 10, 11, 12, 13	-	↓
			-	3	-	1, 2, 4, 7, 10, 11, 12, 13	-	
			-	4	-	1, 2, 3, 7, 10, 11, 12, 13	-	
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-	1	-	2, 3, 4, 7, 10, 11, 12, 13	6	14
		↓	-	2	-	1, 3, 4, 7, 10, 11, 12, 13	↓	↓
			-	3	-	1, 2, 4, 7, 10, 11, 12, 13		
			-	4	-	1, 2, 3, 7, 10, 11, 12, 13		
"OR" Logical "0" Output Voltage	V_{OL}	6	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
		↓	2	-	-	1, 3, 4, 7, 10, 11, 12, 13	-	↓
			3	-	-	1, 2, 4, 7, 10, 11, 12, 13	-	
			4	-	-	1, 2, 3, 7, 10, 11, 12, 13	-	
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay								
(Fan-Out = 3)	t_{1+5-}	5	1	5	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
	t_{1-5+}	5	↓	5	-	↓	-	↓
	t_{1+6+}	6		6	-		-	
	t_{1-6-}	6		6	-		-	
(Fan-Out = 15)	t_{1+5-}	5		5	-		-	
	t_{1-5+}	5		5	-		-	
	t_{1+6+}	6		6	-		-	
	t_{1-6-}	6		6	-		-	
Rise Time (Fan-Out = 3)	t_{5+}	5		5	-		-	
	t_{6+}	6		6	-		-	
Fall Time (Fan-Out = 3)	t_{5-}	5		5	-		-	
	t_{6-}	6	↓	6	-	↓	-	↓

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

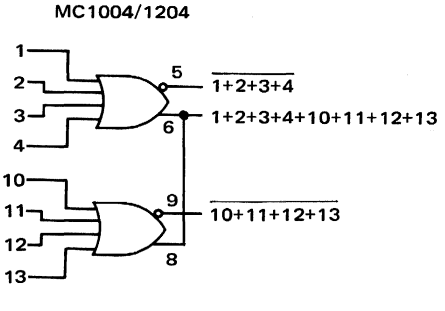


Switching waveforms shown for pulse in on pin 1 and pulse out on pins 5 and 6, however all other input-output combinations will meet the limits specified.

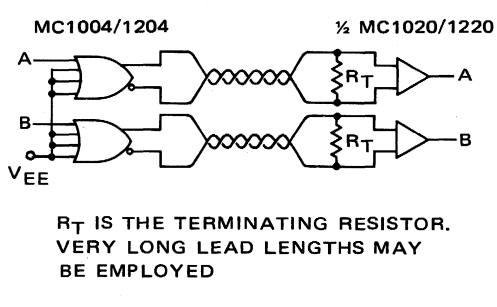
APPLICATIONS INFORMATION

The MC1004-1006/MC1204-1206 dual 4-input OR/NOR gates are very useful in generating system logic due to their flexibility. By employing negative logic on the inputs (low level of – 1.6 V is considered true), the AND/NAND logic function is obtained from the basic gate. Since complementary inputs are available in MECL system, OR/NOR-AND/NAND logic may be employed, reducing the package count in the system. An 8-input OR or AND gate is obtained by tying the OR outputs together and using positive or negative logic. The dual 4-input gate is also useful for driving two twisted pair lines where the lines must carry independent information. For a further discussion of twisted pair driving and receiving, refer to MC1020/MC1220 Line Receiver.

8-INPUT "OR" GATE (positive logic) or 8-INPUT "AND" GATE (negative logic)



DUAL 4-INPUT GATE USED TO DRIVE TWO BALANCED TWISTED PAIR LINES

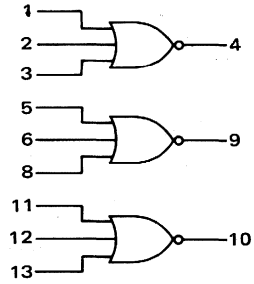


MC1007 thru MC1009
MC1207 thru MC1209

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

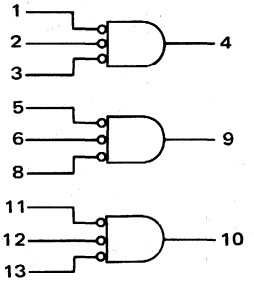
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$4 = \overline{1 + 2 + 3}$

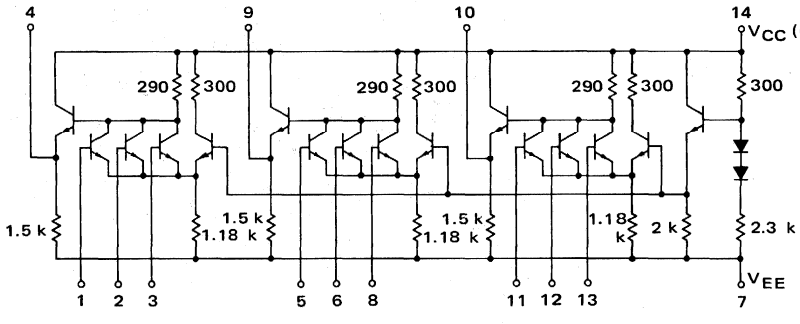
NEGATIVE LOGIC



$4 = \overline{1 \cdot 2 \cdot 3}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = MC1007/MC1207 — 110 mW typical
MC1008/MC1208 — 75 mW typical
MC1009/MC1209 — 60 mW typical

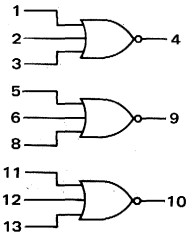
MC1007/MC1207 CIRCUIT SCHEMATIC



MC1008/MC1208
Omit output pulldown resistors to pins 9 and 10.

MC1009/MC1209
Omit all output pulldown resistors.

Resistor values are nominal.



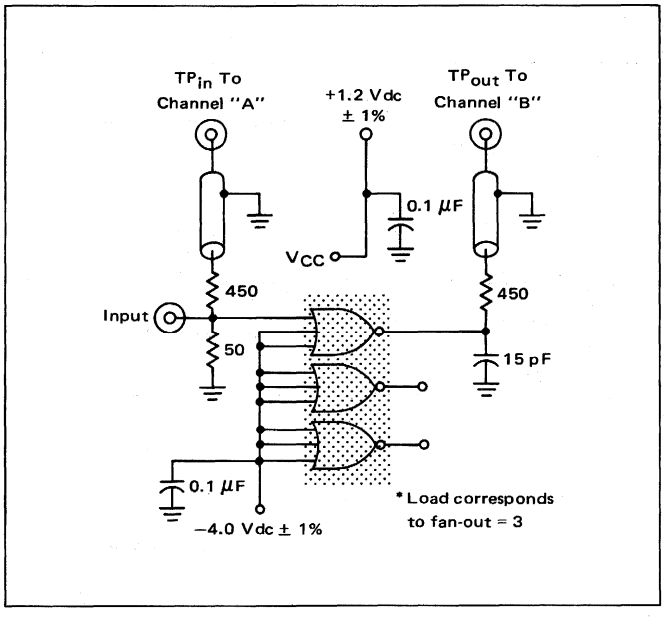
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 k ohm resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1207-1209 Test Limits							MC1007-1009 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7														
MC1207/MC1007			-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
MC1208/MC1008			-	-	-	20	-	-		-	-	-	20	-	-	
MC1209/MC1009			-	-	-	16	-	-		-	-	-	16	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-		-	-		-	-	-		-	-	
		3	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	4	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	4	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay																
(Fan-Out = 3)	t_{1+4-}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.5	ns
	t_{1-4+}		4.0	7.0	4.0	7.0	6.0	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{1+4-}		18	-	18	-	22	-		18	-	18	-	20	-	
	t_{1-4+}		5.0	-	5.0	-	9.0	-		5.0	-	5.0	-	7.0	-	
Rise Time (Fan-Out = 3)	t_{4+}		5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.5	8.0	
Fall Time (Fan-Out = 3)	t_{4-}		6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.0	9.0	

*Individually test each input using the pin connections shown.
‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

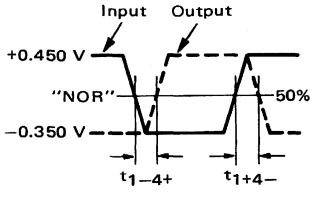
SWITCHING TIME TEST CIRCUIT @ 25°C



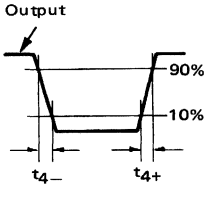
	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1207-1209	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1007-1009	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1207/MC1007			-	-	-	1, 2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
MC1208/MC1008			-	-	-	↓	-	↓
MC1209/MC1009		↓	-	-	-		-	
Input Current	I_{in}	1	-	-	1	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
		2	-	-	2	1, 3, 5, 6, 7, 8, 11, 12, 13	-	↓
		3	-	-	3	1, 2, 5, 6, 7, 8, 11, 12, 13	-	
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	4	1	-	-	2, 3, 5, 6, 7, 8, 11, 12, 13	4	14
		↓	2	-	-	1, 3, 5, 6, 7, 8, 11, 12, 13	↓	↓
			3	-	-	1, 2, 5, 6, 7, 8, 11, 12, 13		
"NOR" Logical "0" Output Voltage	V_{OL}	4	-	1	-	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
		↓	-	2	-	1, 3, 5, 6, 7, 8, 11, 12, 13	-	↓
			-	3	-	1, 2, 5, 6, 7, 8, 11, 12, 13	-	
Switching Times Propagation Delay			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
(Fan-Out = 3)	t_{1+4-}	4	1	4	-	2, 3, 5, 6, 7, 8, 11, 12, 13	-	14
	t_{1-4+}				-		-	
(Fan-Out = 15)	t_{1+4-}				-		-	
	t_{1-4+}				-		-	
Rise Time (Fan-Out = 3)	t_{4+}				-		-	
Fall Time (Fan-Out = 3)	t_{4-}	↓	↓	↓	-	↓	-	↓

PROPAGATION DELAY



RISE AND FALL TIMES



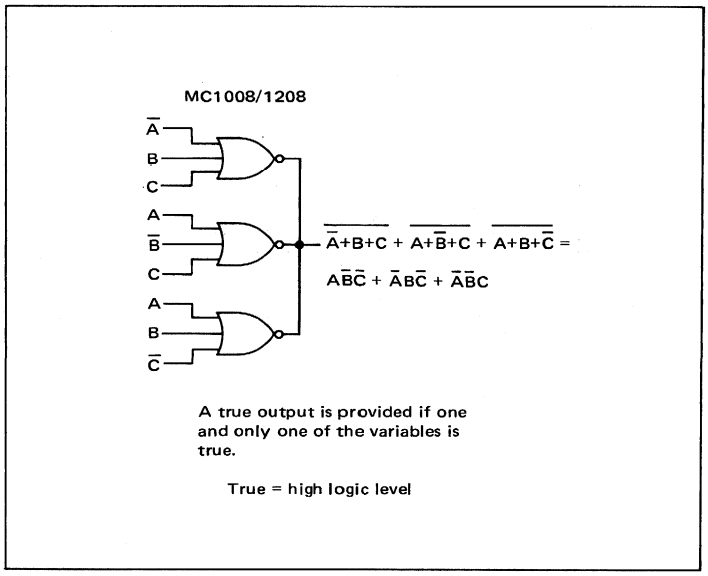
SWITCHING TIME WAVEFORMS

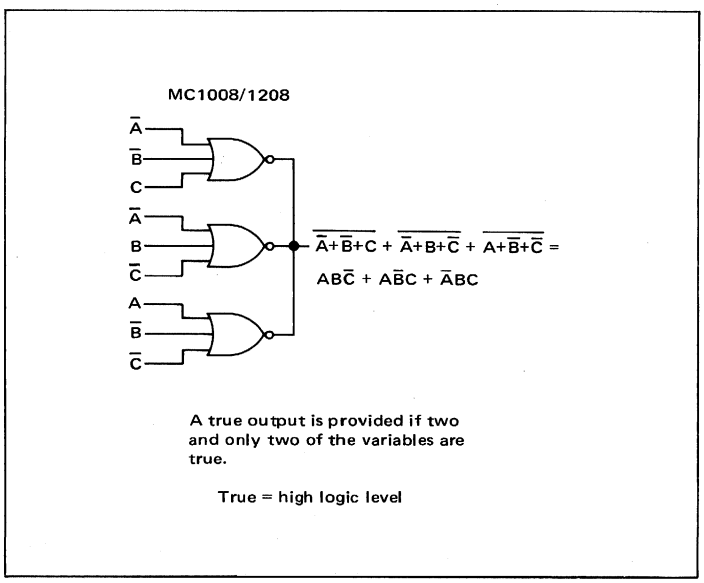
Switching waveforms shown for pulse in on pin 1 and pulse out on pin 4, however all other input-output combinations will meet the limits specified.

Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

APPLICATIONS INFORMATION

The MC1007-1009/MC1207-1209 triple 3-input gates provide NOR outputs only, due to the pin limitation of the 14-lead package. The three options on the emitter follower pull-down resistors, as on all of the basic gates, provide a significant power savings when the wired-OR feature is utilized. The power dissipation of additional emitter-follower resistors and additional gates to perform the OR function is eliminated. By making liberal use of the wired-OR feature, power dissipation in a logic system may be reduced by one-half. If fast propagation delay time through a logic chain is required, an additional gate propagation delay of 4.0 to 5.0 ns is saved each time the wired-OR option is employed. Shown below are two examples of an MC1008/MC1208 with the outputs wired together.



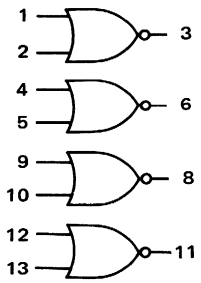


MC1010 thru MC1012
MC1210 thru MC1212

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

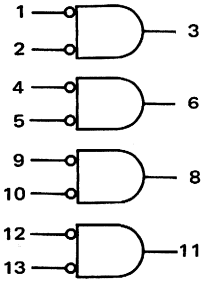
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$3 = \overline{1 + 2}$

NEGATIVE LOGIC

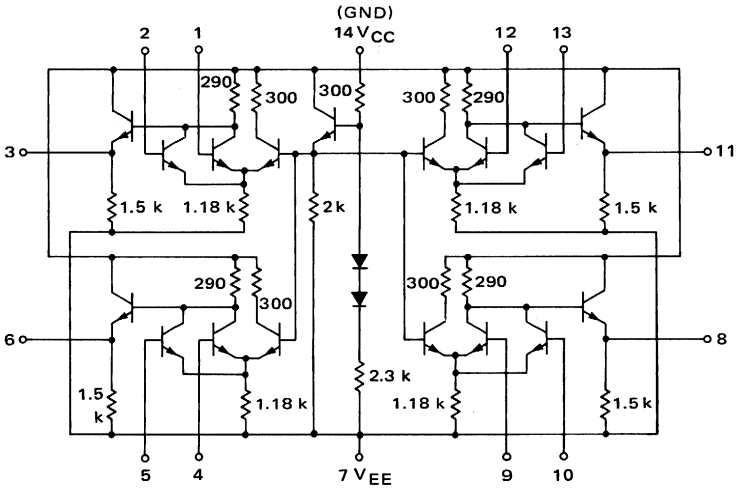


$3 = \overline{1 \cdot 2}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25

Power Dissipation: MC1010/MC1210 – 115 mW typical
MC1011/MC1211 – 95 mW typical
MC1012/MC1212 – 65 mW typical

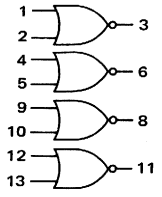
MC1010/MC1210 CIRCUIT SCHEMATIC



MC1011/MC1211
Omit pulldown resistors on pins 3 and 6

MC1012/MC1212
Omit all output pulldown resistors

Resistor values are nominal.



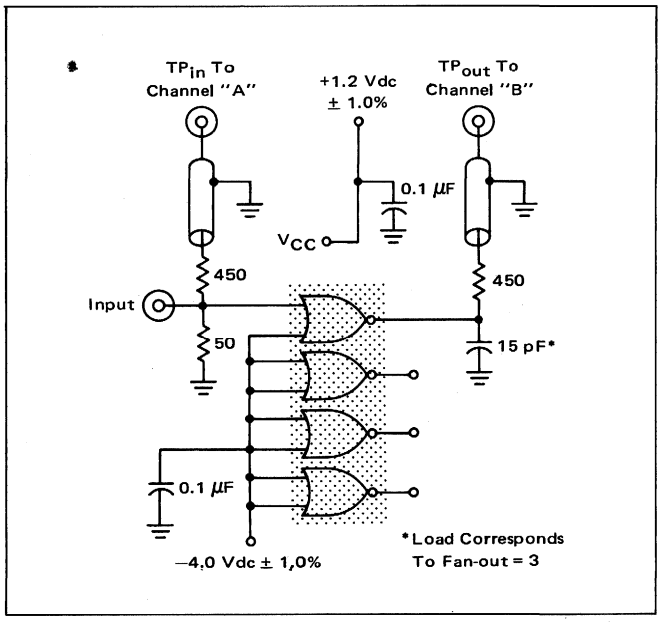
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1210-1212 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1010-1012 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1210/MC1010			-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1211/MC1011			-	-	-	26	-	-		-	-	-	26	-	-	
MC1212/MC1012			-	-	-	18	-	-		-	-	-	18	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times Propagation Delay			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
(Fan-Out = 3)	t_{1+3-}	3	4.0	7.5	4.5	7.5	6.0	9.0	ns	4.0	7.5	4.5	7.5	5.5	8.5	ns
	t_{1-3+}		5.0	7.0	5.0	7.0	6.0	9.0		5.0	7.0	5.0	7.0	5.5	8.0	
(Fan-Out = 15)	t_{1+3-}		18	-	18	-	22	-		18	-	18	-	20	-	
	t_{1-3+}		6.0	-	6.0	-	9.0	-		6.0	-	6.0	-	7.0	-	
Rise Time (Fan-Out = 3)	t_{3+}		4.0	7.5	4.0	7.0	5.0	8.0		4.0	7.0	4.0	7.0	4.5	7.5	
Fall Time (Fan-Out = 3)	t_{3-}		6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	

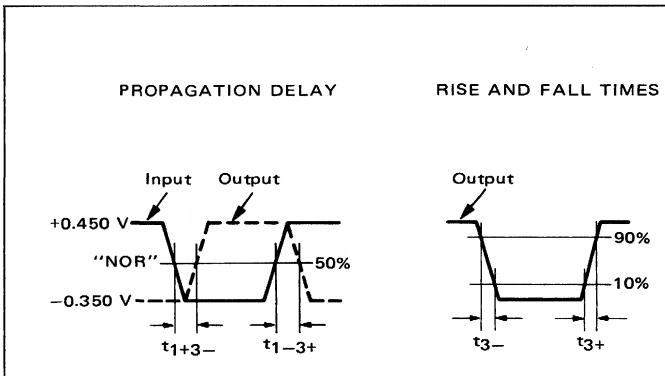
*Individually test each input using the pin connections shown.
‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc	
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	
MC1210-1212	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
MC1010-1012	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1210/MC1010			-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
MC1211/MC1011			-	-	-	↓	-	↓
MC1212/MC1012			-	-	-		-	
Input Current	I_{in}	1	-	-	1	2, 4, 5, 7, 9, 10, 12, 13	-	14
		2	-	-	2	1, 4, 5, 7, 9, 10, 12, 13	-	14
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	1	-	-	2, 4, 5, 7, 9, 10, 12, 13	3	14
		3	2	-	-	1, 4, 5, 7, 9, 10, 12, 13	3	14
"NOR" Logical "0" Output Voltage	V_{OL}	3	-	1	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
		3	-	2	-	1, 4, 5, 7, 9, 10, 12, 13	-	14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Propagation Delay (Fan-Out = 3)	t_{1+3-}	3	1	3	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
	t_{1-3+}		↓	↓	-	↓	-	↓
(Fan-Out = 15)	t_{1+3-}				-		-	
	t_{1-3+}				-		-	
Rise Time (Fan-Out = 3)	t_{3+}				-		-	
Fall Time (Fan-Out = 3)	t_{3-}	↓	↓	↓	-	↓	-	↓



Input Pulse t_r and t_f = 5.0 ± 0.5 ns

Switching waveforms shown for pulse in on pin 1 and pulse out on pin 3, however all other input-output combinations will meet the limits specified.

SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1010-1012/MC1210-1212 quad 2-input NOR gates are very useful in building more complex functions. For example, two R-S flip-flops may be obtained by cross-coupling gates, or a single gated R-S flip-flop may be obtained (see diagram below). Dual clocked R-S flip-flops are available in MECL II (see flip-flop section). The quad 2-input gate may also be used as a dual exclusive OR or NOR by ORing the outputs as shown below.

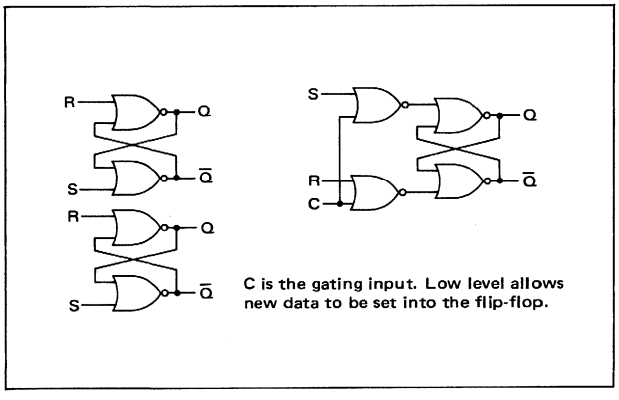
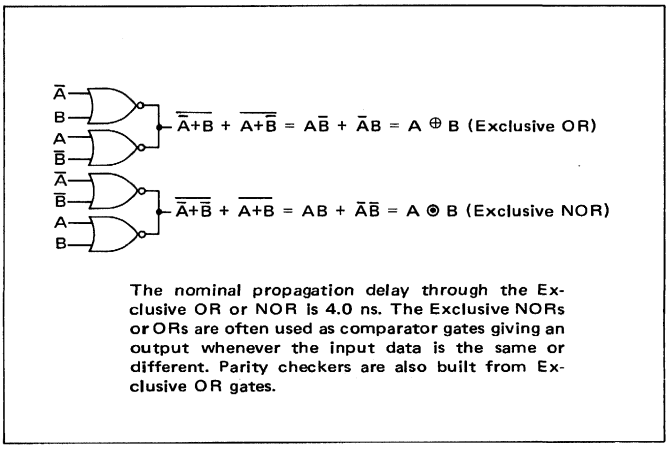


FIGURE 1 - FLIP-FLOPS OBTAINED BY USING MC1010-1012/MC1210-1212 GATES

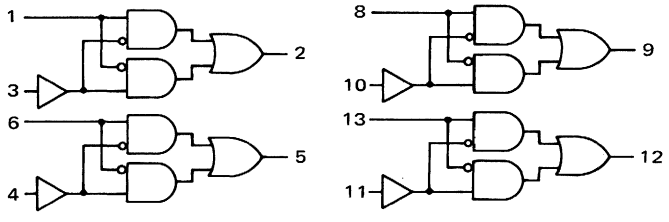
FIGURE 2 - DUAL EXCLUSIVE "OR" or "NOR" GATES



MC1030
MC1230

Four gate arrays designed to provide four Exclusive OR functions. The output is high if and only if one input is high and all other inputs are low.

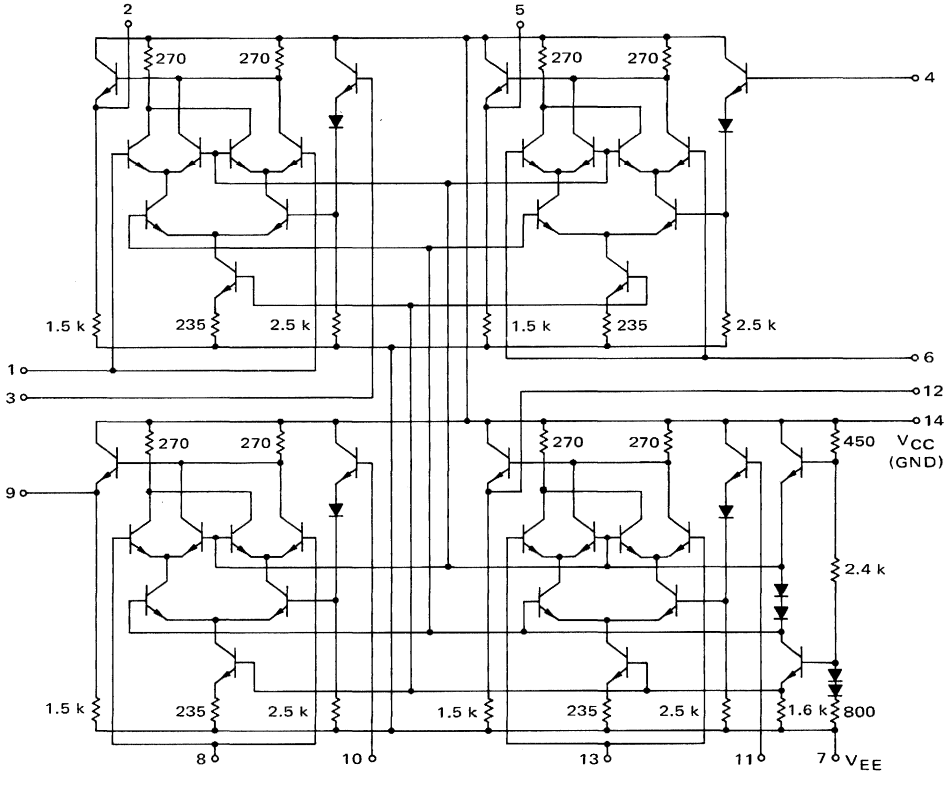
POSITIVE LOGIC



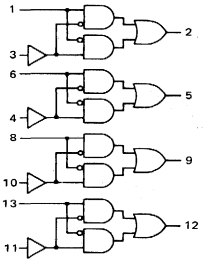
$2 = 1 \cdot \overline{3} + \overline{1} \cdot 3$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal



ELECTRICAL CHARACTERISTICS

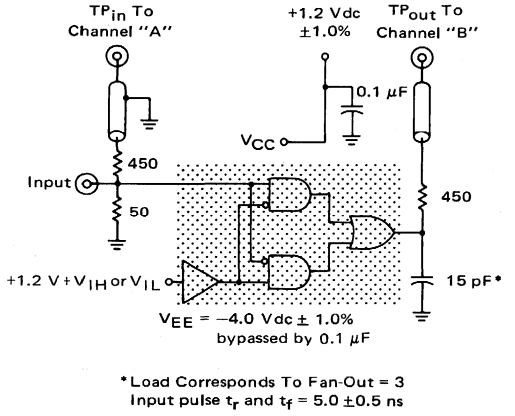
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1230 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1030 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	--	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
		3	-	-	-	100	—	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	1	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
		3	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
Logical "1" Output Voltage	V_{OH} ‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{1+2-}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns
	t_{1-2+}	↓		8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{1+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
	t_{3+2-}		5.0	8.5	5.0	8.5		10		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{3-2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
Rise Time	t_{2+}		5.0	8.5	5.0	8.5		9.5		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
Fall Time	t_{2-}			8.5		8.5		10			8.5		8.5	6.0	9.0	
	t_{2-}	↓	6.0	9.0	6.0	9.0	↓	10	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

*V_{IL} or V_{IH} value as given plus +1.2 V

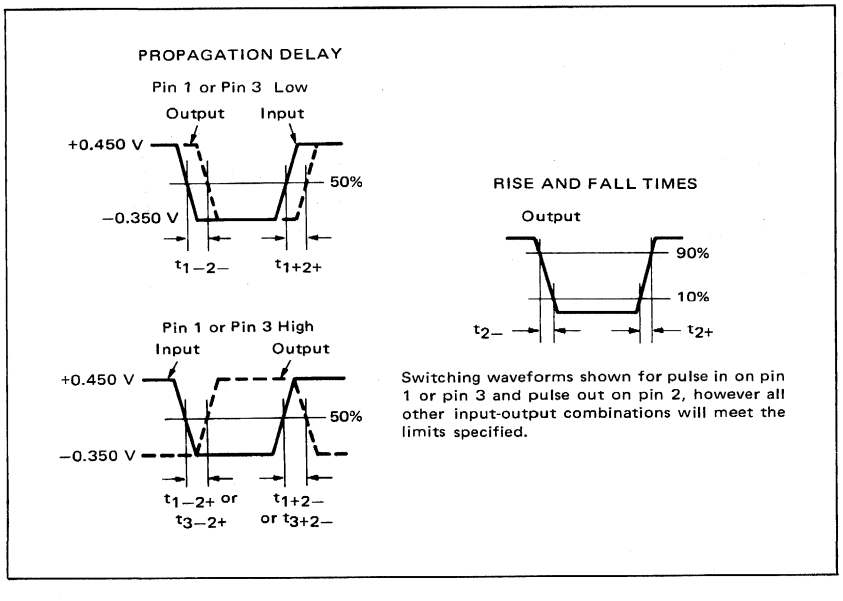
SWITCHING TIME TEST CIRCUIT @ 25°C



*Load Corresponds To Fan-Out = 3
Input pulse t_r and t_f = 5.0 ±0.5 ns

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1230	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1030	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1	-	-	1	3, 7	-	14
		3	-	-	3	1, 7	-	14
Input Leakage Current	I_R	1	-	-	-	1, 3, 7	-	14
		3	-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	V_{OH} ‡	2	1	3	-	7	2	14
		2	3	1	-	7	2	14
Logical "0" Output Voltage	V_{OL}	2	1, 3	-	-	7	-	14
		2	-	1, 3	-	7	-	14
Switching Times (Fan-Out = 3)			V_{IL}*	V_{IH}*	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{1+2-}	2	-	3	1	7	2	14
	t_{1-2+}		-	3				
	t_{1+2+}		3	-				
	t_{1-2-}		3	-				
	t_{3+2-}		-	1	3			
	t_{3-2+}		-	1				
	t_{3+2+}		1	-				
	t_{3-2-}		1	-				
Rise Time	t_{2+}		-	3	1			
	t_{2+}		1	-	3			
Fall Time	t_{2-}		-	3	1			
	t_{2-}		1	-	3			



Switching waveforms shown for pulse in on pin 1 or pin 3 and pulse out on pin 2, however all other input-output combinations will meet the limits specified.

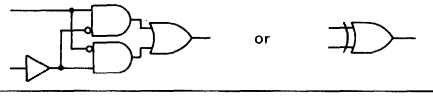
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

SAMPLE TRUTH TABLE

Pin No.	Inputs		Output
	1	3	2
	0	0	0
	0	1	1
	1	0	1
	0	0	0

The Exclusive OR may be symbolized as:



The MC1030/MC1230 quad Exclusive OR gate is a high-speed device employing the series gating technique. The quad Exclusive OR (⊕) is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision circuitry, and code conversion circuitry. The output of each Exclusive OR is high if the two inputs are at different logic levels, while it is low if the inputs are at the same level.

Figure 1 illustrates the comparison of two 8-bit words. The OR output goes high if any Source "A" bit is not the same as the corresponding Source "B" bit. The comparison of two 16-bit words is possible by using two more MC1030/MC1230's, the other half of the MC1004/MC1204, and ORing the two OR outputs together. Note that the MC1030/MC1230 gates are paired together (in Wired-OR configuration) to save extra inputs on the MC1004/MC1204. Typical propagation delay time from inputs to the output of the MC1004/MC1204 is 10 ns.

Figure 2 illustrates checking the bits of a word for odd parity; if the sum of the inputs is odd, the output will be high. (It is also possible to mix MC1030/MC1230 quad Exclusive OR gates and MC1031/MC1231 quad Exclusive NOR gates to obtain the same function.)

FIGURE 1 – DATA COMPARATOR

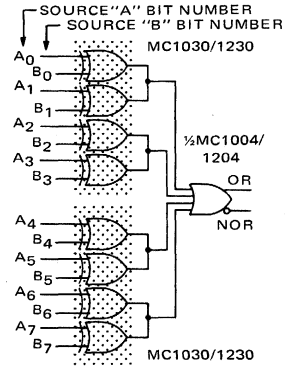
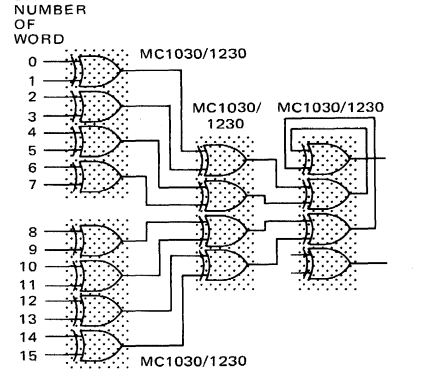


FIGURE 2 – 25 ns 16-BIT PARITY CHECKER (Odd Parity)

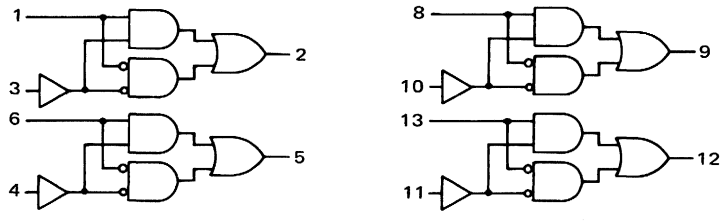


QUAD EXCLUSIVE "NOR" GATES

MC1031
MC1231

Four gate arrays designed to provide four Exclusive NOR functions. The output is high if and only if the two inputs are at the same logic level.

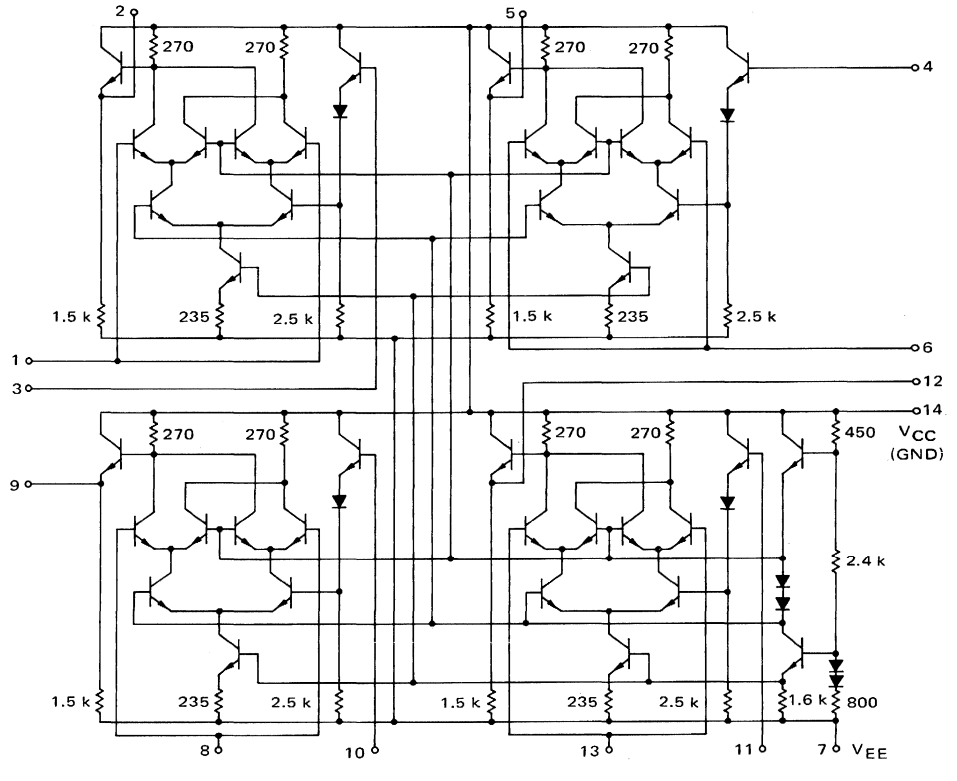
POSITIVE LOGIC



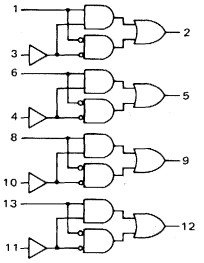
$2 = 1 \cdot 3 + \overline{1} \cdot \overline{3}$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal



ELECTRICAL CHARACTERISTICS

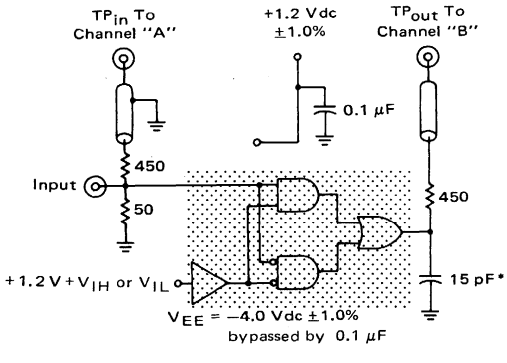
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1231 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1031 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	—	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
		3	-	-	-	100	—	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	1	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
		3	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
Logical "1" Output Voltage	V_{OH} ‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{1+2-}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns
	t_{1-2+}	↓	↓	8.0	↓	8.0	↓	9.0	↓	↓	8.0	↓	8.0	5.0	8.5	↓
	t_{1+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
	t_{3+2-}		5.0	8.5	5.0	8.5		10		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{3-2+}		↓	8.0	↓	8.0		9.0		↓	8.0	↓	8.0	5.0	8.5	
	t_{3+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
Rise Time	t_{2+}		5.0	8.5	5.0	8.5		9.5		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{2+}		↓	8.0	↓	8.0		9.0		↓	8.0	↓	8.0	5.0	8.5	
Fall Time	t_{2-}			8.5		8.5		10			8.5		8.5	6.0	9.0	
	t_{2-}	↓	6.0	9.0	6.0	9.0	↓	10	↓	6.0	9.0	6.0	9.0	6.0	9.5	↓

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

*V_{IL} or V_{IH} value as given plus +1.2 V

SWITCHING TIME TEST CIRCUIT @ 25°C

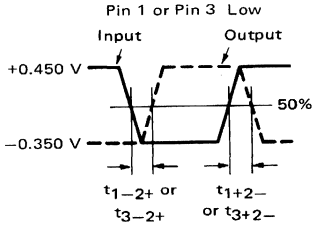


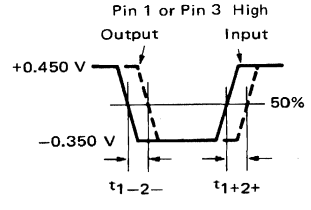
*Load Corresponds To Fan-Out = 3
Input pulse t_r and t_f = 5.0 ±0.5 ns

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1231	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1031	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

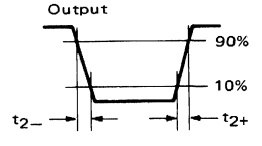
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1	-	-	1	3, 7	-	14
		3	-	-	3	1, 7	-	14
Input Leakage Current	I_R	1	-	-	-	1, 3, 7	-	14
		3	-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	V_{OH} ‡	2	1, 3	-	-	7	2	14
		2	-	1, 3	-	7	2	14
Logical "0" Output Voltage	V_{OL}	2	1	3	-	7	-	14
		2	3	1	-	7	-	14
Switching Times (Fan-Out = 3)			V_{IL}*	V_{IH}*	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{1+2-}	2	3	-	1	7	2	14
	t_{1-2+}		3	-				
	t_{1+2+}		-	3				
	t_{1-2-}		-	3				
	t_{3+2-}		1	-	3			
	t_{3-2+}		1	-				
	t_{3+2+}		-	1				
	t_{3-2-}		-	1				
Rise Time	t_{2+}		3	-	1			
	t_{2+}		-	1	3			
Fall Time	t_{2-}		3	-	1			
	t_{2-}		-	1	3			

PROPAGATION DELAY





RISE AND FALL TIMES



Switching waveforms shown for pulse in on pin 1 or pin 3 and pulse out on pin 2, however all other input-output combinations will meet the limits specified.

SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1031/MC1231 quad Exclusive NOR gate is obtained by changing circuit interconnections of the MC1030/MC1230 through use of a different metal mask. The quad Exclusive NOR ($\odot$) is useful for data comparison, parity generation and checking, decision circuitry, code conversion circuitry, and frequency mixing. The output of each Exclusive NOR is high if the two inputs are at the same logic levels. The Exclusive NOR is the logical complement or inversion of the Exclusive OR.

Figure 1 illustrates a controlled data inverter in which parallel data can be either inverted or not inverted with a single control level. For example, the input information is passed directly to the output if C is at a high level. Exclusive OR gates may also be used to perform this function. The C input would be inverted for the same logic function.

Figure 2 illustrates checking the bits of a word for even parity; if the sum of the inputs is even, the output will be high. (It is also possible to mix MC1031/MC1231 quad Exclusive NOR gates and MC1030/MC1230 quad Exclusive OR gates to obtain the same function.)

SAMPLE TRUTH TABLE

Pin No.	Inputs		Output
	1	3	2
	0	0	1
	0	1	0
	1	0	0
	1	1	1

The Exclusive NOR may be symbolized as:

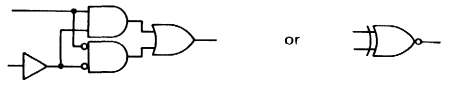


FIGURE 1 – CONTROLLED DATA INVERTER

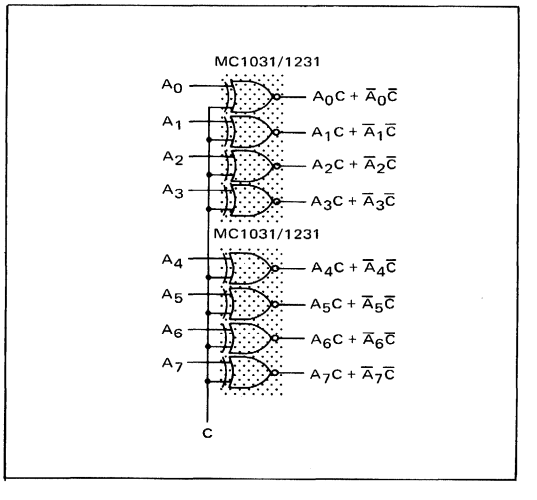
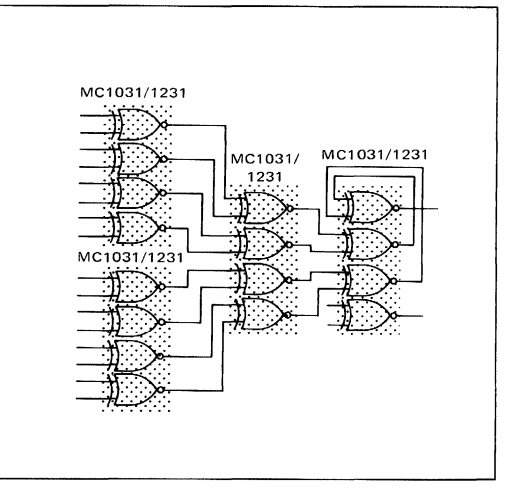


FIGURE 2 – 25 ns 16-BIT PARITY CHECKER (Even Parity)

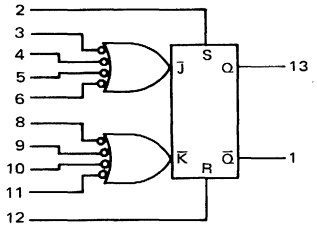


85-MHz AC-COUPLED
J-K FLIP-FLOPS

MC1013
MC1213

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\overline{J}$ and $\overline{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ Inputs Are Static

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

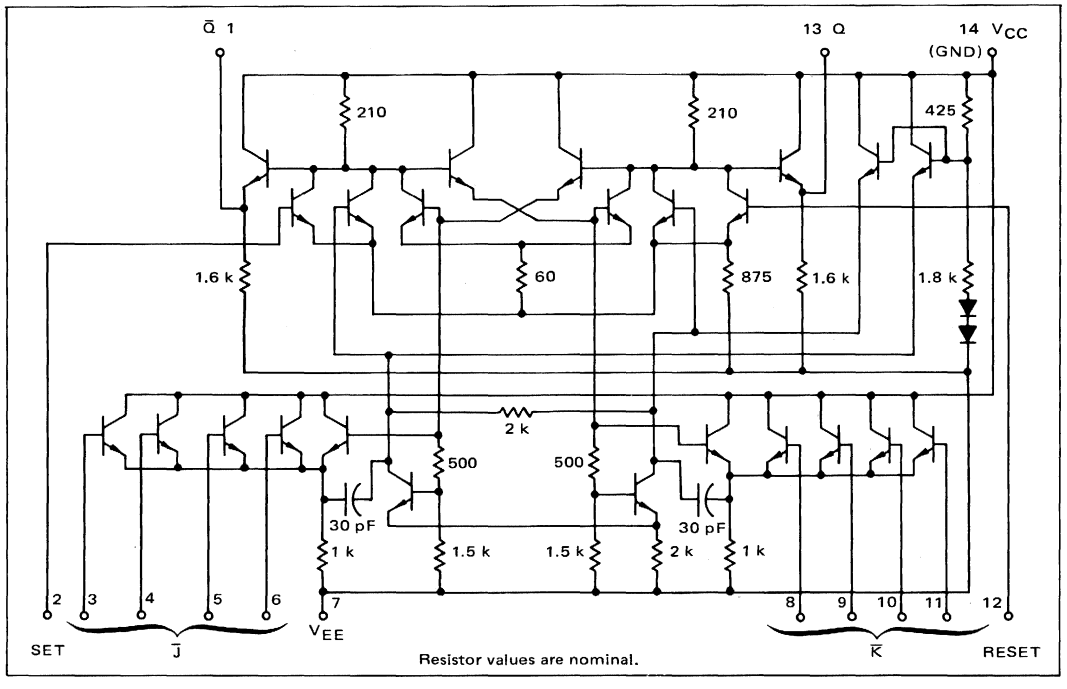
Pin No.	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

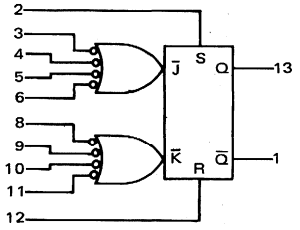
*Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
**$\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1213 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1013 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	29	-	-	mAdc	-	-	-	29	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		3	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		4	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		5	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		6	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		8	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		9	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		10	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		11	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		12	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc
		12	-1.16	-1.34	-1.09	-1.21	-0.93	-1.07	Vdc	-1.11	-1.25	-1.09	-1.21	-1.02	-1.14	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	70	-	-	-	MHz	-	-	70	-	-	-	MHz
Sensitivity (No Toggle)	-	1	←		See Figure 1			→		←		See Figure 1			→	
		13	←		See Figure 1			→		←		See Figure 1			→	
Sensitivity (Toggle)	-	1, 13	←		See Figure 2			→		←		See Figure 2			→	
Switching Times ④			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	6.5	9.0	ns
	t_{6+1-}	1	↓	↓	↓	↓	7.5	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{8+13+}	13	↓	↓	↓	↓	8.0	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{8+13-}	13	↓	↓	↓	↓	7.5	↓	↓	↓	↓	↓	↓	↓	↓	↓
Rise Time	t_{1+}	1	4.0	7.5	4.0	7.5	5.5	9.5	↓	4.0	7.5	4.0	7.5	5.0	8.0	↓
	t_{13+}	13	4.0	↓	4.0	↓	5.5	9.5	↓	4.0	↓	4.0	↓	↓	8.0	↓
Fall Time	t_{1-}	1	5.0	↓	5.0	↓	7.5	10	↓	5.0	↓	5.0	↓	↓	8.5	↓
	t_{13-}	13	5.0	↓	5.0	↓	7.5	10	↓	5.0	↓	5.0	↓	↓	8.5	↓

* Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

①$V_{in(set)} = V_{OH}$ then $V_{OL(max)}$.

②$V_{in(reset)} = V_{OH}$ then $V_{OL(max)}$.

③Input voltage is adjusted to obtain $dV_{"1"}/dV_{in} = \infty$.

④AC fan-out = 3

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc		
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L		
MC1213	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5		
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5		
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5		
MC1013	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5		
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5		
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5		

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	dV_{in}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	↓
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"$\overline{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"$\overline{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "$\overline{Q}$" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2 ③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12 ③	14
			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc			(+1.2V)
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	6, 8	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
Sensitivity (No Toggle)	-	1	6, 8	1	-	↓	-	-	↓
		13	6, 8	13	-		-	-	
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-		-	-	
Switching Times ④									
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-	↓	-	-	↓
	t_{8+13+}	13	8	13	-		-	-	
	t_{8+13-}	13	8	13	-		-	-	
Rise Time	t_{1+}	1	6	1	-		-	-	
	t_{13+}	13	8	13	-		-	-	
Fall Time	t_{1-}	1	6	1	-		-	-	
	t_{13-}	13	8	13	-	↓	-	-	↓

FIGURE 1 - SENSITIVITY (NO TOGGLE)

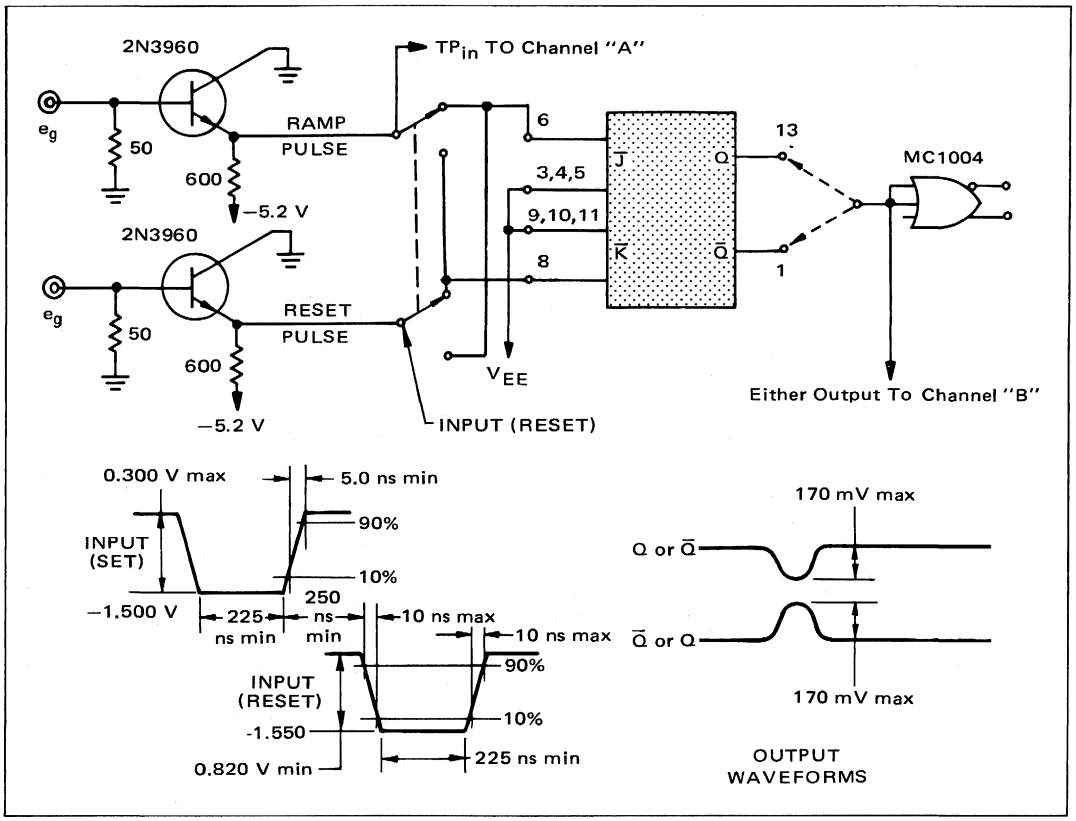
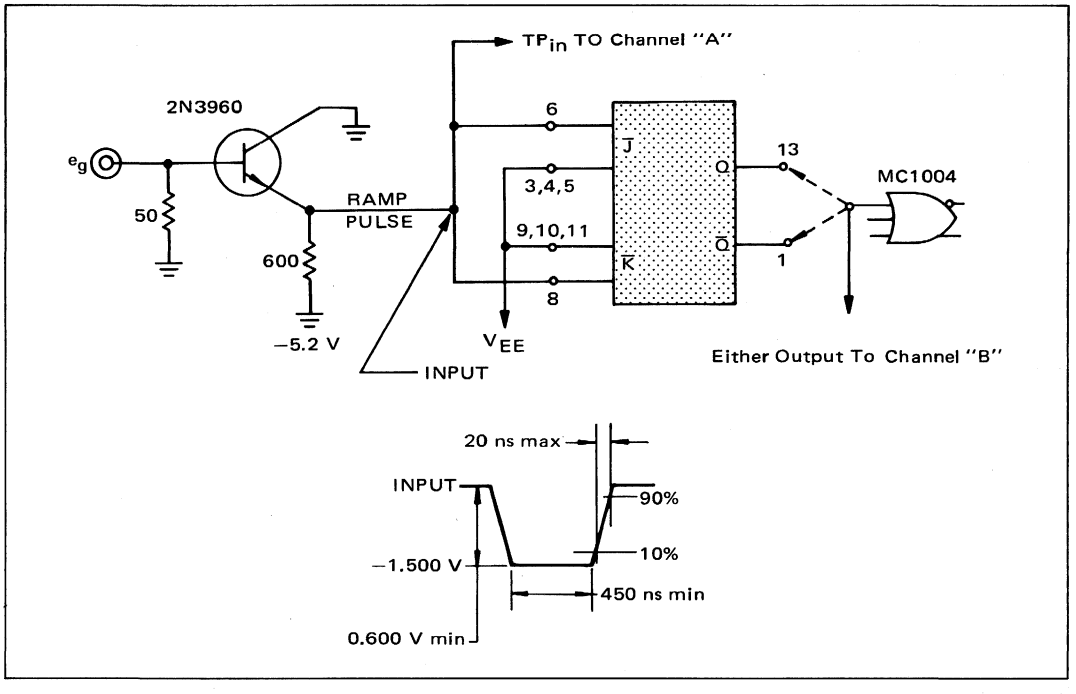


FIGURE 2 - SENSITIVITY (TOGGLE)



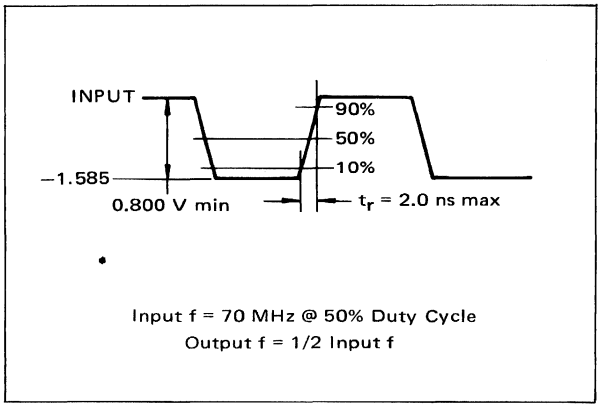
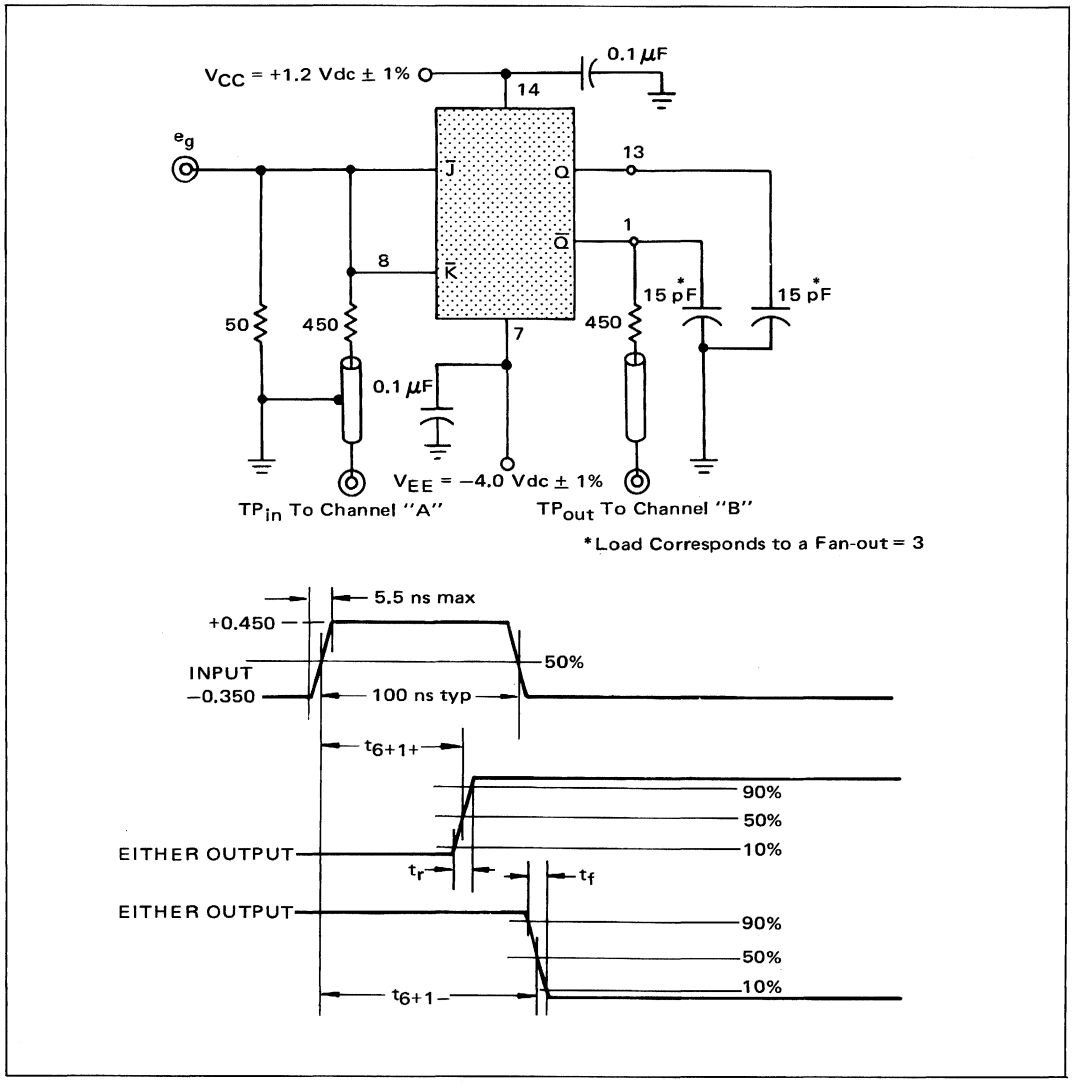


FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATIONS INFORMATION

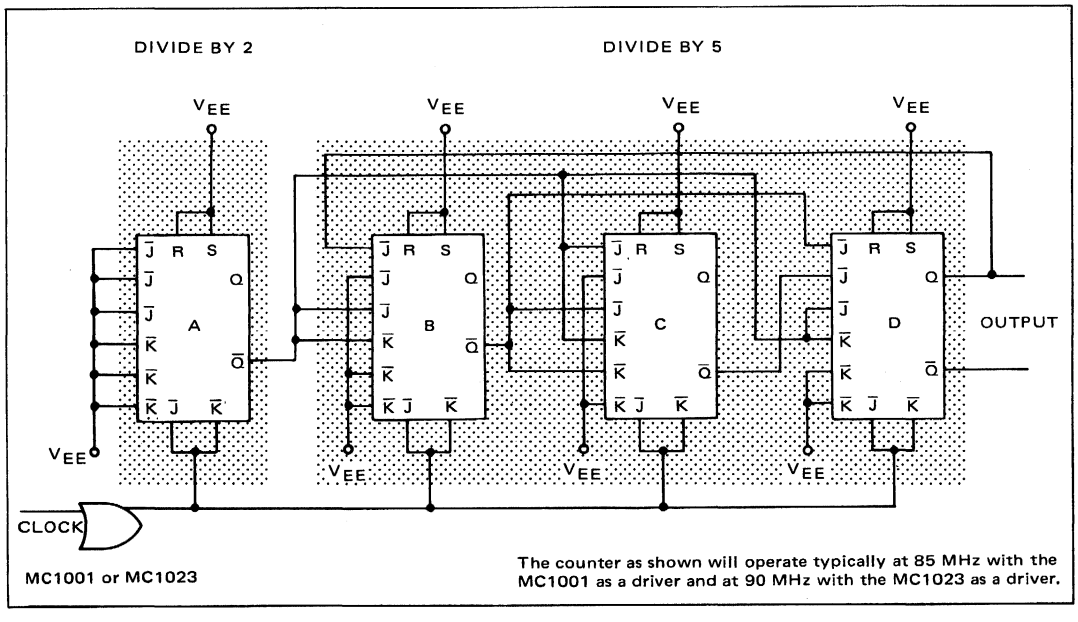
The MC1013/MC1213 J-K flip-flop is used in both counter and shift register applications. Typically the flip-flop will shift and toggle at 85 MHz. Flip-flop operation is illustrated by the curves shown on page 2-125. For a complete characterization of the device, refer to Application Note AN-280. Circuit operation is essentially the same as the MC314/MC364 flip-flop which is explained in Application Note AN-244. Due to the four $\overline{J}$ and four $\overline{K}$ inputs, many clocked and ripple through counters may be built without additional logic. Figure 5 is a table illustrating the $\overline{J}$ and $\overline{K}$ input equations for clocked counters, divide by 3 through 10. Figure 6 is a clocked BCD counter utilizing the logic equations shown in the table.

FIGURE 5 - INPUT EQUATIONS FOR CLOCKED COUNTERS

Divide By:	$\overline{J}_A$	$\overline{K}_A$	$\overline{J}_B$	$\overline{K}_B$	$\overline{J}_C$	$\overline{K}_C$	$\overline{J}_D$	$\overline{K}_D$
3	B	0	$\overline{A}$	0	--	--	--	--
4	0	0	$\overline{A}$	$\overline{A}$	--	--	--	--
5	C	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	0	--	--
6	0	0	$\overline{A}+C$	$\overline{A}$	$\overline{A+B}$	$\overline{A}$	--	--
7	BC	0	$\overline{A}$	$\overline{A+C}$	$\overline{A+B}$	$\overline{B}$	--	--
8	0	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	--	--
9	D	0	$\overline{A}$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	$\overline{A+B+C}$	0
10	0	0	$\overline{A}+D$	$\overline{A}$	$\overline{A+B}$	$\overline{A+B}$	$\overline{A+B+C}$	$\overline{A}$

0 (logic zero) $\leqslant -1.6$ V (pin usually tied to V_{EE}).
All but $\div 7$ may be obtained without additional gating.
All $\overline{J}$ inputs and all $\overline{K}$ inputs are ORed together.

FIGURE 6 - CLOCKED BCD COUNTER USING MECL $\overline{J}$-$\overline{K}$ FLIP-FLOPS



The counter as shown will operate typically at 85 MHz with the MC1001 as a driver and at 90 MHz with the MC1023 as a driver.

FIGURE 7 - TYPICAL TOGGLE FREQUENCY versus V_{EE}

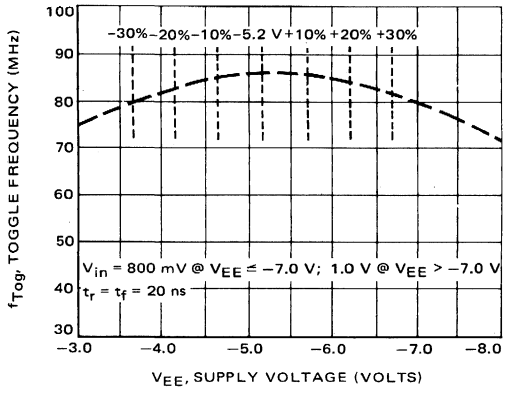


FIGURE 8 - TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

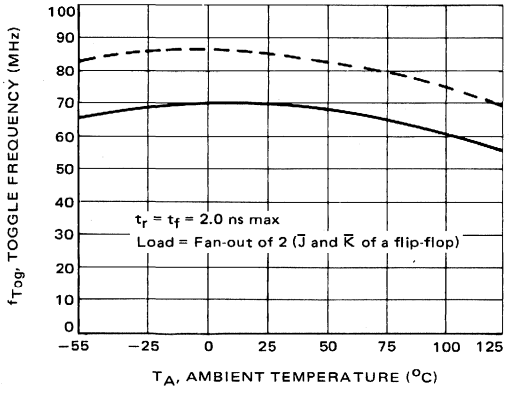
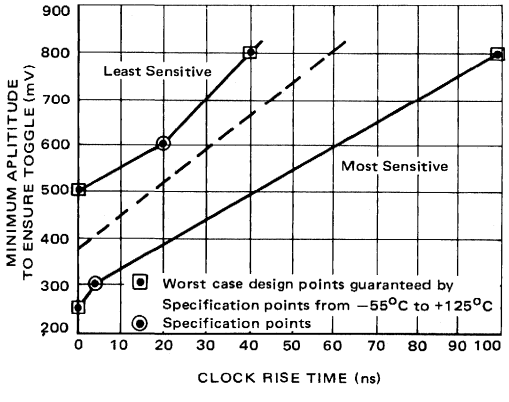


FIGURE 9 - AMPLITUDE versus RISE TIME TO INSURE TOGGLE



ALL UNUSED INPUTS RETURNED TO V_{EE}.
V_{EE} = −5.2 V, V_{in} = 800 mV, T_A = 25°C unless otherwise noted.
——— WORST CASE – – – – TYPICAL

FIGURE 10 - TIME TO DOMINATE

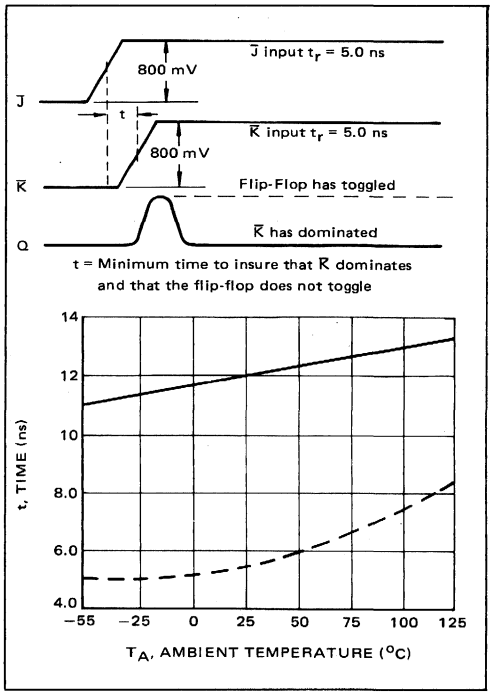
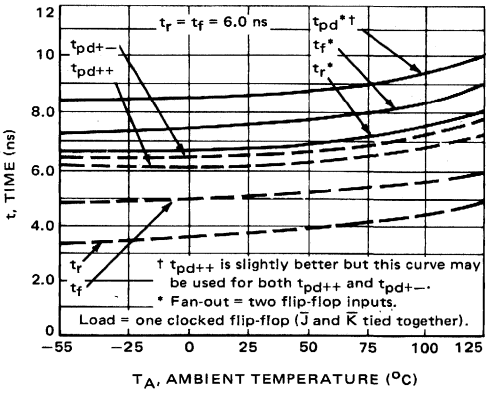


FIGURE 11 - PROPAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE

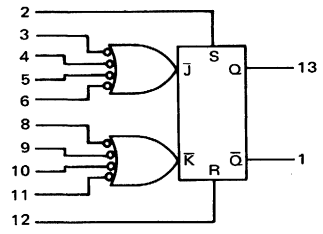


120-MHz AC-COUPLED
J-K FLIP FLOPS

MC1027

Designed for use at clock frequencies to 100 MHz minimum (120 MHz typical). Logic performing inputs ($\overline{J}$ and $\overline{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 2
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ Inputs Are Static

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

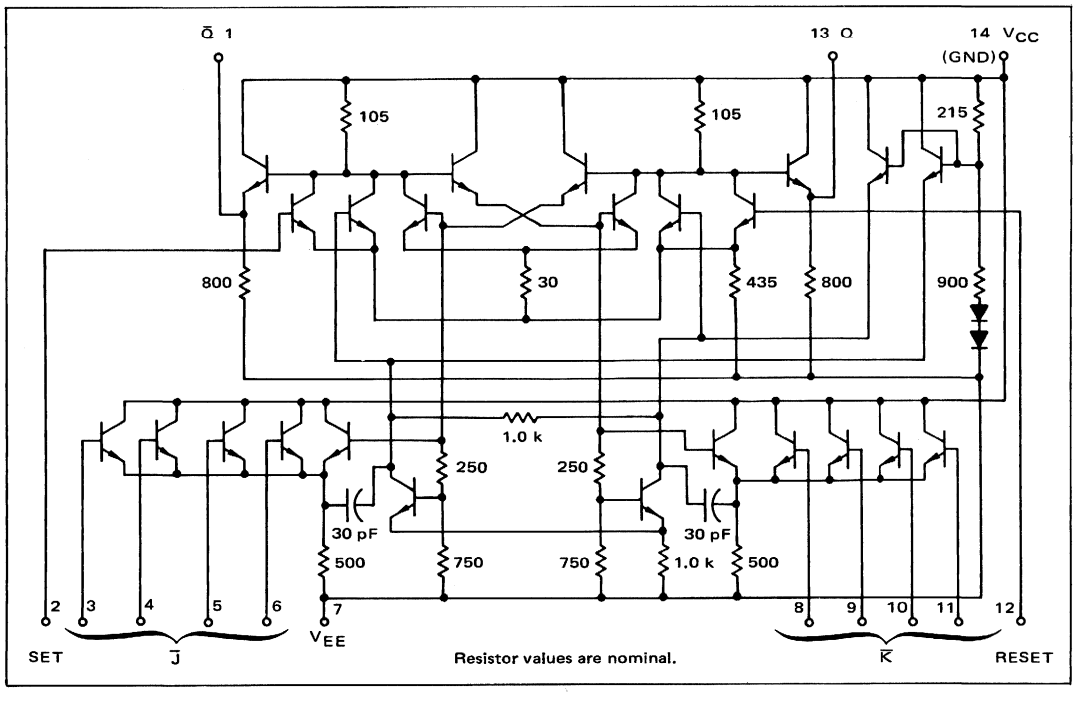
Pin No.	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

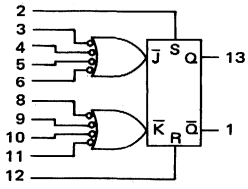
All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

*Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
**$\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

CIRCUIT SCHEMATIC





ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1027 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	58	-	-	mAdc
Input Current	I_{in}	2	-	-	-	200	-	-	μAdc
		3	-	-	-		-	-	
		4	-	-	-		-	-	
		5	-	-	-		-	-	
		6	-	-	-		-	-	
		8	-	-	-		-	-	
		9	-	-	-		-	-	
		10	-	-	-		-	-	
		11	-	-	-		-	-	
		12	-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	1.0	-	5.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	13	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-1.13	-1.31	-1.11	-1.27	-1.04	-1.21	Vdc
		12	-1.13	-1.31	-1.11	-1.27	-1.04	-1.21	Vdc
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	-	-	100	-	-	-	MHz
Sensitivity (No Toggle)	-	1	←		See Figure 1			→	
		13	←		See Figure 1			→	
Sensitivity (Toggle)	-	1, 13	←		See Figure 2			→	
Switching Times ④			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{6+1+}	1	4.0	6.0	4.0	6.0	5.0	8.0	ns
	t_{6+1-}	1							
	t_{8+13+}	13							
	t_{8+13-}	13							
Rise Time	t_{1+}	1							
	t_{13+}	13							
Fall Time	t_{1-}	1							
	t_{13-}	13							

*Individually test each input using the pin connections shown.

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)

① $V_{in(set)} = V_{OH}$ then $V_{OL(max)}$.

② $V_{in(reset)} = V_{OH}$ then $V_{OL(max)}$.

③ Input voltage is adjusted to obtain $dV_{"1"}/dV_{in} = \infty$.

④ AC fan-out = 3

@Test Temperature	$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L
	TEST VOLTAGE/CURRENT VALUES				
	Vdc ±1.0%				mAdc
0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	dV_{in}	V_{CC} (Gnd)
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:						
Power Supply Drain Current	I_E	7	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
Input Current	I_{in}	2	-	-	2	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
		3	-	-	3	2, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	↓
		4	-	-	4	2, 3, 5, 6, 7, 8, 9, 10, 11, 12	-	-	
		5	-	-	5	2, 3, 4, 6, 7, 8, 9, 10, 11, 12	-	-	
		6	-	-	6	2, 3, 4, 5, 7, 8, 9, 10, 11, 12	-	-	
		8	-	-	8	2, 3, 4, 5, 6, 7, 9, 10, 11, 12	-	-	
		9	-	-	9	2, 3, 4, 5, 6, 7, 8, 10, 11, 12	-	-	
		10	-	-	10	2, 3, 4, 5, 6, 7, 8, 9, 11, 12	-	-	
		11	-	-	11	2, 3, 4, 5, 6, 7, 8, 9, 10, 12	-	-	
		12	-	-	12	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	13	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13	-	14
"Q" Logical "0" Output Voltage	V_{OL}	13	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	-	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	-	12 ②	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1	-	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	-	2 ①	3, 4, 5, 6, 7, 8, 9, 10, 11, 12	-	-	14
"Q" or "$\bar{Q}$" Latch Voltage	V_L	2	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	2 ③	14
		12	-	-	-	3, 4, 5, 6, 7, 8, 9, 10, 11	-	12 ③	14
			Pulse In	Pulse Out					
Input Toggle Frequency (See Figures 3 & 4)	f_{Tog}	13	6, 8	13	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
Sensitivity (No Toggle)	-	1	6, 8	1	-	↓	-	-	14
		13	6, 8	13	-		-	-	↓
Sensitivity (Toggle)	-	1, 13	6, 8	1, 13	-		-	-	
Switching Times ④						$V_{EE} = -4.0$ Vdc			+1.2V
Propagation Delay	t_{6+1+}	1	6	1	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	-	14
	t_{6+1-}	1	6	1	-	↓	-	-	↓
	t_{8+13+}	13	8	13	-		-	-	
	t_{8+13-}	13	8	13	-		-	-	
Rise Time	t_{1+}	1	6	1	-		-	-	
	t_{13+}	13	8	13	-		-	-	
Fall Time	t_{1-}	1	6	1	-		-	-	
	t_{13-}	13	8	13	-	↓	-	-	↓

FIGURE 1 - SENSITIVITY (NO TOGGLE)

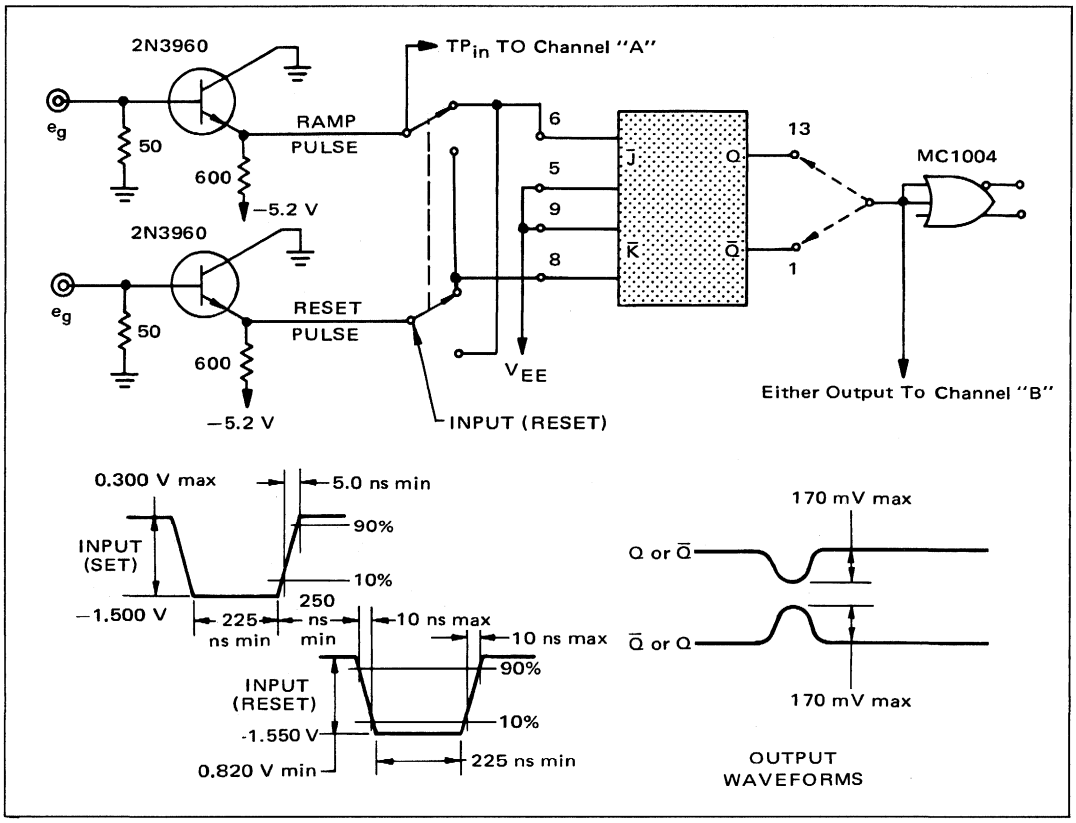
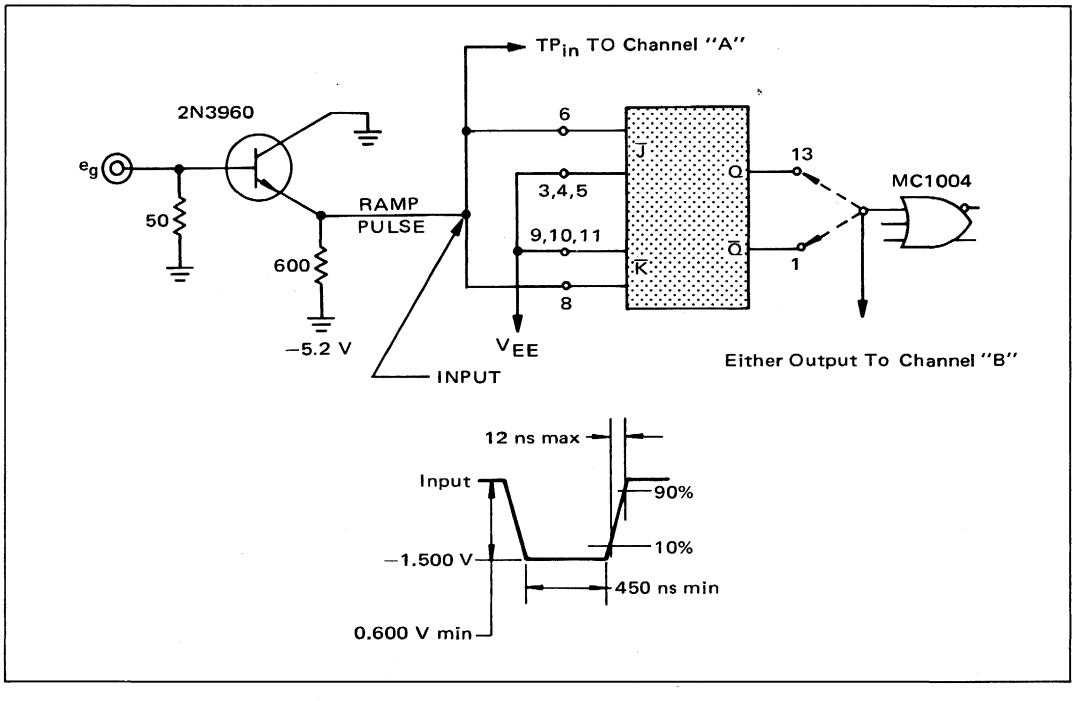


FIGURE 2 - SENSITIVITY (TOGGLE)



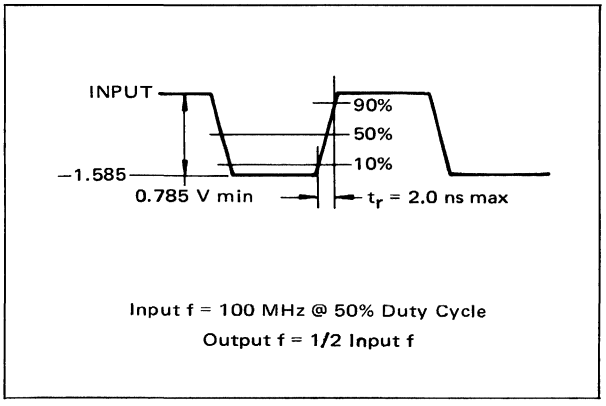
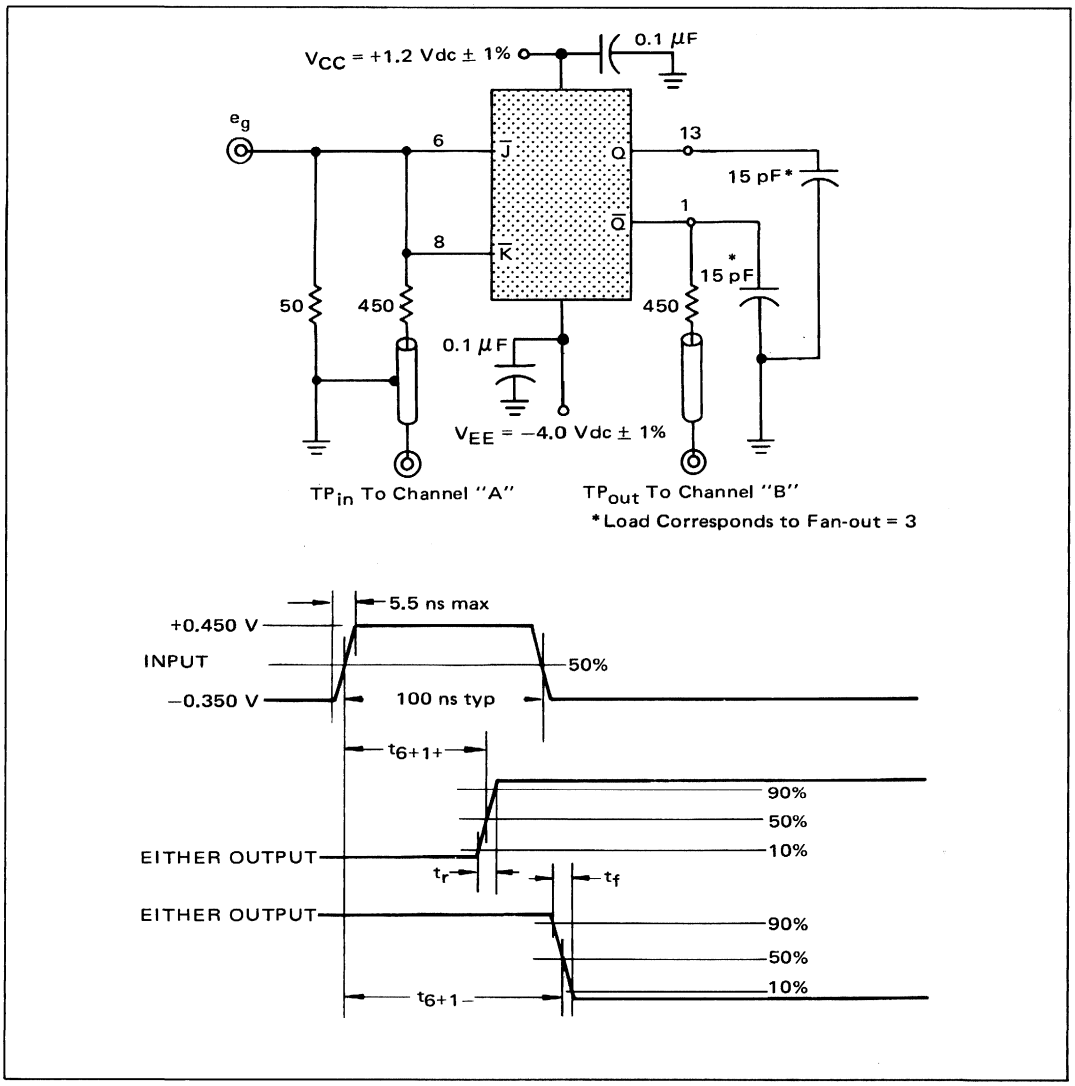


FIGURE 3 - INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

FIGURE 4 - SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



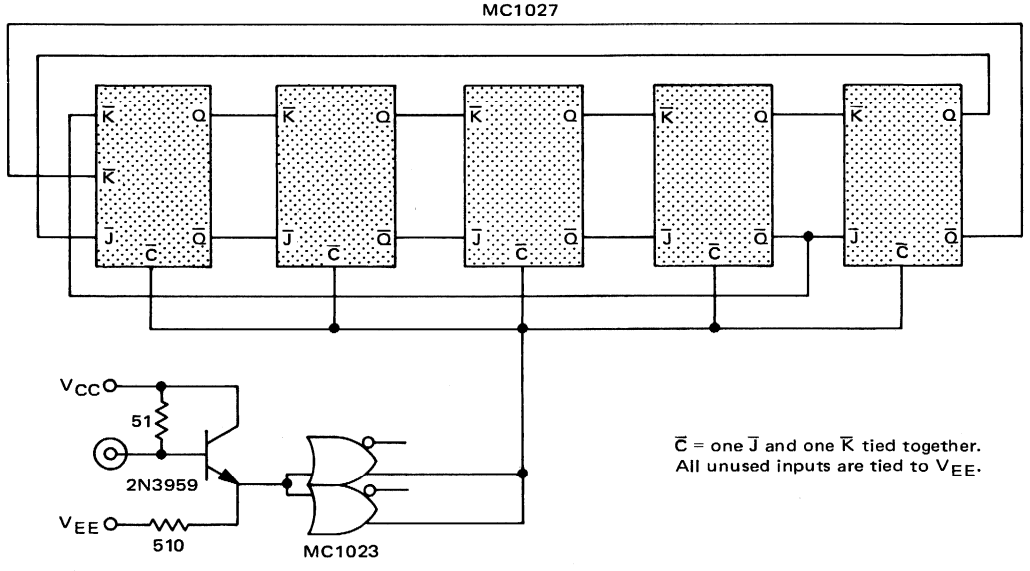
APPLICATIONS INFORMATION

The MC1027 flip-flop is obtained by reducing all resistor values of the MC1013 by a factor of two. The resultant flip-flop is no longer limited by circuit design, but by device speeds. Typically the MC1027 will operate 50% faster than the MC1013. Power dissipation is doubled over that of the MC1013, but circuit operation is the same. The MC1023 clock driver is recommended for driving the MC1027 to its full capability. (The MC1023 high-speed clock driver exhibits propagation delay and rise times of about 2.0 ns when driving five flip-flops.) Maximum operating frequency depends upon layout techniques. Short lead lengths with low impedance lines are recommended. A 100+MHz shift counter is shown in Figure 5.

Operation of the MC1027 is very uniform with negligible variation observed with temperature change from 0°C to +75°C. Propagation delay is nominally 4.5 ns, with rise and fall times varying from 3.5 to 4.0 ns with a load of another flip-flop on the output.

FIGURE 5 - 100 + MHz "SWITCH-TAIL" RING COUNTER

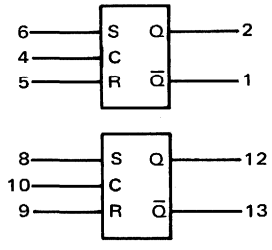
Shift pattern of five "0"s and five "1"s is assured by logic feedback from the fourth to first stage.



MC1014
MC1214

Two dc Set-Reset flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element and may be teamed with the MC1015/MC1215 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



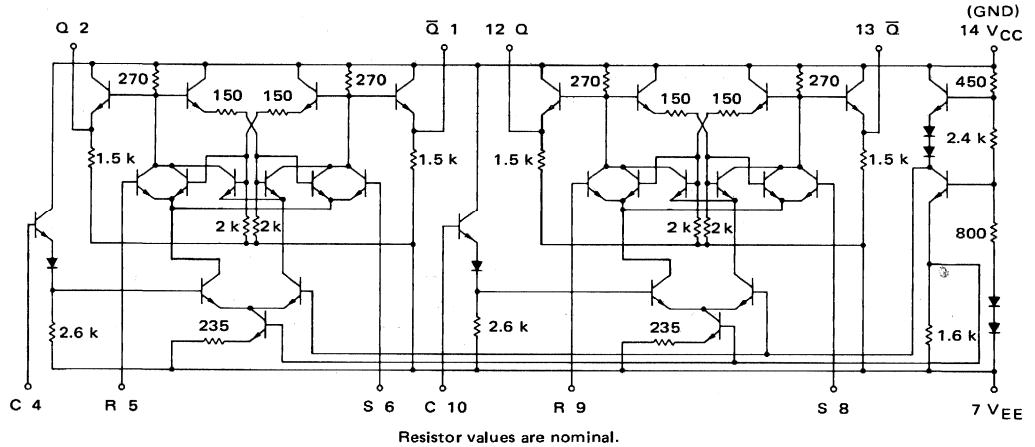
TRUTH TABLE

R	S	C	Q^{n+1}
0	1	1	1
1	0	1	0
0	0	1	Q^n
1	1	1	N.D.
*	*	0	Q^n

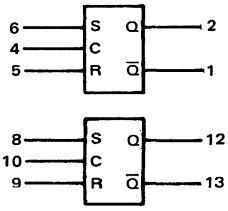
*Either State
N.D. = Not Defined

DC Input Loading Factor: C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop.
The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1214 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1014 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		5	-	-	-	150	-	-	↓	-	-	-	150	-	-	↓
		6	-	-	-	150	-	-		-	-	-	150	-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4+1-}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	ns
	t_{4+1+}	1	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5			
	t_{4+2+}	2	5.0	8.5	5.0	8.5				5.0	8.5	5.0	8.5			
	t_{4+2-}	2	6.0	9.0	6.0	9.0				6.0	9.0	6.0	9.0			
Rise Time	t_{1+}	1						10.0						7.0	10.0	
	t_{2+}	2						10.0								
Fall Time	t_{1-}	1	5.0	8.5			8.0	11.5								
	t_{2-}	2	5.0	8.5			8.0	11.5								
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	5.0	8.0	5.0	8.0	7.0	10.5	ns	5.0	8.0	5.0	8.0	6.0	9.0	ns
	t_{5+1+}	1						10.0							8.5	
	t_{6+2+}	2						10.0							8.5	
	t_{5+2-}	2						10.5							9.0	
Rise Time	t_{1+}	1	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5	
	t_{2+}	2	6.0	9.0	6.0	9.0	8.0	10.0		6.0	9.0	6.0	9.0	7.0	9.5	
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11.5		5.0	8.5	5.0	8.5	6.0	10.0	

*Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1014/MC1214 is a dual R-S flip-flop with a positive clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1015/MC1215 negative-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

@Test Temperature		TEST VOLTAGE/CURRENT VALUES						
		Vdc ±1.0%				V ± 50 mV	mAdc	
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	
MC1214 −55°C		-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5	
MC1214 +25°C		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
MC1214 +125°C		-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5	
MC1014 0°C		-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5	
MC1014 +25°C		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
MC1014 +75°C		-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	-	14
		5	-	-	4, 5	6, 7, 8, 9, 10	-	-	14
		6	-	-	4, 6	5, 7, 8, 9, 10	-	-	14
Input Leakage Current	I_R	Inputs*	-	-	-	4, 5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-	4, 6	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "0" Output Voltage	V_{OL}	2	-	4, 5	-	4, 7, 8, 9, 10	6	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-	4, 5	-	4, 7, 8, 9, 10	6	1	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-	4, 6	-	5, 7, 8, 9, 10	5	-	14
Switching Times (Fan-Out = 3)			Pulse In	$V_{IH\ min}$ +1.2 Vdc	Pulse Out	V_{EE} = −4.0 Vdc			(+1.2V)
Clock Inputs Propagation Delay	t_{4+1-}	1	4	-	1	5, 6, 7, 8, 9, 10	-	-	14
	t_{4+1+}	1	↓	-	1	↓	-	-	↓
	t_{4+2+}	2		-	2		-	-	
	t_{4+2-}	2		-	2		-	-	
Rise Time	t_{1+}	1		-	1		-	-	
	t_{2+}	2		-	2		-	-	
Fall Time	t_{1-}	1		-	1		-	-	
	t_{2-}	2	↓	-	2	↓	-	-	↓
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	6	4	-	7, 8, 9, 10	-	-	14
	t_{5+1+}	1	5	↓	1	↓	-	-	↓
	t_{6+2+}	2	6		2		-	-	
	t_{5+2-}	2	5		2		-	-	
Rise Time	t_{1+}	1	6		1		-	-	
	t_{2+}	2	↓		2		-	-	
Fall Time	t_{1-}	1			1		-	-	
	t_{2-}	2	↓	↓	2	↓	-	-	↓

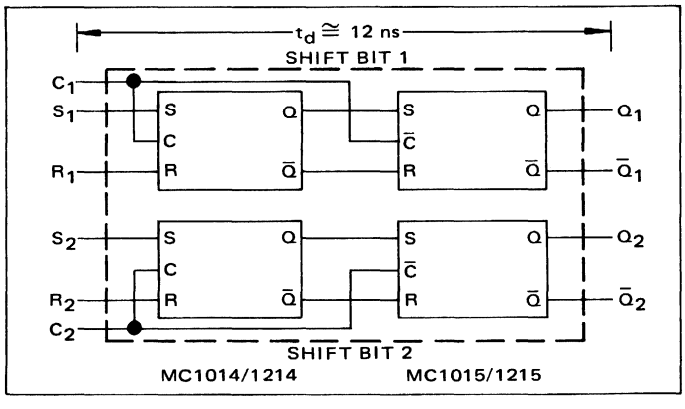
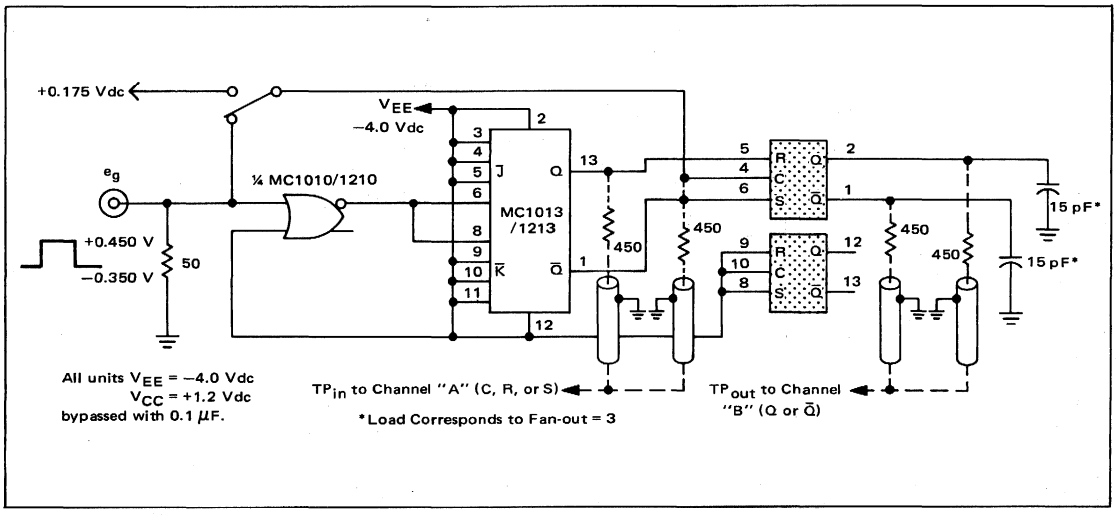
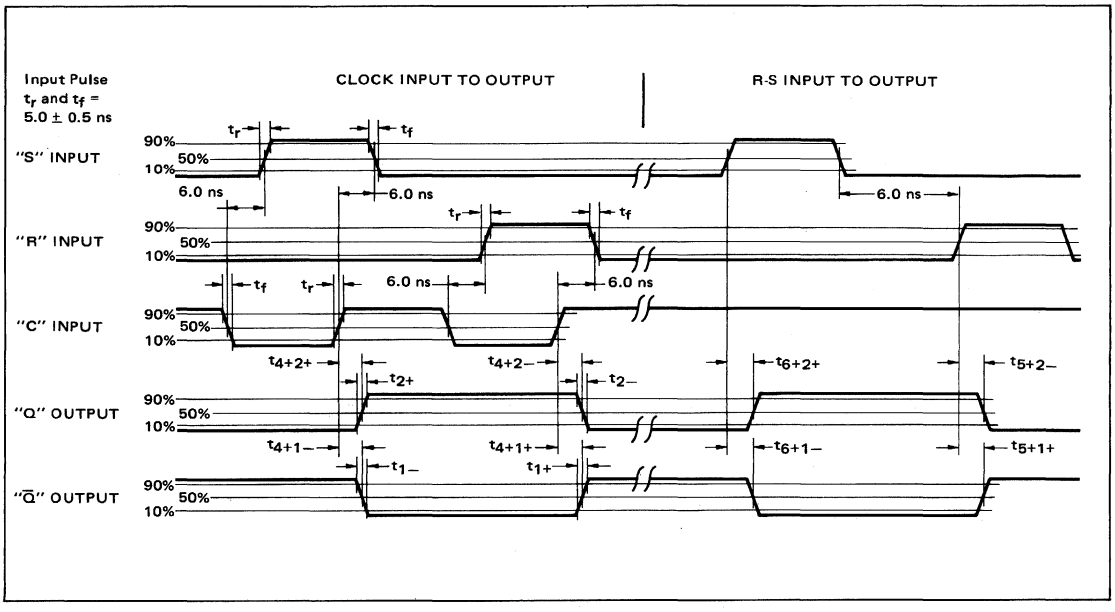


FIGURE 1 - MC1014/MC1214 AND MC1015/MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

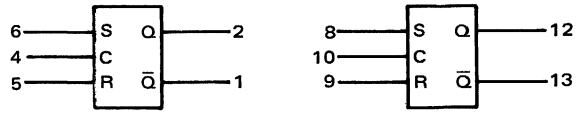


DUAL R-S FLIP-FLOPS
WITH NEGATIVE CLOCK

MC1015
MC1215

Two dc Set-Reset flip-flops with a negative clock input provided for each flip-flop. This unit is useful as a dual storage element and may be teamed with the MC1014/MC1214 for shift register functions with a minimum number of packages.

POSITIVE LOGIC



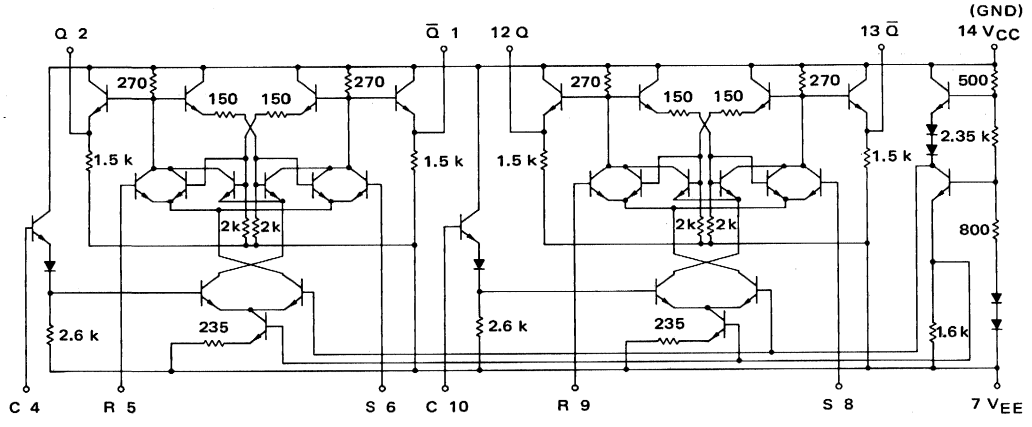
DC Input Loading Factor : C = 1; S, R = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

TRUTH TABLE

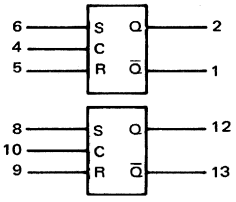
R	S	C	Q^{n+1}
0	1	0	1
1	0	0	0
0	0	0	Q^n
1	1	0	N.D.
*	*	1	Q^n

*Either State
N.D. = Not Defined

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop.
The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1215 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1015 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		5	-	-	-	150	-	-	↓	-	-	-	150	-	-	↓
		6	-	-	-	150	-	-		-	-	-	150	-	-	
Input Leakage Current	Inputs*	4,5,6	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	t_{4-1-}	1	6.0	10.0	6.0	10.0	8.0	12.0	ns	6.0	10.0	6.0	10.0	7.0	11.0	ns
	t_{4-1+}	1	5.0	8.5	5.0	8.5	7.0	10.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{4-2+}	2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{4-2-}	2	6.0	10.0	6.0	10.0	8.0	12.0		6.0	10.0	6.0	10.0	7.0	11.0	
Rise Time	t_{1+}	1	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
	t_{2+}	2														
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11.0		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11.0	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	5.0	8.0	5.0	8.0	7.0	11.0	ns	5.0	8.0	5.0	8.0	6.0	9.0	ns
	t_{5+1+}	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	t_{6+2+}	2														
	t_{5+2-}	2														
Rise Time	t_{1+}	1	6.0	9.0	6.0	9.0				6.0	9.0	6.0	9.0	7.0	10.0	
	t_{2+}	2	6.0	9.0		9.0	↓	↓			9.0		9.0			
Fall Time	t_{1-}	1	5.0	8.0		8.5	8.0	11.5		↓	8.5	↓	8.5	↓	↓	
	t_{2-}	2	5.0	8.0	↓	8.5	8.0	11.5	↓		8.5		8.5			↓

* Individually test each input using the pin connections shown.
‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

APPLICATIONS INFORMATION

The MC1015/MC1215 is a dual R-S flip-flop with a negative clock input for each flip-flop. An extra level of gating is accomplished with only 2.0 ns increase in propagation delay. This device may be used with the MC1014/MC1214 positive-clock R-S flip-flop in a single-phase clocked master-slave type of shift register as shown in Figure 1.

@Test Temperature		TEST VOLTAGE/CURRENT VALUES						
		Vdc ±1.0%				±50 mV	mAdc	
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	
MC1215	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5	
MC1015	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5	

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:						V_{CC} (Gnd)
			$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	V_{BB}	I_L	
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 6, 7, 8, 9	-	-	14
Input Current	I_{in}	4	-	-	4	5, 6, 7, 8, 9, 10	-	-	14
		5	-	-	5	4, 6, 7, 8, 9, 10	-	-	14
		6	-	-	6	4, 5, 7, 8, 9, 10	-	-	14
Input Leakage Current	Inputs*	4, 5, 6	-	-	-	4, 5, 6, 7, 8, 9, 10	-	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	2	4	6	-	5, 7, 8, 9, 10	5	2	14
"Q" Logical "0" Output Voltage	V_{OL}	2	4	5	-	4, 7, 8, 9, 10	6	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	1	4	5	-	4, 7, 8, 9, 10	6	1	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	1	4	6	-	5, 7, 8, 9, 10	5	-	14
Switching Times (Fan-Out = 3)			$V_{IL\ max}$ +1.2 Vdc	Pulse In	Pulse Out	V_{EE} = −4.0 Vdc			+1.2V
Clock Inputs Propagation Delay	t_{4-1-}	1	-	4	1	5, 6, 7, 8, 9, 10	-	-	14
	t_{4-1+}	1	-		1		-	-	
	t_{4-2+}	2	-		2		-	-	
	t_{4-2-}	2	-		2		-	-	
Rise Time	t_{1+}	1	-		1		-	-	
	t_{2+}	2	-		2		-	-	
Fall Time	t_{1-}	1	-		1		-	-	
	t_{2-}	2	-		2		-	-	
Set-Reset Inputs Propagation Delay	t_{6+1-}	1	4	6	1	7, 8, 9, 10	-	-	14
	t_{5+1+}	1		5	1		-	-	
	t_{6+2+}	2		6	2		-	-	
	t_{5+2-}	2		5	2		-	-	
Rise Time	t_{1+}	1		6	1		-	-	
	t_{2+}	2			2		-	-	
Fall Time	t_{1-}	1			1		-	-	
	t_{2-}	2			2		-	-	

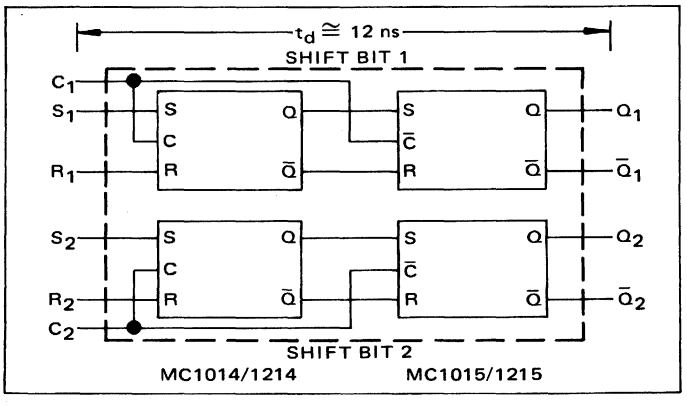
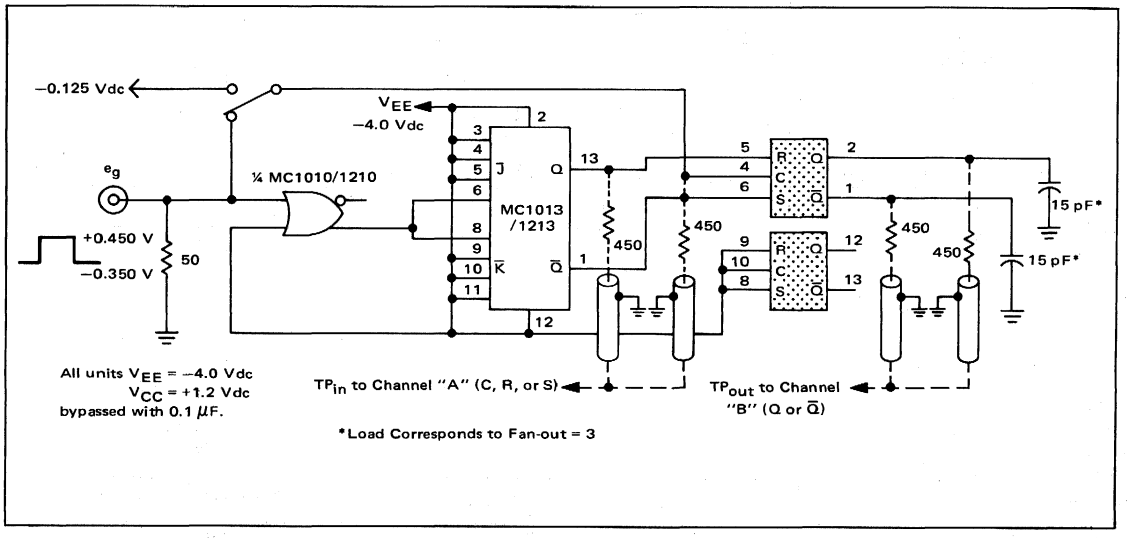
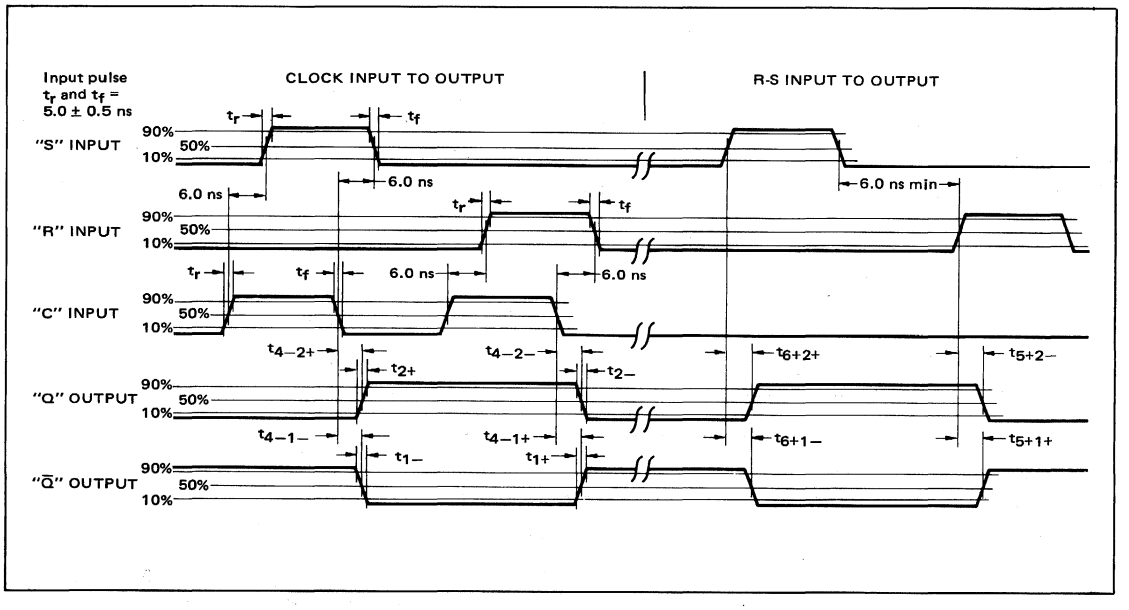


FIGURE 1 - MC1014/MC1214 AND MC1015/ MC1215 CONNECTED TO MAKE TWO MASTER-SLAVE SHIFT REGISTER ELEMENTS

SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

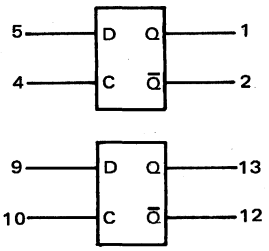


DUAL R-S FLIP-FLOPS
WITH SINGLE RAIL INPUT
AND NEGATIVE CLOCK

MC1016
MC1216

Two dc storage flip-flops with a positive clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state.

POSITIVE LOGIC

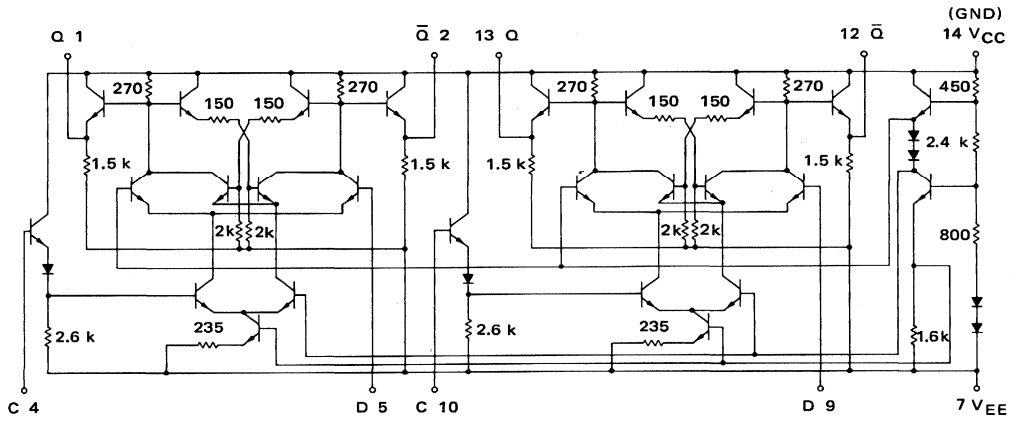


DC Input Loading Factor : C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typical

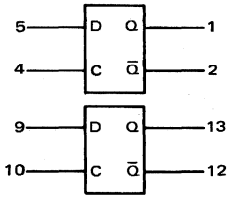
TRUTH TABLE

D	C	Q^{n+1}
0	0	Q^n
1	0	Q^n
0	1	0
1	1	1

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1216 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1016 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		5	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		5	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs																
Propagation Delay	t_{4+1-}	1	6.0	9.0	6.0	9.0	7.0	10.5	ns	6.0	9.0	6.0	9.0	6.0	9.5	ns
	t_{4+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5		5.0	8.0	5.0	8.0	5.0	8.5	
	t_{4+2+}	2	5.0	8.0	5.0	8.0	6.0	9.5		5.0	8.0	5.0	8.0	5.0	8.5	
	t_{4+2-}	2	6.0	9.0	6.0	9.0	7.0	10.5		6.0	9.0	6.0	9.0	6.0	9.5	
Rise Time	t_{1+}	1	5.0	7.5	5.0	7.5	6.0	9.5		5.0	7.5	5.0	7.5	5.0	8.0	
	t_{2+}	2	5.0	7.5	5.0	7.5	6.0	9.5		5.0	7.5	5.0	7.5	5.0	8.0	
Fall Time	t_{1-}	1	6.0	8.5	6.0	8.5	7.0	10.5		6.0	8.5	6.0	8.5	6.0	9.5	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
Set Inputs																
Propagation Delay	t_{5+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
	t_{5-1-}	1					7.0	10.5								
	t_{5+2-}	2					7.0	10.5								
	t_{5-2+}	2					6.0	9.5								
Rise Time	t_{1+}	1		7.5		7.5		9.0			7.5		7.5		8.0	
	t_{2+}	2		7.5		7.5		9.0			7.5		7.5		8.0	
Fall Time	t_{1-}	1		8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	
	t_{2-}	2		8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L	
MC1216	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
MC1016	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

Characteristic	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	-	4, 10	-	5, 7, 9	-	14
Input Current	-	-	4	5, 7, 9, 10	-	14
	-	-	4, 5	7, 9, 10	-	14
Input Leakage Current	-	-	-	4, 5, 7, 9, 10	-	14
	-	-	-	4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage‡	-	4, 5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	5	4	-	7, 9, 10	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	5	4	-	7, 9, 10	2	14
"$\bar{Q}$" Logical "0" Output Voltage	-	4, 5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3)	Pulse In	$V_{IH\ min}$ +1.2 Vdc	Pulse Out	V_{EE} = −4.0 Vdc		(+1.2V)
Clock Inputs Propagation Delay	4	-	1	7, 9, 10	-	14
		-	1		-	
		-	2		-	
		-	2		-	
Rise Time		-	1		-	
		-	2		-	
Fall Time		-	1		-	
		-	2		-	
Set Inputs Propagation Delay	5	4	1	7, 9, 10	-	14
			1		-	
			2		-	
			2		-	
Rise Time			1		-	
			2		-	
Fall Time			1		-	
			2		-	

APPLICATIONS INFORMATION

The MC1016/MC1216 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.

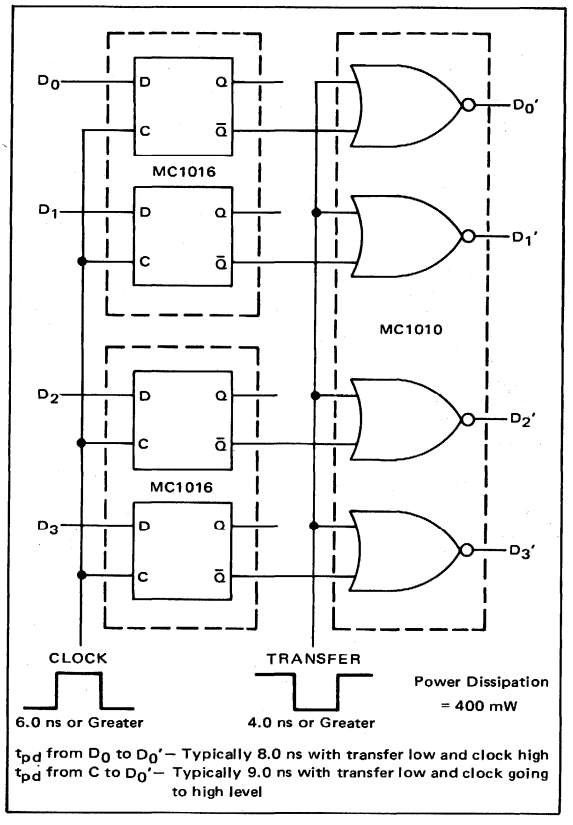


FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

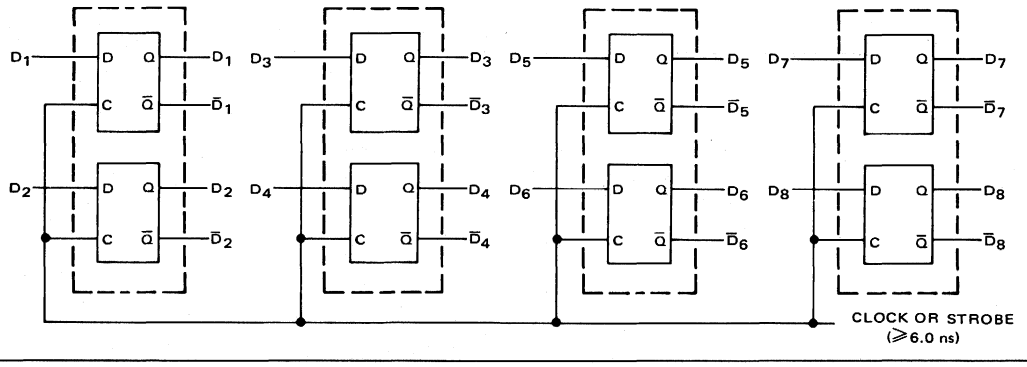
FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)

TRUTH TABLE

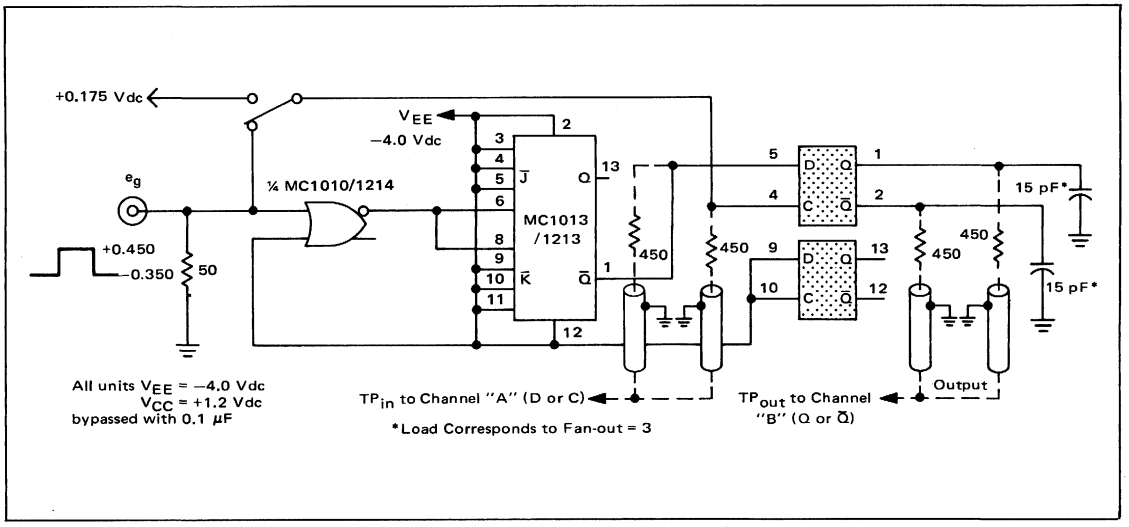
D	C	Q^{n+1}	$\bar{Q}^{n+1}$
ϕ	0	Q^n	$\bar{Q}^n$
0	1	0	1
1	1	1	0

ϕ = Either state may be present

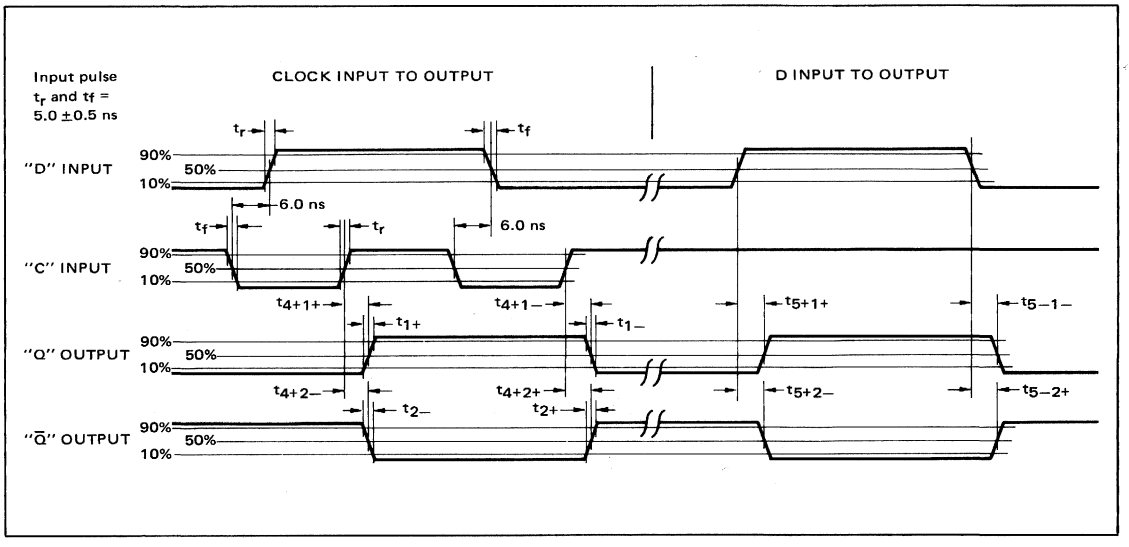
t_{pd} from D_{in} to Q or $\bar{Q} \approx 4.0$ ns
t_{pd} from C_{in} to Q or $\bar{Q} \approx 6.0$ ns



SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

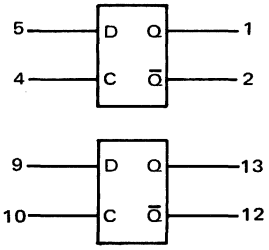


DUAL R-S FLIP-FLOPS
WITH SINGLE RAIL INPUT
AND POSITIVE CLOCK

MC1033
MC1233

Two dc storage flip-flops with a negative clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state. It may be teamed with the MC1016/MC1216 for shift register functions with a minimum number of packages.

POSITIVE LOGIC

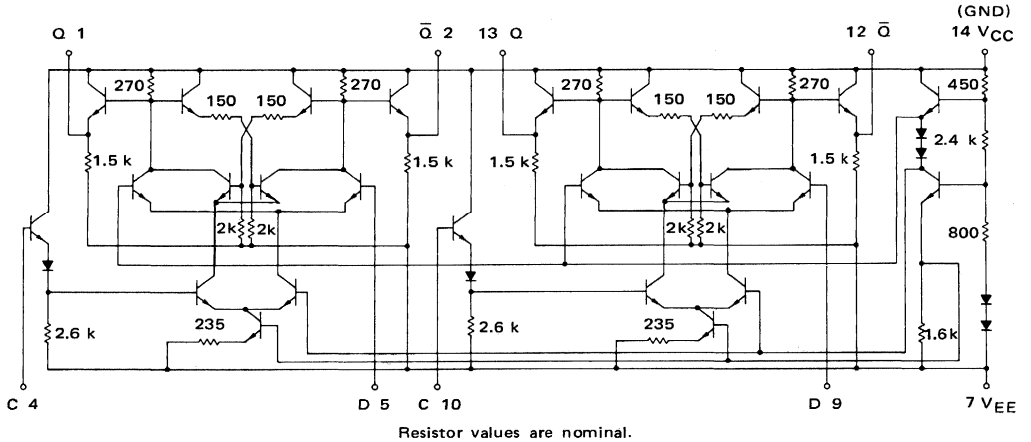


TRUTH TABLE

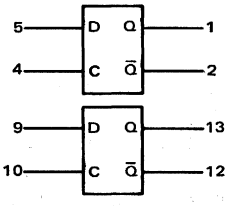
D	C	Q^{n+1}
0	1	Q^n
1	1	Q^n
0	0	0
1	0	1

DC Input Loading Factor: C = 1; D = 1.5
DC Output Loading Factor = 25
Power Dissipation = 140 mW typ

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1233 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1033 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	I_{in}	4	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		5	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
Input Leakage Current	I_R	4	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		5	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}†	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs																
Propagation Delay	t_{4-1+}	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	7.0	9.5	ns
	t_{4-1-}	1	5.0	10	5.0	10	7.0	12		5.0	10	5.0	10	6.0	11	
	t_{4-2+}	2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{4-2-}	2	6.0	10	6.0	10	8.0	12		6.0	10	6.0	10	7.0	11	
Rise Time	t_{1+}	1	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
	t_{2+}	2														
Fall Time	t_{1-}	1	5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
	t_{2-}	2	5.0	8.5	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Set Inputs																
Propagation Delay	t_{5+1+}	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
	t_{5-1-}	1					7.0	10.5								
	t_{5+2-}	2					7.0	10.5								
	t_{5-2+}	2		↓		↓	6.0	9.5			↓		↓		↓	
Rise Time	t_{1+}	1		7.5		7.5		9.0			7.5		7.5		8.0	
	t_{2+}	2		7.5	↓	7.5	↓	9.0		↓	7.5	↓	7.5	↓	8.0	
Fall Time	t_{1-}	1		8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	
	t_{2-}	2	↓	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	10	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1233	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
MC1233	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
MC1233	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1033	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
MC1033	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
MC1033	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	4, 10	-	5, 7, 9	-	14
Input Current	I_{in}	4	-	-	4	5, 7, 9, 10	-	14
		5	-	-	5	4, 7, 9, 10	-	14
Input Leakage Current	I_R	4	-	-	-	4, 5, 7, 9, 10	-	14
		5	-	-	-	4, 5, 7, 9, 10	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	1	4	5	-	7, 9, 10	1	14
"Q" Logical "0" Output Voltage	V_{OL}	1	4, 5	-	-	7, 9, 10	-	14
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	2	4, 5	-	-	7, 9, 10	2	14
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	2	4	5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3)			$V_{IL\ max}$ +1.2 Vdc	Pulse In	Pulse Out	V_{EE} = −4.0 Vdc		(+1.2V)
Clock Inputs								
Propagation Delay	t_{4-1+}	1	4	-	1	7, 9, 10	-	14
	t_{4-1-}	1	↓	-	1	↓	-	↓
	t_{4-2+}	2		-	2		-	
	t_{4-2-}	2		-	2		-	
Rise Time	t_{1+}	1		-	1		-	
	t_{2+}	2		-	2		-	
Fall Time	t_{1-}	1		-	1		-	
	t_{2-}	2	↓	-	2	↓	-	↓
Set Inputs								
Propagation Delay	t_{5+1+}	1	5	4	1	7, 9, 10	-	14
	t_{5-1-}	1	↓	↓	1	↓	-	↓
	t_{5+2-}	2			2		-	
	t_{5-2+}	2			2		-	
Rise Time	t_{1+}	1			1		-	
	t_{2+}	2			2		-	
Fall Time	t_{1-}	1			1		-	
	t_{2-}	2	↓	↓	2	↓	-	↓

APPLICATIONS INFORMATION

The MC1033/MC1233 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.

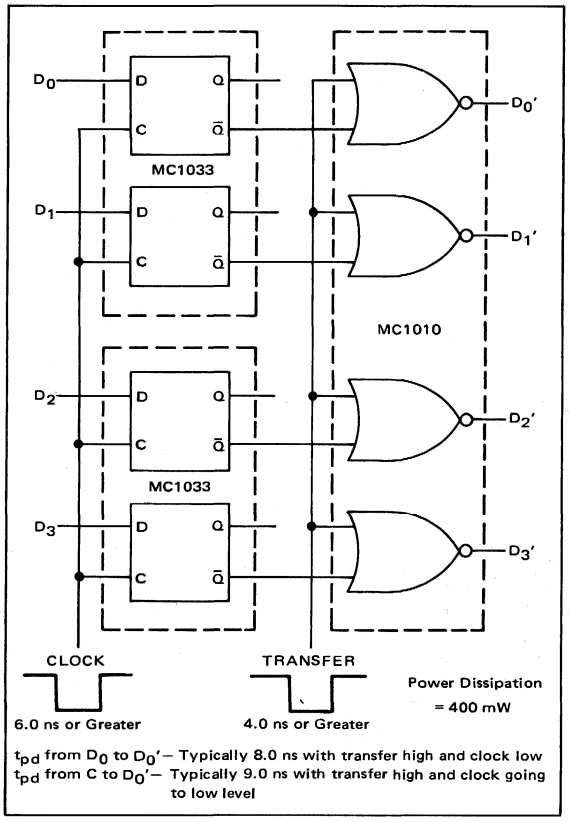


FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)

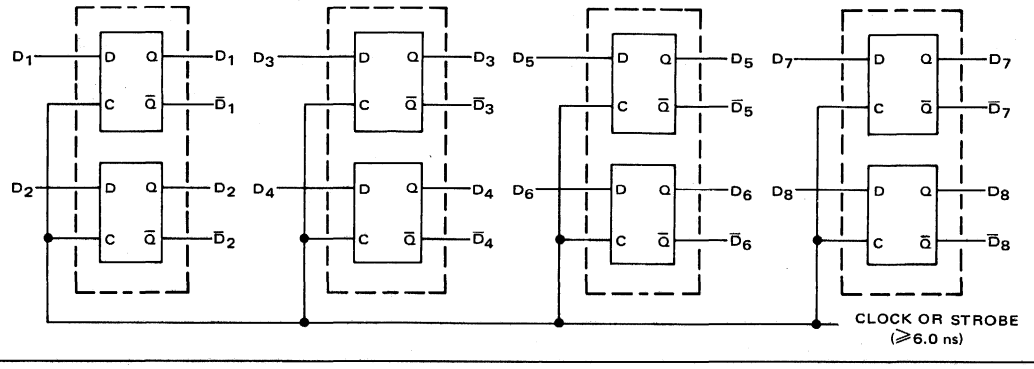
FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)

TRUTH TABLE

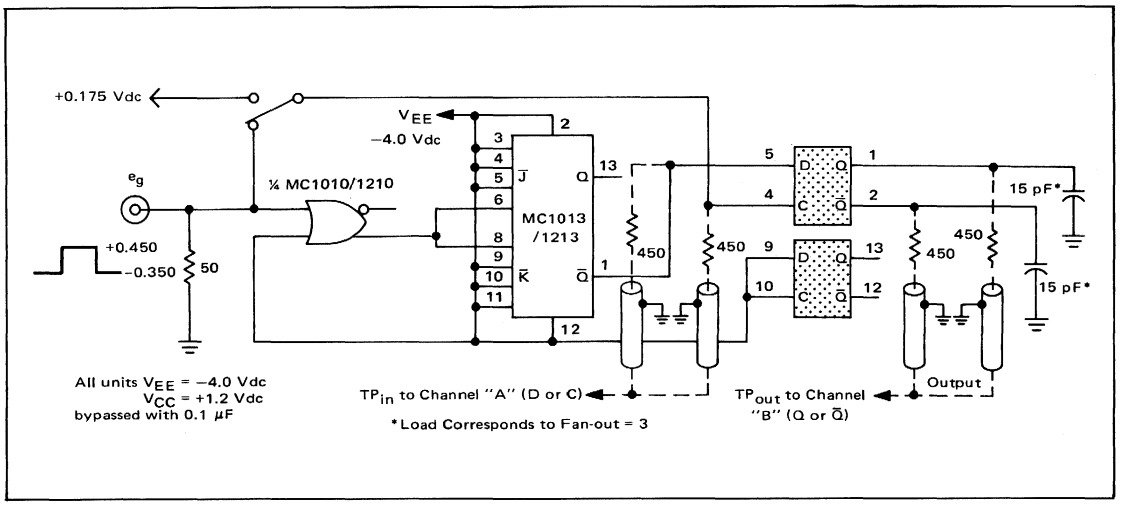
D	C	Q^{n+1}	$\bar{Q}^{n+1}$
ϕ	1	Q^n	$\bar{Q}^n$
0	0	0	1
1	0	1	0

ϕ = Either state may be present

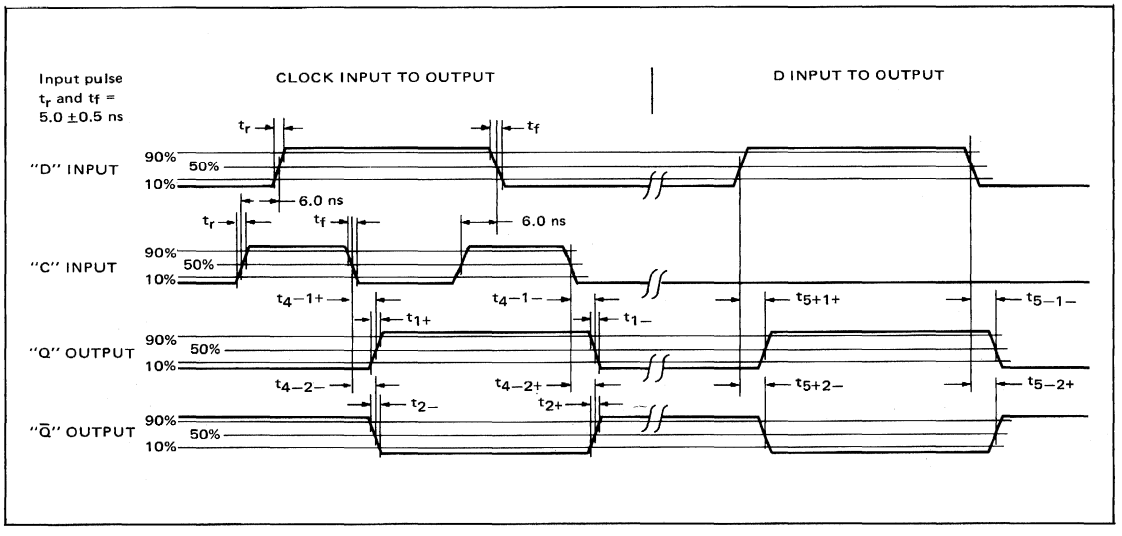
t_{pd} from D_{in} to Q or $\bar{Q} \approx 4.0$ ns
t_{pd} from C_{in} to Q or $\bar{Q} \approx 6.0$ ns



SWITCHING TIME TEST CIRCUIT
$T_A = 25^oC$



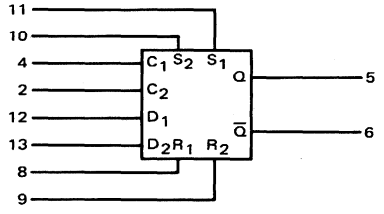
SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM



MC1022
MC1222

Designed for clocked-storage operation based on the "master-slave" principle. Operation depends only on voltage levels, therefore the shape of the clock waveform becomes unimportant in determining the state of the flip-flop. When the clock is low, the input data is stored in the "master" and is subsequently transferred to the "slave" when the clock is high, making the data available at the outputs. In this operation the "master" is disabled before the slave is enabled, due to the design of the internal threshold skew. Along with two data and two Clock inputs, the unit provides two SET and two RESET inputs that are independent of the Clock.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

R-S TRUTH TABLE

Pin No.	R 8 or 9	S 10 or 11	Q^{n+1} 5	$\bar{Q}^{n+1}$ 6
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

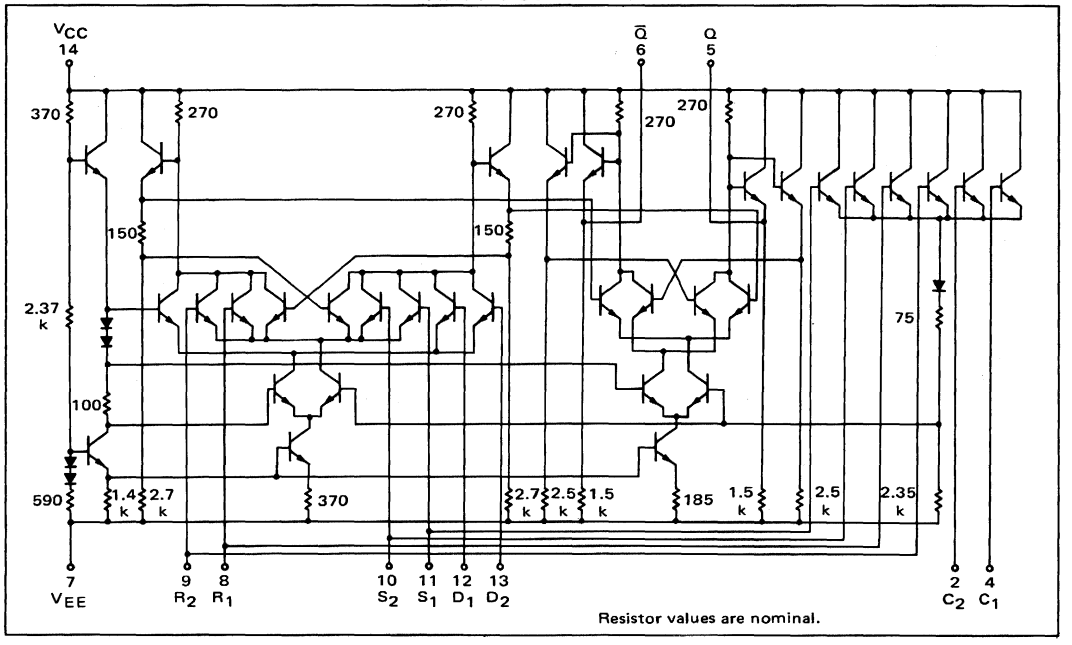
N.D. = Not Defined

CLOCKED TRUTH TABLE

Pin No.	D 12 or 13	C 2 or 4	Q^{n+1} 5	$\bar{Q}^{n+1}$ 6
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

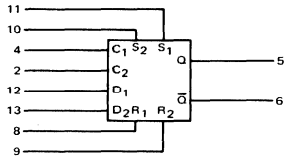
*A "1" or Clock input is defined for this flip-flop as a change in level from a low input to a high input.

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS



Characteristic	Symbol	Pin Under Test	MC1222 Test Limits							MC1022 Test Limits						
			−55°C		+25°C		+125°C		Unit	0°C		+25°C		+75°C		Unit
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	7	-	-	-	27	-	-	mAdc	-	-	-	27	-	-	mAdc
Input Current	I_{in}	2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		4	-	-	-		-	-		-	-	-		-	-	
		8	-	-	-		-	-		-	-	-		-	-	
		9	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
		11	-	-	-		-	-		-	-	-		-	-	
		12	-	-	-		-	-		-	-	-		-	-	
		13	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		5†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		5†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"$\bar{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		6†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		6†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Input Propagation Delay	t_{2+5-}	5	8.0	12	8.0	12	11	15	ns	8.0	12	8.0	12	9.0	13	ns
	t_{2+5+}	5	7.0	11	7.0	11	12	18		7.0	11	7.0	11	9.0	13	
	t_{2+6+}	6	7.0	11	7.0	11	12	18		7.0	11	7.0	11	9.0	13	
	t_{2+6-}	6	8.0	12	8.0	12	11	15		8.0	12	8.0	12	9.0	13	
Rise Time	t_{5+}, t_{6+}	5, 6	5.0	7.5	5.0	8.5	7.0	11		5.0	8.0	5.0	8.5	6.0	9.0	
Fall Time	t_{5-}, t_{6-}	5, 6	7.0	9.5	7.0	11.5	8.0	13		7.0	10.5	7.0	11.5	8.0	12	
Set Input Propagation Delay	t_{10+5+}	5	8.0	12	8.0	13	10	22	ns	8.0	12	8.0	13	10	14	ns
	t_{10+5+}	5		12	8.0	13	10	22			12	8.0	13	10	14	
	t_{10+6-}	6		13	9.0	14	11	19			13	9.0	14	11	15	
	t_{10+6-}	6		13	9.0	14	11	19			13	9.0	14	11	15	
Reset Input Propagation Delay	t_{9+5-}	5	8.0	13	9.0	14	11	19	ns	8.0	13	9.0	14	11	15	ns
	t_{9+5-}	5		13	9.0	14	11	19			13	9.0	14	11	15	
	t_{9+6+}	6		12	8.0	13	10	22			12	8.0	13	10	14	
	t_{9+6+}	6		12	8.0	13	10	22			12	8.0	13	10	14	

*Individually test each input using the pin connections shown.

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

† Output level to be measured after clock transition on pin 2 or 4 through one positive-going and one negative-going edge. (V_{IH}, V_{IL})

MC1022, MC1222 (continued)

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ± 1.0%				mAdc	
		V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	
MC1222	−55°C	-1.580	-0.990	-	-5.2	-2.5	
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5	
	+125°C	-1.380	-0.700	-	-5.2	-2.5	
MC1022	0°C	-1.525	-0.895	-	-5.2	-2.5	
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5	
	+75°C	-1.435	-0.775	-	-5.2	-2.5	

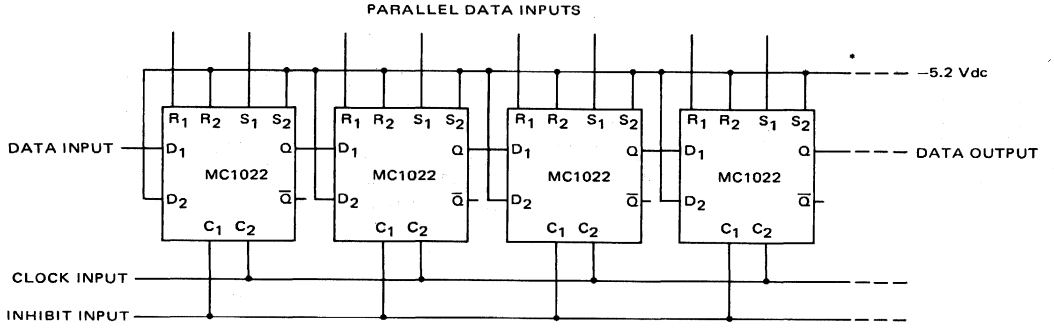
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
Input Current	I_{in}	2	-	-	2	4, 7, 8, 9, 10, 11, 12, 13	-	14
		4	-	-	4	2, 7, 8, 9, 10, 11, 12, 13	-	↓
		8	-	-	8	2, 4, 7, 9, 10, 11, 12, 13	-	
		9	-	-	9	2, 4, 7, 8, 10, 11, 12, 13	-	
		10	-	-	10	2, 4, 7, 8, 9, 11, 12, 13	-	
		11	-	-	11	2, 4, 7, 8, 9, 10, 12, 13	-	
		12	-	-	12	2, 4, 7, 8, 9, 10, 11, 13	-	
		13	-	-	13	2, 4, 7, 8, 9, 10, 11, 12	-	
Input Leakage Current	I_R	Inputs*	-	-	-	2, 4, 7, 8, 9, 10, 11, 12, 13	-	14
"Q" Logical "1" Output Voltage‡	V_{OH}‡	5	-	10	-	2, 4, 7, 8, 9, 11, 12, 13	5	14
		5†	-	13	-	2, 7, 8, 9, 10, 11, 12	5	14
"Q" Logical "0" Output Voltage	V_{OL}	5	-	9	-	2, 4, 7, 8, 10, 11, 12, 13	-	14
		5†	13	-	-	4, 7, 8, 9, 10, 11, 12	-	14
"$\overline{Q}$" Logical "1" Output Voltage‡	V_{OH}‡	6	-	8	-	2, 4, 7, 9, 10, 11, 12, 13	6	14
		6†	12	-	-	4, 7, 8, 9, 10, 11, 13	6	14
"$\overline{Q}$" Logical "0" Output Voltage	V_{OL}	6	-	11	-	2, 4, 7, 8, 9, 10, 12, 13	-	14
		6†	-	12	-	2, 7, 8, 9, 10, 11, 13	-	14
Switching Times Clock Input					Pulse In	V_{EE} − 4.0 Vdc	Pulse Out	(+1.2Vdc)
Propagation Delay	t_{2+5-}	5	-	-	2	4,7,8,9,10,11,12,13	5	14
	t_{2+5+}	5	-	-	↓	↓	5	↓
	t_{2+6+}	6	-	-			6	
	t_{2+6-}	6	-	-			6	
Rise Time	t_{5+}, t_{6+}	5, 6	-	-			5,6	
Fall Time	t_{5-}, t_{6-}	5, 6	-	-	↓	↓	5,6	↓
Set Input Propagation Delay	t_{10+5+}	5	-	2	10	4,7,8,11,12,13	5	14
	t_{10+5+}	5	2	-	↓	↓	5	↓
	t_{10+6-}	6	-	2			6	
	t_{10+6-}	6	2	-	↓	↓	6	↓
Reset Input Propagation Delay	t_{9+5-}	5	-	2	9	4,7,8,11,12,13	5	14
	t_{9+5-}	5	2	-	↓	↓	5	↓
	t_{9+6+}	6	-	2			6	
	t_{9+6+}	6	2	-	↓	↓	6	↓

APPLICATIONS INFORMATION

The MC1022/MC1222 single-phase Type D flip-flop offers advantages over the J-K flip-flop in applications such as single-rail operation. Since a true master-slave design is utilized, the input data may be asynchronous. There is no chance of data "rippling through" if the clock is in the low state. The SET and RESET inputs are also completely independent of the clock and will override the clock, setting both the master and the slave portions of the flip-flop. All the logic inputs are duplicated and ORed together internally, giving additional flexibility.

A low-level clock state (logic "0") allows information to be transferred to the master portion of the flip-flop through a "D" input. The master will continuously update itself to changing data as long as the clock is at a low level. When the clock goes to the high level, the master is disabled and the data transferred to the slave, thereby becoming available at the outputs. The thresholds of the master and slave portions of the flip-flop are internally offset to give a "raceless" flip-flop (i.e., the master is disabled before the slave is enabled, and vice versa). Thus the flip-flop operation is independent of the rise and fall times of the clock waveforms.

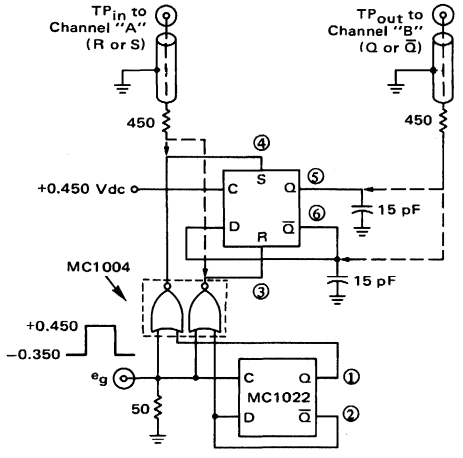
50 MHz SHIFT REGISTER



*Unused inputs should be returned to V_{EE}.

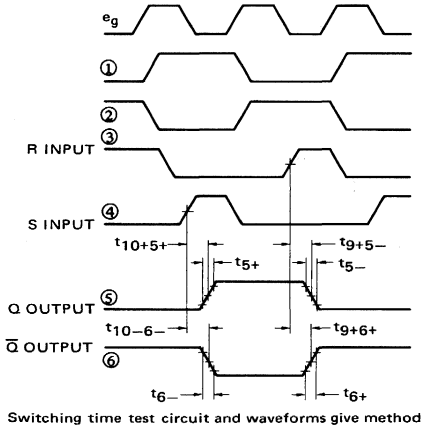
A "1" level on the Inhibit input may be used to stop the shifting of data through the register. Parallel data may be brought into the register asynchronously since SET or RESET data internally inhibits the clock.

SWITCHING TIME TEST CIRCUIT (T_A = 25°C)



All Units V_{EE} = −4.0 Vdc, V_{CC} = +1.2 Vdc } bypassed with 0.1 μF
Unused inputs returned to V_{EE}.

SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

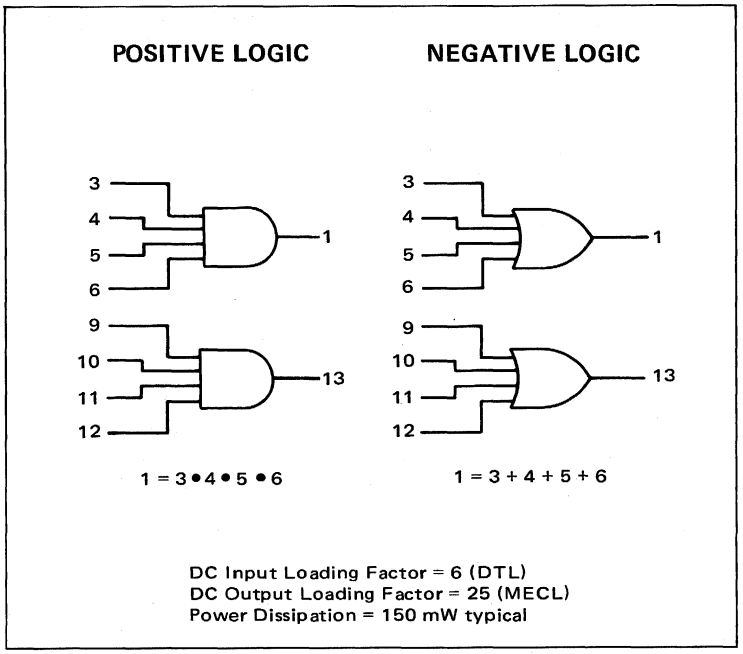


Switching time test circuit and waveforms give method of test with input pulses on pins 9 or 10 and output pulses on pins 5 and 6. Other tests specified and other combinations are tested in same manner and will meet limits specified.

SATURATED LOGIC-TO-MECL
DUAL TRANSLATORS

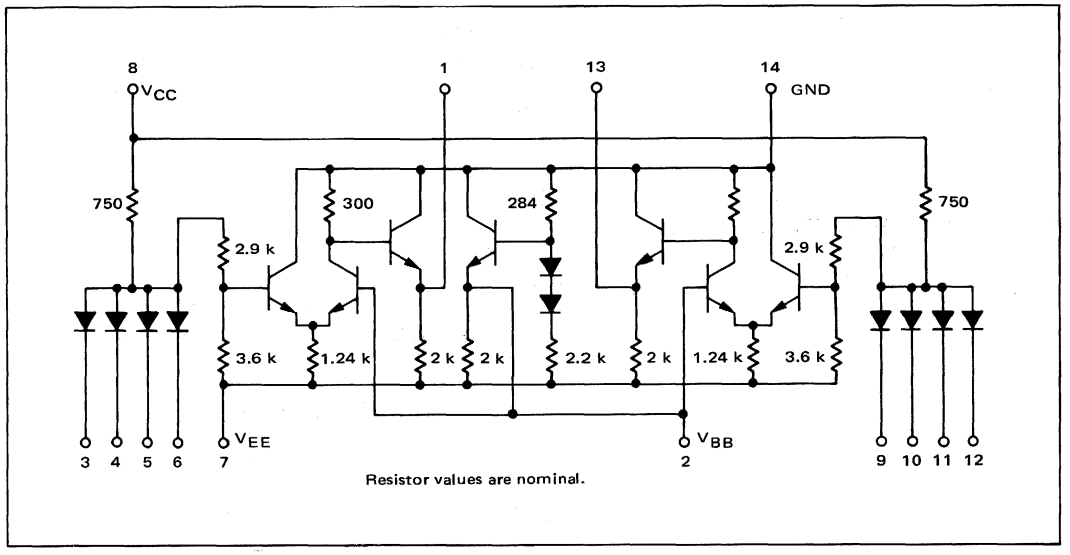
MC1017
MC1217

Dual level translator intended for converting saturated logic levels to MECL signal levels. The translator provides the positive logic OR function.

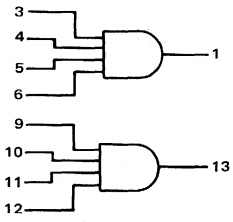


DC Input Loading Factor = 6 (DTL)
DC Output Loading Factor = 25 (MECL)
Power Dissipation = 150 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

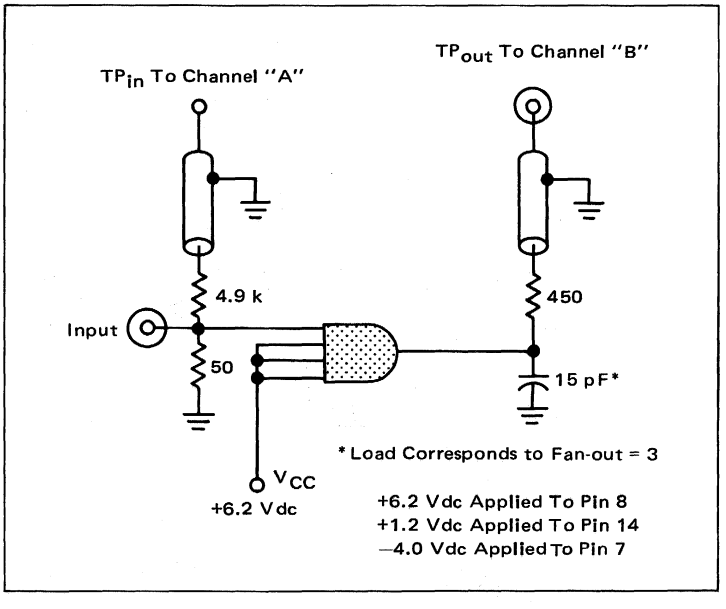
Test procedures are shown for only one translator.
The other translator is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1217 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1017 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Positive Supply Drain Current	I_C	8	-	-	-	4.0	-	-	mAdc	-	-	-	4.0	-	-	mAdc
Negative Supply Drain Current	I_E	7	-	-	-	24	-	-	mAdc	-	-	-	24	-	-	mAdc
Input Diode Reverse Current	I_R	3	-	-	-	0.2	-	2.0	μAdc	-	-	-	0.2	-	2.0	μAdc
		4	-	-	-	↓	-	↓	↓	-	-	-	↓	-	↓	↓
		5	-	-	-		-			-	-	-		-		
		6	-	-	-		-			-	-	-		-		
Input Diode Forward Current	I_F	3	-	-	-	7.5	-	-	mAdc	-	-	-	7.5	-	-	mAdc
		4	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		5	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
"OR" Logical "1" Output Voltage	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		1														
		1														
Bias Driver Output Voltage‡	V_{BB}†	2	-1.33	-1.19	-1.23	-1.09	-1.09	-0.95	Vdc	-1.28	-1.14	-1.23	-1.09	-1.19	-1.04	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{3+1+}	1	17	22	15	20	13	18	ns	16	21	15	20	14	19	ns
	t_{3-1-}	↓	13	18	15	20	19	25	↓	14	19	15	20	17	22	↓
Rise Time	t_{1+}		7.0	10	7.0	10	8.0	12		7.0	10	7.0	10	7.0	11	
Fall Time	t_{1-}		7.0	10	7.0	10	8.0	12		7.0	10	7.0	10	7.0	11	

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

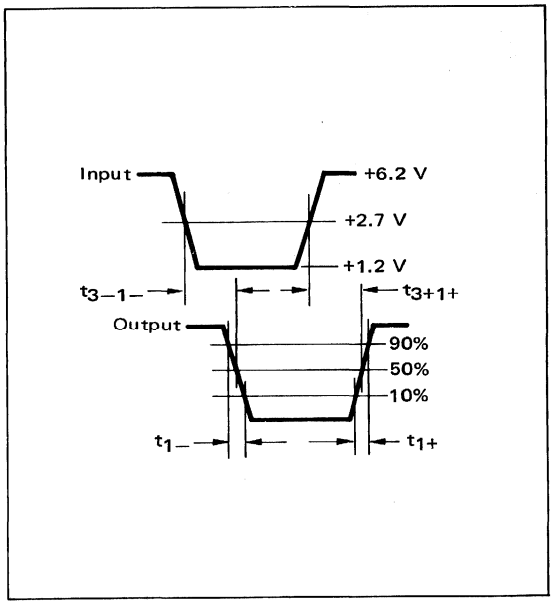
† V_{BB} limits apply from no load (0 mA) to full load (-1.0 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	mAdc I_L
MC1217	−55°C	2.1	0.5	-	5.0	-5.2	-2.5
	+25°C	2.0	1.0	8.0	5.0	-5.2	-2.5
	+125°C	2.0	0.7	8.0	5.0	-5.2	-2.5
MC1017	0°C	2.0	0.85	-	5.0	-5.2	-2.5
	+25°C	1.9	1.00	8.0	5.0	-5.2	-2.5
	+75°C	1.8	0.85	8.0	5.0	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{EE}	I_L	V_{CC} (Gnd)
Positive Supply Drain Current	I_C	8	-	-	-	8	7	-	14
Negative Supply Drain Current	I_E	7	-	-	-	8	7	-	14
Input Diode Reverse Current	I_R	3	-	-	3	-	-	-	4,5,6,14
		4	-	-	4	-	-	-	3,5,6,14
		5	-	-	5	-	-	-	3,4,6,14
		6	-	-	6	-	-	-	3,4,5,14
Input Diode Forward Current	I_F	3	-	-	-	8	7	-	3,14
		4	-	-	-	↓	↓	-	4,14
		5	-	-	-			-	5,14
		6	-	-	-			-	6,14
"OR" Logical "1" Output Voltage	V_{OH}‡	1	3,4,5,6	-	-	8	7	1	14
"OR" Logical "0" Output Voltage	V_{OL}	1	-	3	-	8	7	-	14
		1	-	4	-	↓	↓	-	↓
		1	-	5	-			-	
		1	-	6	-			-	
Bias Driver Output Voltage‡	V_{BB}†	2	-	-	-	8	7	2†	14
Switching Times			Pulse In	Pulse Out		(+6.2 V)	(−4.0 V)		(+1.2 V)
Propagation Delay	t_{3+1+}	1	1	3	-	8	7	-	14
	t_{3-1-}	↓	↓	↓	-	↓	↓	-	↓
Rise Time	t_{1+}				-			-	
Fall Time	t_{1-}				-			-	



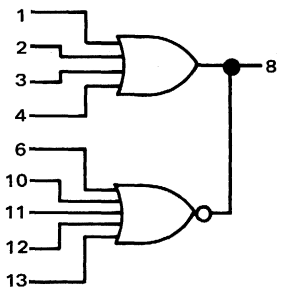
SWITCHING TIME WAVEFORMS

MECL-TO-SATURATED LOGIC TRANSLATORS

MC1018
MC1218

Level translator intended for converting MECL signal levels to saturated logic levels. The translator will provide the positive logic OR or logic NOR function by connecting the internal bias driver output to the corresponding inputs of the differential amplifier. i.e., when pin 4 is connected to the reference bias, pin 5, pins 6, 10, 11 12, and 13 become the inputs of a 5-input NOR gate. When pin 6 is connected to the reference bias, pin 5, pins 1, 2, 3, and 4 become the inputs of a 4-input OR gate.

POSITIVE LOGIC

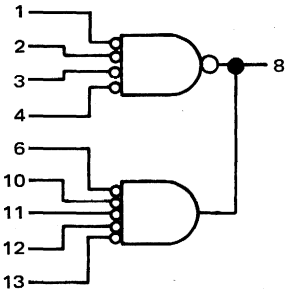


$8 = 1+2+3+4$

or

$8 = \overline{6+10+11+12+13}$

NEGATIVE LOGIC



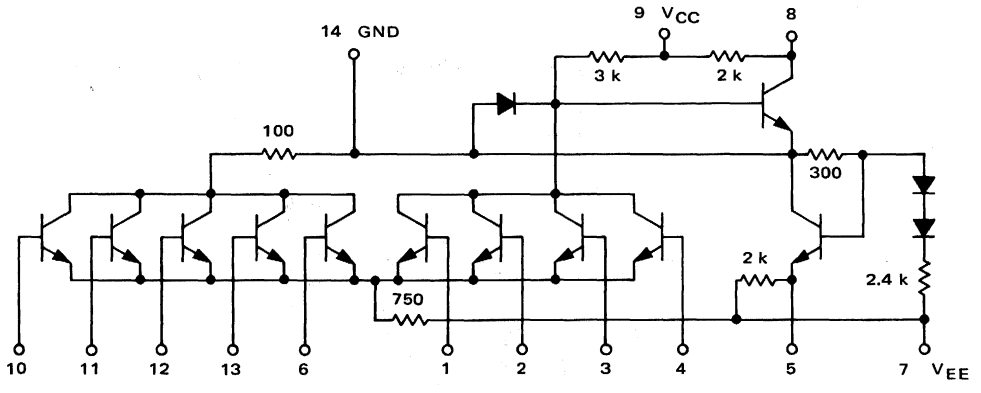
$8 = \overline{1} \cdot \overline{2} \cdot \overline{3} \cdot \overline{4}$

or

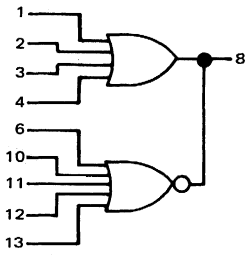
$8 = \overline{6 \cdot 10 \cdot 11 \cdot 12}$

DC Input Loading Factor = 2 (MECL)
DC Output Loading Factor = 7 (DTL)
Power Dissipation = 55 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



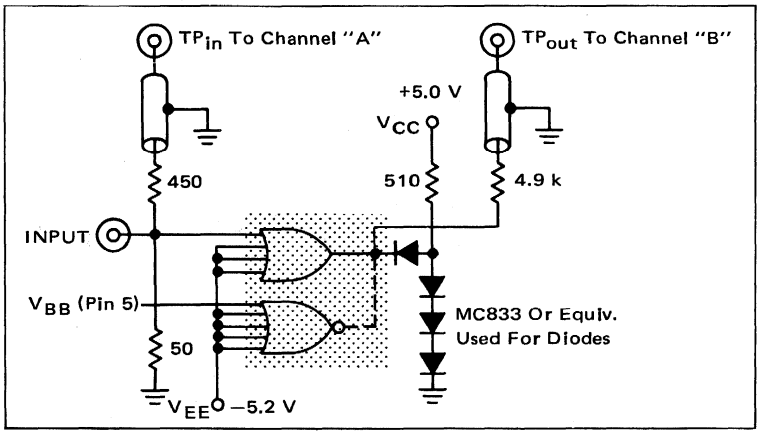
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1218 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1018 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Positive Supply Drain Current	I_C	9	-	-	-	3.0	-	-	mAdc	-	-	-	3.0	-	-	mAdc
Negative Supply Drain Current	I_E	7	-	-	-	11.0	-	-	mAdc	-	-	-	11.0	-	-	mAdc
Input Current	I_{in}	1	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
		2	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓
		3	-	-	-		-	-		-	-	-		-	-	
		4	-	-	-		-	-		-	-	-		-	-	
		6	-	-	-		-	-		-	-	-		-	-	
		10	-	-	-		-	-		-	-	-		-	-	
		11	-	-	-		-	-		-	-	-		-	-	
		12	-	-	-		-	-		-	-	-		-	-	
		13	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	1, 2, 3, 4*	-	-	-	0.2	-	2.0	μAdc	-	-	-	0.2	-	2.0	μAdc
		6, 10, 11, 12, 13*	-	-	-	0.2	-	2.0	μAdc	-	-	-	0.2	-	2.0	μAdc
Output Voltage High	V_{OH}	8	-	-	4.6	-	4.4	-	Vdc	-	-	4.6	-	4.5	-	Vdc
			-	-	↓	-	↓	-	↓	-	-	↓	-	↓	-	↓
			-	-		-		-		-	-		-		-	
			-	-		-		-		-	-		-		-	
			-	-		-		-		-	-		-		-	
Output Voltage Low	V_{OL}	8	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓
			-		-		-			-		-		-		
			-		-		-			-		-		-		
			-		-		-			-		-		-		
			-		-		-			-		-		-		
Bias Driver Output Voltage	V_{BB} ①	5	-1.33	-1.19	-1.23	-1.09	-1.09	-0.95	Vdc	-1.28	-1.14	-1.23	-1.09	-1.19	-1.04	Vdc
Output Short Circuit Current	I_{SC}	8	-	-4.0	-	-3.8	-	-3.6	mAdc	-	-3.9	-	-3.8	-	-3.6	mAdc
			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Switching Times	t_{1-8-}	8	19	25	19	25	19	25	ns	19	25	19	25	19	25	ns
	t_{1+8+}	↓	8.0	12	8.0	12	10	14	↓	8.0	12	8.0	12	9.0	13	↓
	t_{6-8+}		8.0	12	8.0	12	10	14		8.0	12	8.0	12	9.0	13	
	t_{6+8-}		19	25	19	25	19	25		12	25	19	25	19	25	

① V_{BB} is supplied from pin 5, and applies from no load (0 mA) to full load (-1.0 mAdc)

* Individually test each input using the pin connections shown.

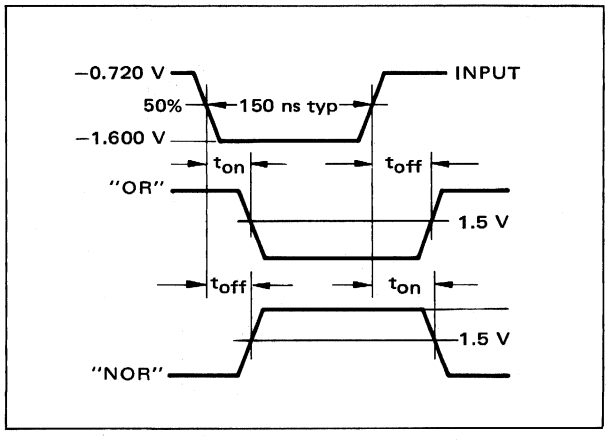
SWITCHING TIME TEST CIRCUIT @ 25°C



Circuit Shown For OR Configurations.
Connect Pin 5 to 4 For NOR.

@Test Temperature		TEST VOLTAGE/CURRENT VALUES									
		Vdc ±1.0%						μA	mAdc		
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{CC}	V_{EE}	V_{BB}	I_{OH}	I_{OL}	I_L	
MC1218	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	5.0	-5.2	①	-120	11.4	-1.0	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	5.0	-5.2	①	-120	12.0	-1.0	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	5.0	-5.2	①	-120	10.8	-1.0	
MC1018	0°C	-5.2 to -1.350	-1.070 to -0.740	-	5.0	-5.2	①	-120	12.0	-1.0	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	5.0	-5.2	①	-120	12.0	-1.0	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	5.0	-5.2	①	-120	11.4	-1.0	

Characteristic	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:									
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{CC}	V_{EE}	V_{BB}	I_{OH}	I_{OL}	I_L	V_{CC} (Gnd)
Positive Supply Drain Current	9	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	14
Negative Supply Drain Current	7	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	14
Input Current	1	-	-	1	9	2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
	2	-	-	2		1, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	
	3	-	-	3		1, 2, 4, 7, 10, 11, 12, 13	6	-	-	-	
	4	-	-	4		1, 2, 3, 7, 10, 11, 12, 13	6	-	-	-	
	6	-	-	6		1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	
	10	-	-	10		1, 2, 3, 6, 7, 11, 12, 13	4	-	-	-	
	11	-	-	11		1, 2, 3, 6, 7, 10, 12, 13	4	-	-	-	
	12	-	-	12		1, 2, 3, 6, 7, 10, 11, 13	4	-	-	-	
	13	-	-	13		1, 2, 3, 6, 7, 10, 11, 12	4	-	-	-	
Input Leakage Current	1, 2, 3, 4*	-	-	-	9	1, 2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
	6, 10, 11, 12, 13*	-	-	-	9	1, 2, 3, 6, 7, 10, 11, 12, 13	4	-	-	-	
Output Voltage High	8	6, 10, 11, 12, 13	-	-	9	1, 2, 3, 7	4	8	-	-	14
		-	1	-		2, 3, 4, 7, 10, 11, 12, 13	6		-	-	
		-	2	-		1, 3, 4, 7, 10, 11, 12, 13			-	-	
		-	3	-		1, 2, 4, 7, 10, 11, 12, 13			-	-	
		-	4	-		1, 2, 3, 7, 10, 11, 12, 13			-	-	
Output Voltage Low	8	1, 2, 3, 4	-	-	9	7, 10, 11, 12, 13	6	-	8	-	14
		-	6	-		1, 2, 3, 7, 10, 11, 12, 13	4	-		-	
		-	10	-		1, 2, 3, 6, 7, 11, 12, 13		-		-	
		-	11	-		1, 2, 3, 6, 7, 10, 12, 13		-		-	
		-	12	-		1, 2, 3, 6, 7, 10, 11, 13		-		-	
		-	13	-		1, 2, 3, 6, 7, 10, 11, 12		-		-	
Bias Driver Output Voltage	5	-	-	-	9	7	-	-	-	5	14
Output Short Circuit Current	8	-	-	4	9	1, 2, 3, 7, 10, 11, 12, 13	6	-	-	-	8, 14
		Pulse In	Pulse Out								
Switching Times	8	1	8	-	9	2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	14
		1		-		2, 3, 4, 7, 10, 11, 12, 13	6	-	-	-	
		6		-		1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	
		6		-		1, 2, 3, 7, 10, 11, 12, 13	4	-	-	-	

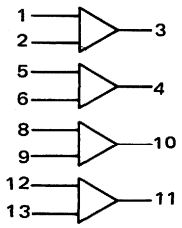


SWITCHING TIME WAVEFORMS

MC1020
MC1220

Four differential amplifiers with emitter follower outputs, intended for use as a comparator or for sensing differential signals over long lines. Each amplifier provides the OR or NOR logic function depending on which input is biased at a given reference voltage.

POSITIVE LOGIC

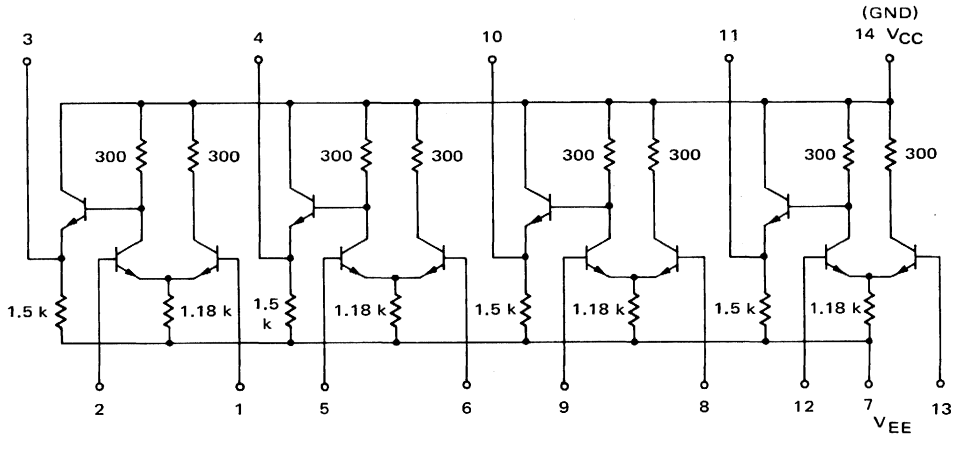


DC Input Loading Factor = 1
DC Output Loading Factor = 25

TRUTH TABLE

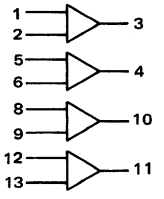
1	2	3	
6	5	4	
8	9	10	
13	12	11	
V_{BB}	H	L	NOR
V_{BB}	L	H	NOR
H	V_{BB}	H	OR
L	V_{BB}	L	OR

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line receiver.
The other line receivers are tested in the same manner.



	@Test Temperature
MC1220	−55°C
	+25°C
	+125°C
MC1020	0°C
	+25°C
	+75°C

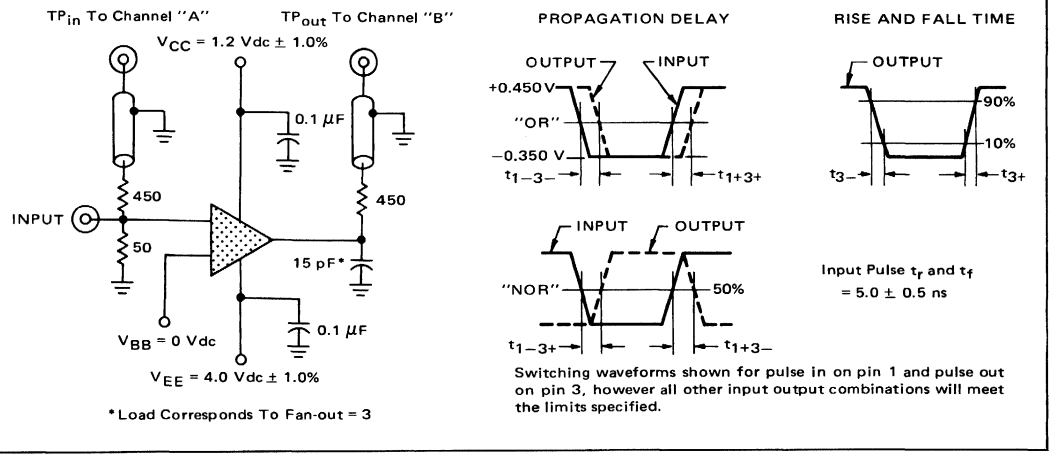
Characteristic	Symbol	Pin Under Test	MC1220 −55°C Min	MC1220 −55°C Max	MC1220 +25°C Min	MC1220 +25°C Max	MC1220 +125°C Min	MC1220 +125°C Max	Unit	MC1020 0°C Min	MC1020 0°C Max	MC1020 +25°C Min	MC1020 +25°C Max	MC1020 +75°C Min	MC1020 +75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	28	-	-	mAdc	-	-	-	28	-	-	mAdc
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	1	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
		2	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+3+}	3	4.0	7.0	4.0	7.0	5.0	8.0	ns	4.0	7.0	4.0	7.0	4.0	7.5	ns
	t_{1-3-}		4.0	7.0	4.0	7.0	5.0	8.0		4.0	7.0	4.0	7.0	4.0	7.5	
Rise Time (Fan-Out = 3)	t_{3+}		4.0	7.0	4.0	7.0	5.0	8.0		4.0	7.0	4.0	7.0	4.0	7.5	
Fall Time (Fan-Out = 3)	t_{3-}		5.0	8.0	5.0	8.0	6.0	9.0		5.0	8.0	5.0	8.0	5.0	8.5	

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

TEST VOLTAGE/CURRENT VALUES					
Vdc ±1.0%					mAdc
$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L
-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-1.270	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-1.025	-2.5
-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-1.210	-2.5
-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-1.175	-2.5
-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-1.115	-2.5

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:						V_{CC} (Gnd)
$V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	V_{BB}	I_L	
-	-	-	2,5,7,9,12	1,6,8,13	-	14
-	-	1	5,6,7,8,9,12,13	2	-	14
-	-	2	5,6,7,8,9,12,13	1	-	14
-	-	-	1,5,6,7,8,9,12,13	2	-	14
-	-	-	2,5,6,7,8,9,12,13	1	-	14
2	-	-	5,6,7,8,9,12,13	1	3	14
-	2	-	5,6,7,8,9,12,13	1	-	14
-	1	-	5,6,7,8,9,12,13	2	-	14
1	-	-	5,6,7,8,9,12,13	2	-	14
Pulse In	Pulse Out		V_{EE} = −4.0 Vdc			(+1.2V)
1	3	-	5,6,7,8,9,12,13	2	-	14
		-			-	
		-			-	
		-			-	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



APPLICATIONS INFORMATION

The MC1020/MC1220 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. Any MECL II gate with differential outputs may be used to drive the twisted pair line. The line is terminated in its characteristic impedance (around 100 ohms). A voltage divider is formed between the high-level gate output, the terminating resistor, and the pull-down resistor on the low-level gate output. The equivalent dc circuit is shown in Figure 2. The voltage swing across the terminating resistor (R_T) is typically ± 275 mV. Any input voltage swing in excess of 120 mV is adequate due to the voltage gain of the MC1020/MC1220. The output of the line receiver is the same as a standard MECL II gate. For worst-case pull-down resistors in the driving gate (1.5 k ohms ± 20%) and a $V_{OH\ min}$, the differential drop across an R_T of 100 ohms is ± 230 mV.

Very long lines may be used with excellent results. The only restriction on lead length (other than common mode noise) is series line resistance. The nominal voltage drop across R_T is actually shared with the series resistance of the twisted pair line. The resistance of # 22 AWG wire averages about 16 ohms per 1000 feet, while # 24 AWG wire averages about 26 ohms per 1000 feet. For very long lines, an additional voltage drop across R_T is easily obtained by paralleling additional pull-down resistors with those internal to the driver gate. For example, by paralleling a 1.5 k ohm resistor with each output, the voltage drop across R_T is effectively doubled.

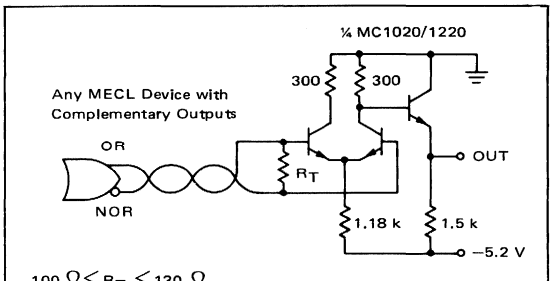
Extensive data have shown that a positive transient of 1.0 V or a negative transient of 1.8 V may be introduced on the twisted pair line before noise can propagate through another MECL device tied to the line receiver output. This method of data transmission is useful at frequencies to 50 MHz and results in the highest bandwidth – noise immunity product obtainable with digital logic. A twisted pair is recommended for clock distribution in high-speed systems since distribution skew time may be balanced out by adjusting line lengths. Propagation delay times are approximately 1.0 ns per eight inches of line.

In system design it is often convenient to organize information transfer with a data bus or "party-line" approach. In this application, one of many sources may "talk" to the common data line and multiple receivers may "listen". Figure 3 illustrates such a data bus utilizing MECL II gates as drivers and MC1020's as line receivers. Note that the line is unbalanced, but this will in turn allow all drivers to be ORed together. Bandwidth of data distribution is excellent. The technique may be used to 50 MHz at 25°C and to 40 MHz over the entire military temperature range. Noise immunity is also good due to the low impedance methods of transmission and the common mode rejection of the line receiver. The following results were obtained during an evaluation of the data bus shown in Figure 3 under worst-case conditions:

Number of driver gates: 6
Number of receivers: 8
Line length: 24 feet
Differential temperature from transmitter gate to receiver gate: 100°C
Maximum operating frequency: 40 MHz
Total terminating resistance: 45 ohms
Differential power supply voltage from transmitter gate to receiver gate: ± 5.0%

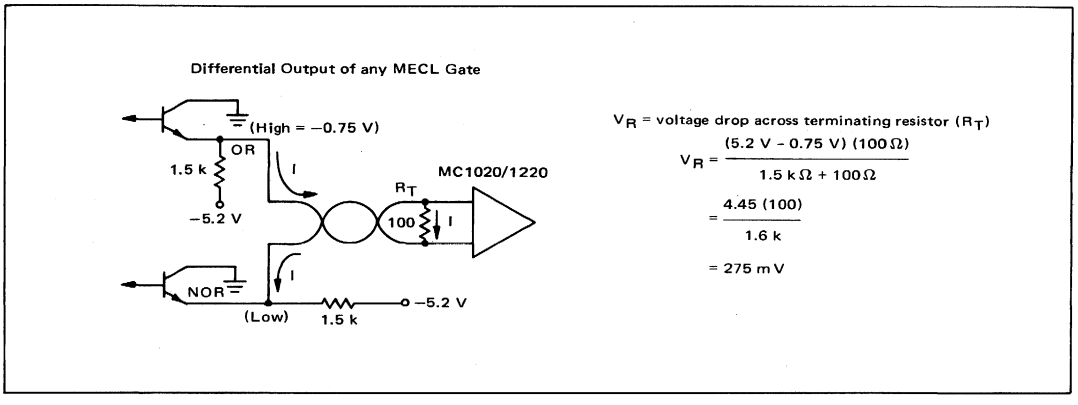
The quad line receiver can also be used in many linear applications. The voltage gain is typically 7.0, with a bandwidth of approximately 70 MHz for each differential amplifier. The device makes an excellent FM limiter with minimal phase shift. By employing feedback, both selective band-pass amplifiers and notch frequency rejection amplifiers may be built. Figure 4 shows ¼ of the quad line receiver used as a parallel tuned-crystal oscillator that exhibits excellent stability.

FIGURE 1 - MECL LINE RECEIVER



$100\ \Omega < R_T < 130\ \Omega$
Driver worst-case R_E = 1.8 kΩ @ R_T = 100 Ω and V_R = 230 mV
Differential Gain = 15 dB or 6.0 V/V
Common Mode Gain = −18 dB or 0.12 V/V
Common Mode Voltage Rejection = 1.8 V (Negative pulse on lines)
1.0 V (Positive pulse on lines)

FIGURE 2 - LINE RECEIVER DC EQUIVALENT CIRCUIT



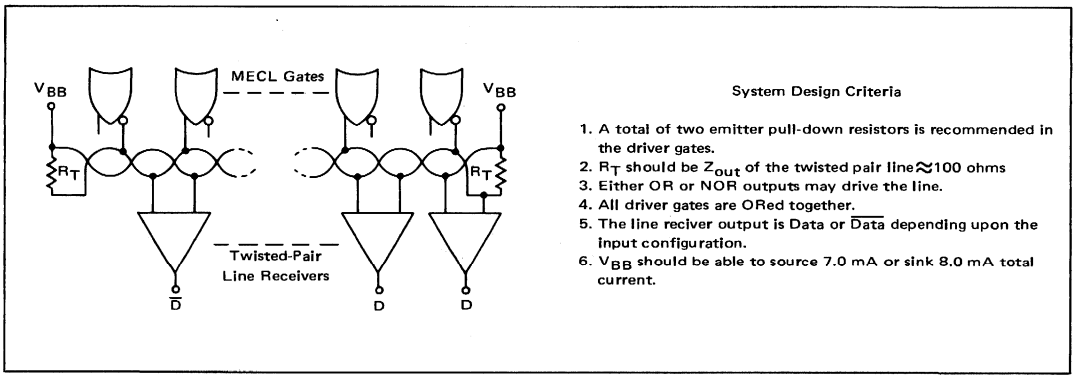
V_R = voltage drop across terminating resistor (R_T)

$$V_R = \frac{(5.2\ V - 0.75\ V)\ (100\,\Omega)}{1.5\,k\Omega + 100\,\Omega}$$

$$= \frac{4.45\ (100)}{1.6\ k}$$

$$= 275\ mV$$

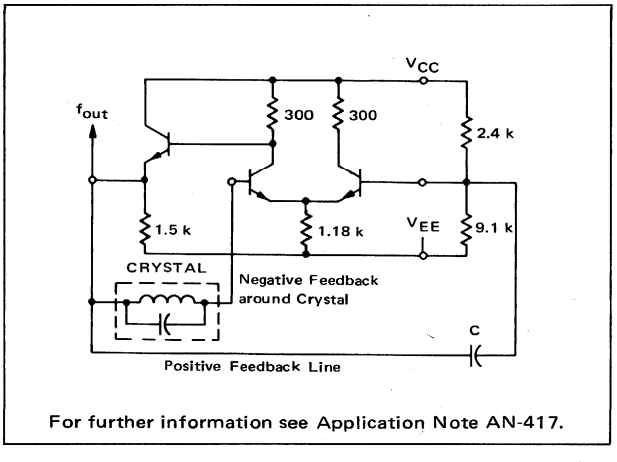
FIGURE 3 - DATA BUS DRIVING WITH MECL II



System Design Criteria

1. A total of two emitter pull-down resistors is recommended in the driver gates.
2. R_T should be Z_{out} of the twisted pair line≈100 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line reciver output is Data or $\overline{\text{Data}}$ depending upon the input configuration.
6. V_{BB} should be able to source 7.0 mA or sink 8.0 mA total current.

FIGURE 4 - ¼ MC1020/1220 AS A PARALLEL-TUNED CRYSTAL OSCILLATOR



For further information see Application Note AN-417.

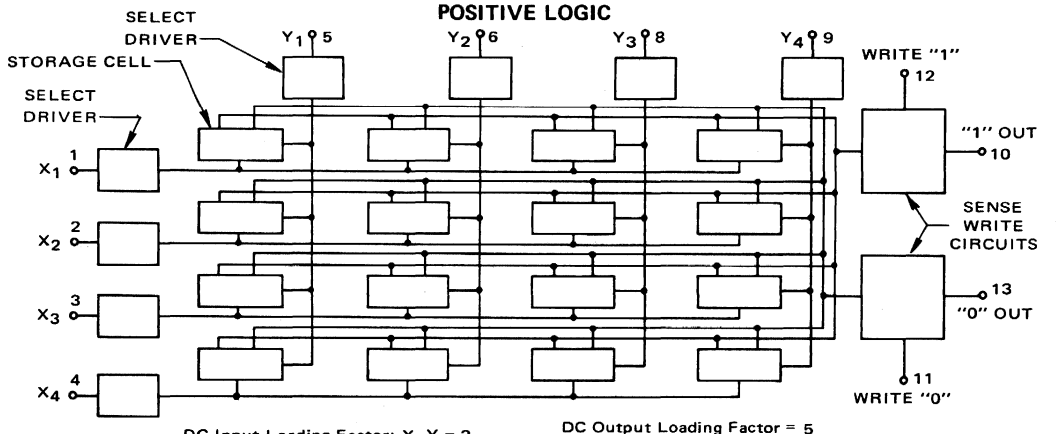
MC1036
MC1037

Designed for high-speed systems capable of cycle times as low as 50 ns. The memory is comprised of 16 multiple-emitter flip-flops, eight input emitter followers, and two nonsaturating complementary Sense/Write circuits. The flip-flops form an addressable 4 by 4 memory matrix that exhibits non-destructive readout for all 16 bits.

In operation a single bit is selected by applying a logical "1" to the coincident "X" and "Y" address lines. This gives a "read" condition where the sense amplifier outputs indicate the storage state of the selected bit. For example, if the bit store is a logical "1", the Sense "1" amplifier output will be a logical "1" and the Sense "0" amplifier will indicate the complement. With the desired "X" and "Y" lines at a logical "1", writing is accomplished by applying a logical "1" to the Write "1" input or to the Write "0" to obtain a bit store of a "1" or a "0" respectively.

The emitter-coupled sense amplifier outputs permit Wired-OR operation so that word expansion is easily obtained.

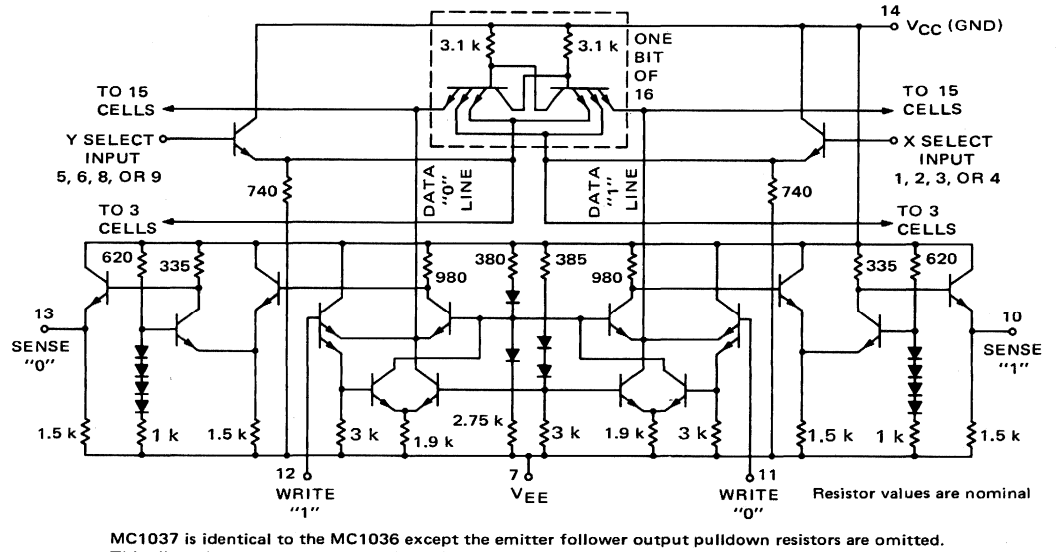
POSITIVE LOGIC



DC Input Loading Factor: X, Y = 2
Write = 0.5

DC Output Loading Factor = 5
Power Dissipation = 250 mW typical
Maximum Power Supply Variation = ±10%

CIRCUIT SCHEMATIC



MC1037 is identical to the MC1036 except the emitter follower output pulldown resistors are omitted. This allows large memory array design utilizing the Wired-OR feature, and minimum power dissipation.

ELECTRICAL CHARACTERISTICS

For MC1036 and MC1037: Test procedures are shown for only the X_1 input, for the X_1, $Y_{1,2,3,4}$ storage cells. To complete testing, sequence through remaining inputs, associated with remaining storage cells.

For MC1037 only: Outputs under test are connected to V_{EE} through 1.5 kΩ resistor.

@Test Temperature	V_{IH}	$V_{IH\ max}$	V_{IL}	V_{EE}	I_L
	TEST VOLTAGE/CURRENT VALUES				
	Vdc ± 1.0%				mAdc
0°C	-0.890	-	-1.525	-5.2	-0.5
+25°C	-0.850	-0.700	-1.500	-5.2	-0.5
+75°C	-0.790	-	-1.435	-5.2	-0.5

Characteristic	Symbol	Pin Under Test	MC1036, MC1037 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IH\ max}$	V_{IL}	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	66	-	-	mAdc	1,5	-	2,3,4,6,8,9,11,12	7	-	14
Input Current	2 I_{in}	1	-	-	-	200	-	-	μAdc	-	1	2, 3, 4, 5, 6, 8, 9, 11, 12	7	-	14
	0.5 I_{in}	11	-	-	-	50	-	-	↓	-	11	1, 2, 3, 4, 5, 6, 8, 9, 12	↓	-	↓
	0.5 I_{in}	12	-	-	-	50	-	-	↓	-	12	1, 2, 3, 4, 5, 6, 8, 9, 11	↓	-	↓
Input Leakage Current	I_R	1	-	-	-	1.0	-	5.0	μAdc	-	-	2, 3, 4, 5, 6, 8, 9, 11, 12	1, 7	-	14
		11	-	-	-	1.0	-	5.0	↓	-	-	1, 2, 3, 4, 5, 6, 8, 9, 12	7, 11	-	↓
		12	-	-	-	1.0	-	5.0	↓	-	-	1, 2, 3, 4, 5, 6, 8, 9, 11	7, 12	-	↓
Sense "1" Logical "1" Output Voltage‡	V_{OH}‡	10	-0.935	-0.740	-0.850	-0.700	-0.790	-0.615	Vdc	1, 5, 12*	-	2, 3, 4, 6, 8, 9, 11	7	10	14
		↓	↓	↓	↓	↓	↓	↓	↓	1, 6, 12*	-	2, 3, 4, 5, 8, 9, 11	↓	↓	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 8, 12*	-	2, 3, 4, 5, 6, 9, 11	↓	↓	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 9, 12*	-	2, 3, 4, 5, 6, 8, 11	↓	↓	↓
Sense "1" Logical "0" Output Voltage	V_{OL}	10	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	1, 5, 11*	-	2, 3, 4, 6, 8, 9, 12	7	-	14
		↓	↓	↓	↓	↓	↓	↓	↓	1, 6, 11*	-	2, 3, 4, 5, 8, 9, 12	↓	-	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 8, 11*	-	2, 3, 4, 5, 6, 9, 12	↓	-	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 9, 11*	-	2, 3, 4, 5, 6, 8, 12	↓	-	↓
Sense "0" Logical "1" Output Voltage‡	V_{OH}‡	13	-0.935	-0.740	-0.850	-0.700	-0.790	-0.615	Vdc	1, 5, 11*	-	2, 3, 4, 6, 8, 9, 12	7	13	14
		↓	↓	↓	↓	↓	↓	↓	↓	1, 6, 11*	-	2, 3, 4, 5, 8, 9, 12	↓	↓	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 8, 11*	-	2, 3, 4, 5, 6, 9, 12	↓	↓	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 9, 11*	-	2, 3, 4, 5, 6, 8, 12	↓	↓	↓
Sense "0" Logical "0"	V_{OL}	13	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc	1, 5, 12*	-	2, 3, 4, 6, 8, 9, 11	7	-	14
		↓	↓	↓	↓	↓	↓	↓	↓	1, 6, 12*	-	2, 3, 4, 5, 8, 9, 11	↓	-	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 8, 12*	-	2, 3, 4, 5, 7, 9, 11	↓	-	↓
		↓	↓	↓	↓	↓	↓	↓	↓	1, 9, 12*	-	2, 3, 4, 5, 6, 8, 11	↓	-	↓
Switching Times†			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out	V_{IL} + 1.2 Vdc	V_{EE} − 4.0 Vdc		(+1.2 Vdc)
Write Recovery	t_{12-13-}	13	22	30	22	30	25	35	ns	12	13	2, 3, 4, 6, 8, 9, 12	7	-	14
Output Turn-Off	t_{5+13+}	13	17	20	17	20	19	22	↓	1, 5	13	↓	↓	-	↓
Output Turn-On	t_{1-13-}	13	17	20	17	20	19	22	↓	1, 5	13	↓	↓	-	↓

* V_{IH} applied momentarily to pin 11 or 12 as shown for 25 ns minimum.

† Pins 1 and 5 at V_{IH} +1.2 Vdc.

‡ V_{OH} limits apply from no load (0 mA) to full load (-0.5 mA)

APPLICATIONS INFORMATION

A memory consisting of 16 words of N bits per word can be realized by connecting the selection lines of N 16-bit memories in parallel as shown in Figure 4. This results in a 4 by 4 selection matrix such that a word is selected by raising one X line and one Y line to the high state. The maximum value of N in this basic configuration is determined by the maximum fan-out of the gate used to drive the array. The recommended maximum N in this configuration is 12 (each input represents 2 dc loads) if MECL II gates are used to drive the X and Y selection lines and the wiring capacitance is a maximum of 3.0 pF per input.

The number of words can be increased by emitter ORing the outputs and/or using output gating. The emitter ORing technique is shown in Figure 5 for an N-bit by 16M-word memory. Memories 11, 21, . . ., N1 are MC1036's and the remaining units are MC1037's. In this way power dissipation is minimized and no external pulldown resistors are required. The maximum recommended M is 16 and the wiring capacitance should be a maximum of 3.0 pF per output.

A 256-word by 12-bit memory can be constructed without input or output gating (excluding selection gating) if the wiring capacitance can be kept reasonably small. The number of words and the number of bits per word can be increased by proper input and output gating.

FIGURE 1 – MINIMUM "WRITE" PULSE WIDTH versus TEMPERATURE

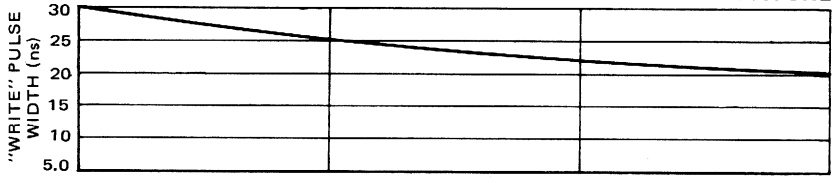


FIGURE 2 – TYPICAL "WRITE" RECOVERY TIME versus TEMPERATURE

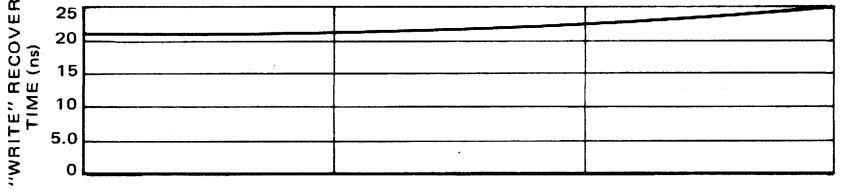


FIGURE 3 – TYPICAL "READ" TIME versus TEMPERATURE

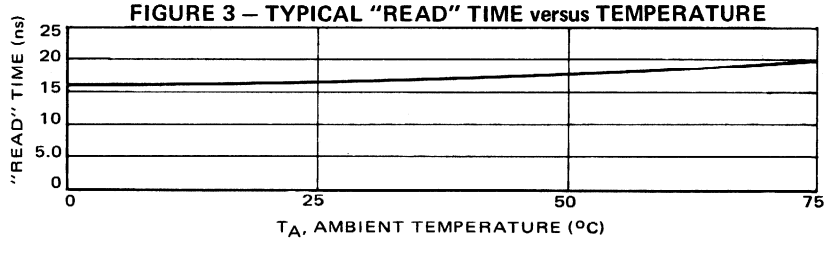


FIGURE 4 – 16-WORD BY N-BIT MEMORY

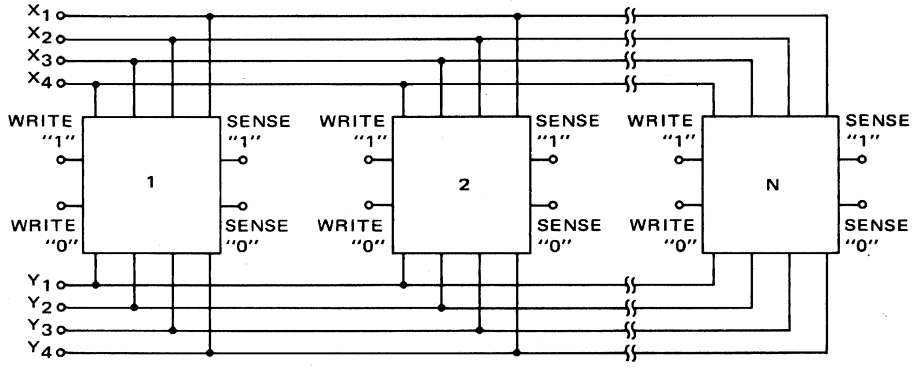
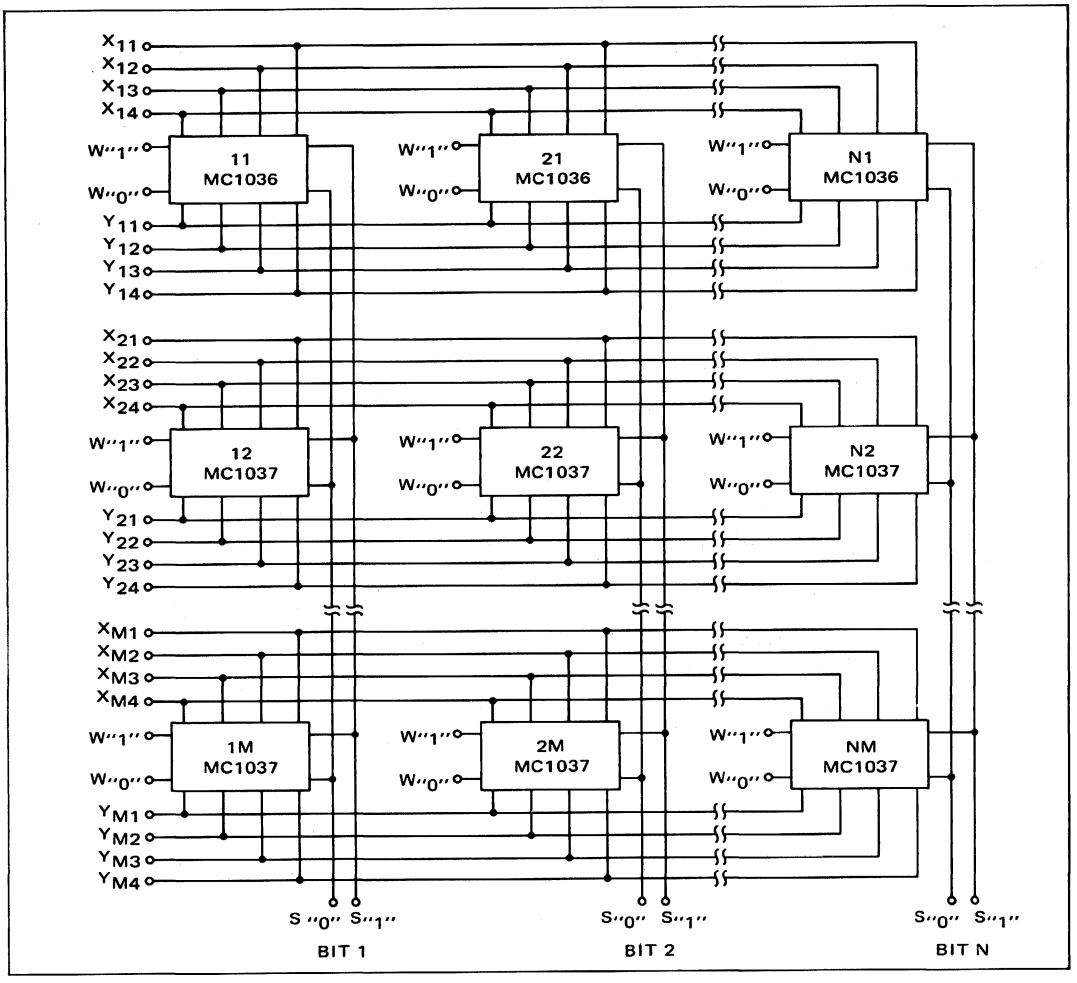
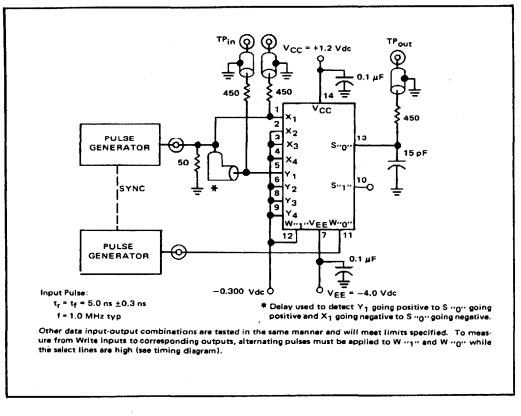


FIGURE 5 – INTERCONNECTION TECHNIQUE FOR N-BIT BY 16M-WORD MEMORY

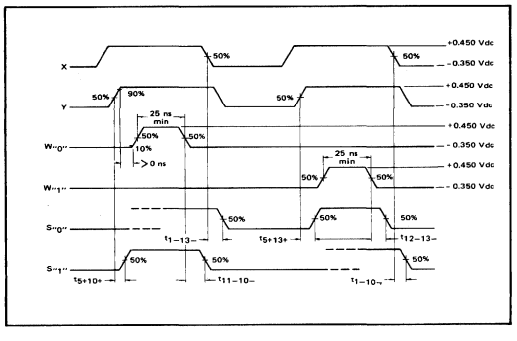


SWITCHING TIME TEST CIRCUIT @ 25°C

(For t_{1-13-} and t_{5+13+})



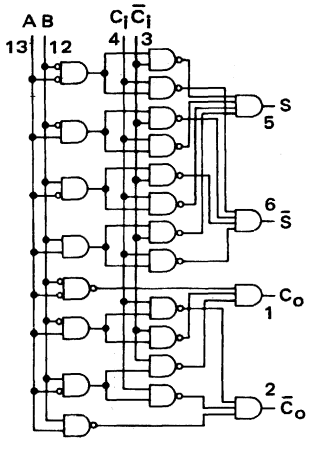
TIMING DIAGRAM @ T_A = 25°C



MC1019
MC1219

Provides the SUM, $\overline{SUM}$, CARRY, and $\overline{CARRY}$ functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN and $\overline{CARRY\ IN}$.

POSITIVE LOGIC



TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
A	B	C_i	$\overline{C}_i$	S	$\overline{S}$	C_o	$\overline{C}_o$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	1	0	1	0

$S = ABC_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$

$\bar{S} = \bar{A}\bar{B}\bar{C}_i + \bar{A}BC_i + A\bar{B}C_i + ABC_i$

$C_o = ABC_i + AB\bar{C}_i + A\bar{B}C_i + \bar{A}BC_i$

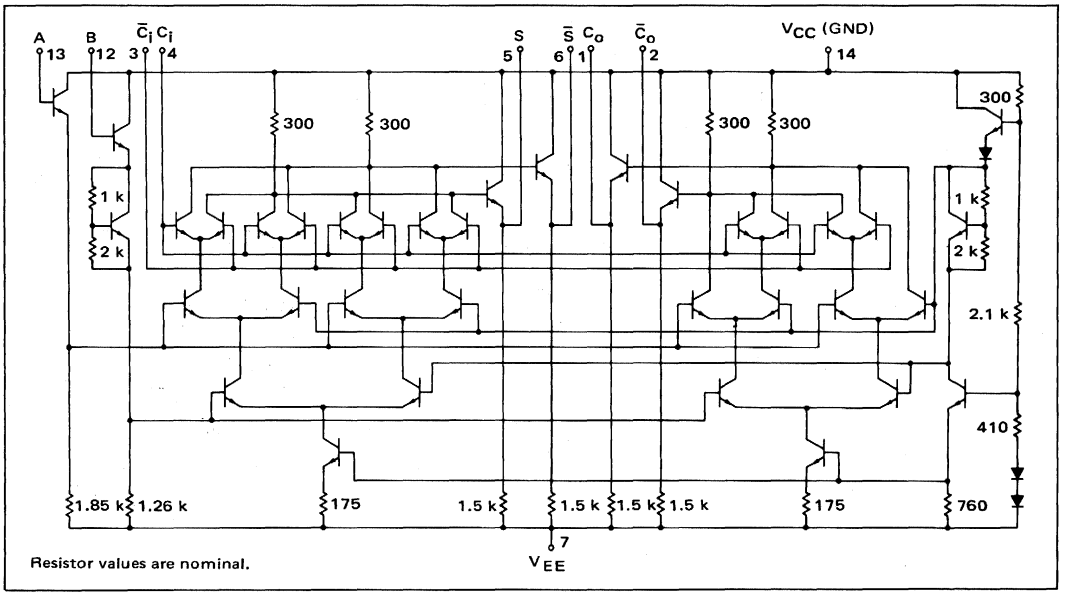
$\bar{C}_o = \bar{A}\bar{B}\bar{C}_i + A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i$

DC Input Loading Factor: A, B = 1
C_l, $\overline{C}_l$ = 2

DC Output Loading Factor = 25

Power Dissipation = 110 mW typical

CIRCUIT SCHEMATIC

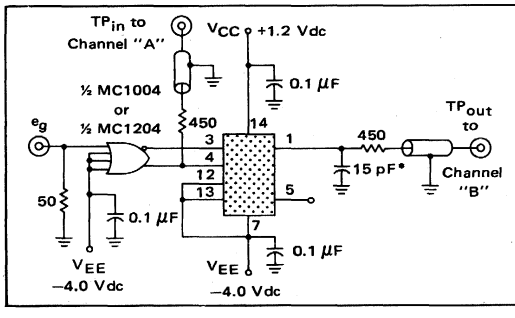


Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1219 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1019 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
Input Current	$2\ I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2\ I_{in}$	4	-	-	-	200	-	-	↓	-	-	-	200	-	-	↓
	I_{in}	12	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
	I_{in}	13	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"SUM" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"SUM" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"CARRY" Logical "1" Output Voltage ‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"CARRY" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Addend Input Propagation Delay	t_{12-5+}	5	8.0	13.0	8.0	13.0	8.0	13.0	ns	8.0	13.0	8.0	13.0	8.0	13.0	ns
	t_{12+5-}	5	7.0	11.5	↓	12.0	10.0	16.0	↓	↓	12.0	↓	12.0	9.0	14.0	↓
	t_{12+1+}	1	8.0	12.0	↓	12.0	11.0	17.0	↓	↓	12.0	↓	12.0	↓	14.0	↓
	t_{12-1-}	1	9.0	14.5	9.0	14.5	10.0	15.0	↓	9.0	14.5	9.0	14.5	↓	14.5	↓
Rise Time	t_{5+}	5	8.0	13.0	9.0	14.0	9.0	14.0	↓	9.0	14.0	9.0	14.0	↓	14.0	↓
	t_{1+}	1	5.0	8.5	5.0	8.5	8.0	12.0	↓	5.0	8.5	5.0	8.5	7.0	10.0	↓
Fall Time	t_{5-}	5	↓	8.0	↓	8.5	7.0	11.5	↓	↓	8.5	↓	8.5	6.0	9.5	↓
	t_{1-}	1	↓	8.0	↓	8.0	7.0	10.0	↓	↓	8.0	↓	8.0	6.0	9.0	↓
Augend Input Propagation Delay	t_{13+5-}	5	6.0	8.5	6.0	8.5	7.0	10.5	ns	6.0	8.5	6.0	8.5	6.0	9.5	ns
	t_{13-5+}	↓	5.0	8.5	5.0	8.5	↓	11.0	↓	5.0	8.5	5.0	8.5	↓	9.0	↓
Rise Time	t_{5+}	↓	↓	↓	6.0	9.0	↓	11.0	↓	6.0	9.0	6.0	9.0	↓	9.5	↓
Fall Time	t_{5-}	↓	↓	↓	5.0	8.5	↓	11.0	↓	5.0	8.5	5.0	8.5	↓	9.5	↓
Carry Input Propagation Delay	t_{4-5+}	5	3.0	5.0	3.0	5.0	3.0	5.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}	↓	4.0	7.5	4.0	7.5	6.0	10.0	↓	4.0	7.5	4.0	7.5	5.0	8.5	↓
Rise Time	t_{5+}	↓	5.0	8.0	6.0	8.5	7.0	10.5	↓	6.0	8.5	6.0	8.5	6.0	9.5	↓
Fall Time	t_{5-}	↓	5.0	8.0	5.0	8.5	7.0	11.0	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓

*Individually test each input using the pin connections shown. ‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA)



SWITCHING TIME TEST CIRCUIT @ 25°C

*Load corresponds to fan-out = 3.

Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input–output combinations specified may be tested similarly according to the full subtractor truth table.

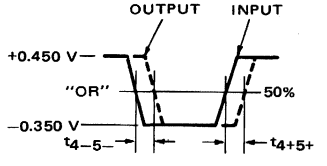
Input pulse t_r and t_f = 5.0 ± 0.5 ns

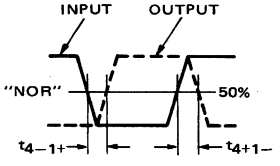
	@Test Temperature	TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	mAdc I_L
MC1219	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1019	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\,min}$ to $V_{IL\,max}$	$V_{IH\,min}$ to $V_{IH\,max}$	$V_{IH\,max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	3, 4, 7, 12, 13	-	14
Input Current	$2\,I_{in}$	3	4, 13	-	3, 12	7	-	14
	$2\,I_{in}$	4	3, 12	-	4, 13	↓	-	↓
	I_{in}	12	3, 13	-	4, 12		-	
	I_{in}	13	3, 12	-	4, 13		-	
Input Leakage Current	I_R	Inputs*	-	-		3, 4, 7, 12, 13	-	14
"SUM" Logical "1" Output Voltage‡	V_{OH}‡	5	3, 12, 13	4	-	7	5	14
		↓	4, 13	3, 12	-	↓	↓	↓
			4, 12	3, 13	-			
			3	4, 12, 13	-			
"SUM" Logical "0" Output Voltage	V_{OL}	5	4, 12, 13	3	-	7	-	14
		↓	3, 13	4, 12	-	↓	-	↓
			3, 12	4, 13	-		-	
			4	3, 12, 13	-		-	
"CARRY" Logical "1" Output Voltage ‡	V_{OH}‡	1	3, 13	4, 12	-	7	1	14
		↓	3, 12	4, 13	-	↓	↓	↓
			4	3, 12, 13	-			
			3	4, 12, 13	-			
"CARRY" Logical "0" Output Voltage	V_{OL}	1	4, 12, 13	3	-	7	-	14
		↓	3, 12, 13	4	-	↓	-	↓
			4, 13	3, 12	-		-	
			4, 12	3, 13	-		-	
Switching Times (Fan-out = 3)			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Addend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5	↓	5	-	↓	-	↓
	t_{12+1+}	1		1	-		-	
	t_{12-1-}	1		1	-		-	
Rise Time	t_{5+}	5		5	-		-	
	t_{1+}	1		1	-		-	
Fall Time	t_{5-}	5		5	-		-	
	t_{1-}	1	↓	1	-	↓	-	↓
Augend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓
Carry Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}	↓	↓	↓	-	↓	-	↓
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}	↓	↓	↓	-	↓	-	↓

SWITCHING TIME WAVEFORMS

PROPAGATION DELAY





RISE AND FALL TIMES

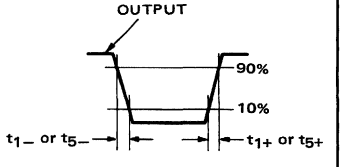
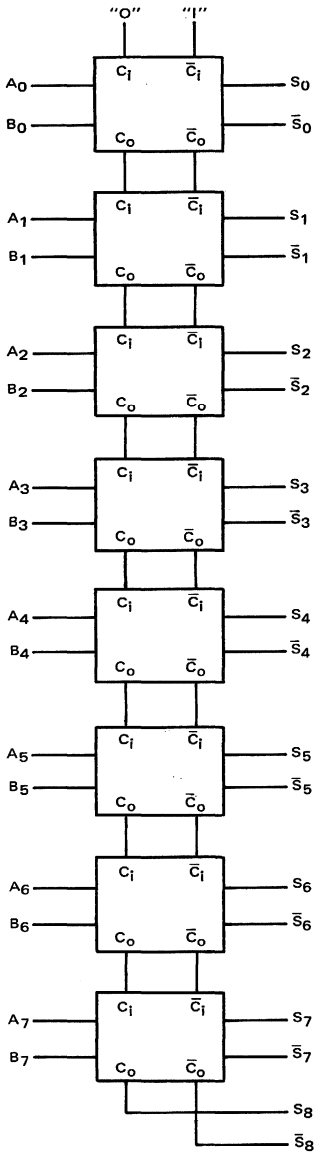


FIGURE 1 - 8 BIT
RIPPLE-THROUGH ADDER



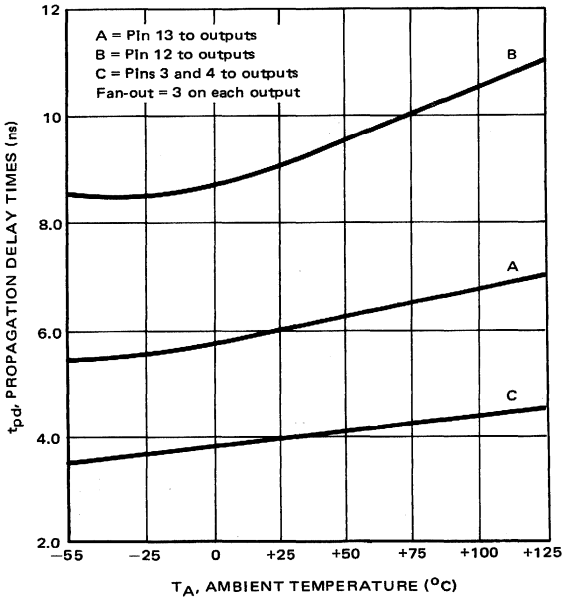
Total Add Time for 8 stage ripple through is typically 37 ns.

APPLICATIONS INFORMATION

The MC1019/MC1219 full adder exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Carry. This device permits practical ripple-through adders as shown in Figure 1, as well as ripple-through multipliers.

The schematic of the full adder illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The B input is translated negative two levels, to switch current between either the left or right branch of the tree. The A input is translated negative one level to switch current at the second level of branching. The Carry inputs switch current through the third level of branching. Depending upon the eight possible combinations of inputs, one specific branch in the Sum generating tree will be carrying current. Thus the proper output state is determined. The Carry generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the Inputs to outputs are shown in Figure 2.

FIGURE 2 - TYPICAL PROPAGATION DELAY TIMES

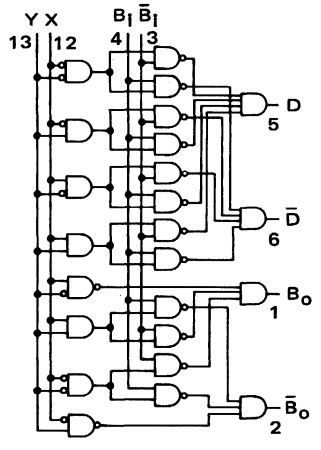


FULL SUBTRACTORS

MC1021
MC1221

Provides the DIFFERENCE, $\overline{\text{DIFFERENCE}}$, BORROW OUT, and $\overline{\text{BORROW OUT}}$ functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN and $\overline{\text{BORROW IN}}$.

POSITIVE LOGIC



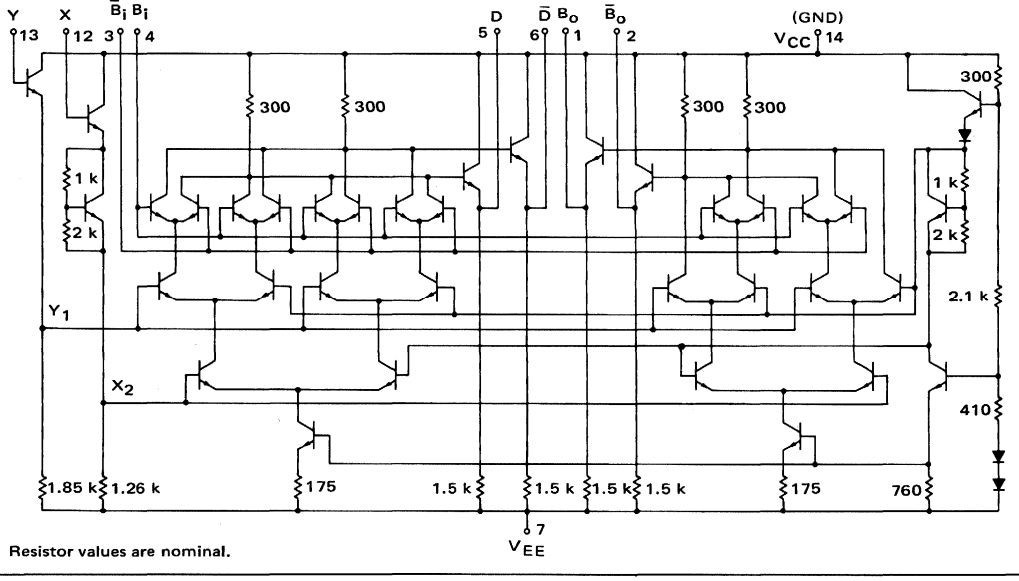
$$D = YXB_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$$
$$\bar{D} = \bar{Y}\bar{X}\bar{B}_i + YXB_i + Y\bar{X}B_i + \bar{Y}XB_i$$
$$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + Y\bar{X}B_i + YXB_i$$
$$\bar{B}_o = \bar{Y}\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}XB_i + YX\bar{B}_i$$

DC Input Loading Factor: X, Y = 1 B_i, $\bar{B}_i$ = 2
DC Output Loading Factor = 25
Power Dissipation = 110 mW typical

TRUTH TABLE

INPUT LOGIC LEVEL				OUTPUT LOGIC LEVEL			
X	Y	B_i	$\bar{B}_i$	D	$\bar{D}$	B_o	$\bar{B}_o$
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0

CIRCUIT SCHEMATIC



Resistor values are nominal.

ELECTRICAL CHARACTERISTICS

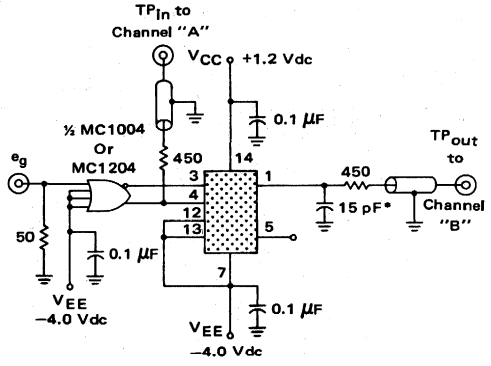
Characteristic	Symbol	Pin Under Test	MC1221 Test Limits							MC1021 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
Input Current	$2\ I_{in}$	3	-	-	-	200	-	-	μAdc	-	-	-	200	-	-	μAdc
	$2\ I_{in}$	4	-	-	-	200	-	-	↓	-	-	-	200	-	-	↓
	I_{in}	12	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
	I_{in}	13	-	-	-	100	-	-	↓	-	-	-	100	-	-	↓
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"DIFFERENCE" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"DIFFERENCE" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	↓	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	↓
"BORROW" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	↓	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	↓
"BORROW" Logical "0" Output Voltage	V_{OL}	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	↓	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	↓
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Minuend Input Propagation Delay	t_{12-5+}	5	9.0	14	8.0	13	9.0	14.5	ns	8.0	13	8.0	13	8.0	13	ns
	t_{12+5-}	5	8.0	13	8.0	13.5	11	17	↓	8.0	13.5	8.0	13.5	9.0	15	↓
	t_{12-1+}	1	↓	14	7.0	12.5	9.0	14.5	↓	7.0	12.5	7.0	12.5	8.0	13	↓
	t_{12+1-}	1	↓	13.5	8.0	13.5	11	17	↓	8.0	13.5	8.0	13.5	9.0	15	↓
Rise Time	t_{5+}	5	↓	13	9.0	14	10	14	↓	9.0	14	9.0	14	9.0	14	↓
	t_{1+}	1	↓	13	7.0	12	9.0	14	↓	7.0	12	7.0	12	8.0	13	↓
Fall Time	t_{5-}	5	5.0	8.0	5.0	8.5	7.0	11.5	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
	t_{1-}	1	5.0	8.0	5.0	8.0	7.0	11.0	↓	5.0	8.0	5.0	8.0	6.0	9.0	↓
Subtrahend Input Propagation Delay	t_{13+5-}	5	5.0	8.5	5.0	8.5	7.0	11	ns	5.0	8.5	5.0	8.5	6.0	9.5	ns
	t_{13-5+}	↓	6.0	9.0	5.0	8.5	7.0	11.5	↓	5.0	8.5	5.0	8.5	6.0	9.0	↓
Rise Time	t_{5+}	↓	5.0	8.5	6.0	9.0	8.0	11	↓	6.0	9.0	6.0	9.0	7.0	9.5	↓
Fall Time	t_{5-}	↓	5.0	8.5	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓
Borrow Input Propagation Delay	t_{4-5+}	5	3.0	5.5	3.0	5.0	4.0	6.0	ns	3.0	5.0	3.0	5.0	3.0	5.0	ns
	t_{4+5-}	↓	4.0	7.5	4.0	7.5	6.0	10	↓	4.0	7.5	4.0	7.5	5.0	8.5	↓
Rise Time	t_{5+}	↓	5.0	8.0	6.0	8.5	8.0	10.5	↓	6.0	8.5	6.0	8.5	7.0	10	↓
Fall Time	t_{5-}	↓	5.0	8.0	5.0	8.5	7.0	11	↓	5.0	8.5	5.0	8.5	6.0	9.5	↓

*Individually test each input using the pin connections shown.
‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

@Test Temperature		TEST VOLTAGE/CURRENT VALUES				
		Vdc ±1.0%				mAdc
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L
MC1221	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1021	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	3, 4, 7, 12, 13	-	14
Input Current	$2\ I_{in}$	3	4, 13		3, 12	7	-	14
	$2\ I_{in}$	4	3, 12		4, 13		-	
	I_{in}	12	3, 13		4, 12		-	
	I_{in}	13	3, 12		4, 13		-	
Input Leakage Current	I_R	Inputs*	-	-	-	3, 4, 7, 12, 13	-	14
"DIFFERENCE" Logical "1" Output Voltage‡	V_{OH}‡	5	3, 12, 13 4, 13 4, 12 3	4 3, 12 3, 13 4, 12, 13	-	7	5	14
"DIFFERENCE" Logical "0" Output Voltage	V_{OL}	5	4, 12, 13 3, 13 3, 12 4	3 4, 12 4, 13 3, 12, 13	-	7	-	14
"BORROW" Logical "1" Output Voltage‡	V_{OH}‡	1	3, 12, 13 3, 12 4, 12 3	4 4, 13 3, 13 4, 12, 13	-	7	1	14
"BORROW" Logical "0" Output Voltage	V_{OL}	1	4, 12, 13 4, 13 3, 13 4	3 3, 12 4, 12 3, 12, 13	-	7	-	14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		+1.2V
Minuend Input Propagation Delay	t_{12-5+}	5	12	5	-	7	-	14
	t_{12+5-}	5		5	-		-	
	t_{12-1+}	1		1	-		-	
	t_{12+1-}	1		1	-		-	
Rise Time	t_{5+}	5		5	-		-	
	t_{1+}	1		1	-		-	
Fall Time	t_{5-}	5		5	-		-	
	t_{1-}	1		1	-		-	
Subtrahend Input Propagation Delay	t_{13+5-}	5	13	5	-	7	-	14
	t_{13-5+}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	
Borrow Input Propagation Delay	t_{4-5+}	5	4	5	-	7	-	14
	t_{4+5-}				-		-	
Rise Time	t_{5+}				-		-	
Fall Time	t_{5-}				-		-	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

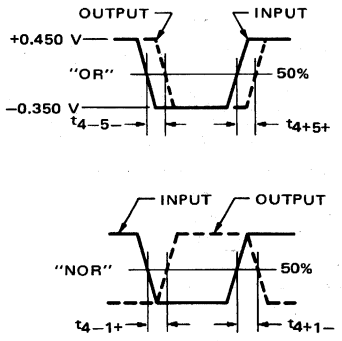


*Load corresponds to fan-out = 3

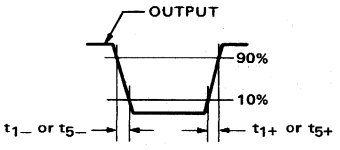
Switching test circuit is shown for pulse in on pin 4 and pulse out on pin 1, however all other input-output combinations specified may be tested simularly according to the full adder truth table.

Input pulse t_r and t_f = 5.0 ± 0.5 ns.

PROPAGATION DELAY



RISE AND FALL TIME

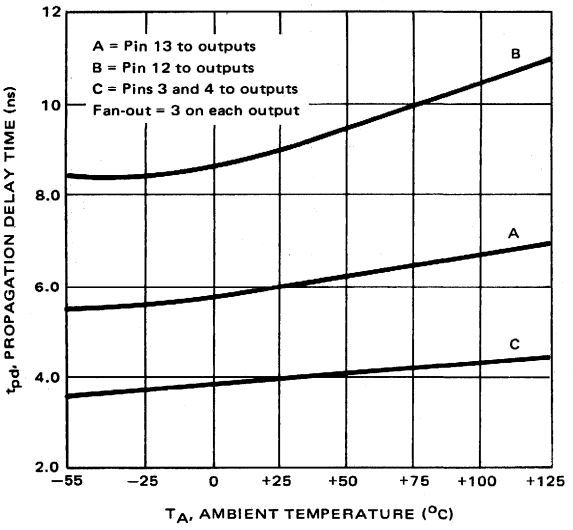


APPLICATIONS INFORMATION

The MC1021/MC1221 full subtractor is identical to the full adder except for the interconnection metalization. It exhibits an average propagation delay time of 5.0 ns per stage in a system employing ripple Borrow. This device permits building of ripple-through dividers.

The schematic of the full subtractor illustrates the techniques employed to obtain the necessary logic equations. A compensated current source drives a transistor "tree" with three levels of branching. The X input is translated negative two levels, to switch current between either the left or right branch of the tree. The Y input is translated negative one level to switch current at the second level of branching. Depending upon the eight possible combinations of inputs, one specific branch level in the Difference generating tree will be carrying current. Thus the proper output state is determined. The Borrow generating tree operates in the same manner. This series gating technique results in the best speed-power product obtainable with bipolar technology. Typical propagation delay times from the inputs to outputs are shown.

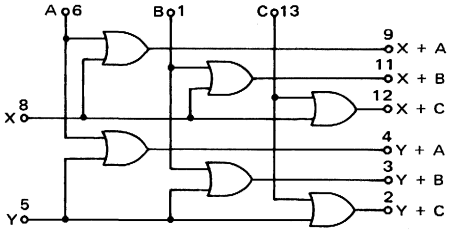
TYPICAL PROPAGATION DELAY TIMES



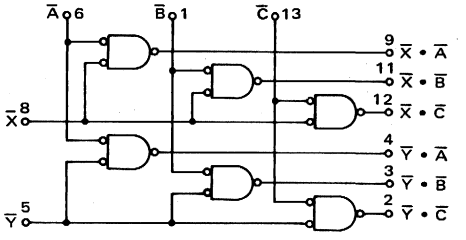
MC1029
MC1229

A 2 X 3 array of 2-input OR gates, designed primarily for the handling of data in a digital system.

POSITIVE LOGIC



NEGATIVE LOGIC

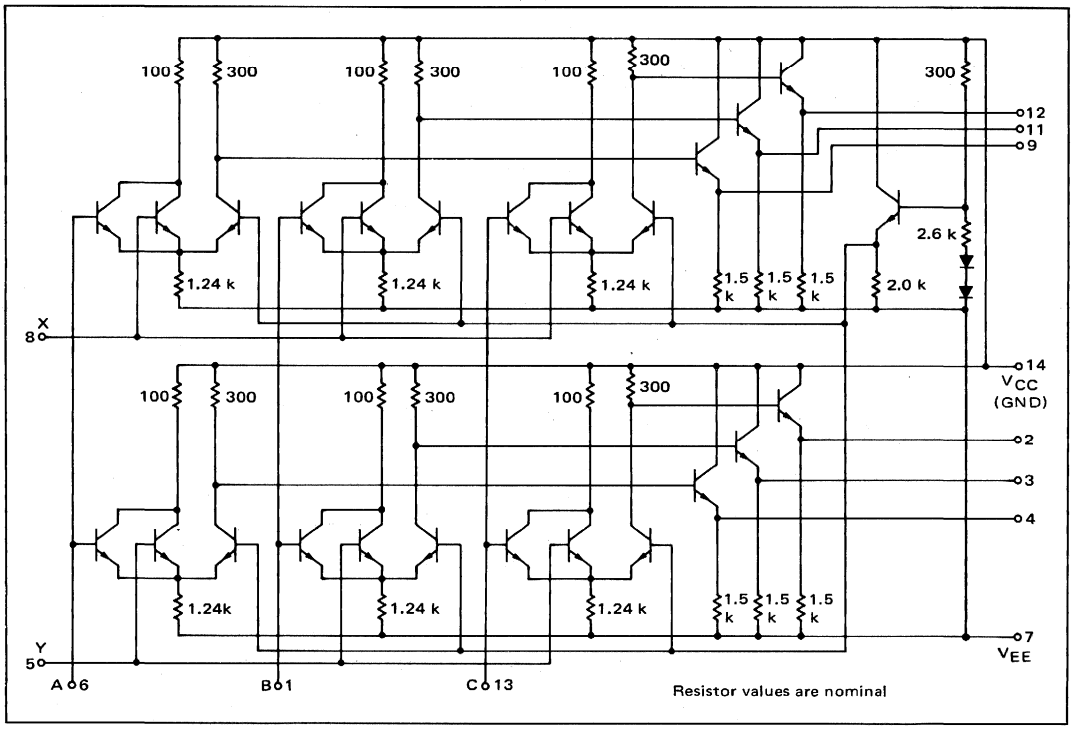


DC Input Loading Factors: X, Y = 3; A, B, C = 2
DC Output Loading Factor = 25
Power Dissipation = 160 mW typical

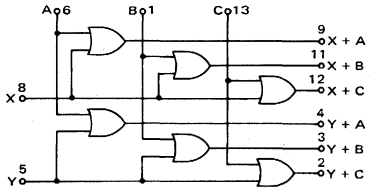
TRUTH TABLE (POSITIVE LOGIC)

					PIN NUMBER					
X	Y	A	B	C	9	11	12	4	3	2
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	0	0
0	1	0	0	0	0	0	0	1	1	1
1	0	0	0	0	1	1	1	0	0	0

CIRCUIT SCHEMATIC



Resistor values are nominal

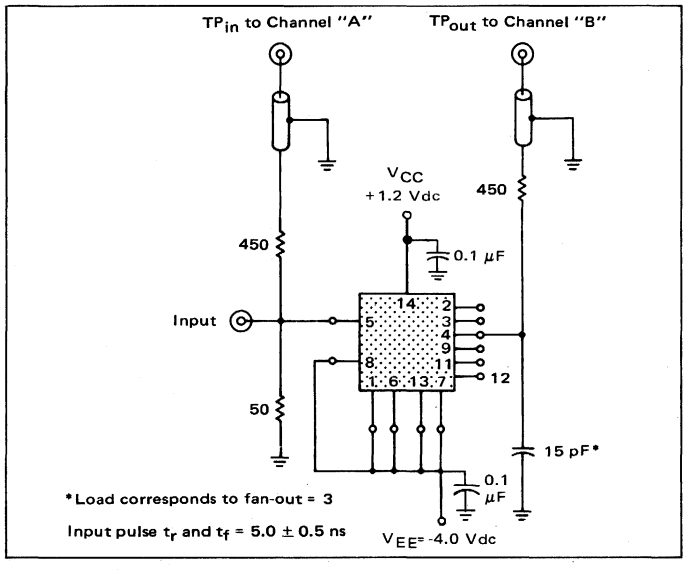


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1229 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1029 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	45	-	-	mAdc
Input Current	I_{in}	5	-	-	-	300	-	-	μAdc	-	-	-	300	-	-	μAdc
		8	-	-	-	300	-	-		-	-	-	300	-	-	
		1	-	-	-	200	-	-		-	-	-	200	-	-	
		6	-	-	-	200	-	-		-	-	-	200	-	-	
		13	-	-	-	200	-	-		-	-	-	200	-	-	
Input Leakage Current	I_R	5, 8*	-	-	-	0.6	-	3.0	μAdc	-	-	-	0.6	-	3.0	μAdc
		1, 6, 13*	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
Logical "1" Output Voltage	V_{OH}‡	3, 11† 4, 9† 2, 12† 2, 3, 4† 9, 11, 12†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
Logical "0" Output Voltage	V_{OL}	3, 11† 4, 9† 2, 12† 2, 3, 4† 9, 11, 12†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{5+4+}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.0	ns
	t_{5-4-}		4.0	7.5	4.0	7.5	6.0	9.0		4.0	7.5	4.0	7.5	5.0	8.0	
Rise Time	t_{4+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{4-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	
Propagation Delay	t_{1+3+}	3	4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.0	
	t_{1-3-}		4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.0	
Rise Time	t_{3+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{3-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	

* Individually test each input using the pin connections shown. † Individually test each output using the pin connections shown.

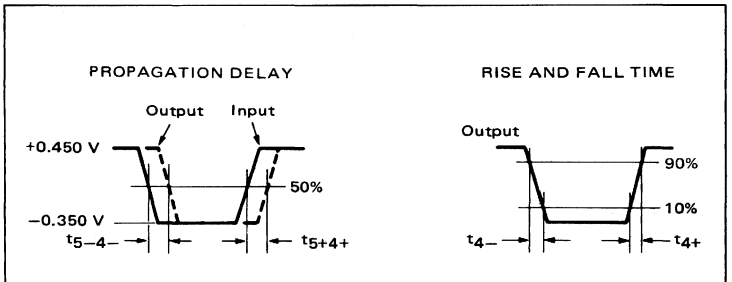
SWITCHING TIME TEST CIRCUIT @ 25°C



@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1229	−55°C	-1.580	-0.990	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+125°C	-1.380	-0.700	-	-5.2	-2.5
MC1029	0°C	-1.525	-0.895	-	-5.2	-2.5
	+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
	+75°C	-1.435	-0.775	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 5, 6, 7, 8, 13	-	14
Input Current	I_{in}	5	-	-	5	1, 6, 7, 8, 13	-	14
		8	-	-	8	1, 5, 6, 7, 13	-	↓
		1	-	-	1	5, 6, 7, 8, 13	-	
		6	-	-	6	1, 5, 7, 8, 13	-	
		13	-	-	13	1, 5, 6, 7, 8	-	
Input Leakage Current	I_R	5, 8*	-	-	-	1, 5, 6, 7, 8, 13	-	14
		1, 6, 13*	-	-	-	1, 5, 6, 7, 8, 13	-	14
Logical "1" Output Voltage	V_{OH}‡	3, 11†	-	1	-	5, 6, 7, 8, 13	‡	14
		4, 9†	-	6	-	1, 5, 7, 8, 13	↓	↓
		2, 12†	-	13	-	1, 5, 6, 7, 8		
		2, 3, 4†	-	5	-	1, 6, 7, 8, 13		
		9, 11, 12†	-	8	-	1, 5, 6, 7, 13	↓	↓
Logical "0" Output Voltage	V_{OL}	3, 11†	1	-	-	5, 6, 7, 8, 13	-	14
		4, 9†	6	-	-	1, 5, 7, 8, 13	-	↓
		2, 12†	13	-	-	1, 5, 6, 7, 8	-	
		2, 3, 4†	5	-	-	1, 6, 7, 8, 13	-	
		9, 11, 12†	8	-	-	1, 5, 6, 7, 13	↓	↓
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay	t_{5+4+}	4	5	4	-	1, 6, 7, 8, 13	-	14
	t_{5-4-}	↓	↓	↓		↓		↓
Rise Time	t_{4+}							
Fall Time	t_{4-}	↓	↓	↓		↓		
Propagation Delay	t_{1+3+}	3	1	3	-	5, 6, 7, 8, 13	-	
	t_{1-3-}	↓	↓	↓		↓		
Rise Time	t_{3+}							
Fall Time	t_{3-}	↓	↓	↓		↓		↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.



SWITCHING TIME WAVEFORMS

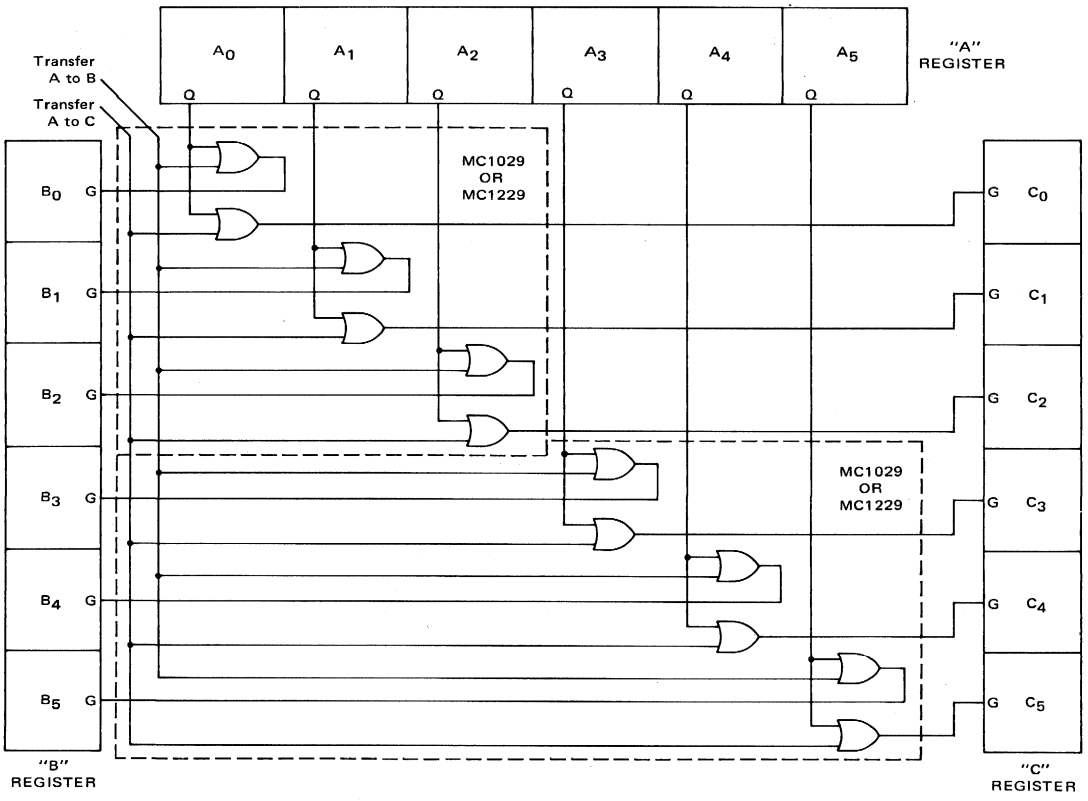
Test circuit and waveforms show input pulse on pin 5 and output pulse on pin 4, however, all other input-output combinations tested in a similar manner will meet limits specified.

APPLICATIONS INFORMATION

The MC1029/MC1229 data distributor is a 2 X 3 array of 2-input OR gates, as shown in the logic diagram. Inputs X and Y may be used as control inputs to transfer the data on inputs A, B, and C, to the outputs on pins 9, 11, and 12, or to the outputs on pins 4, 3, and 2. Also, if it is desired to distribute data to three destinations, inputs X and Y may be used for data and A, B, and C as control inputs. The data distributor utilizes negative logic; i.e., the positive OR function becomes the negative AND. Data is transferred for a low level on the control inputs.

The data distributor is an example of the manner in which part of a logic system may be partitioned to reduce wiring and package count. Figure 1 illustrates the logic required for the transfer of data from "A" register to "B" register gating or to "C" register gating. Six stages per register are shown in the figure but arrays of any desired length may be built. The typical propagation delay of the data distributor in a system is 5.0 ns, permitting the rapid transfer of data through distribution gating. If data distribution is done on a double-rail basis instead of single-rail as shown, then twice the number of data distributors are required.

FIGURE 1 – REGISTER DATA TRANSFER



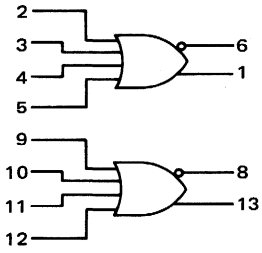
DUAL 4-INPUT
CLOCK DRIVER

MC1023

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

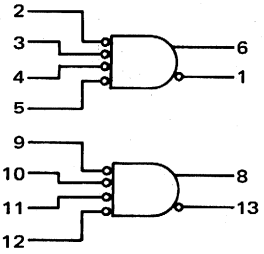
This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.

POSITIVE LOGIC



$6 = \overline{2 + 2 + 4 + 5}$
$1 = 2 + 3 + 4 + 5$

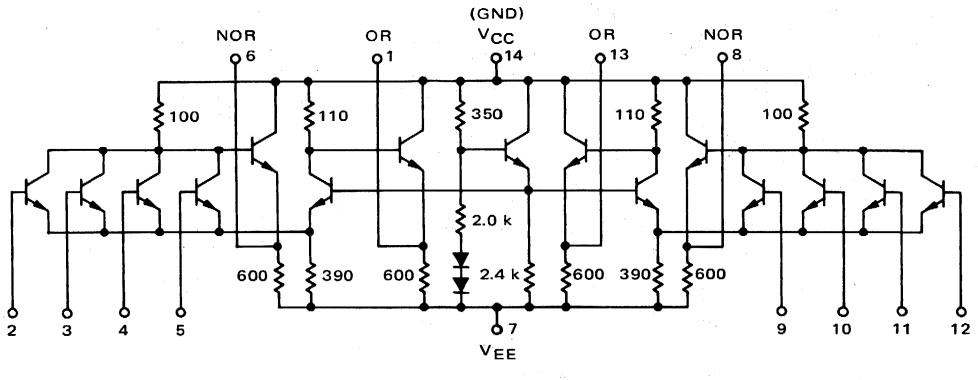
NEGATIVE LOGIC



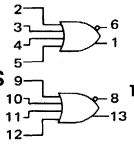
$6 = \overline{2 \bullet 3 \bullet 4 \bullet 5}$
$1 = 2 \bullet 3 \bullet 4 \bullet 5$

DC Input Loading Factor = 3
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal.



ELECTRICAL CHARACTERISTICS

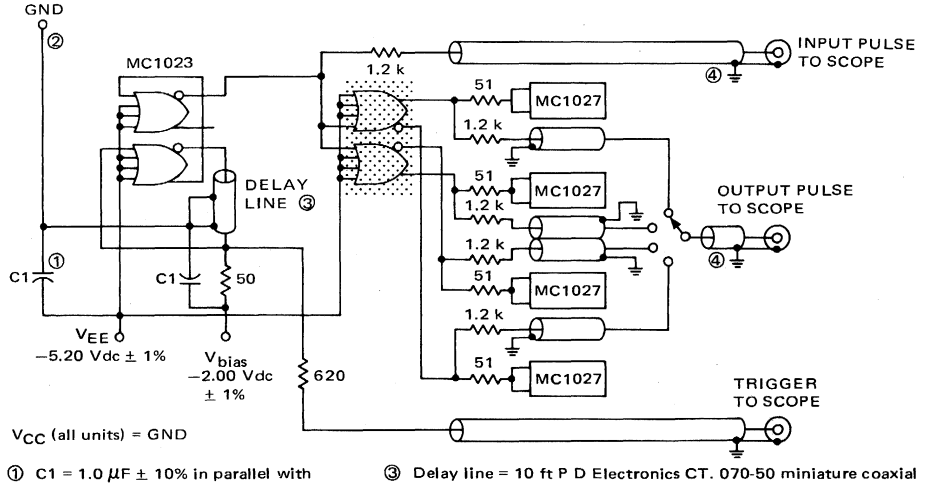
Test is shown for only one gate. The other gate is tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES				
	Vdc ±1.0%				mAdc
	$V_{OL\ max}$	$V_{OH\ min}$	$V_{OH\ max}$	V_{EE}	I_L
0°C	-1.530	-0.930	-0.750	-5.2	-2.5
+25°C	-1.500	-0.850	-0.700	-5.2	-2.5
+75°C	-1.440	-0.790	-0.635	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	MC1023P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{OL\ max}$	$V_{OH\ min}$	$V_{OH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	61	-	-	mAdc	-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
Input Current	I_{in}	2	-	-	-	300	-	-	μAdc	-	-	2	3, 4, 5, 7, 9, 10, 11, 12	-	14
		3	-	-	-	↓	-	-	↓	-	-	3	2, 4, 5, 7, 9, 10, 11, 12	-	↓
		4	-	-	-		-	-		-	-	4	2, 3, 5, 7, 9, 10, 11, 12	-	
		5	-	-	-		-	-		-	-	5	2, 3, 4, 7, 9, 10, 11, 12	-	
Input Leakage Current	I_R	2	-	-	-	1.0	-	5.0	μAdc	-	-	-	2, 3, 4, 5, 7, 9, 10, 11, 12	-	14
		3	-	-	-	↓	-	↓	↓	-	-	-		-	↓
		4	-	-	-		-			-	-	-		-	
		5	-	-	-		-			-	-	-		-	
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc	2	-	-	3, 4, 5, 7, 9, 10, 11, 12	6	14
			↓	↓	↓	↓	↓	↓	↓	3	-	-	2, 4, 5, 7, 9, 10, 11, 12	↓	↓
										4	-	-	2, 3, 5, 7, 9, 10, 11, 12		
										5	-	-	2, 3, 4, 7, 9, 10, 11, 12		
"NOR" Logical "0" Output Voltage	V_{OL}	6	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc	-	2	-	3, 4, 5, 7, 9, 10, 11, 12	-	14
			↓	↓	↓	↓	↓	↓	↓	-	3	-	2, 4, 5, 7, 9, 10, 11, 12	-	↓
										-	4	-	2, 3, 5, 7, 9, 10, 11, 12	-	
										-	5	-	2, 3, 4, 7, 9, 10, 11, 12	-	
"OR" Logical "1" Output Voltage‡	V_{OH}‡	1	-0.930	-0.750	-0.850	-0.700	-0.790	-0.635	Vdc	-	2	-	3, 4, 5, 7, 9, 10, 11, 12	6	14
			↓	↓	↓	↓	↓	↓	↓	-	3	-	2, 4, 5, 7, 9, 10, 11, 12	↓	↓
										-	4	-	2, 3, 5, 7, 9, 10, 11, 12		
										-	5	-	2, 3, 4, 7, 9, 10, 11, 12		
"OR" Logical "0" Output Voltage	V_{OL}	1	-2.050	-1.530	-2.000	-1.500	-1.940	-1.440	Vdc	2	-	-	3, 4, 5, 7, 9, 10, 11, 12	-	14
			↓	↓	↓	↓	↓	↓	↓	3	-	-	2, 4, 5, 7, 9, 10, 11, 12	-	↓
										4	-	-	2, 3, 5, 7, 9, 10, 11, 12	-	
										5	-	-	2, 3, 4, 7, 9, 10, 11, 12	-	
Switching Times Propagation Delay			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out				
(Fan-Out = 2)*	t_{5+6-}	6	2.0	3.5	2.0	3.5	3.0	4.5	ns	5	6	-	2, 3, 4, 7, 9, 10, 11, 12	-	14
	t_{5-6+}	6	2.0	3.0	2.0	3.0	3.0	4.0			6	-		-	
	t_{5+1+}	1	2.0	3.0	2.0	3.0	3.0	4.0			1	-		-	
	t_{5-1-}	1	2.0	3.5	2.0	3.5	3.0	4.5			1	-		-	
(Fan-Out = 10)*	t_{5+6-}	6	2.5	3.5	2.5	3.5	3.0	5.0			6	-		-	
	t_{5-6+}	6	2.0	3.5	2.0	3.5	3.0	5.0			6	-		-	
	t_{5+1+}	1	2.0	3.5	2.0	3.5	3.0	5.0			1	-		-	
	t_{5-1-}	1	2.5	3.5	2.5	3.5	3.0	5.0			1	-		-	
Rise Time (Fan-Out = 2)*	t_{6+}	6	2.0	4.0	2.0	4.0	3.5	5.0			6	-		-	
	t_{1+}	1	2.0	4.0	2.0	4.0	3.5	5.0			1	-		-	
(Fan-Out = 10)*	t_{6+}	6	3.0	5.5	3.0	5.5	5.0	7.5			6	-		-	
	t_{1+}	1	3.0	5.5	3.0	5.5	5.0	7.5			1	-		-	
Fall Time (Fan-Out = 2)*	t_{6-}	6	2.0	4.5	2.0	4.5	3.0	5.5			6	-		-	
	t_{1-}	1	2.0	4.5	2.0	4.5	3.0	5.5			1	-		-	
(Fan-Out = 10)*	t_{6-}	6	3.0	5.5	3.0	5.5	5.0	7.5			6	-		-	
	t_{1-}	1	3.0	5.5	3.0	5.5	5.0	7.5	↓	↓	1	-	↓	-	↓

‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). * A fan-out is defined as one $\overline{J}$ or $\overline{K}$ input.

SWITCHING TIME TEST CIRCUIT

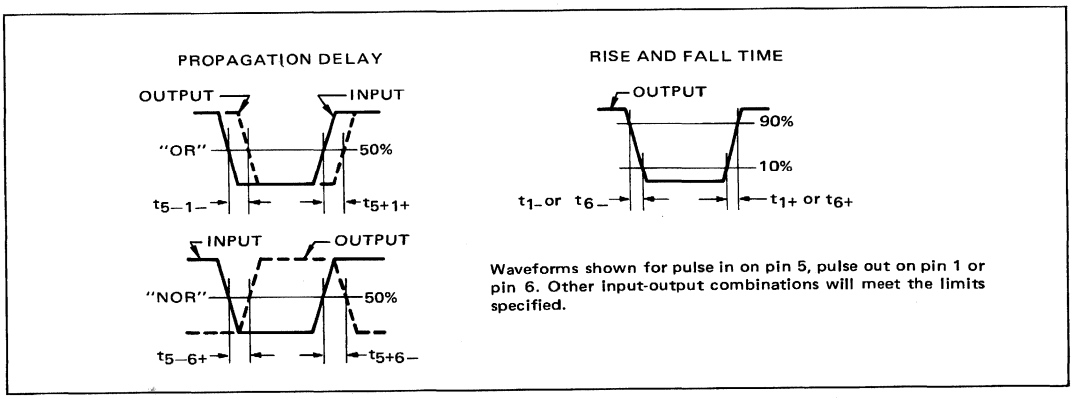


① C1 = 1.0 μF ± 10% in parallel with 0.001 μF ± 10%

② All leads to ground as short as possible

③ Delay line = 10 ft P D Electronics CT. 070-50 miniature coaxial cable or equivalent. Other internal fixture cables are same type.

④ All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Plug directly into 50-ohm input of scope.



Waveforms shown for pulse in on pin 5, pulse out on pin 1 or pin 6. Other input-output combinations will meet the limits specified.

APPLICATIONS INFORMATION

The MC1023 is a dual high-speed gate designed for use as a clock driver which allows the MECL II flip-flops to operate at their full speed capability. More advanced processing techniques than those used on standard MECL II are employed for the clock driver, resulting in an improved speed-power product. The dual gate exhibits typical propagation delay times of 2.0 ns. Due to this short propagation delay, the gate makes an ideal clock driver for long shift registers where the clock pulse may be distributed with minimal skew time over the entire register length.

Since rise and fall times may be as fast as 1.0 ns under light loading, the following precautions must be taken during layout. The MC1023 will not drive back-plane point-to-point wiring satisfactorily. Due to the fast logic transitions a maximum length of three inches for point-to-point wiring is recommended. Lower impedance printed wires allow longer line lengths. Due to the low output impedance (5.0 ohms) of the MC1023, additional terminating resistance to −5.2 V may be employed. This reduces fall time for capacitive loads and propagation delay to negative-going outputs. Figure 1 shows typical curves for output voltage versus load current. Figures 2 through 7 show curves for rise, fall, and propagation delay times versus loading for a typical gate. Capacitance of 5.0 pF per fan-out was used during the tests. This is conservative, since stray and input capacitance is closer to 4.0 pF per fan-out when driving flip-flops in high-speed designs.

The MC1023 is also very useful for providing the additional levels of gating required for some counting configurations such as divide-by-seven and divide-by-thirteen counters. The maximum frequency of operation of such a counter depends upon the flip-flop and gating delay which determines the minimum "up time" of the clock waveforms. Due to its short propagation delay the MC1023 when used with an MC1027 allows a divide-by-seven counter to operate up to 100 MHz.

Due to the 5.0-ohm output impedance the clock driver will also drive low impedance lines. When driving a 50-ohm termination to −2.0 V the output "1" level will be reduced by a maximum of 0.100 V. The minimum "1" level is approximately −0.950 V with a load current of 21 mA, reducing voltage noise immunity by 0.100 V. Noise power or energy noise immunity is still good due to the very low gate output impedance and low line impedance.

Two additional applications of the MC1023 are shown in Figures 8 and 9.

FIGURE 1 - TYPICAL OUTPUT CHARACTERISTICS

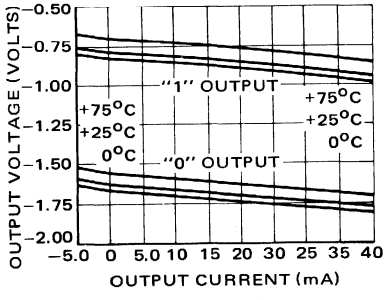


FIGURE 2 - RISE TIME

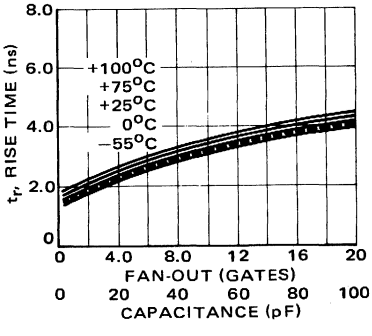
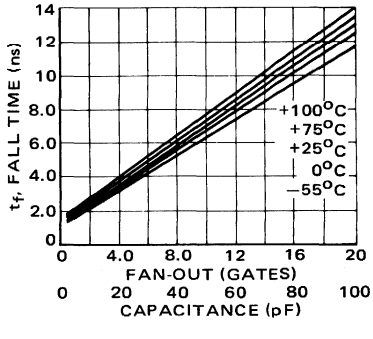


FIGURE 3 - FALL TIME



APPLICATIONS INFORMATION (continued)

FIGURE 4 - t_{pd+-}

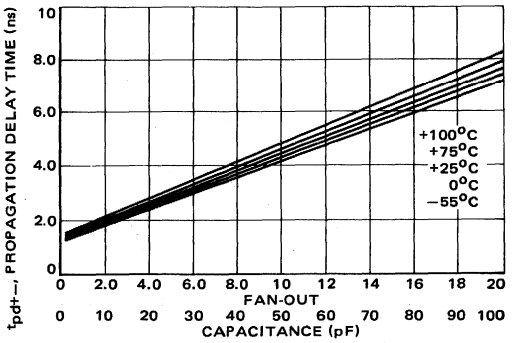


FIGURE 5 - t_{pd-+}

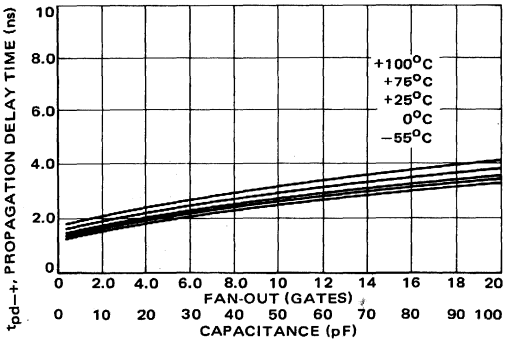


FIGURE 6 - t_{pd++}

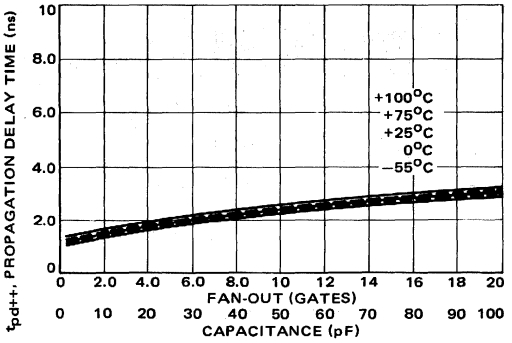


FIGURE 7 - t_{pd--}

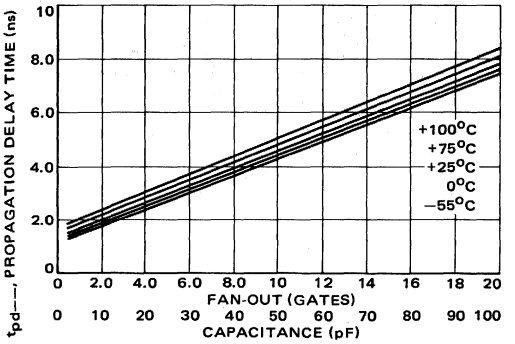
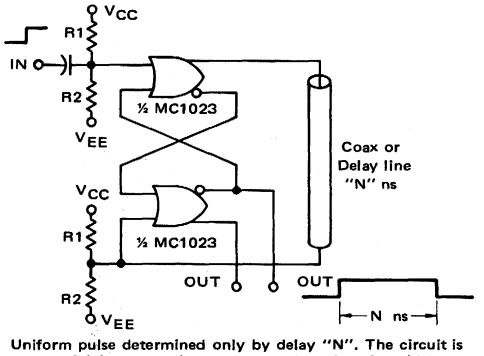


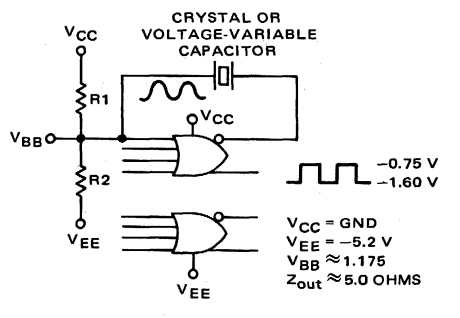
FIGURE 8 - MC1023 AS A ONE SHOT AND CLOCK SHAPER



Uniform pulse determined only by delay "N". The circuit is very useful for generating accurate and stable pulse widths or reshaping clock pulse width. Pulse widths down to 3.0 ns are obtainable.

Circuit courtesy of Mr. O. Gene Gabbard, Member of Technical staff, Communications Satellite Corporation.

FIGURE 9 - MC1023 AS A CRYSTAL OSCILLATOR



Power Dissipation = ¼ Watt
The Gate is Useful to 150+ MHz

For specific frequencies of operation, the crystal feedback may be obtained from the OR output. For further information see Application Note AN-417.

MHTL

INTEGRATED CIRCUITS
MC660 SERIES

MHTL

INTEGRATED CIRCUITS

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NUMERICAL INDEX
(Functions and Characteristics)

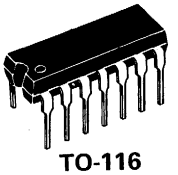
V_{CC} = 15 V ±1.0 V, T_A = 25°C, Case 93

Function	Type -30 to + 75°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
Expandable Dual 4-Input NAND Gate (active pullup)	MC660P	10	110	88/26 ①	3-8
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661P	10	125	88/26 ①	3-10
Expandable Dual 4-Input Line Driver	MC662P	30	140	180/26 ①	3-20
Dual J-K Flip-Flop	MC663P	9	–	200	3-22
Master-Slave R-S Flip-Flop	MC664P	8	–	160	3-24
Quad 2-Input NAND Gate (passive pullup)	MC668P	10	125	176/52 ①	3-16
Dual 4-Input Expander	MC669P	–	–	–	3-26
Triple 3-Input NAND Gate (passive pullup)	MC670P	10	125	132/39 ①	3-12
Triple 3-Input NAND Gate (active pullup)	MC671P	10	110	132/39 ①	3-14
Quad 2-Input NAND Gate (active pullup)	MC672P	10	110	176/52 ①	3-18

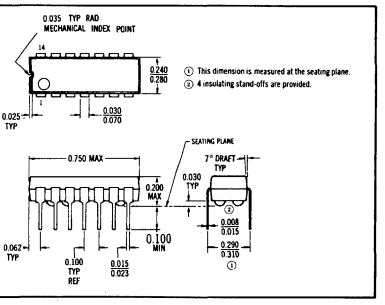
① Input High/Inputs Low

UNIBLOC* PLASTIC PACKAGE CASE 93

*Trademark of Motorola Inc.



TO-116



MAXIMUM RATINGS $T_A = 25^oC$

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, < 1.0 s	V_{CC}	 18 20	Vdc
Input Voltage (MC669P Expanders Reverse Voltage)	V_{in}	−1.0/+18 18	Vdc
Output Current (into outputs) MC660, 661, 670, 671, 668, 672 MC662 MC663 MC664 MC669	−	 30 60 28 26 −	mAdc
Input Reverse Current @ 20 V	I_R	0.5	mAdc
Forward Current (individual) MC669P	I_F	30	mAdc
Operating Temperature Range	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

TEST LIMITS TOLERANCE

$T_A = \pm 3^oC$ $V_R = \pm 1\%$ $V_{CC} = \pm 1\%$ $V_{IL} = \pm 1\%$ $V_{IH} = \pm 1\%$ $V_F = \pm 1\%$ $I_{OL} = \pm 1\%$ $I_{OH} = \pm 1\%$

DEFINITIONS

CP Clock Pulse

I_{CEX} Collector-to-emitter leakage of the output transistor

I_{CCH} V_{CC} current drain when all inputs are high

I_{CCL} V_{CC} current drain when all inputs are low

I_F Forward current of input diodes for unit input load

$2\,I_F$ Forward current of input diodes which are equal to twice unit load

I_{OH} Test current flowing into the output pin when output is high. (Negative)

I_{OL} Test current flowing into output pin when output is low

I_R Reverse current of input diodes with V_R applied

$2\,I_R$ Reverse current of two input diodes with V_R applied

I_{SC} Short-circuit current obtained from device output when output is high

t_{pd+} Propagation delay time for a positive-going output pulse

t_{pd-} Propagation delay time for a negative-going output pulse

V_{CC} Device power supply voltage

V_{CCH} High power supply voltage

V_{CCL} Low power supply voltage

V_{CEX} Collector-to-emitter voltage of the output transistor

V_F Input voltage when measuring I_F

V_{IH} Threshold voltage for high input voltage state

V_{IL} Threshold voltage for low input voltage state

V_{OH} Output high voltage state with I_{OH} flowing out of pin

V_{OL} Output low voltage state with I_{OL} flowing into pin

V_R Reverse voltage for input diode leakage test

V_X Threshold voltage for low input voltage state on expander unit

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- The outputs of the passive pullup gates may be tied together to perform the wired-collector OR function. For each added gate subtract 1.2 output loading factor (fan-out).
- The outputs of the active pullup devices should not be tied together.

HIGH THRESHOLD LOGIC

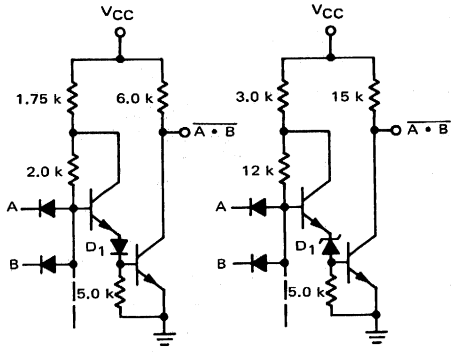
The High Threshold Logic (MHTL) family of integrated circuit devices was developed for applications requiring a higher degree of inherent electrical noise immunity than is available with the more standard forms of integrated circuit logic families. The basic MHTL logic gate is similar to the Diode Transistor Logic (MDTL) gate circuit as can be seen in Figure 1. A considerably larger input threshold characteristic is exhibited by the MHTL devices by using a reversed biased base-emitter junction which operates in the breakdown avalanche mode (sometimes referred to as zener operation) as compared to a forward biased diode junction for the corresponding D_1 element in the MDTL gate. A typical 7.5 volt input signal is required to turn on the MHTL output inverting transistor while a 1.5 volt signal is necessary for MDTL.

The higher threshold characteristic of MHTL requires a higher V_{CC} supply and is specified at 15 volts ±1.0 V tolerance. In order to keep the power dissipation within reasonable levels, higher values of resistance are used in MHTL than for corresponding resistors in the MDTL circuit. These resistance values also allow the outputs of gates to be interconnected to provide the "wired - or" logic function. The propagation delay of MHTL is in the order of 110 nanoseconds and consequently is a relatively slow logic family, a property which aids in rejecting noise. A comparison of transfer curves is made in Figure 2 illustrating the large logic swing available from MHTL.

An active output pullup configuration is available for the MHTL devices and is shown in Figure 3. The active output arrangement will allow the circuits to handle capacitive loads at a higher speed than is obtainable with the passive pullup configuration. Additionally, the impedance in the high state is considerably less, and consequently makes the family more immune to electrical noise. The active output configuration also allows for a more powerful arrangement to interface with discrete components.

In summary the MHTL devices may be characterized as an integrated circuit family with a high degree of inherent noise immunity, a high input threshold and a large logic swing. These characteristics make the line very attractive for use where electrical noise is an important consideration, as well as for applications where interfacing with various discrete components is required.

FIGURE 1–GATE COMPARISONS



MODIFIED DIODE-TRANSISTOR LOGIC

HIGH THRESHOLD LOGIC WITH PASSIVE PULLUP

FIGURE 2–TRANSFER CURVES

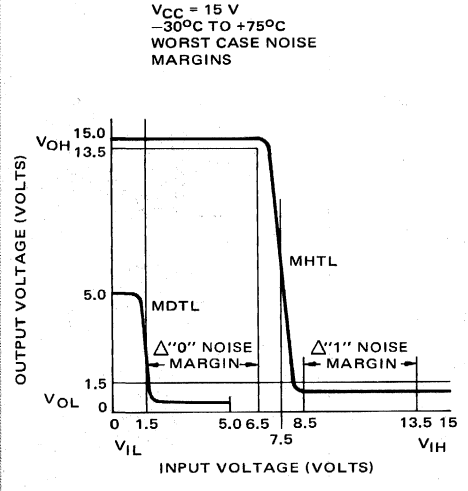
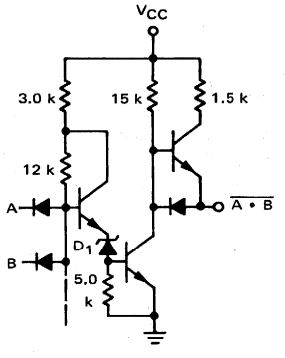
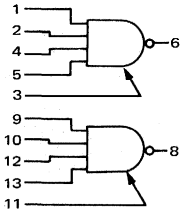


FIGURE 3–MHTL GATE WITH ACTIVE PULLUP



The logic diagrams shown describe the circuits of the MHTL line and permit quick selection of circuits required to implement a particular logic system. Pertinent information, such as logic equations and truth tables is provided to show line compatability. Package pin numbers and loading factors for each device are specified with each logic diagram. The numbers at the ends of the terminals are package pin numbers.

MC660P
EXPANDABLE DUAL 4-INPUT GATE
(with active output pullup)

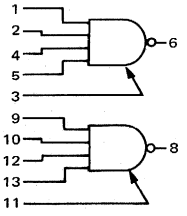


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC661P
EXPANDABLE DUAL 4-INPUT GATE
(with passive output pullup)

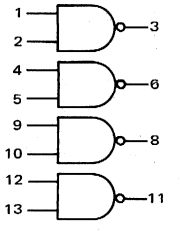


Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 88 mW
Inputs Low - 26 mW

MC668P
QUAD 2-INPUT GATE
(with passive output pullup)

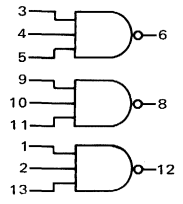


Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

MC670P
TRIPLE 3-INPUT GATE
(with passive output pullup)

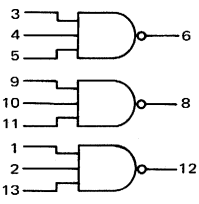


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC671P
TRIPLE 3-INPUT GATE
(with active output pullup)

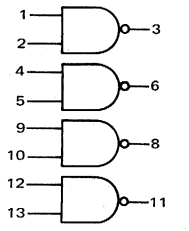


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 132 mW
Inputs Low - 39 mW

MC672P
QUAD 2-INPUT GATE
(with active output pullup)



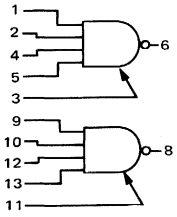
Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High - 176 mW
Inputs Low - 52 mW

LOGIC DIAGRAMS (continued)

MC662P
EXPANDABLE DUAL 4-INPUT LINE DRIVER
(with active output pullup)

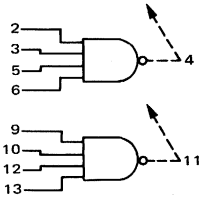


Positive Logic = $\overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 140 ns typ
Typical Total Power Dissipation
Inputs High - 180 mW
Inputs Low - 26 mW

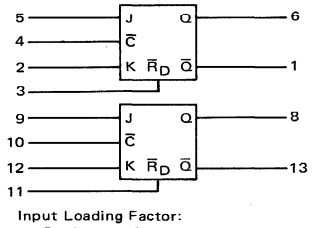
MC669P
DUAL 4-INPUT EXPANDERS



Positive Logic: $4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

Input Loading Factor = 1

MC663P
DUAL J-K FLIP-FLOP



Input Loading Factor:
$\overline{R}_D$ Input = 2
$\overline{C}$ Input = 1.5
Other Inputs = 1

Output Loading Factor = 9

Total Power Dissipation = 200 mW typ
Toggle Frequency = 3.0 MHz typ

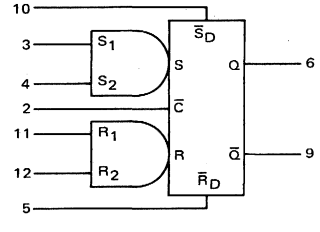
TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}_n$	Q_n

Direct input ($\overline{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\overline{R}_D$ causes a low state "0" at the Q output and the complement at the $\overline{Q}$ output.

MC664P
MASTER-SLAVE R-S FLIP-FLOP



Input Loading Factor:
$\overline{C}$ Input = 3
Other Inputs = 1

Output Loading Factor = 8

Total Power Dissipation = 160 mW typ
Toggle Frequency = 3.0 MHz typ

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

CLOCKED OPERATION *

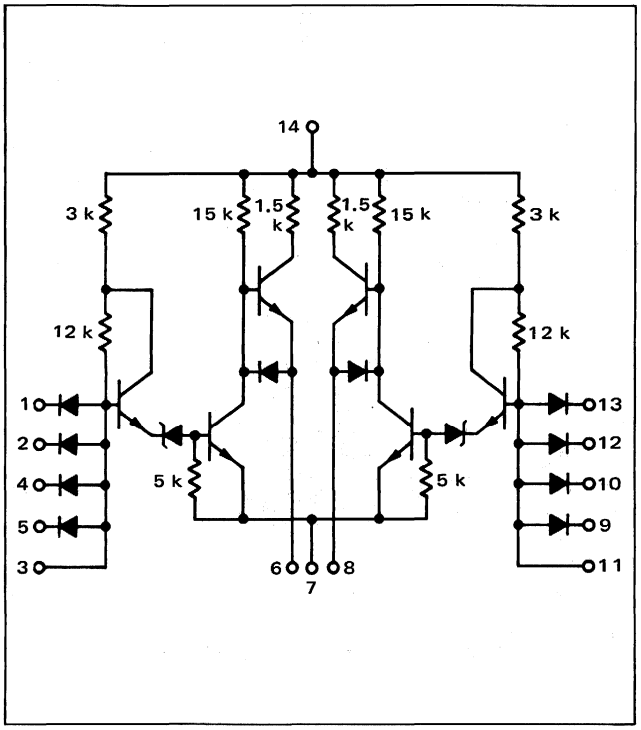
t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

* Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.

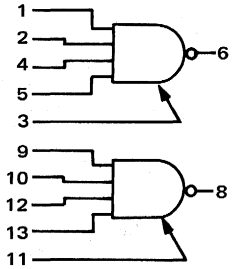
0 = low state
1 = high state
NC = No change
NA = Not allowed
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

EXPANDABLE DUAL 4-INPUT GATE

MC660P



This device consists of two expandable 4-input NAND gates with active output pullup.

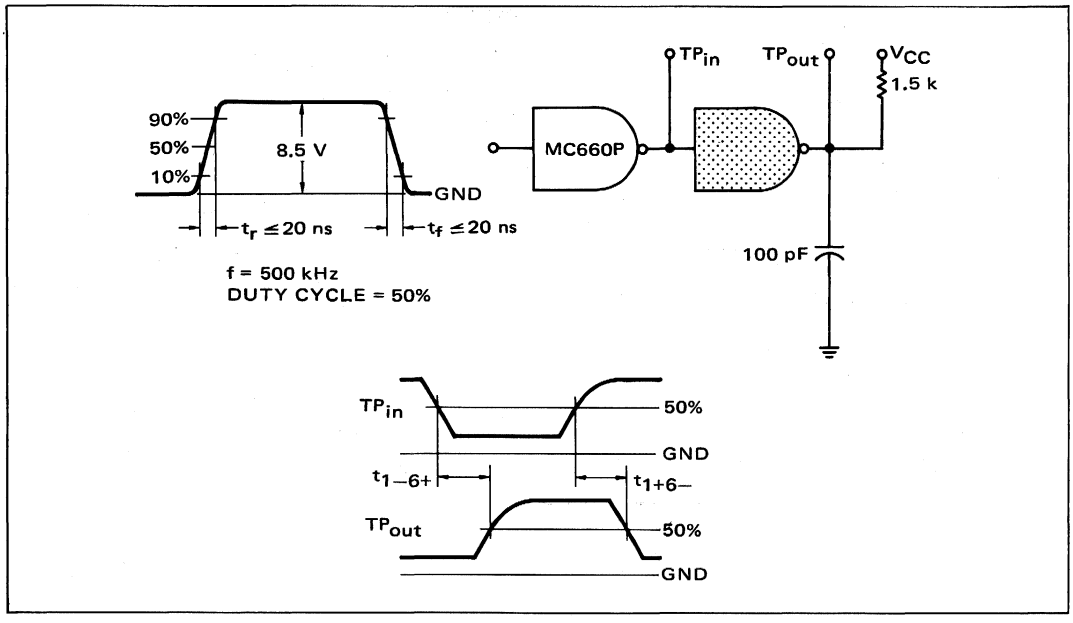


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

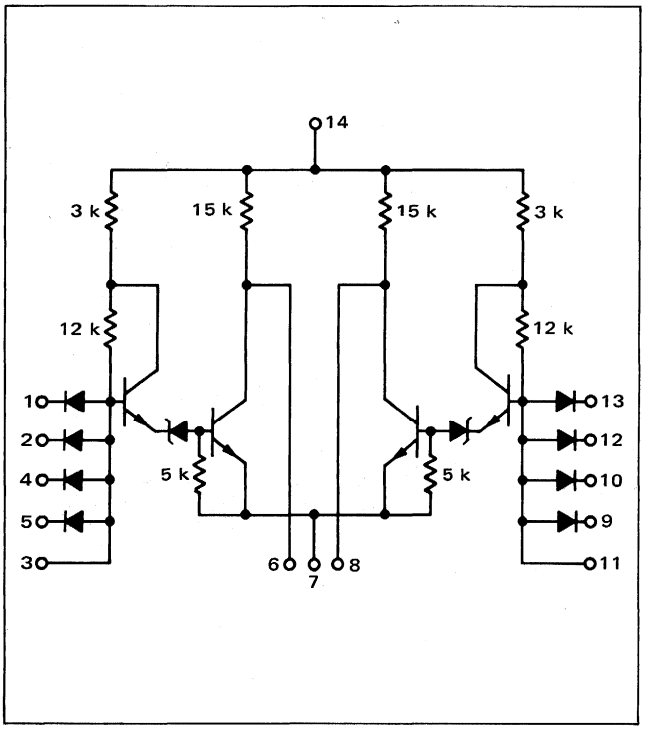
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
mA		Volts									
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	

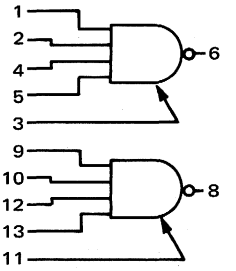
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	200	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC661P



This device consists of two expandable 4-input NAND gates with passive output pullup.

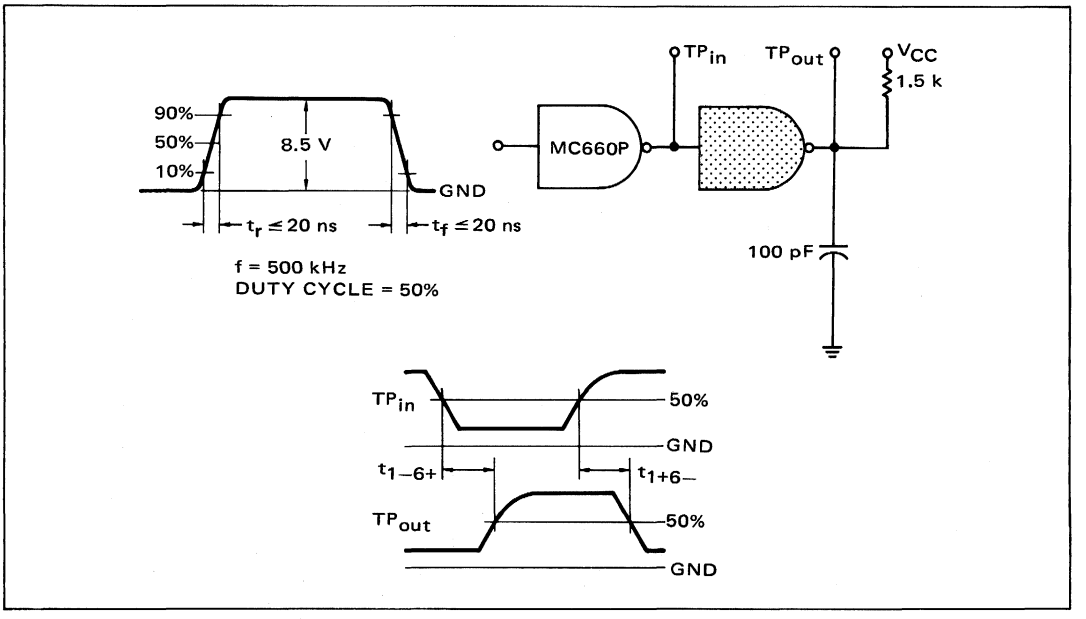


Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 88 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



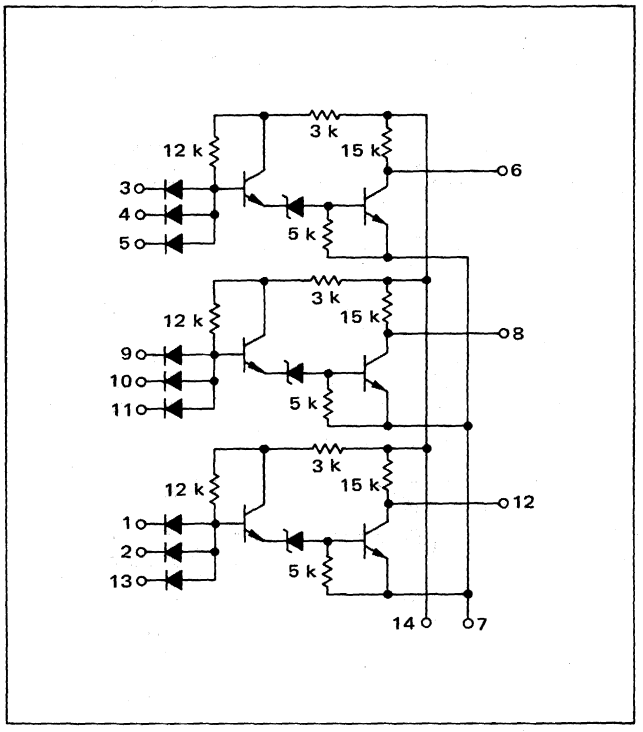
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gate is tested in the same manner.

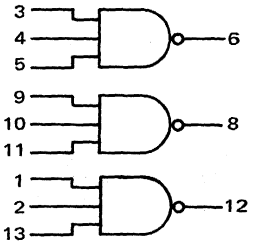
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_X	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC670P



This device consists of three 3-input NAND gates with passive output pull-up.

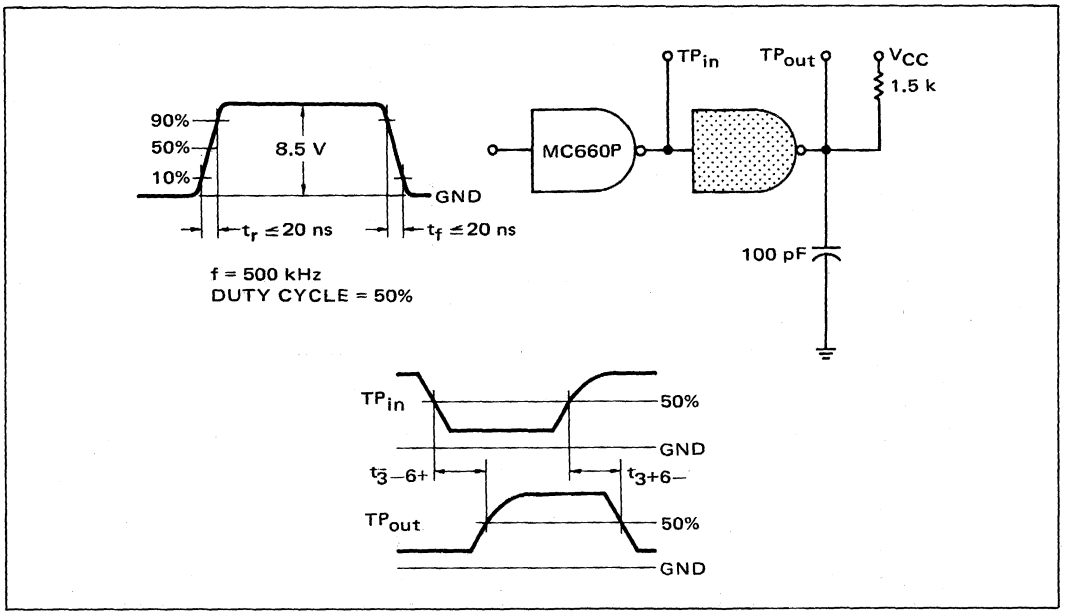


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

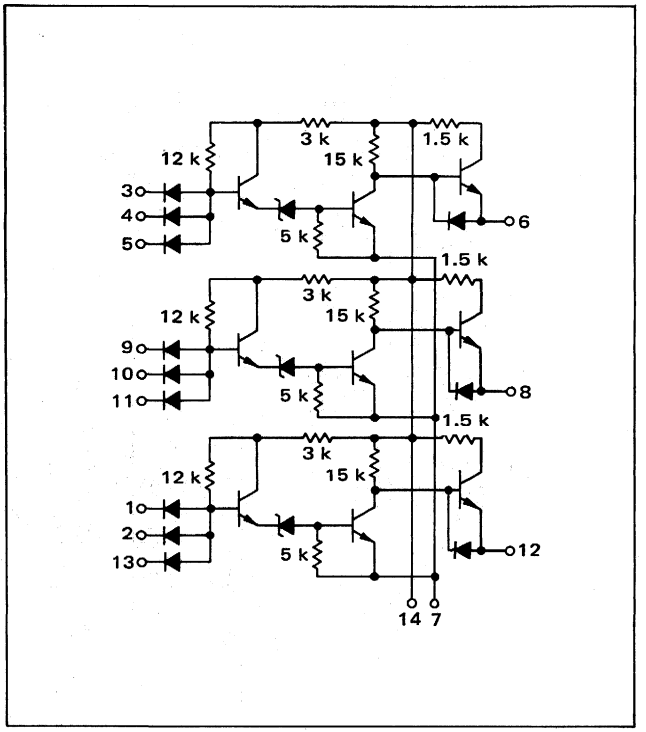
Test procedures are shown for only one gate.
The other gates are tested in the same manner.

			TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
			mA		Volts								
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
			12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	

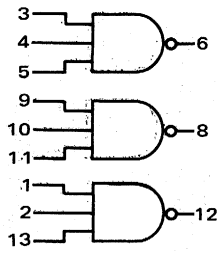
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 5	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	3	-	-	-	-	4, 5	14	-	↓
		↓	-	-	↓	-	↓	-		-	↓	4	-	-	-	-	3, 5	↓	-	
			-	-		-		-		-		5	-	-	-	-	3, 4		-	
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	3, 6, 7
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4, 5, 7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	3, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-		-	3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6, 14	-	-	-	3, 7
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4, 5	-	-	-	14	7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	3, 5	-	-	-	↓	↓
		5	-	-	-		-			-	-	-	-	5	3, 4	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 3, 4, 5, 7, 9, 10, 11, 13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{3-6+}	6	-	-	-	250	-	-	ns	3	6	-	-	-	-	-	14	-	-	7
	t_{3+6-}	6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC671P



This device consists of three 3-input NAND gates with active output pull-up.

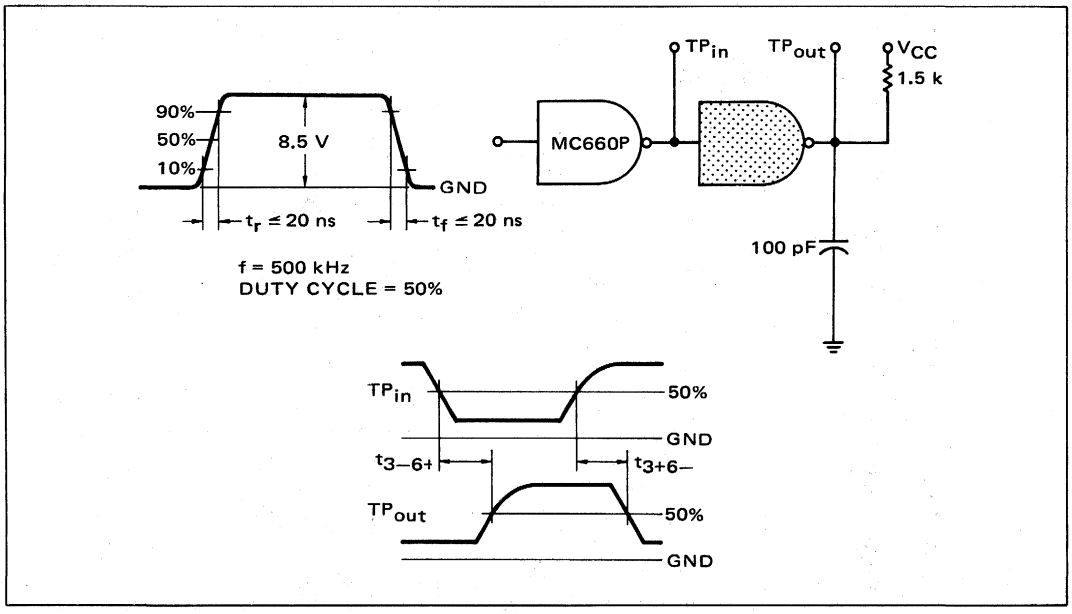


Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



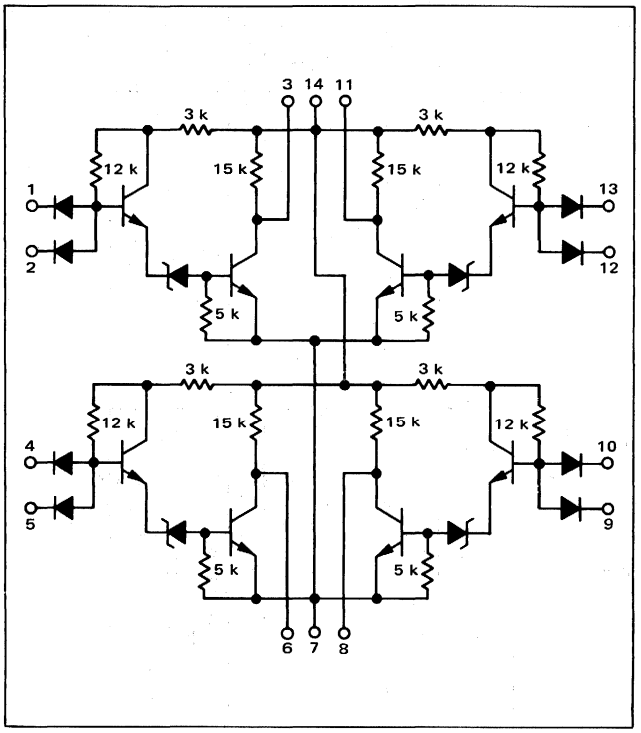
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

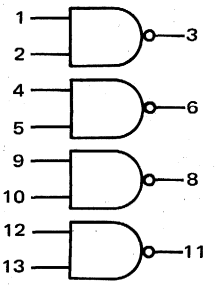
			TEST LIMITS							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			−30°C		+25°C		+75°C			TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
										mA		Volts								
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3,4,5	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-	Vdc	-	6	3	-	-	-	-	4,5	14	-	↓
		↓	-	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	3,5	↓	-	
			-	-		-		-		-		5	-	-	-	-	3,4		-	
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	3,6,7
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4,5,7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	3,5,7
		5	-	-	-		-			-	-	-	-	-	5	-	-		-	3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6,14	-	-	-	3,7
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4,5	-	-	-	14	7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	3,5	-	-	-	↓	↓
		5	-	-	-		-			-	-	-	-	5	3,4	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,7,9,10,11,13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{3-6+}	6	-	-	-	200	-	-	ns	3	6	-	-	-	-	-	14	-	-	7
	t_{3+6-}	6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC668P



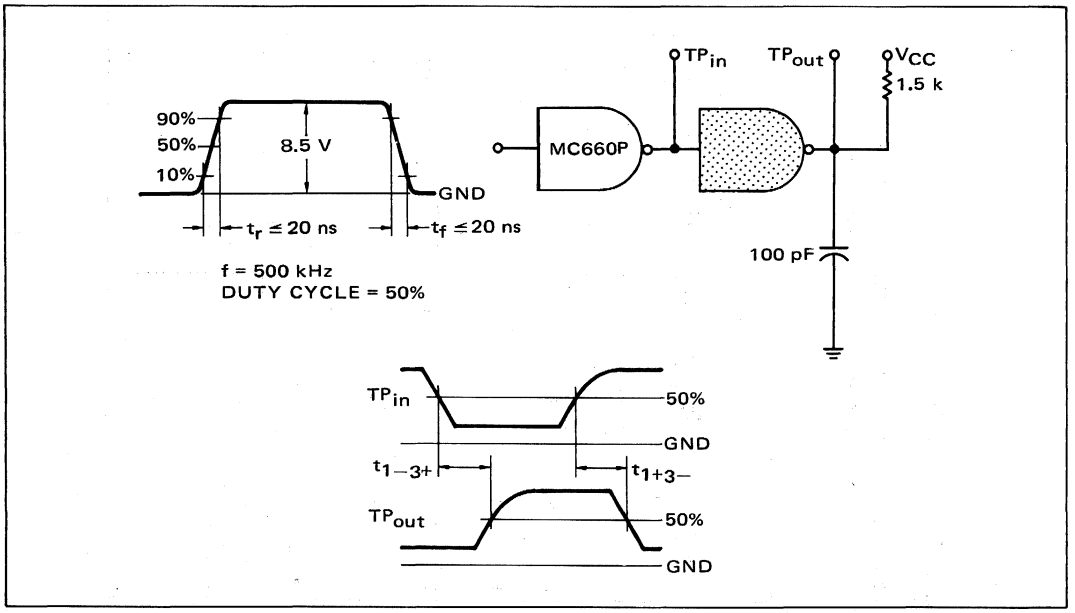
This device consists of four 2-input NAND gates with passive output pull-up.



Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 176 mW
Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



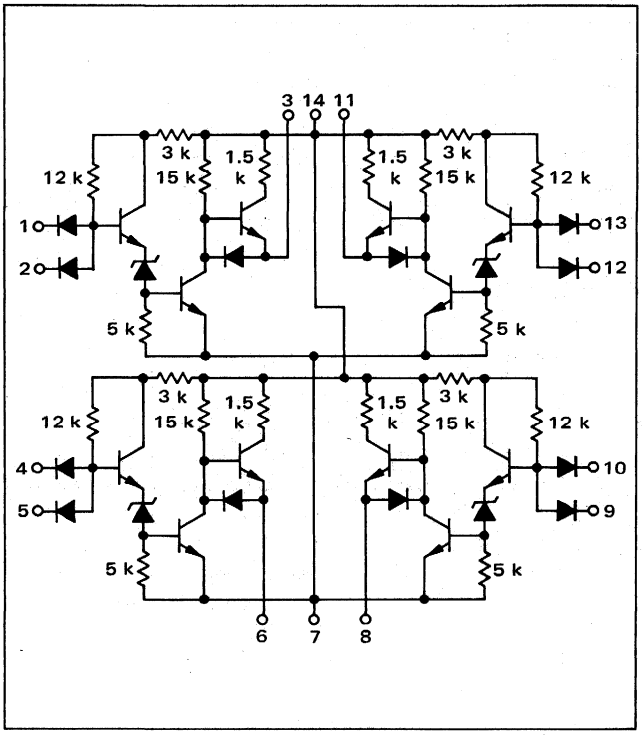
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gates are tested in the same manner.

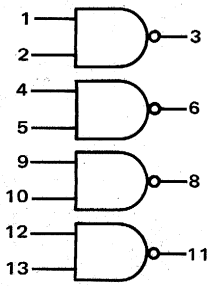
										TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
										mA		Volts								
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
			TEST LIMITS							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
			−30°C		+25°C		+75°C													
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1,2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	↓	-	3	1	-	-	-	-	2	14	-	↓
		3	-	-	12.5	-	12.5	-		-	3	2	-	-	-	-	1	14	-	
Short-Circuit Current	I_{SC}	3	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2,7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3+}	3	-	-	-	250	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1+3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC672P



This device consists of four 2-input NAND gates with active output pull-up.

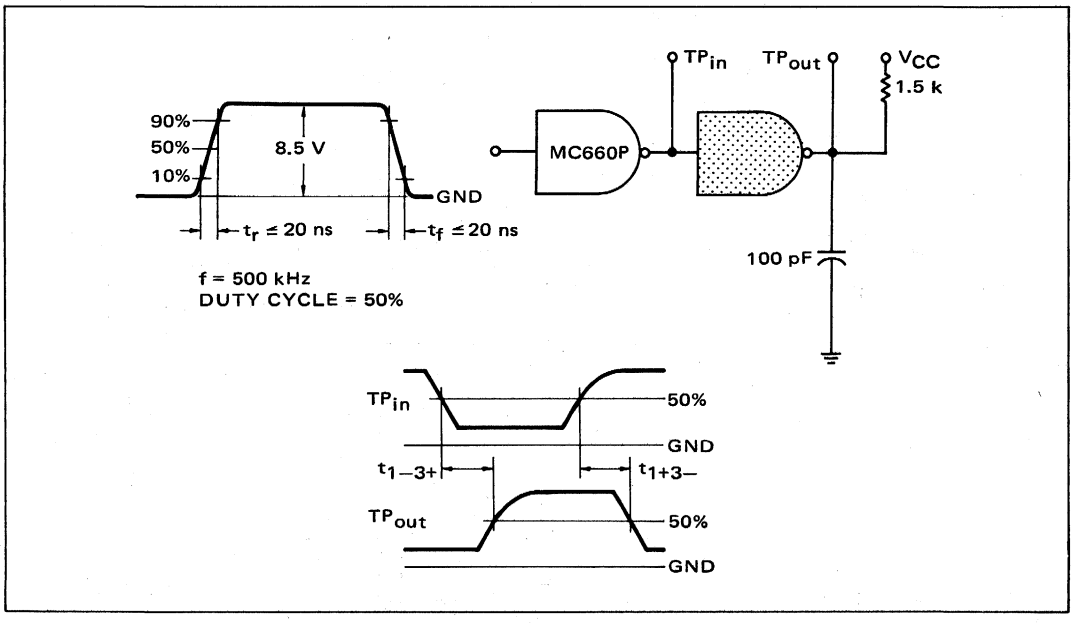


Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Input High = 176 mW
Inputs Low = 52 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



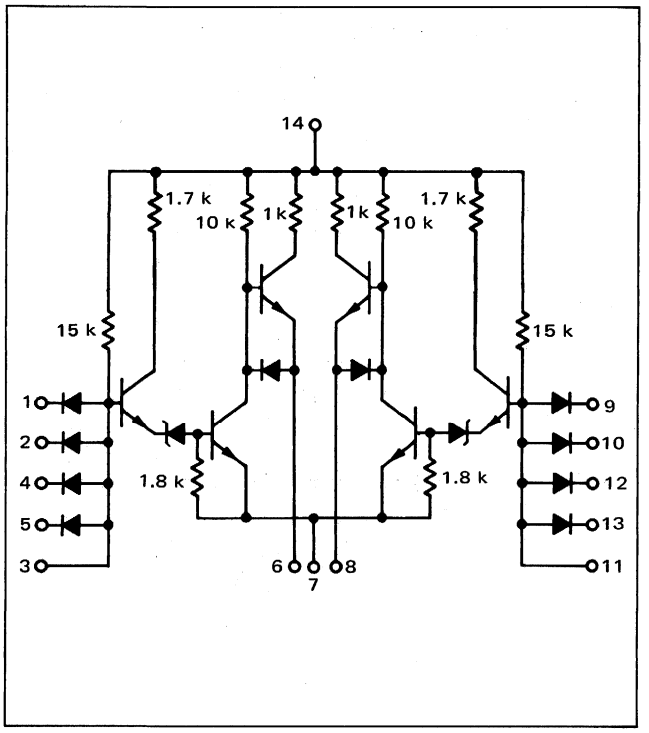
ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
The other gates are tested in the same manner.

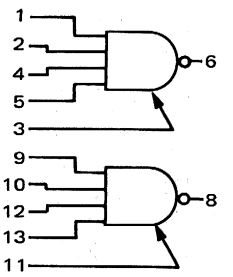
			TEST LIMITS							TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
										mA		Volts								
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
			−30°C		+25°C		+75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1,2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	Vdc	-	3	1	-	-	-	-	2	14	-	7
		3	-	-	12.5	-	12.5	-	Vdc	-	3	2	-	-	-	-	1	14	-	7
Short-Circuit Current	I_{SC}	3	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2,7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7,9,10,12,13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3+}	3	-	-	-	200	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1+3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC662P



This device consists of two expandable 4-input NAND line drivers with active output pullup. This device allows fan-out to 30 MHTL gates and drives large capacitive loads.

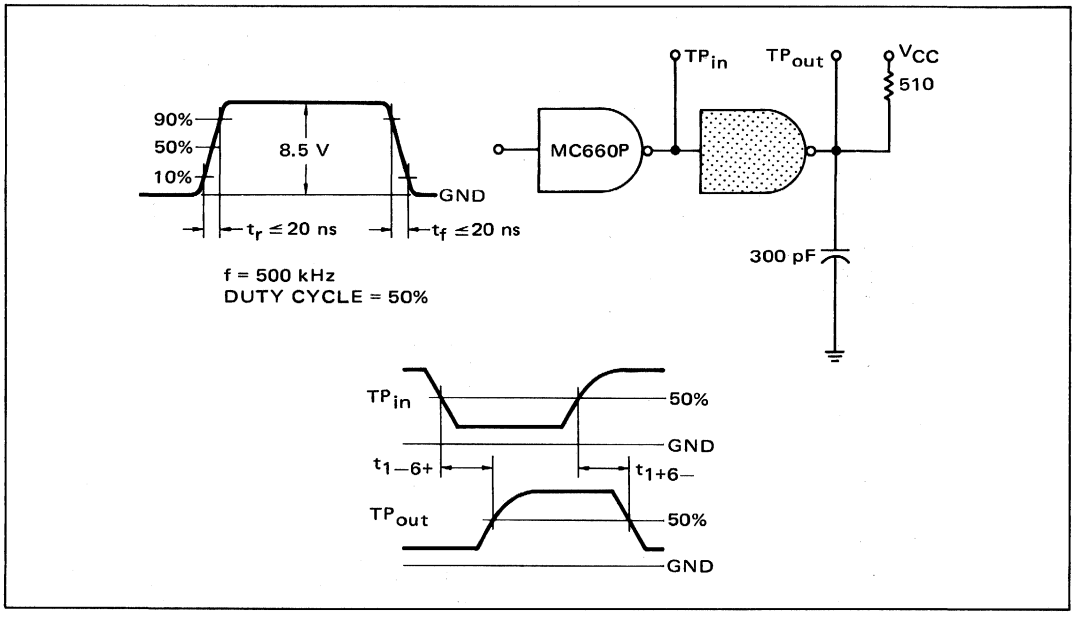


Positive Logic = $\overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 40 ns typ
Typical Total Power Dissipation
Input High = 180 mW
Inputs Low = 26 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

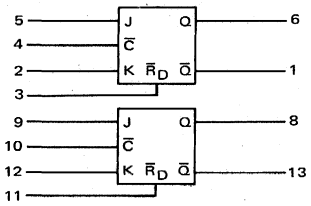
Test procedures are shown for one driver only.
The other driver is tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_X	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										36.0	-0.09	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2,4,5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1,4,5		-	
			-	-		-		-		-		4	-	-	-	-	-	1,2,5		-	
			-	-		-		-		-		5	-	-	-	-	-	1,2,4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-10.0	-25.0	-10.0	-25.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,6,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,3,4,5,7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1,3,4,5,7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1,2,4,5,7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1,2,3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2,4,5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1,4,5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1,2,5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1,2,4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
	I_{CCH}	14	-	-	-	17	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6+}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

MC663P

Two J-K flip-flops in a single package. Each flip-flop has a direct reset input in addition to the clocked inputs.



TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1

Output Loading Factor = 9

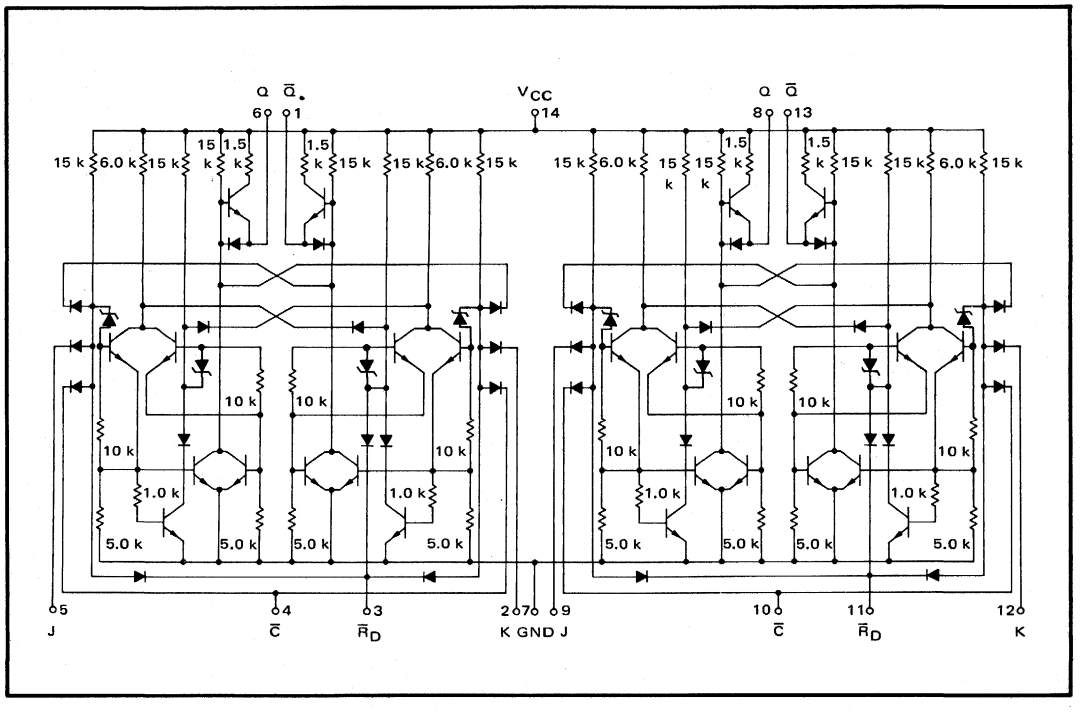
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 200 mW typ

Direct input ($\bar{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

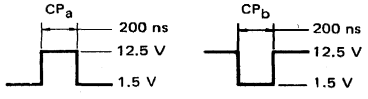


ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

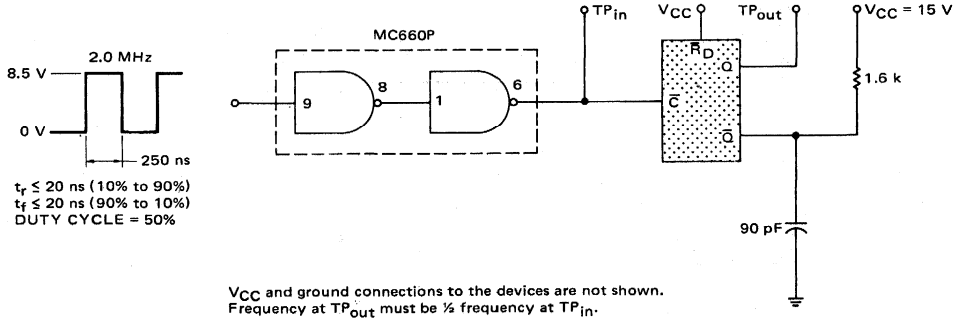
Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CCL}	Volts V_{CCH}	CP_a	CP_b	Ground
										10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0			
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}			
Output Voltage	V_{OL}	1	-	1.5	-	1.5	-	1.5	Vdc	1	-	2	3,5	-	-	14	-	4	-	7
		6	-	1.5	-	1.5	-	1.5		6	-	5	2,3	-	-	14	-	4	-	7
	V_{OH}	1	-	-	12.5	-	12.5	-		-	1	2,3	5	-	-	14	-	4	-	7
		1	-	-	12.5	-	12.5	-		-	1	5	2,3	-	-	14	-	4	-	7
		6	-	-	12.5	-	12.5	-		-	6	2	3,5	-	-	14	-	4	-	7
Short-Circuit Current	I_{SC}	1	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	3,4	-	-	-	-	14	-	-	1,7
Reverse Current	I_R	2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	14	-	-	-	3,4,5,7
	$3I_R$	3	-	-	-	6.0	-	6.0		-	-	-	-	-	3	2,4,5,14	-	-	-	7
	$2I_R$	4	-	-	-	4.0	-	4.0		-	-	-	-	-	4	14	-	-	-	2,3,5,7
	I_R	5	-	-	-	2.0	-	2.0		-	-	-	-	-	5	14	-	-	-	2,3,4,7
Forward Current	I_F	2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	-	-	14	-	4	7
		3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	-	-	14	-	-	2,4,5,7
		4	-	-	-	-1.20	-	-1.20		-	-	-	-	4	-	-	2,5,14	-	-	7
		5	-	-	-	-1.20	-	-1.20		-	-	-	-	5	-	-	14	-	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2,3,4,5,7,9,10,11,12
	I_{CCH}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.



$t_r \leq 1.0\ \mu s$ (10% to 90%)
$t_f \leq 1.0\ \mu s$ (90% to 10%)

TOGGLE MODE TEST CIRCUIT

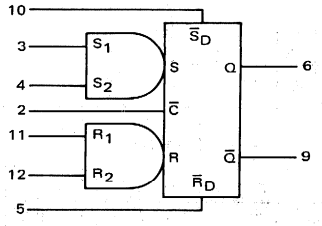


$t_r \leq 20$ ns (10% to 90%)
$t_f \leq 20$ ns (90% to 10%)
DUTY CYCLE = 50%

V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

MC664P

A dc coupled R-S flip-flop operating on the master-slave principle. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.



Input Loading Factor:
$\overline{C}$ Input = 3
Other Inputs = 1

Output Loading Factor = 8

Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 160 mW typ

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

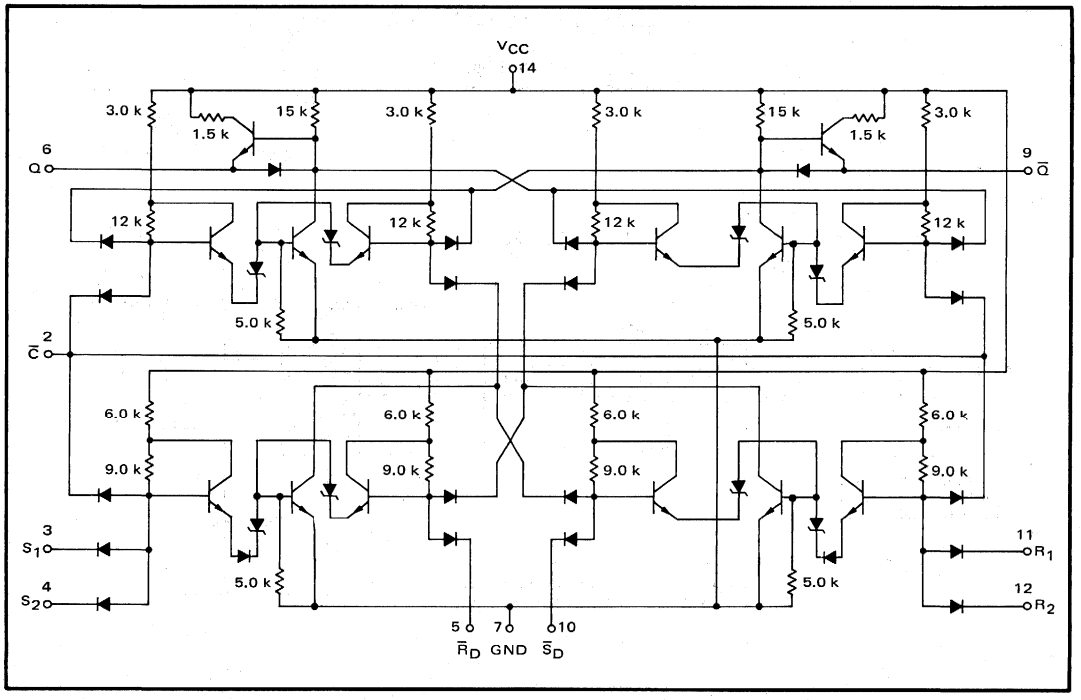
NC = No change
NA = Not allowed

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:

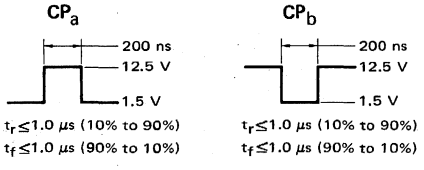
Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n



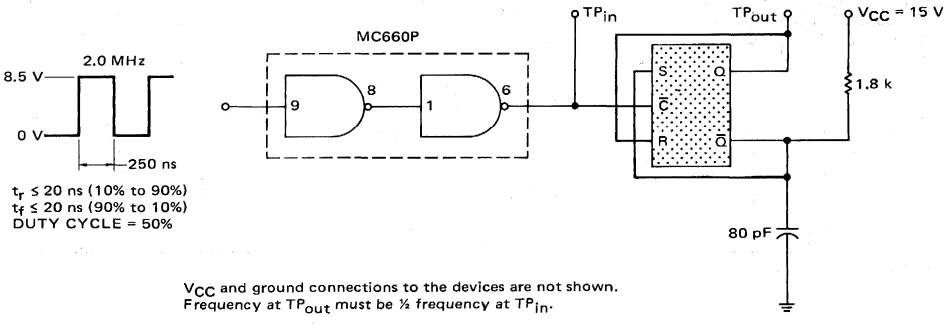
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	CP_a	CP_b	Ground
										9.6	-0.024	6.50	8.50	1.5	16.0	14.0	16.0			
Output Voltage	V_{OL}	6*	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 11, 12	-	-	14	-	-	5	7
		6	-	↓	-	↓	-	↓	↓	6	-	4	3, 5, 11, 12	-	-	↓	-	2	-	7
		6	-		-		-			6	-	3	4, 5, 11, 12	-	-		-	2	-	7
		9‡	-		-		-			9	-	-	3, 4, 11, 12	-	-		-	-	10	7
		9	-		-		-			9	-	11	3, 4, 10, 12	-	-		-	2	-	7
		9	-		-		-			9	-	12	3, 4, 10, 11	-	-		-	2	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	-	5	-	-	14	-	-	-	2, 3, 4, 7, 10, 11, 12
		9	-	-	12.5	-	12.5	-		-	9	-	10	-	-	14	-	-	-	2, 3, 4, 5, 7, 11, 12
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 5	10	-	-	-	14	-	-	6, 7, 9
		9	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 10	5	-	-	-	14	-	-	6, 7, 9
Reverse Current	$4I_R$	2§	-	-	-	8.0	-	8.0	µAdc	-	-	-	5	-	2	14	-	-	-	3, 4, 7, 10, 11, 12
	$4I_R^{\dagger}$	2†	-	-	-	8.0	-	8.0		-	-	-	10	-	2	14	-	-	-	3, 4, 5, 7, 11, 12
	I_R	3	-	-	-	2.0	-	2.0		-	-	-	-	-	3	14	-	-	-	2, 4, 7
		4	-	-	-	↓	-	↓		-	-	-	-	-	4	14	-	-	-	2, 3, 7
		5	-	-	-		-			-	-	-	2, 11, 12	-	5	14	-	-	-	7
		10	-	-	-		-			-	-	-	2, 3, 4	-	10	14	-	-	-	7
		11	-	-	-		-			-	-	-	-	-	11	14	-	-	-	2, 7, 12
		12	-	-	-	↓	-	↓	↓	-	-	-	-	-	12	14	-	-	-	2, 7, 11
Forward Current	$3I_F$	2	-	-	-	-3.60	-	-3.60	mAdc	-	-	-	5	2	3, 4, 11, 12	-	14	-	-	7, 10
	$3I_F$	2	-	-	-	-3.60	-	-3.60		-	-	-	10	2	3, 4, 11, 12	-	14	-	-	5, 7
	I_F	3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	2, 4	-	14	-	-	7
		4	-	-	-		-			-	-	-	-	4	2, 3	-	14	-	-	7
		5	-	-	-		-			-	-	-	-	5	-	-	14	-	-	2, 7, 10, 11, 12
		10	-	-	-		-			-	-	-	-	10	-	-	14	-	-	2, 3, 4, 5, 7
		11	-	-	-		-			-	-	-	-	11	2, 12	-	14	-	-	7
		12	-	-	-	↓	-	↓	↓	-	-	-	-	12	2, 11	-	14	-	-	7
Power Drain Current	I_{CCL}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 10, 11, 12
	I_{CCH}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.
*Apply momentary ground to pins 9 and 10 prior to clock pulse
‡Apply momentary ground to pins 5 and 6 prior to clock pulse
§Apply momentary ground to pin 9
†Apply momentary ground to pin 6

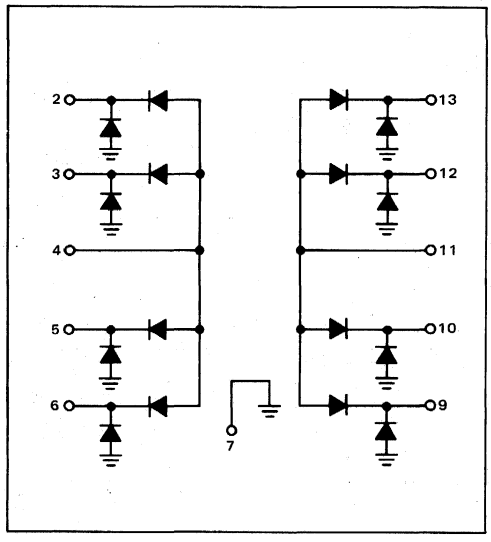


TOGGLE MODE TEST CIRCUIT

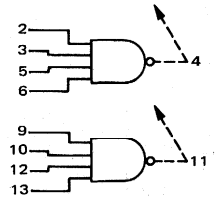


VCC and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

MC669P



This device consists of two independent high voltage diode networks with characteristics matched to the input of the gate and buffer elements in the MHTL logic family. Its use increases the fan-in capability of other MHTL devices to a maximum of 20 while having negligible effect on their performance.



Positive Logic: $4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

Input Loading Factor = 1

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander.
The other expander is tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_F	V_R	Gnd
										TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_F = 1.2	Volts V_R = 16.0	
Forward Voltage	V_F	4	-	1.0	-	0.9	-	0.8	Vdc	4	-	2,7
			-		-		-				-	3,7
			-		-		-				-	5,7
			-		-		-				-	6,7
Reverse Current	I_R	2	-	2.0	-	2.0	-	2.0	μAdc	-	2	3,5,6,7
		3	-		-		-			-	3	2,5,6,7
		5	-		-		-			-	5	2,3,6,7
		6	-		-		-			-	6	2,3,5,7
	$2\,I_R$	4	-	-	-	4.0	-	-		-	4	7

Pins not listed are left open

MTTL

INTEGRATED CIRCUITS
MC500/MC400 SERIES

MTTL

INTEGRATED CIRCUITS

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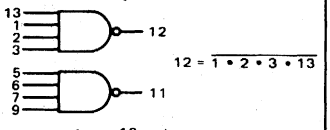
NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 5.0 V, T_A = 25°C

Function	Type		Output Loading Factor Each Output		Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
	Case 609, 93 0 to +75°C	Case 609 −55 to +125°C	MC400 Series	MC500 Series			
Dual 4-Input NAND Gate	MC400 MC450	MC500 MC550	12 6	15 7	10	30	4-14
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC401 MC451	MC501 MC551	12 6	15 7	12	30	4-24
Single 8-Input NAND Gate	MC402 MC452	MC502 MC552	12 6	15 7	12	15	4-10
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC403 MC453	MC503 MC553	12 6	15 7	11	35	4-27
Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC404 MC454	MC504 MC554	12 6	15 7	12	25	4-20
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC405 MC455	MC505 MC555	12 6	15 7	12	20	4-16
Expandable 8-Input NAND Gate	MC406 MC456	MC506 MC556	12 6	15 7	18	15	4-12
Line Driver	MC407 MC457	MC507 MC557	12 6	15 7	25 @ 1000 pF Load	60	4-50
Quad 2-Input NAND Gate	MC408 MC458	MC508 MC558	12 6	15 7	10	60	4-22
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC409 MC459	MC509 MC559	12 6	15 7	–	–	4-48
Dual 4-Input Expander for AND-OR-INVERT Gates	MC410 MC460	MC510 MC560	12 6	15 7	–	–	4-46
Dual 4-Input Expander for NAND Gates	MC411 MC461	MC511 MC561	12 6	15 7	–	–	4-44
Triple 3-Input NAND Gate	MC412 MC462	MC512 MC562	12 6	15 7	10	45	4-18
R-S Flip-Flop	MC413 MC463	MC513 MC563	12 6	15 7	f = 20 MHz	30	4-42
AND J-K Flip-Flop	MC415 MC465	MC515 MC565	12 6	15 7	f = 20 MHz	40	4-32
OR J-K Flip-Flop	MC416 MC466	MC516 MC566	12 6	15 7	f = 20 MHz	50	4-37
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC420 MC470	MC520 MC570	12 6	15 7	12	40	4-30

GATES

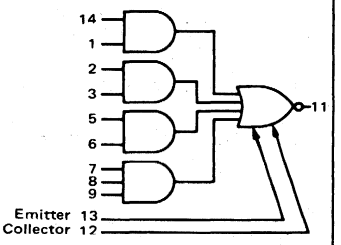
MC400/MC450 MC500/MC550
Dual 4-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

t_{pd} = 10 ns typ
P_D = 30 mW typ/pkg

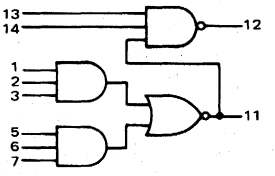
MC401/MC451 MC501/MC551
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate



$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + \ldots}$

t_{pd} = 12 ns typ
P_D = 30 mW typ/pkg

MC403/MC453 MC503/MC553
2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement

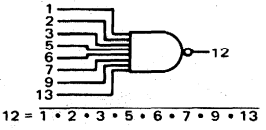


$12 = \overline{11 \cdot 13 \cdot 14}$

$11 = (1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7)$

t_{pd} = 11 ns typ
P_D = 35 mW typ/pkg

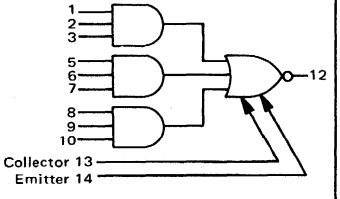
MC402/MC452 MC502/MC552
Single 8-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

t_{pd} = 12 ns typ
P_D = 15 mW typ/pkg

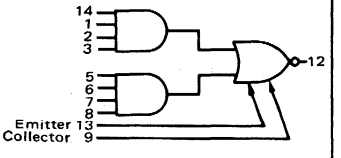
MC404/MC454 MC504/MC554
Expandable 3-Wide 3-Input AND-OR-INVERT Gate



$12 = \overline{(1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + (8 \cdot 9 \cdot 11) + \ldots}$

t_{pd} = 12 ns typ
P_D = 25 mW typ/pkg

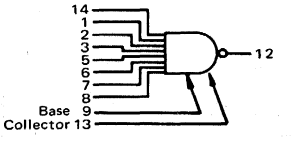
MC405/MC455 MC505/MC555
Expandable 2-Wide 4-Input AND-OR-INVERT Gate



$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8) + \ldots}$

t_{pd} = 12 ns typ
P_D = 20 mW typ/pkg

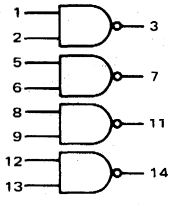
MC406/MC456 MC506/MC556
Expandable 8-Input NAND Gate



$12 = \overline{1 \cdot 3 \cdot 5 \cdot 7 \cdot 8 \cdot 14 \cdot \ldots}$

t_{pd} = 18 ns typ
P_D = 15 mW typ/pkg

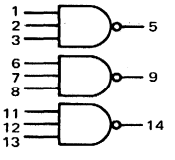
MC408/MC458 MC508/MC558
Quad 2-Input NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 10 ns typ
P_D = 60 mW typ/pkg

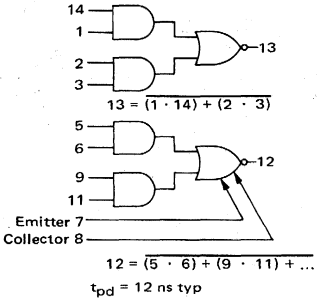
MC412/MC462 MC512/MC562
Triple 3-Input NAND Gate



$5 = \overline{1 \cdot 2 \cdot 3}$

t_{pd} = 10 ns typ
P_D = 45 mW typ/pkg

MC420/MC470 MC520/MC570
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate



$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$

$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + \ldots}$

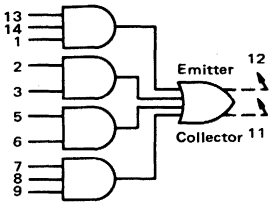
t_{pd} = 12 ns typ
P_D = 40 mW typ/pkg

LOGIC DIAGRAMS (continued)

EXPANDERS

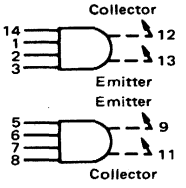
MC409/MC459 MC509/MC559

4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates



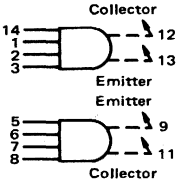
MC410/MC460 MC510/MC560

Dual 4-Input Expander for AND-OR-INVERT Gates



MC411/MC461 MC511/MC561

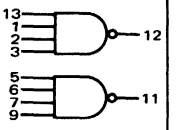
Dual 4-Input Expander for NAND Gates



DRIVER

MC407/MC457 MC507/MC557

Dual 4-Input Line Driver



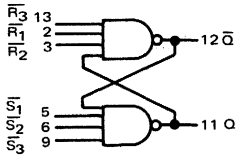
$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

t_{pd} = 25 ns typ
@ 1000 pF Load
P_D = 60 mW typ/pkg

FLIP-FLOPS

MC413/MC463 MC513/MC563

R-S Flip-Flop



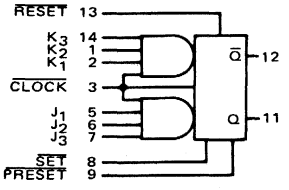
$\overline{R}$	$\overline{S}$	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	Not allowed	
0	1	0	1
1	0	1	0
1	1	Q_n	$\overline{Q}_n$

Where $\overline{R} = \overline{R}_1 \cdot \overline{R}_2 \cdot \overline{R}_3$
$\overline{S} = \overline{S}_1 \cdot \overline{S}_2 \cdot \overline{S}_3$

f = 20 MHz
P_D = 30 mW

MC415/MC465 MC515/MC565

AND J-K Flip-Flop



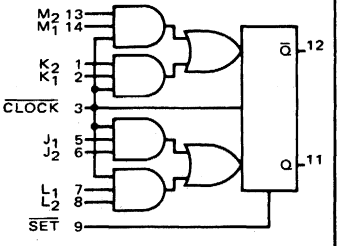
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

f = 20 MHz
P_D = 40 mW

MC416/MC466 MC516/MC566

OR J-K Flip-Flop



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care
Where $J = J_1 \cdot J_2$
$L = L_1 \cdot L_2$
$K = K_1 \cdot K_2$
$M = M_1 \cdot M_2$

f = 20 MHz
P_D = 50 mW

MTTL

GENERAL INFORMATION SECTION

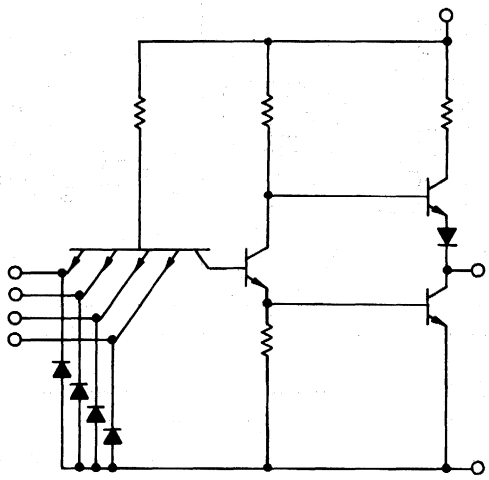
INTRODUCTION

MTTL transistor-transistor logic is a medium speed, high-noise-immunity family of saturating integrated logic circuits.

The circuits in the MTTL family are identified by a multiple emitter input transistor and an active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The active pull-up output configuration provides low impedance in the high output state. The resulting low impedances in both states provide excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 – TYPICAL MTTL CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage – Continuous MC500 Series MC400 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC500 Series MC400 Series	-55 to +125 0 to +75	°C
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°C
Maximum Junction Temperature MC500/550 Series MC400/450 Series	 +175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Flat Package Plastic Dual-In-Line	 0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Flat Package Plastic Dual-In-Line	 0.26 0.30	°C/mW

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL family. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range:
MC500/550 Series = −55 to +125°C
MC400/450 Series = 0 to +75°C

Output Drive Capability
Other Gates (Output Loading Factor):
MC500 Series = 15 MC500 or MC550 Series Gates.
MC550 Series = 7 MC500 or MC550 Series Gates.
MC400 Series = 12 MC400 or MC450 Series Gates.
MC450 Series = 6 MC400 or MC450 Series Gates.

Capacitance = 600 pF

Output Impedance
High State = 70 ohms (unsaturated) nominal
Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
+5.5 volts maximum
−0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance
High State = 400 k ohms nominal
Low State = 4.0 k ohms nominal

Worst-Case DC Noise Margin
High State — MC500/550 series 0.700 volt minimum
MC400/450 series 0.600 volt minimum
Low State — MC500/550 series 0.750 volt minimum
MC400/450 series 0.750 volt minimum

Power Dissipation
15 mW per gate typical
40-50 mW per flip-flop typical

Switching Speeds(1)
Average Propagation Delay = 10 ns per gate typical
18 ns per flip-flop typical
Rise Time = 2.5 ns typical
Fall Time = 1.5 ns typical

Flip-Flop Clock Frequency (MC515/516 Series) = 20 MHz maximum.

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every eight packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL logic circuits is +5.0 Vdc. The typical average dc power dissipation is given for each MTTL circuit.(2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.35 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for V_{CC} = 5.0 V, V_{IL} = 0.45 V and I_{OH} = −5.0 mA:

MC500/550 Series — V_{OH} = 2.8 volts minimum @ −55°C
MC400/450 Series — V_{OH} = 3.0 volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC515/MC516 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

The direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs do not override the clock and will not control the state of the flip-flop until 120 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 20 MHz
Maximum clock fall time	= 150 ns
Minimum clock pulse width	= 20 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= −0.5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 150 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 20 MHz as long as the clock fall time is less than or equal to 150 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to −0.5 volt.

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(1) The switching characteristics of the MTTL family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

(2)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at V_{CC} = +5.0 V.

MC400/450 and MC500/550 MTTL* series integrated circuits are electrically interchangeable with SUHL I† series logic circuits.

SG SF NUMBERS	Description	−55 to +125°C		0 to +75°C	
		Fan-Out = 15	Fan-Out = 7	Fan-Out = 12	Fan-Out = 6
SG40-43	Dual 4-Input NAND Gate	MC500	MC550	MC400	MC450
SG50-53	Expandable 2-Wide 2-2-2-3-Input AND-OR-INVERT Gate	MC501	MC551	MC401	MC451
SG60-63	Single 8-Input NAND Gate	MC502	MC552	MC402	MC452
SG90-93	2-Wide 3-Input AND-OR-INVERT Gate with Gated Complement	MC503	MC553	MC403	MC453
SG100-103	Expandable 3-Wide 3-Input AND-OR-INVERT Gate	MC504	MC554	MC404	MC454
SG110-113	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC505	MC555	MC405	MC455
SG120-123	Expandable 8-Input NAND Gate	MC506	MC556	MC406	MC456
SG130-133	Line Driver	MC507	MC557	MC407	MC457
SG140-143	Quad 2-Input NAND Gate	MC508	MC558	MC408	MC458
SG150-153	4-Wide 3-2-2-3-Input Expander for AND-OR-INVERT Gates	MC509	MC559	MC409	MC459
SG170-173	Dual 4-Input Expander for AND-OR-INVERT Gates	MC510	MC560	MC410	MC460
SG180-183	Dual 4-Input Expander for NAND Gates	MC511	MC561	MC411	MC461
SG190-193	Triple 3-Input NAND Gate	MC512	MC562	MC412	MC462
SF10-13	R-S Flip-Flop	MC513	MC563	MC413	MC463
SF50-53	AND J-K Flip-Flop	MC515	MC565	MC415	MC465
SF60-63	OR J-K Flip-Flop	MC516	MC566	MC416	MC466
SG70-73	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC520	MC570	MC420	MC470

*Trademark of Motorola Inc.
†Trademark of Sylvania Electric Products, Inc.

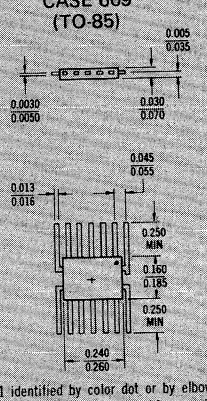
DEFINITIONS

BV_{in} "0"	Input breakdown voltage (ON level)
BV_{in} "1"	Input breakdown voltage (OFF level)
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
f_{Tog}	Toggle frequency
h_{FE}	Forward beta
I_{B1}, I_{B2}	Base current
I_C	Collector Current
I_F	Input forward current
I_{in}	Input current
I_L	Inverse beta current
I_{max}	Maximum rated power supply current with V_{max} applied
I_O	Output breakdown current
I_{OH}	Output high current
I_{OL}	Output low current
I_{OLK}	Output leakage current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input reverse current with V_R applied
I_{SC}	Short circuit current obtained from device output when one or more inputs are low
Pr	Prime fan-out
PRF	Pulse repetition frequency
PW	Pulse width
R_G	Generator resistance
R_L	Load resistance
Std	Standard fan-out
t_f	Fall time
t_{off}	Turn-off delay time
t_{on}	Turn-on delay time
t_{Post}	The minimal time necessary before the $\overline{SET}$, $\overline{PRESET}$ or $\overline{RESET}$ inputs can control the flip-flop after the negative clock edge
t_r	Rise time
Δt_{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate
$\Delta t_{pd}/pF$	Increased propagation delay caused by additional capacitance at expansion points
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
V_{Amp}	Voltage amplitude
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage
V_C	Collector voltage
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CE}	Collector-emitter voltage
V_{CR}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CC}
V_{CRH}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CCH}
V_{DC}	Voltage obtained with two series diodes tied from collector to ground
V_{E1}, V_{E2}, V_{E3}	Emitter voltage
V_{EN}	Enable voltage level
V_{IH}	Voltage for high input voltage state
V_{IHX}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Voltage for low input voltage state
V_{INH}	Inhibit voltage level
V_{max}	Maximum rated power supply voltage (V_{CC})
V_O	Offset voltage
V_{OH}	Output high voltage with I_{OH} flowing out of pin
V_{OL}	Output low voltage with I_{OL} flowing into pin
V_{out}	Output voltage
V_{out} "0"	Output low voltage with V_{th} "1" applied
V_{out} "1"	Output high voltage with V_{th} "0" applied
V_R	Input reverse voltage
V_{th} "0"	Logic "0" threshold voltage
V_{th} "1"	Logic "1" threshold voltage

PACKAGING

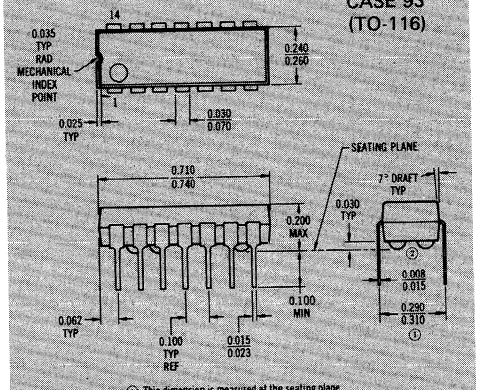
All MTTL integrated circuits are available in the TO-85, 14-lead flat package. MC400 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

CASE 609
(TO-85)



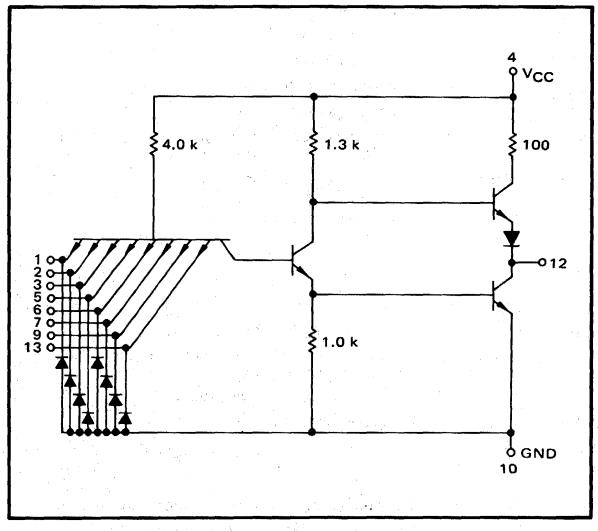
Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

CASE 93
(TO-116)

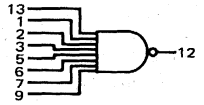


① This dimension is measured at the seating plane.
② 4 insulating stand-offs are provided.

MC502 · MC552
MC402 · MC452



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic:

$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

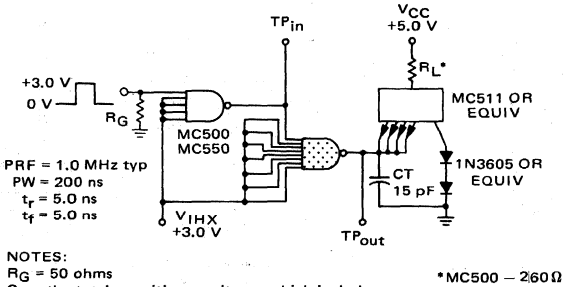
Negative Logic:

$12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 9 + 13}$

Total Power Dissipation = 15 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE	(I_{OL})	TEMPERATURE RANGE
MC502 MC552	1	(−1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC402 MC452	1	(−1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

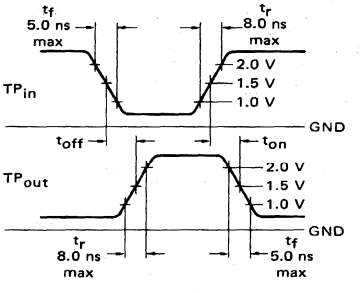
SWITCHING TIME TEST CIRCUITS



NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF

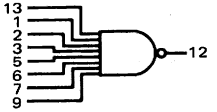
*MC500 – 260Ω
MC550 – 570Ω
MC400 – 330Ω
MC450 – 660Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the gate. To complete testing, sequence through remaining inputs in the same manner.



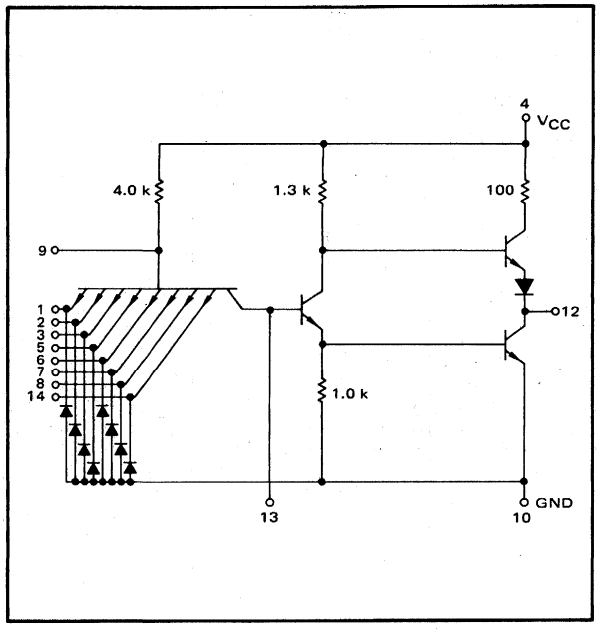
@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC502*, MC552	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC402*, MC452	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC502, MC552 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC402, MC452 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,5,6, 7,9,13	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	-	-	-	5.5	-	-	-	-	-	5.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	-	-	-	5.5	-	-	-	-	-	5.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,9,10,13
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,9,10,13
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I_{PDH}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,10
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	24	-	-	-	-	-	24	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Turn-Off Delay	t_{off}	1,12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Rise Time	t_r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Fall Time	t_f	1,12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10

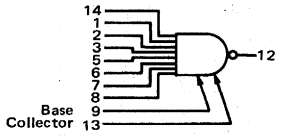
*Prime Fan-Out.

EXPANDABLE 8-INPUT "NAND" GATE

MC506 · MC556
MC406 · MC456



This device consists of an 8-input AND gate driving an output inverter. The base and the collector of the multiple emitter input transistor are available as expander terminals. The number of inputs can be expanded to 20 by using the MC511 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 8 \cdot 14 \cdot \text{Expanders}}$

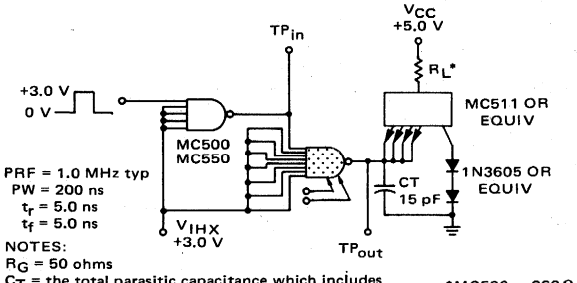
Negative Logic:

$12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 8 + 14 + \text{Expanders}}$

Total Power Dissipation = 15 mW typ/pkg
Propagation Delay Time = 18 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC506 MC556	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC406 MC456	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

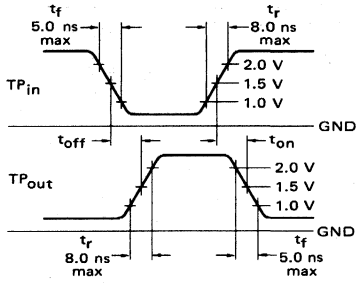


PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

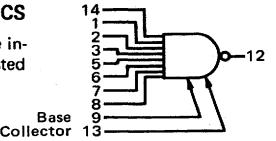
*MC506 – 260 Ω
MC556 – 570 Ω
MC406 – 330 Ω
MC456 – 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the gate. The other inputs are tested in the same manner.



	@ Test Temperature	I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	V_{th1} Volts	V_{th0} Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC506*, MC556	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC406*, MC456	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

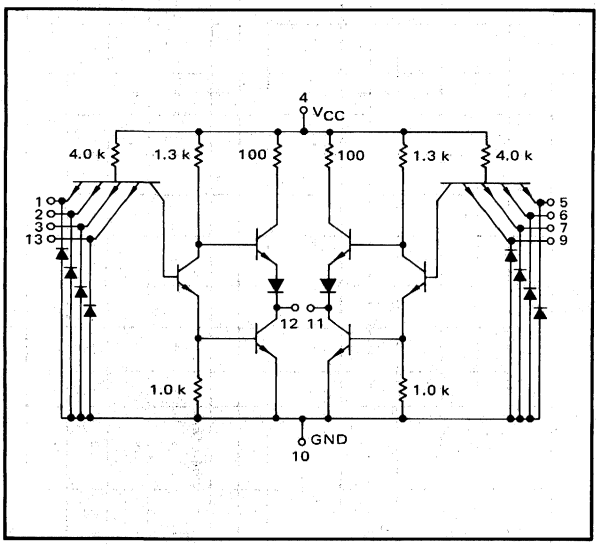
Characteristic	Symbol	Pin Under Test	MC506, MC556 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC406, MC456 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,5,6, 7,8,14	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Output Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 8,10,12,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,10
Power Supply Drain	I_{PDH}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,10
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}†	1,12	-	-	-	28	-	-	-	-	-	28	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,8,14	10
Turn-Off Delay	t_{off}	1,12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,8,14	10
Rise Time	t_r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,8,14	10
Fall Time	t_f	1,12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,8,14	10

* Prime Fan-Out.

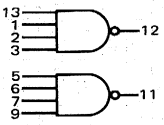
† Add 3.0 ns for each AND expander (1/2 MC511, MC561, MC411, and MC461) used.
Add 2.0 ns t_{pd} for each pF added to either expander points.

DUAL 4-INPUT "NAND" GATE

MC500 · MC550
MC400 · MC450



This device consists of two 4-input NAND gates. The gates can be cross-coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.

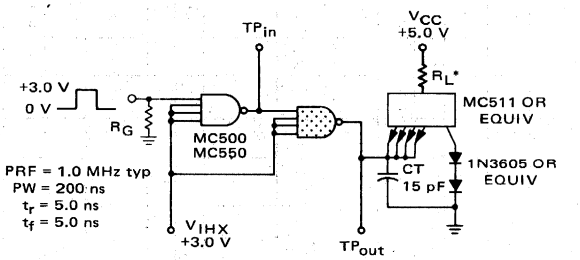


Positive Logic:
$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$
Negative Logic:
$12 = \overline{1 + 2 + 3 + 13}$

Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC500 MC550	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC400 MC450	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

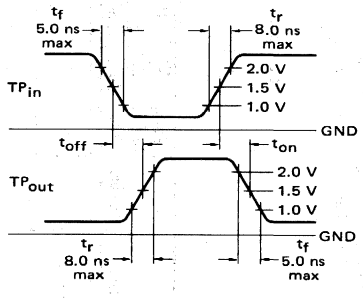
SWITCHING TIME TEST CIRCUIT



NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

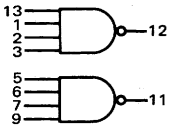
*MC500 — 260 Ω
MC550 — 570 Ω
MC400 — 330 Ω
MC450 — 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

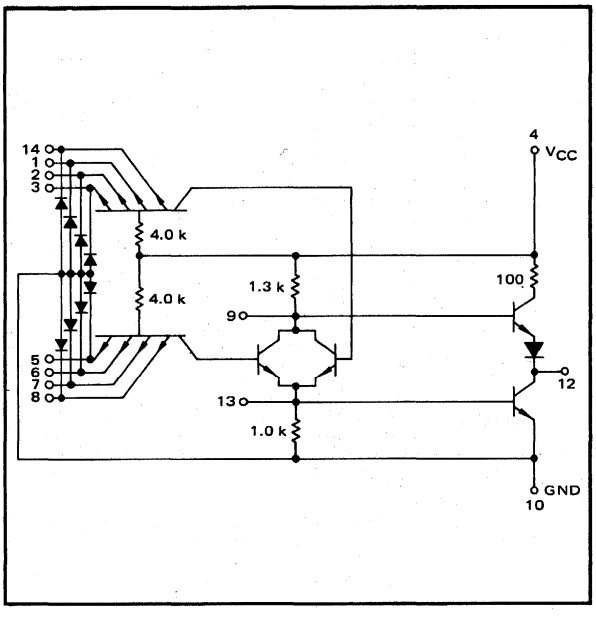


@ Test Temperature	TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	TEST CONDITIONS Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC500*, MC550 −55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
MC500*, MC550 +25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
MC500*, MC550 +125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC400*, MC450 0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
MC400*, MC450 +25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
MC400*, MC450 +75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

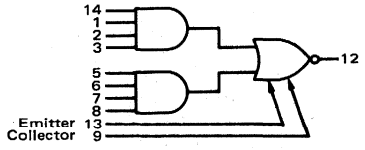
Characteristic	Symbol	Pin Under Test	MC500, MC550 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC400, MC450 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd †
Input Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,13	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,13
Output Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3, 10,13
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 10, 12, 13
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I_{PDH}	4	-	12	-	12	-	12	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Turn-Off Delay	t_{off}	1,12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Rise Time	t_r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Fall Time	t_f	1,12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10

* Prime Fan-Out.
† Ground inputs to gates not under test during ALL tests, unless otherwise noted.
‡ The inputs of all gates must be ungrounded.

MC505 · MC555
MC405 · MC455



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 or MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds



Positive Logic:

$12 = (1 \cdot 2 \cdot 3 \cdot 14) + (5 \cdot 6 \cdot 7 \cdot 8) + (\text{Expanders})$

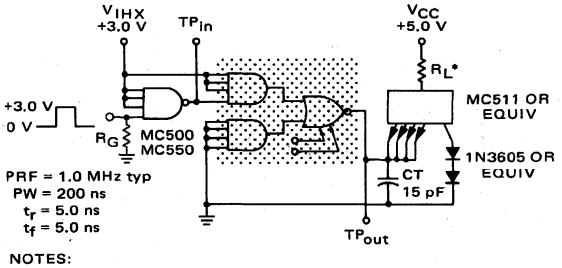
Negative Logic:

$12 = (1 + 2 + 3 + 14) \cdot (5 + 6 + 7 + 8) \cdot (\text{Expanders})$

Total Power Dissipation = 20 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC505 MC555	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC400 MC450	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

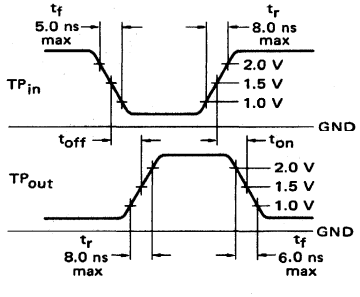


PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

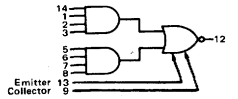
*MC505 – 260 Ω
MC555 – 570 Ω
MC405 – 330 Ω
MC455 – 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.



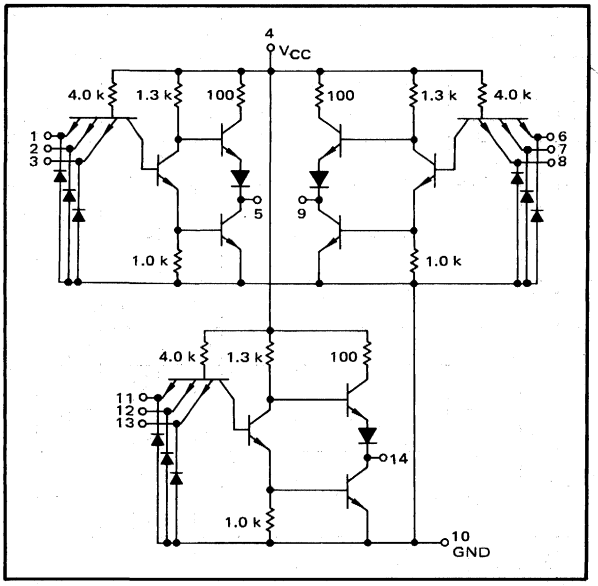
@ Test Temperature		TEST CONDITIONS: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC505*, MC555	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC405*, MC455	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC505, MC555 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC405, MC455 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1,5,6,7, 8,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,8,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	5,6,7,8,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 8,10,14
Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	5,6,7,8,10
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	5,6,7,8,10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6, 7,8,10,14
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10, 12,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	5,6,7,8,10
	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	5,6,7,8,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,8,10,14
Power Supply Drain	I_{PDH}	4	-	7.0	-	7.0	-	7.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	4.0	-	4.0	-	4.0	-	4.0	-	4.0	-	4.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,8,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Turn-Off Delay	t_{off}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Rise Time	t_r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Fall Time	t_f	1,12	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10

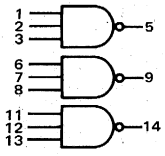
* Prime Fan-Out

TRIPLE 3-INPUT "NAND" GATE

MC512 · MC562
MC412 · MC462



This device consists of a 3-input AND gate driving an output inverter. This gate can be used to build a pulse shaping network for interfacing with discrete component circuits.

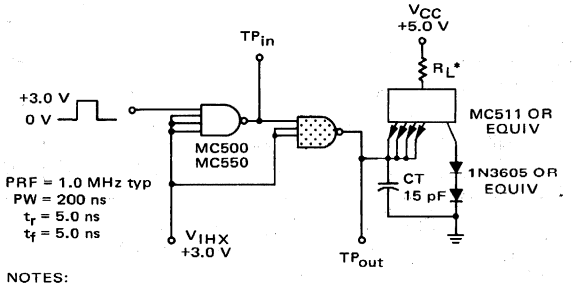


Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$
Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 45 mW typ/pkg
Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC512 MC562	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC412 MC462	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

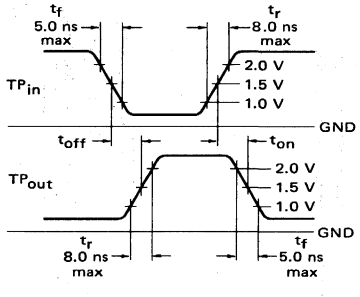
SWITCHING TIME TEST CIRCUIT



NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

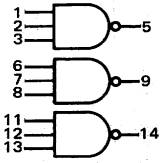
*MC512 – 260Ω
MC562 – 570Ω
MC412 – 330Ω
MC462 – 660Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



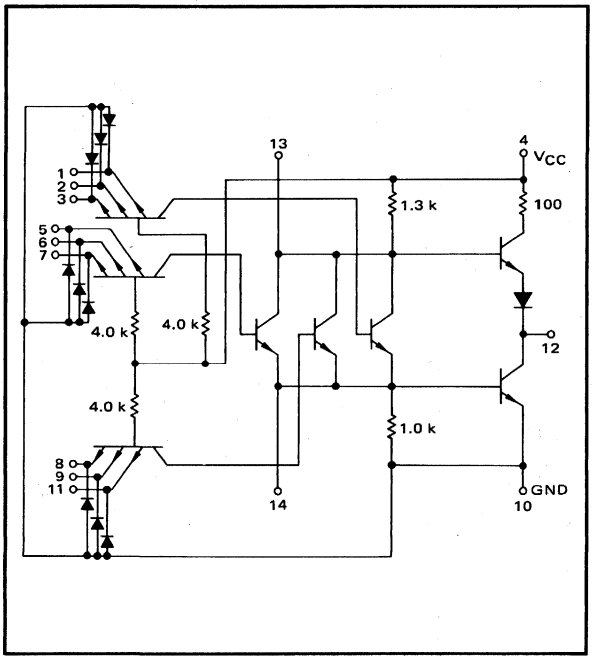
@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	V_{th1} Volts	V_{th0} Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC512*, MC562	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC412*, MC462	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC512, MC562 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC412, MC462 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
Output																												
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	5	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10
Short-Circuit Current	I_{SC}	5	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 5,10
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	5	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	5	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	15	-	-	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11
Power Supply Drain	I_{PDH}	4	-	18	-	18	-	18	-	22.5	-	22.5	-	22.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10 ‡
	I_{PDL}	4	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,6,10,11
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,5	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Turn-Off Delay	t_{off}	1,5	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Rise Time	t_r	1,5	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Fall Time	t_f	1,5	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10

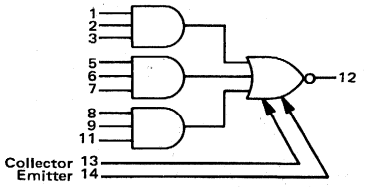
* Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

EXPANDABLE 3-WIDE 3-INPUT "AND-OR-INVERT" GATE

MC504 · MC554
MC404 · MC454



This device consists of three 3-input AND gates ORed together driving an output inverter. The common ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC509 or the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$12 = \overline{(1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7) + (8 \cdot 9 \cdot 11) + (\text{Expanders})}$

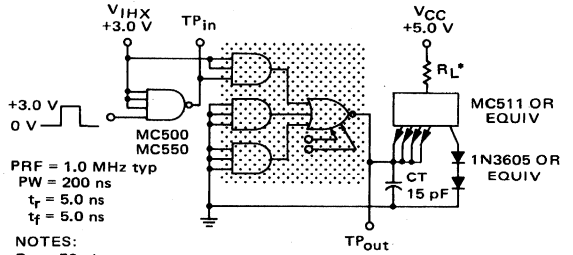
Negative Logic:

$12 = \overline{(1 + 2 + 3) \cdot (5 + 6 + 7) \cdot (8 + 9 + 11) \cdot (\text{Expanders})}$

Total Power Dissipation = 25 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE	(I_{OL})	TEMPERATURE RANGE
MC504 MC554	1	(−1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC404 MC454	1	(−1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

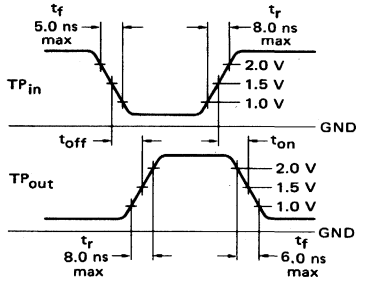


PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

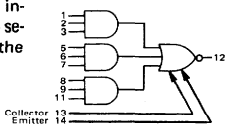
*MC504 — 260 Ω
MC554 — 570 Ω
MC404 — 330 Ω
MC454 — 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing sequence through remaining inputs in the same manner.

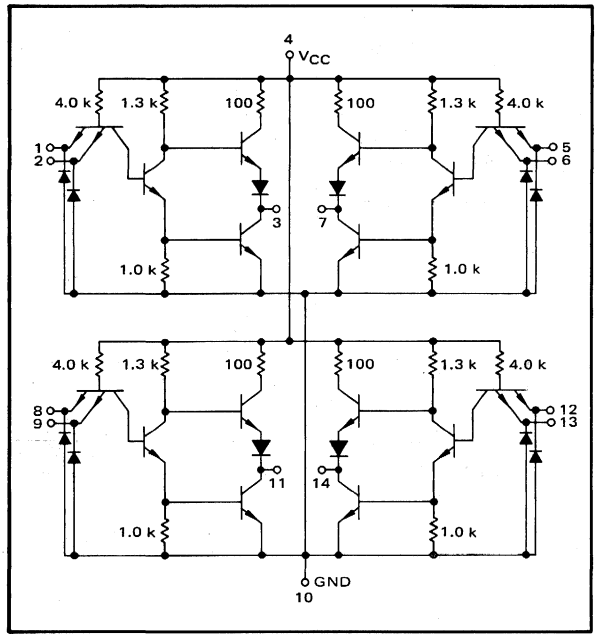


	@ Test Temperature	I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC504*, MC554	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC404*, MC454	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

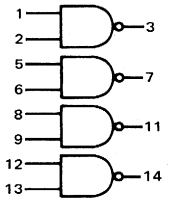
Characteristic	Symbol	Pin Under Test	MC504, MC554 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC404, MC454 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,5,6,7,8,9,10,11
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10,11
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,8,9,10,11
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	5,6,7,8,9,10,11
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10,11
Output Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	5,6,7,8,9,10,11
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	5,6,7,8,9,10,11
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6,7,8,9,10,11
Short-Circuit Current	I_{SC}	12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,11,12
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	5,6,7,8,9,10,11
	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	5,6,7,8,9,10,11
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,11
Power Supply Drain	I_{PDH}	4	-	8.0	-	8.0	-	8.0	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,11
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9,10,11
Turn-Off Delay	t_{off}	1,12	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9,10,11
Rise Time	t_r	1,12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9,10,11
Fall Time	t_f	1,12	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3	5,6,7,8,9,10,11

* Prime Fan-Out

MC508 · MC558
MC408 · MC458



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.

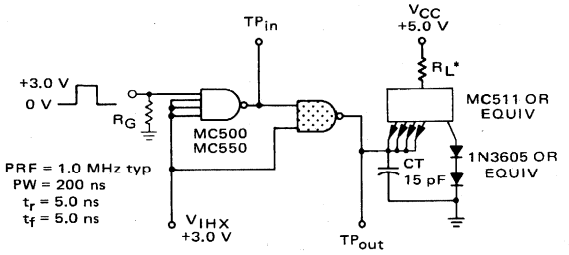


Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1 + 2}$

Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 10 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE	(I_{OL})	TEMPERATURE RANGE
MC508 MC558	1	(−1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC408 MC458	1	(−1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

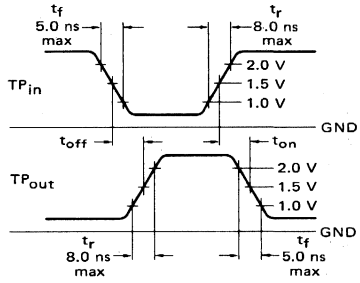
SWITCHING TIME TEST CIRCUIT



NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

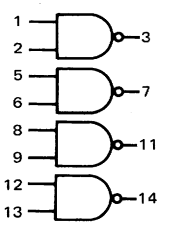
*MC508 – 260 Ω
MC558 – 570 Ω
MC408 – 330 Ω
MC458 – 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.



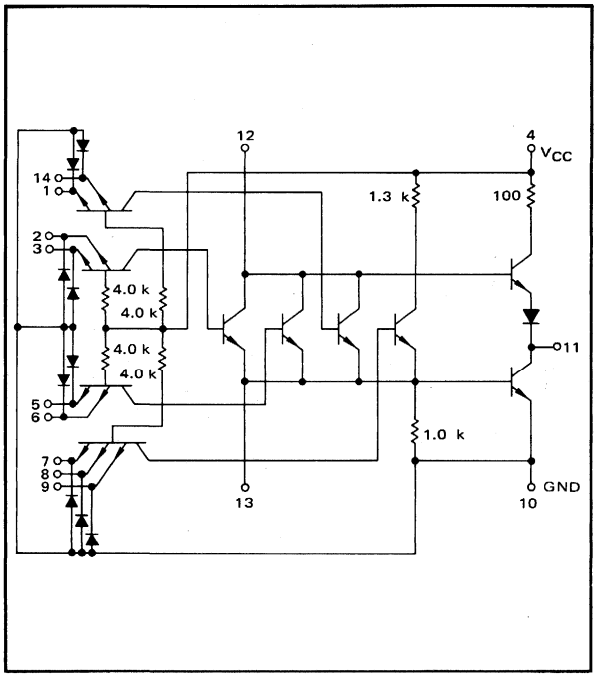
@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC508*, MC558	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC408*, MC458	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC508, MC558 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC408, MC458 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,10
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,10
Output																												
Output Voltage	V_{out} "0"	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	3	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	3	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	1,2,10
Short-Circuit Current	I_{SC}	3	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	3	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,5,8,10,12
Power Supply Drain	I_{PDH}	4	-	24	-	24	-	24	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	12	-	12	-	12	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,5,8,10,12
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,3	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Turn-Off Delay	t_{off}	1,3	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Rise Time	t_r	1,3	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Fall Time	t_f	1,3	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10

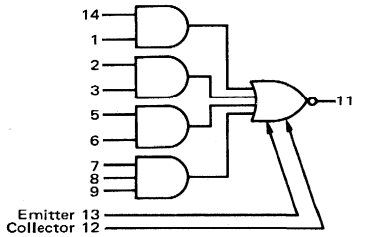
* Prime Fan-Out.
† Ground inputs to gates not under test, during ALL tests unless otherwise noted.
‡ The inputs to all gates must be ungrounded.

EXPANDABLE 4-WIDE
2-2-2-3 INPUT
"AND-OR-INVERT" GATE

MC501 · MC551
MC401 · MC451



This device consists of three 2-input and one 3-input AND gates internally ORed together and then inverted to provide the output. The common ORing nodes are available for expansion and up to 10 AND gates can be ORed together using the MC509 and the MC510 series expanders. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (\text{Expanders})}$

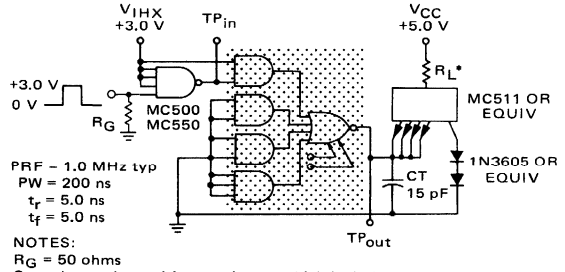
Negative Logic:

$11 = \overline{(14 + 1) \cdot (2 + 3) \cdot (5 + 6) \cdot (7 + 8 + 9) \cdot (\text{Expanders})}$

Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC501 MC551	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC401 MC451	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

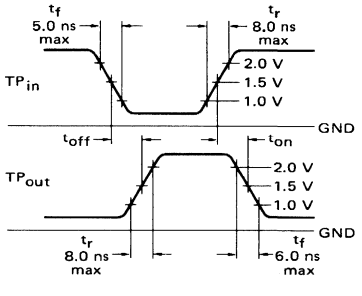


PRF – 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

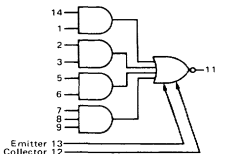
*MC501 – 260 Ω
MC551 – 570 Ω
MC401 – 330 Ω
MC451 – 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one input of the device. To complete testing, sequence through remaining inputs in a similar manner.



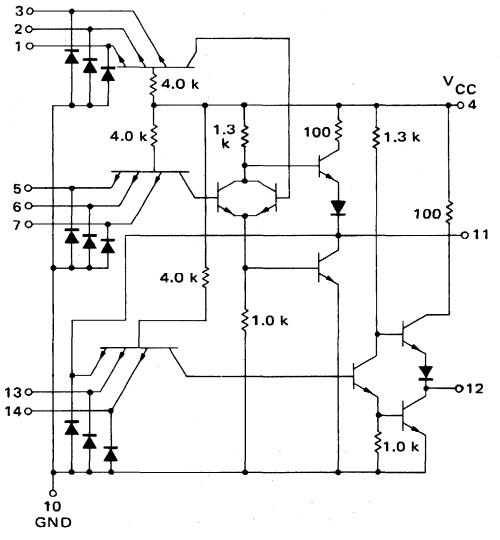
	@ Test Temperature	I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC501*, MC551	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC401*, MC451	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC501, MC551 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC401, MC451 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV_{in}"0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
	BV_{in}"1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14
Output																												
Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	2,3,5,6,7,8,9,10
	V_{out} "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7,8,9,10
Leakage Current	I_{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6,7,8,9,10,14
Short-Circuit Current	I_{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 2, 3, 5, 6, 7,8,9, 10,11,14
Output Voltage	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
	V_{OH}	11	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	12	-	-	-	-	-	12	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Power Supply Drain	I_{PDH}	4	-	9.0	-	9.0	-	9.0	-	11	-	11	-	11	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1, 11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Turn-Off Delay	t_{off}	1, 11	-	-	-	23	-	-	-	-	-	23	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Rise Time	t_r	1, 11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Fall Time	t_f	1, 11	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10

* Prime Fan-Out.

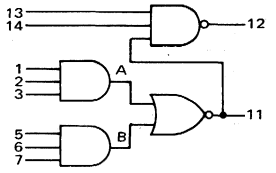
2-WIDE 3-INPUT "AND-OR-INVERT" GATE WITH GATED COMPLEMENT

MC503 · MC553
MC403 · MC453



Pin 11 is an output terminal and should not be used as an input.

This device is the only gate of the basic positive AND-OR-INVERT series that includes an additional 3-input AND-INVERT function on the output. This configuration provides the output and a gated complement in a single package. This device is useful in the design of adders, subtracters and one-shot multivibrators.



Positive Logic

$11 = \overline{(1\cdot2\cdot3) + (5\cdot6\cdot7)}$

$12 = \overline{11}\cdot13\cdot14$

$12 = (1\cdot2\cdot3) + (5\cdot6\cdot7) + \overline{13} + \overline{14}$

Total Power Dissipation = 35 mW typ/pkg

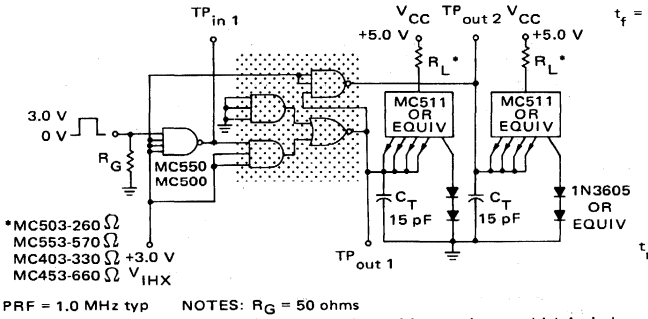
Propagation Delay Times = 11 ns typ (Pin 1 to Pin 11)
10 ns typ (Pin 11 to Pin 12)

TRUTH TABLE

A	B	OUTPUT PIN # 11	PIN #13	PIN #14	OUTPUT PIN # 12
0	1	0	0	0	1
1	0	0	0	1	1
0	1	0	1	0	1
1	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC503 MC553	1 (-1.33 mA)	15 MC500 Series Gates (20 mA) 7 MC500 Series Gates (10 mA)	-55°C to +125°C
MC403 MC453	1 (-1.66 mA)	12 MC400 Series Gates (20 mA) 6 MC400 Series Gates (10 mA)	0°C to +75°C

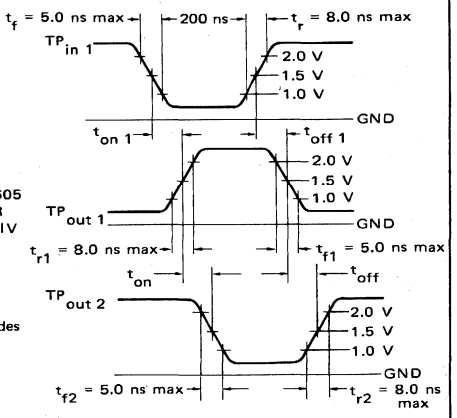
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 8.0 ns max
t_f = 5.0 ns max

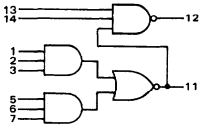
NOTES: R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the AND-OR-INVERT gate, plus one input of the gated complement. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC503*, MC553	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-
MC403*, MC453	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-

Characteristic	Symbol	Pin Under Test	MC503, MC553 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC403, MC453 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,5,6,7,10
		14	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	13	-	-	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6, 7,10
		14	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	-	-	4	-	-	10,13
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,10
		14	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6, 7,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	5,6,7,10
		14	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	14	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6, 7,10
		14	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	14	-	-	-	-	-	-	4	-	-	10,13
Output																												
Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	5,6,7,10
		12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	14	-	-	4	-	-	1,2,3,5,6, 7,10
	V_{out} "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	5,6,7,10
		12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	14	-	4	-	-	1,2,3,5,6, 7,10
Leakage Current	I_{OLK}	11	-	1250	-	1250	-	1250	-	1250	-	1250	-	1250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6, 7,10
		12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	10,13,14
Short-Circuit Current	I_{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10,11
		12	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10,12,13,14
Output Voltage	V_{OH}	11	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	5,6,7,10
		12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	14	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	5,6,7,10
		12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	14	-	-	-	-	4	-	-	1,2,3,5,6, 7,10

ELECTRICAL CHARACTERISTICS (continued)

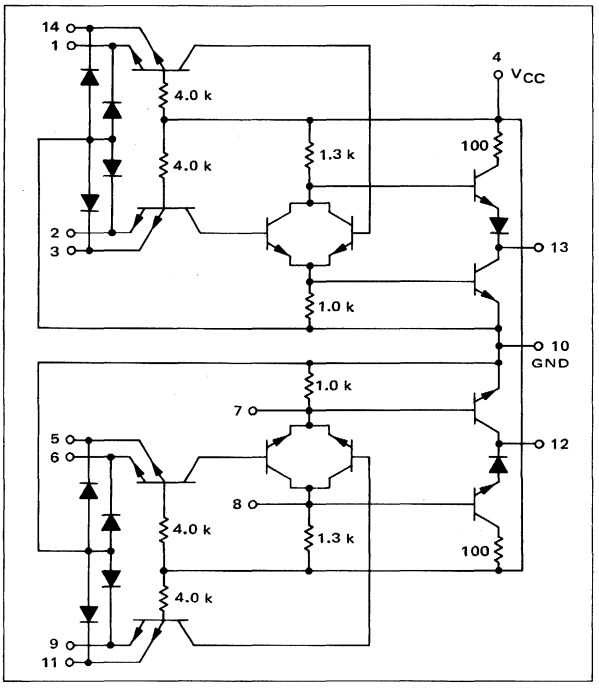
@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC503*, MC553	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	8.0	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	8.0	-
MC403*, MC453	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	7.0	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	7.0	-

Characteristic	Symbol	Pin Under Test	MC503, MC553 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC403, MC453 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	34	-	34	-	34	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6, 7,10,13,14
Power Supply Drain	I_{PDH}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	10	-	10	-	10	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10
		4	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6, 7,10,13,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	$t_{on\,1}$	1, 11	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	$t_{on\,2}$	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Turn-Off Delay	$t_{off\,1}$	1, 11	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	$t_{off\,2}$	11, 12	-	-	-	20	-	-	-	-	-	20	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Rise Time	$t_{r\,1}$	1, 11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	$t_{r\,2}$	11, 12	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
Fall Time	$t_{f\,1}$	1, 11	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10
	$t_{f\,2}$	11, 12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3, 13,14	5,6,7,10

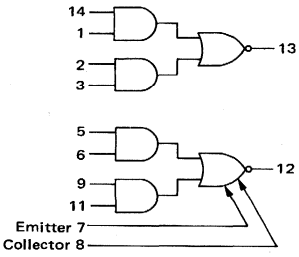
* Prime Fan-Out

EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

MC520 • MC570
MC420 • MC470



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC509 or MC510 expander series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

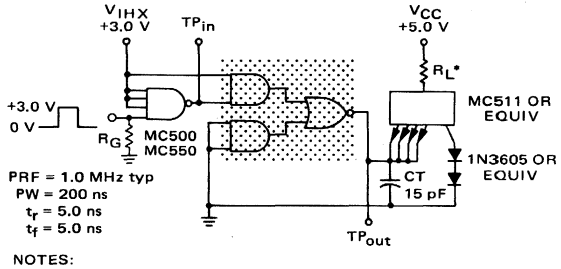
$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$

$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (\text{Expander})}$

Total Power Dissipation = 40 mW typ/pkg
Propagation Delay Time = 12 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC520 MC570	1	(−1.33 mA)	15 7	MC500 series Gates MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC420 MC470	1	(−1.66 mA)	12 6	MC400 series Gates MC400 series Gates	(20 mA) (10 mA)	0° to +75°C

SWITCHING TIME TEST CIRCUIT

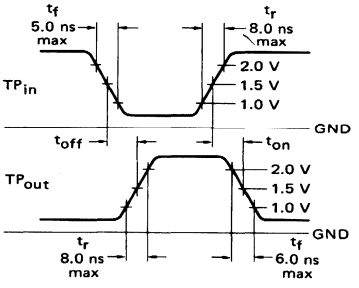


PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
When checking expander side, expander pins should be open.

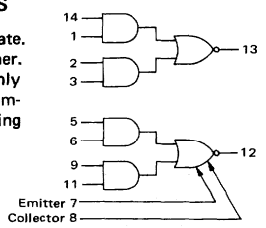
*MC520 — 260 Ω
MC570 — 570 Ω
MC420 — 330 Ω
MC470 — 660 Ω

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

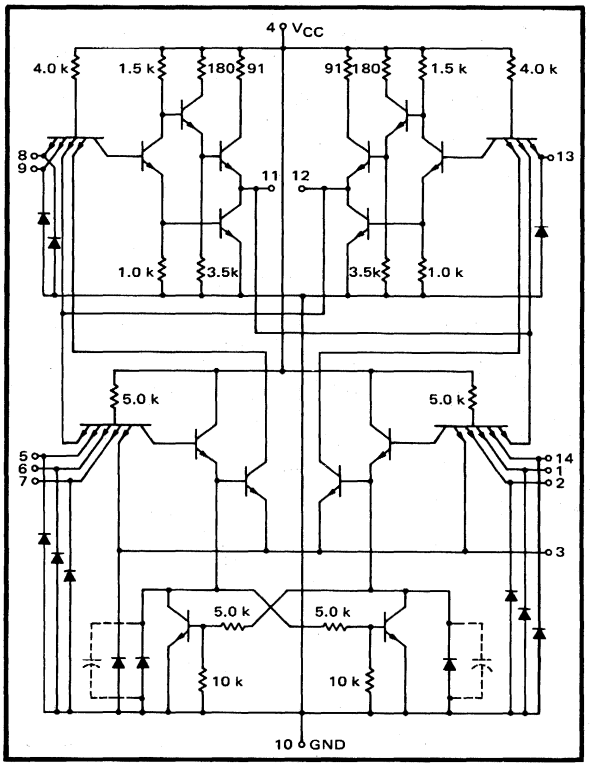


@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	V_{th1} Volts	V_{th0} Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC520*, MC570	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0	-	-
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0	8.0	3.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0	-	-
MC420*, MC470	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0	-	-
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0	7.0	3.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC520, MC570 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC420, MC470 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,14
Output																												
Output Voltage	V_{out} "0"	13	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4	-	-	2,3,10
	V_{out} "1"	13	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	1	-	4	-	-	2,3,10
Leakage Current	I_{OLK}	13	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	13	4	-	-	1,2,3,10,14
Short-Circuit Current	I_{SC}	13	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10, 13,14
Output Voltage	V_{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	-	4	-	-	2,3,10
	V_{OH}	13	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	13	-	1	-	-	-	-	-	4	-	-	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14
Power Supply Drain	I_{PDH}	4	-	14	-	14	-	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	7.0	-	7.0	-	7.0	-	8.0	-	8.0	-	8.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,13	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Turn-Off Delay	t_{off}	1,13	-	-	-	22	-	-	-	-	-	22	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Rise Time	t_r	1,13	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Fall Time	t_f	1,13	-	-	-	6.0	-	-	-	-	-	6.0	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10

* Prime Fan-Out
† Ground inputs to gates not under test during ALL tests unless otherwise noted.
‡ The inputs to all gates must be ungrounded.

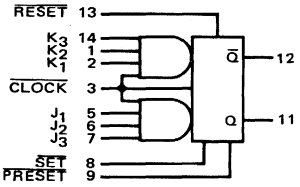
MC515 · MC565
MC415 · MC465



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct $\overline{SET}$, $\overline{PRE\text{-}SET}$, and $\overline{RESET}$ are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and $\overline{Q}$ outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$, $\overline{PRESET}$, or $\overline{RESET}$ inputs.

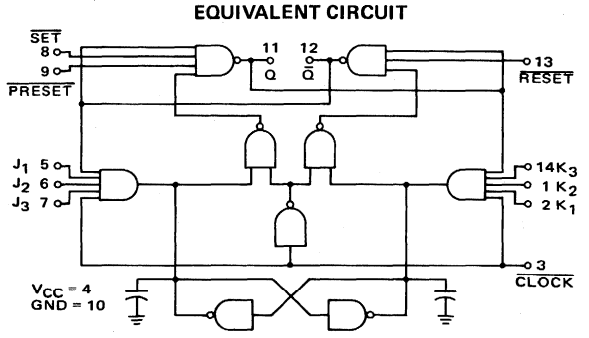
Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

EQUIVALENT CIRCUIT



Total Power Dissipation ≐ 40 mW typ/pkg
Switching Times:
t_{on} = 25 ns typ
t_{off} = 13 ns typ

SERIES	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC515 MC565	1.5	1	(-2.0 mA)	(−1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	−55°C to +125°C
MC415 MC465	1.5	1	(−2.5 mA)	(−1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20ns.

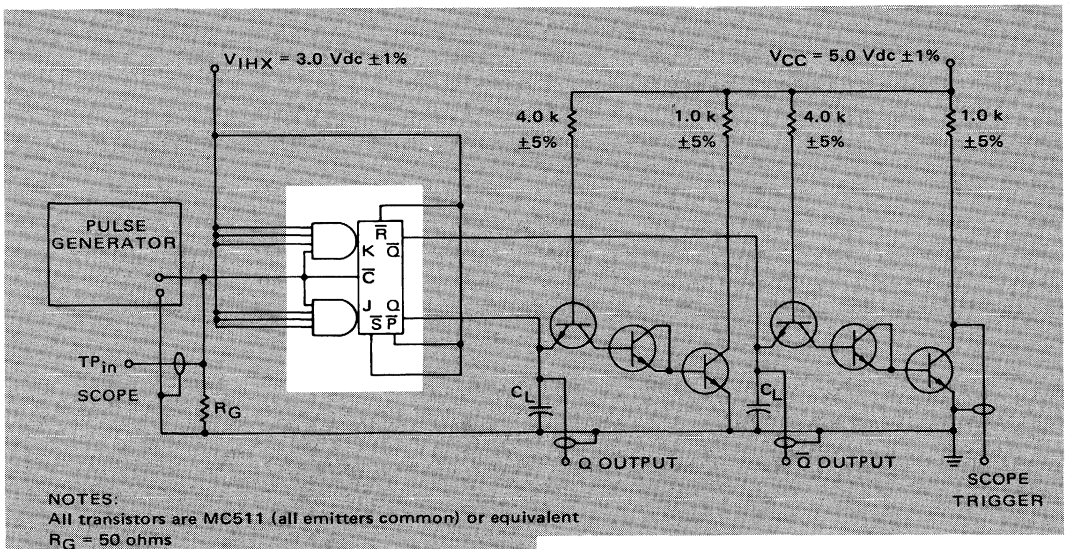
Provides direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{Q}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

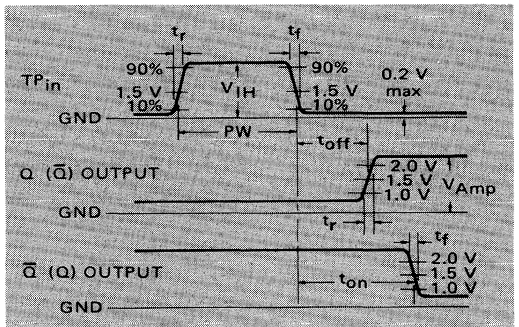
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{PRESET}$ and $\overline{SET}$ are tied to $\overline{Q}$; $\overline{RESET}$ is tied to Q.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

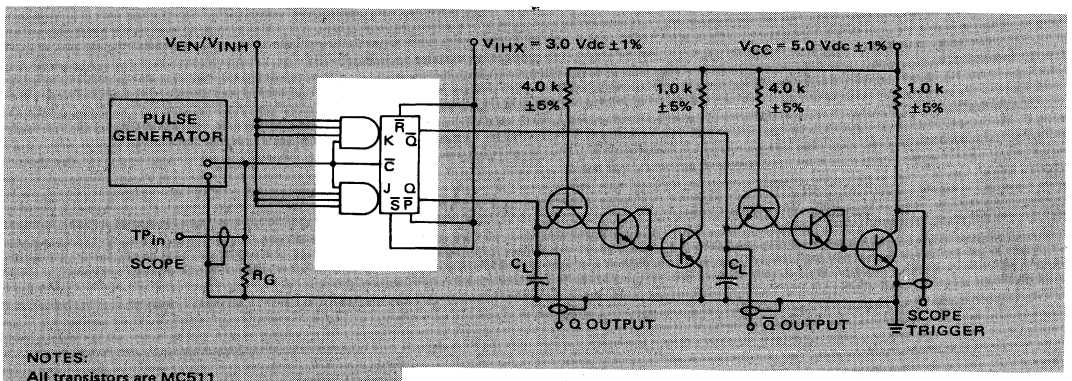
WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	20 MHz max	W
Pulse Width	PW	20 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	150 ns max	Z

INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_r	≤10	≤10	≤10	≤10	≤50	ns
t_f	≤10	≤10	≤10	≤10	150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

ENABLE MODE TEST:
The device under test shall toggle when V_{EN} = 1.8 Vdc ±1% is applied.

INHIBIT MODE TEST:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ±1% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

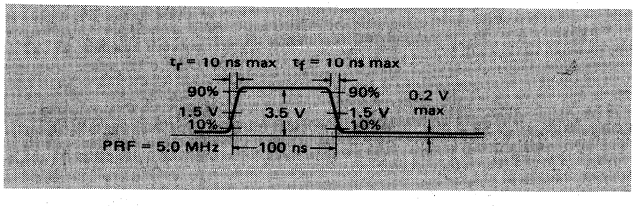
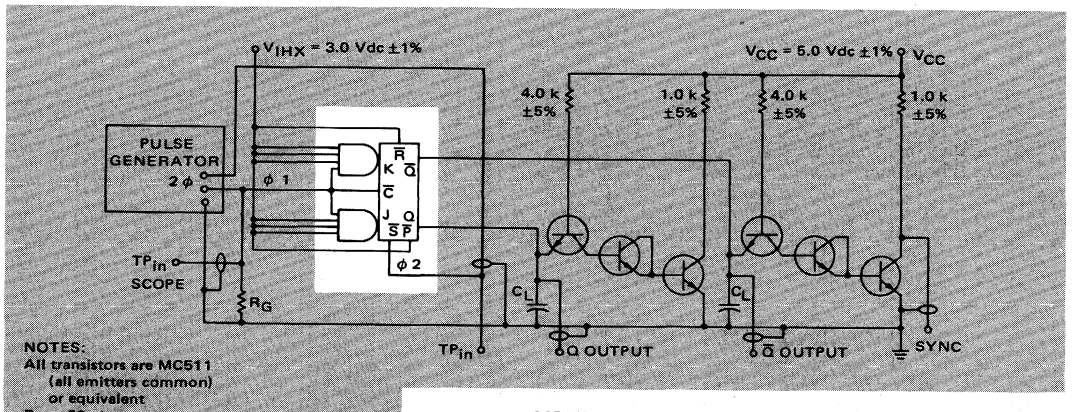


FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



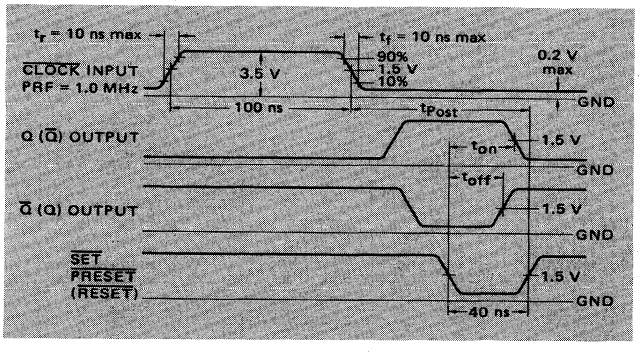
NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance
t_{Post} = Post Time

TEST PARAMETERS

SYMBOL	VALUE	UNIT
t_{Post}	120	ns min
t_{on}	40	ns max
t_{off}	20	ns max

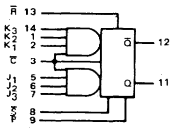
NOTE:
When t_{Post} is 120 ns, SET, PRESET or RESET pulses must actuate the device.
SET, PRESET, and RESET pulse cannot return to the high state before the required post time.
Connections shown for measuring times related to SET terminal only. To measure times at PRESET terminal apply input pulse to Pin 9 in place of Pin 8. To measure times at RESET terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	$2\ I_{in}$ mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,0}$ Volts	$V_{th\,1}$ Volts	V_{out} Volts	V_{CC} Volts
MC515☆, MC565	−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
MC415☆, MC465	0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

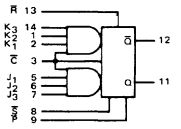
Characteristic	Symbol	Pin Under Test	MC515, MC565 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC415, MC465 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,0}$	$V_{th\,1}$	V_{out}	V_{CC}	Gnd
Input																											
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,10,11,14
		5	-		-		-		-		-		-			-	-	-	-	-	-	5	-	-	-		1,2,3,6,7,10,12,14
		8	-		-		-		-		-		-			-	-	-	-	-	-	8	-	-	-		1,2,3,5,6,7,9,10,12,14
		9	-		-		-		-		-		-			-	-	-	-	-	-	9	-	-	-		1,2,3,5,6,7,8,10,12,14
		13	-		-		-		-		-		-			-	-	-	-	-	-	13	-	-	-		1,2,3,5,6,7,10,11,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	8	-	1	-	-	-	4	10
		5	-		-		-		-		-		-			-	-	-	-	13	-	5	-	-	-		
		8	-		-		-		-		-		-			-	-	-	-		-	8	-	-	-		
		9	-		-		-		-		-		-			-	-	-	-		-	9	-	-	-		
		13	-		-		-		-		-		-			-	-	-	-	8	-	13	-	-	-		
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	8	-	-	-	-	-	4	10
		5		-		-		-		-		-		-		-	-	5	-	13	-	-	-	-	-		
		8		-		-		-		-		-		-		-	-	8	-		-	-	-	-	-		
		9		-		-		-		-		-		-		-	-	9	-		-	-	-	-	-		
		13		-		-		-		-		-		-		-	-	13	-	8	-	-	-	-	-		
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	4	2,3,5,6,7,10,11,14
		5		-		-		-		-		-		-		-	-	5	-	-	-	-	-	-	-		1,2,3,6,7,10,12,14
		8		-		-		-		-		-		-		-	-	8	-	-	-	-	-	-	-		1,2,3,5,6,7,9,10,12,14
		9		-		-		-		-		-		-		-	-	9	-	-	-	-	-	-	-		1,2,3,5,6,7,8,10,12,14
		13		-		-		-		-		-		-		-	-	13	-	-	-	-	-	-	-		1,2,3,5,6,7,10,11,14

* Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.

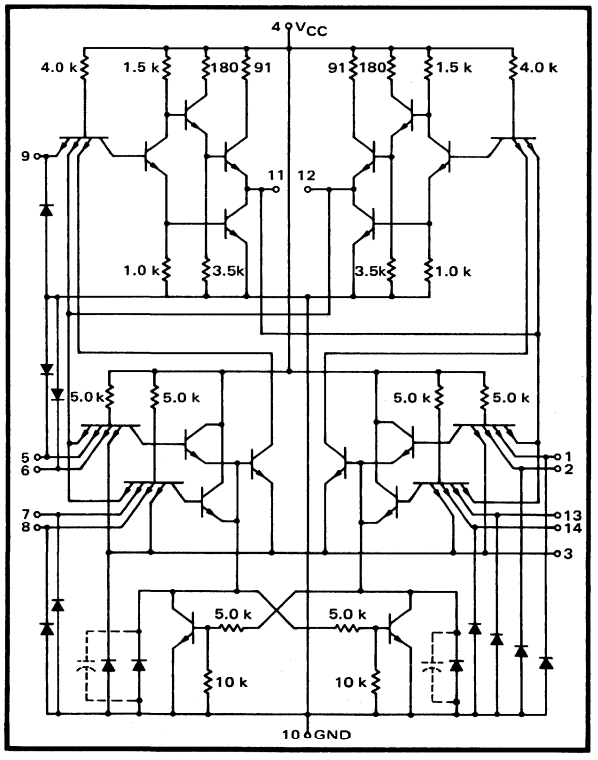


@ Test Temperature		TEST CONDITIONS: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	mA I_{in}	mA $2\,I_{in}$	Volts V_{IL}	Volts V_{IH}	Volts V_R	Volts $V_{th\,0}$	Volts $V_{th\,1}$	Volts V_{out}	Volts V_{CC}
MC515*, MC565	−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
MC415*, MC465	0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC515, MC565 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC415, MC465 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\,I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,0}$	$V_{th\,1}$	V_{out}	V_{CC}	Gnd
Clock Input																											
Forward Current	I_F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	I_L	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	13	-	3	-	-	-	4	10
		3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	8	-	3	-	-	-	4	10
Breakdown Voltage	BV_{in} "0"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	13	-	-	-	-	-	4	10
		3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	8	-	-	-	-	-	4	10
	BV_{in} "1"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	-	-	-	-	-	-	4	1,2,5,6,7,10,14
Output																											
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	13	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	-	9	-	↓	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	-	8	-	↓	3,10,13
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	13	-	-	4	8,10
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	9	-	-	↓	10,13
		11	↓	..	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	8	-	-	↓	10,13
Leakage Current	I_{OLK}	12	-	225	-	225	-	225	-	225	-	225	-	225	μAdc	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,9,10,13,14
		11	-	225	-	225	-	225	-	225	-	225	-	225	μAdc	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I_{SC}	12	-	-	-45	-90	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14
		11	-	-	-45	-90	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	-	13	-	-	-	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	9	-	-	-	-	↓	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	8	-	-	-	-	↓	3,10,13
	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	12	-	-	13	-	-	-	-	-	4	8,10
		11	↓	-		-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	9	-	-	-	-	-	↓	10,13
		11	↓	-		-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	8	-	-	-	-	-	↓	10,13
Power Requirements (Total Device)																											
Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,10,13
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,8,10

* Prime Fan-Out.

MC516 · MC566
MC416 · MC466

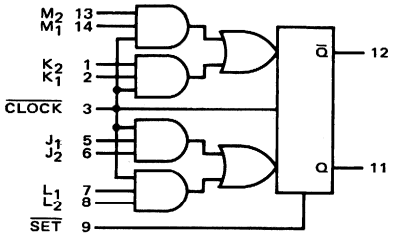


The MC516, MC566, MC416, and MC466 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct $\overline{SET}$ is also available.

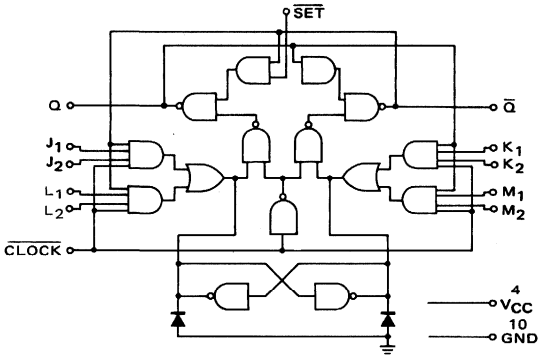
In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Q and the $\overline{Q}$ outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct $\overline{SET}$ input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



EQUIVALENT CIRCUIT



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care
Where $J = J_1 \cdot J_2$
$L = L_1 \cdot L_2$
$K = K_1 \cdot K_2$
$M = M_1 \cdot M_2$

Total Power Dissipation = 60 mW typ/pkg
Switching Times:
t_{on} = 25 ns typ
t_{off} = 13 ns typ

SERIES	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})		TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER			
MC516 MC566	3	1	(−4.0 mA)	(−1.33 mA)	15 MC500 series Gates 7 MC500 series Gates	(20 mA) (10 mA)	−55°C to +125°C
MC416 MC466	3	1	(−5.0 mA)	(−1.66 mA)	12 MC400 series Gates 6 MC400 series Gates	(20 mA) (10 mA)	0°C to +75°C

OPERATING CHARACTERISTICS

Clock fall time $\leq$ 150 ns.

Triggers on clock pulse widths $\geq$ 20 ns.

The application of a "0" state to the $\overline{SET}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state, the information in the temporary storage section is transferred; and the Q and $\overline{Q}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

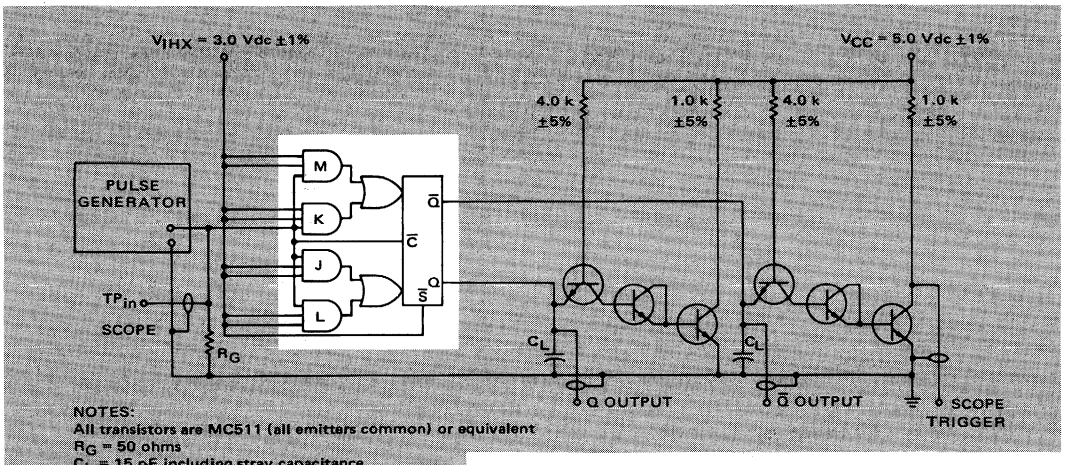
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

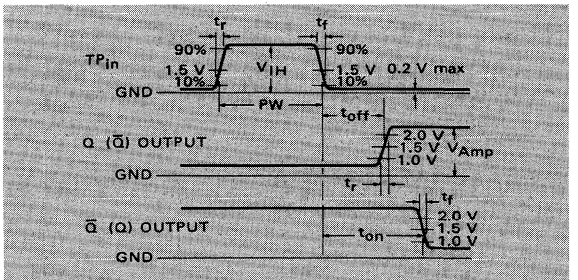
Unused $\overline{SET}$ is tied to $\overline{Q}$.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		40	ns
Rise Time	t_r	V		8.0	ns
Fall Time	t_f	V		5.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

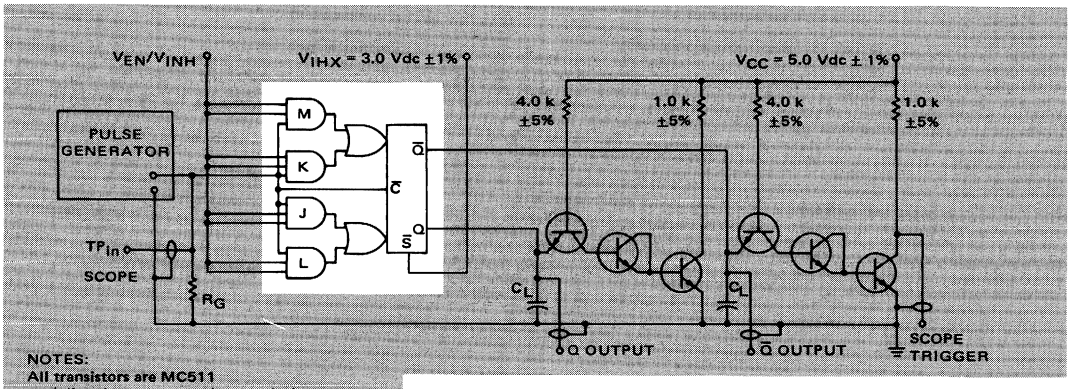
WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	20 MHz max	W
Pulse Width	PW	20 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	150 ns max	Z

INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_r	$\leq$10	$\leq$10	$\leq$10	$\leq$10	$\leq$50	ns
t_f	$\leq$10	$\leq$10	$\leq$10	$\leq$10	150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

ENABLE MODE TEST:
The device under test shall toggle when V_{EN} = 1.8 Vdc ±1% is applied.

INHIBIT MODE TEST:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ±1% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

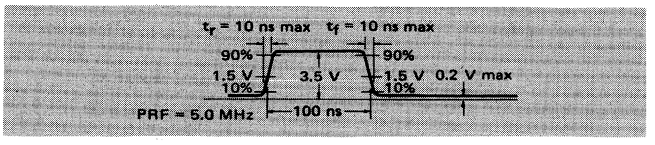
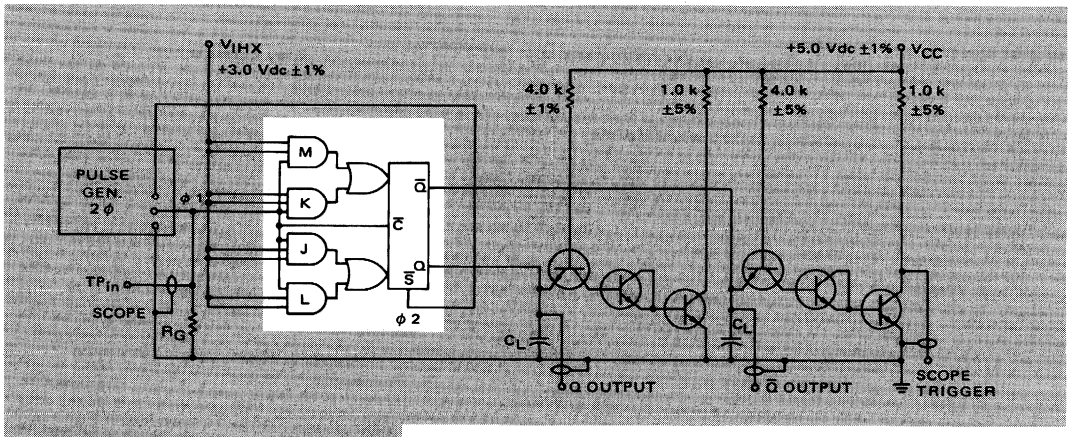


FIGURE 3 – $\overline{SET}$ TERMINAL CHARACTERISTICS TEST CIRCUIT



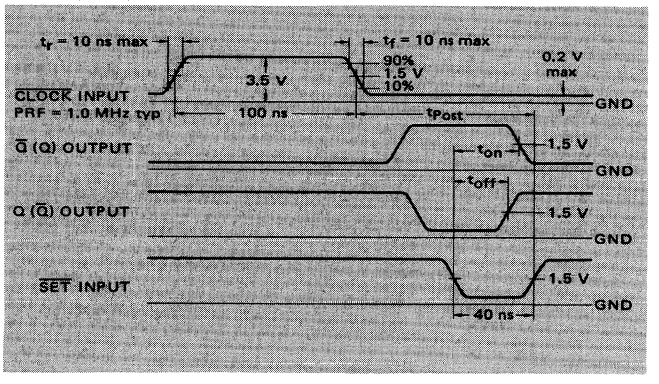
NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance
t_{Post} = Post Time

TEST PARAMETERS

SYMBOL	VALUE	UNIT
t_{Post}	120	ns min
t_{on}	40	ns max
t_{off}	20	ns max

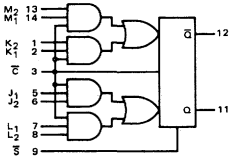
NOTE:
When t_{Post} is 120 ns, $\overline{SET}$ pulse must actuate the device. $\overline{SET}$ pulse cannot return to the high state before the required post time.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J, one K, and the $\overline{SET}$ input. The remaining J, K, L, M inputs are tested in the same manner.



	@ Test Temperature	TEST CONDITIONS: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	mA I_{in}	mA $2\,I_{in}$	mA $4\,I_{in}$	Volts V_{IL}	Volts V_{IH}	Volts V_R	Volts $V_{th\,1}$	Volts $V_{th\,0}$	Volts V_{out}	Volts V_{CC}
MC516*, MC566	−55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC416*, MC466	0°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC516, MC566 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC416, MC466 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\,I_{in}$	$4\,I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	1,2,3,6,7, 8,13,14	-	-	-	↓	5,10,11
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	↓	3,9,10,11
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,8,10,11,13,14
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	9	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	4	9,10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	5	-	-	-	↓	10,11
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	9	-	-	-	↓	10,11
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	9,10
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	10,11
		9	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	9	-	-	-	-	-	-	-	-	↓	10,11
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,10,11,13,14
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14
		9	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	9	-	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14

* Prime Fan-Out

① Momentarily ground pin prior to taking measurement at terminal.

ELECTRICAL CHARACTERISTICS (continued)

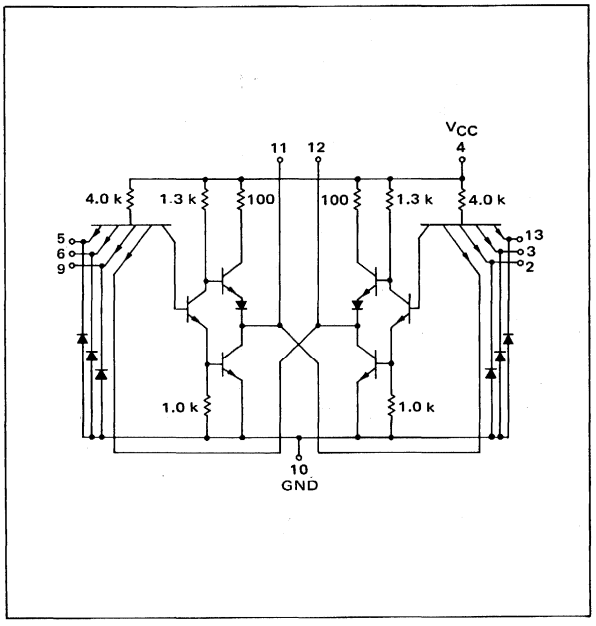
@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	$2\ I_{in}$ mA	$4\ I_{in}$ mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$* Volts	V_{out} Volts	V_{CC} Volts
MC516☆, MC566	−55°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC416☆, MC466	0°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC516, MC566 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC416, MC466 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	$4\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
Clock Input Forward Current	I_F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
Inverse Beta Current	I_L	3	-	400	-	400	-	400	-	400	-	400	-	400	mAdc	-	-	-	-	-	-	-	3	-	-	-	4	9,10
		3	-	400	-	400	-	400	-	400	-	400	-	400	mAdc	-	-	-	-	-	-	-	3	-	-	-	4	10,11
Breakdown Voltage	BV_{in} "0"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	4	10, 11
		3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	4	9,10
	BV_{in} "1"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11①	-	-	-	-	-	-	-	9	-	-	4	3, 10
	V_{out} "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	-	-	9	-	4	3,10
Leakage Current	I_{OLK}	12	-	650	-	650	-	650	-	650	-	650	-	650	μAdc	-	-	-	-	-	-	-	12	-	-	-	4	1,2,3,5,6,7,8,10,11,13,14
		11	-	650	-	650	-	650	-	650	-	650	-	650	μAdc	-	-	-	-	-	-	-	11	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I_{SC}	12	-	-	-45	-90	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13,14
		11	-	-	-45	-90	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	12	-	-	-	-	-	-	-	-	-	4	3,10,11
		11	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	11	-	-	-	-	-	-	-	-	-	4	3,10,12
	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12①	-	-	-	-	-	9	-	-	-	-	4	3,10
		11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11①	-	-	-	-	-	9	-	-	-	-	4	3,10
Breakdown Voltage	I_O	12	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	mAdc	-	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,10,11,13,14
		11	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	mAdc	-	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14
Power Requirements (Total Device) Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,12
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,11

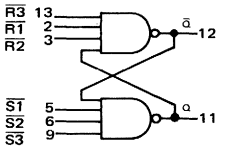
* Prime Fan-Out

① Momentarily ground pin prior to taking measurement at terminal.

MC513 · MC563
MC413 · MC463



This device consists of two independent dual 4-input NAND gates, internally cross coupled to realize a multiple input R-S flip-flop. The circuit can be used to eliminate switch contact bounce and to provide a temporary storage for data.



$\overline{R} = 2 \cdot 3 \cdot 13$

$\overline{S} = 5 \cdot 6 \cdot 9$

Positive Logic =

$11 = Q = \overline{5} + \overline{6} + \overline{9} + \overline{12}$

Total Power Dissipation = 30 mW typ/pkg

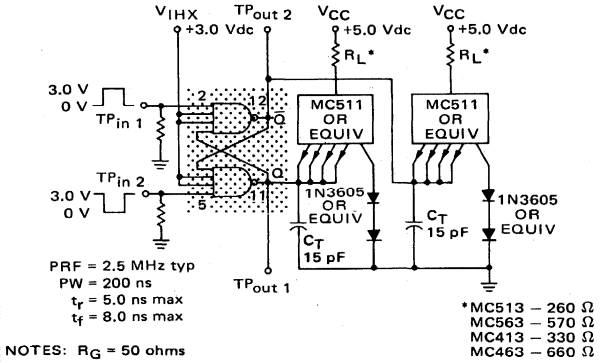
Propagation Delay Time = 20 ns typ (to change state)

TRUTH TABLE (Positive Logic)

$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
0	0	Not Permitted	
0	1	0	1
1	0	1	0
1	1	Q	$\overline{Q}$

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC513 MC563	1 (-1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	−55°C to +125°C
MC413 MC463	1 (-1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

SWITCHING TIME TEST CIRCUIT †



NOTES: R_G = 50 ohms

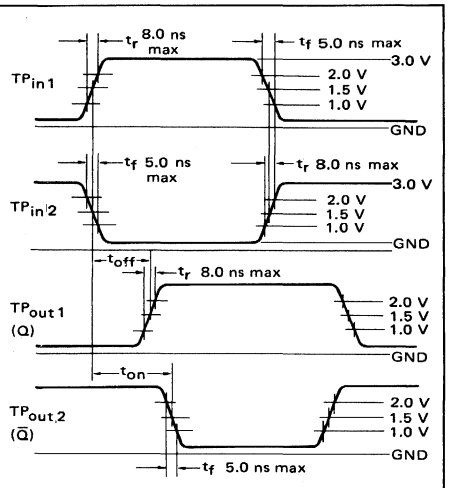
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.

Scope rise time < 1.0 ns

Probe capacitance < 5.0 pF

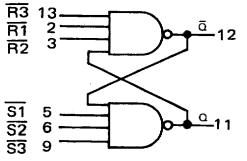
† To measure t_{on}, t_f for Q and t_{off}, t_r for $\overline{Q}$, reverse input polarities.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. The other inputs are tested in the same manner.



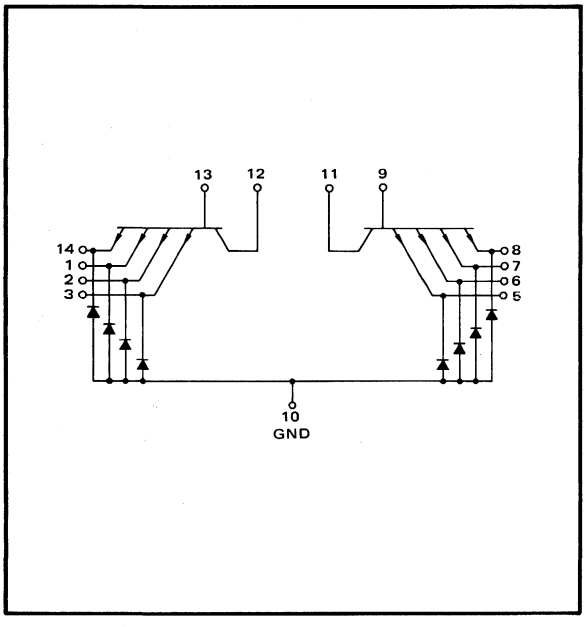
@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}
MC513*, MC563	−55°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC413*, MC463	0°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC513, MC563 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC413, MC463 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
Input																										
Forward Current	I_F	2	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	3,13	-	-	-	4	2,10
		5	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	6,9	-	-	-	4	5,10
Leakage Current	I_R	2	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	2	-	-	-	4	3,10,13
		5	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	5	-	-	-	4	6,9,10
Inverse Beta Current	I_L	2	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	2	-	-	-	4	5,6,9,10
		5	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	5	-	-	-	4	2,3,10,13
Breakdown Voltage	BV_{in}"0"	2	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	2	-	-	-	-	-	-	4	5,6,9,10
		5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	4	2,3,10,13
	BV_{in}"1"	2	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	2	-	-	-	-	-	-	4	3,10,13
		5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	-	-	-	4	6,9,10
Output																										
Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	5	-	-	4	2,3,10,13
	V_{out} "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	5	-	4	2,3,10,13
Leakage Current	I_{OLK}	11	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	-	-	-	-	-	-	-	-	11	4	5,6,9,10
Short-Circuit Current	I_{SC}	11	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	-10	-45	mAdc	-	-	-	-	-	-	-	-	-	4	5,6,9,10,11
Output Voltage	V_{OH}	11	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	11	-	5	-	-	-	-	-	4	2,3,10,13
	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	5	-	-	-	-	4	2,3,10,13
Power Requirements (Total Device)																										
Power Supply Crain	I_{PD}	4	-	-	-	9.0	-	-	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	5,6,9,10
		4	-	-	-	9.0	-	-	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	4	2,3,10,13
Switching Parameters																Pulse In	Pulse Out									
Turn-On Delay	t_{on} ‡	2, 12	-	-	-	30	-	-	-	-	-	30	-	-	ns	2, 5	12	-	-	-	-	-	-	-	4	10
Turn-Off Delay	t_{off} ‡	2, 11	-	-	-	20	-	-	-	-	-	20	-	-	ns	2, 5	11	-	-	-	-	-	-	-	4	10
Rise Time	t_r ‡	2, 11	-	-	-	8.0	-	-	-	-	-	8.0	-	-	ns	2, 5	11	-	-	-	-	-	-	-	4	10
Fall Time	t_f ‡	2, 12	-	-	-	5.0	-	-	-	-	-	5.0	-	-	ns	2, 5	12	-	-	-	-	-	-	-	4	10

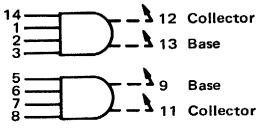
* Prime Fan-Out

‡ To measure t_{on}, t_f for Q and t_{off}, t_r for $\overline{Q}$, reverse input polarities.

MC511 · MC561
MC411 · MC461



This device consists of two independent 4-emitter input transistors, each of which performs the positive logic AND function when used in conjunction with expandable gates. The base and collector of each device is available for expansion. Using the MC511 with the MC506 expandable gate, the number of AND inputs can be expanded to 20.



Total Power Dissipation = 0 mW typ/pkg

Propagation Delay Time:

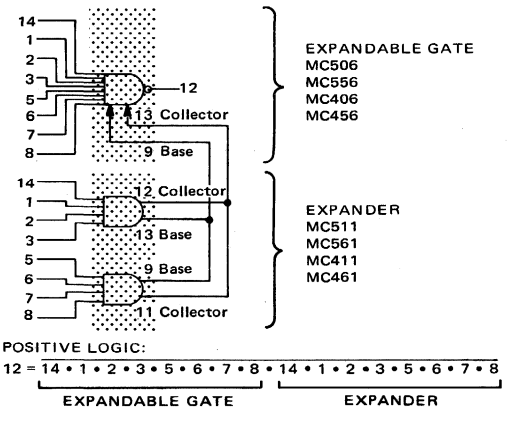
Δt_{pd} = +3.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = +1.6 ns/pF typ
Caused by additional capacitance at expander points.

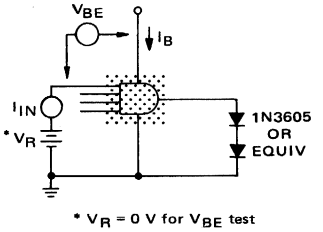
SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC511 MC561	1 (−1.33 mA)	−55°C to +125°C
MC411 MC461	1 (−1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 8-INPUT "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.



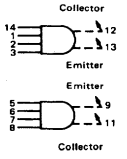
BV_{in} "0", V_{BE}, I_L TEST CIRCUIT



* V_R = 0 V for V_{BE} test

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CONDITIONS mA I_{B1}	I_{B2}	I_{in}	Volts V_R	V_{DC}	V_C
MC511, MC561	−55°C	1.33	1.0	1.0	4.5	**	1.5
	+25°C	1.33	1.0	1.0	4.5	**	1.5
	+125°C	1.33	1.0	1.0	4.5	**	1.5
MC411, MC461	0°C	1.66	1.0	1.0	4.5	**	1.5
	+25°C	1.66	1.0	1.0	4.5	**	1.5
	+75°C	1.66	1.0	1.0	4.5	**	1.5

Characteristic	Symbol	Pin Under Test	MC511, MC561 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC411, MC461 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{B1}	I_{B2}	I_{in}	V_R	V_{DC}	V_C	Gnd†
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	13	-	-	1	-	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	13	-	1	12	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	13	1	-	12	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	13	-	1	-	-	-	2,3,10,14
Base-Emitter Voltage	V_{BE}	13, 1	-	1.3	-	1.1	-	1.0	-	1.3	-	1.2	-	1.1	Vdc	13	-	-	-	12	-	1,10
Base-Collector Voltage	V_{BC}	13, 12	-	1.3	-	1.1	-	1.0	-	1.3	-	1.2	-	1.1	Vdc	-	13	-	-	-	-	10,12
Offset Voltage	V_O	12*	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	Vdc	13	-	-	-	-	-	1,10
Forward Beta	h_{FE}	12	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	-	13	-	-	-	-	12‡	1,10

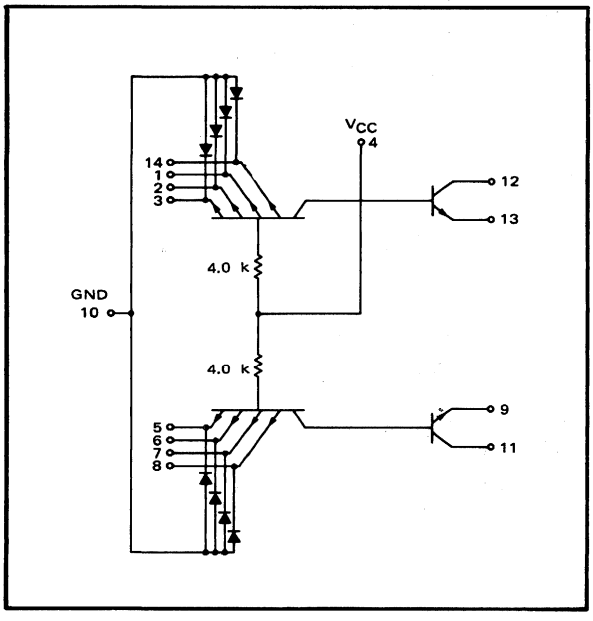
† Ground inputs to expanders not under tests during ALL tests

* Measure V_O from Pin 12 to gnd

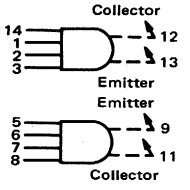
** Voltage obtained with two series diodes tied from collector to gnd.

‡ Measure I_C and calculate Beta. $\left(h_{FE} = \frac{I_C}{I_B}\right)$

MC510 · MC560
MC410 · MC460



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC509 series and the MC510 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 10 mW typ/Pkg.

Propagation Delay Time:

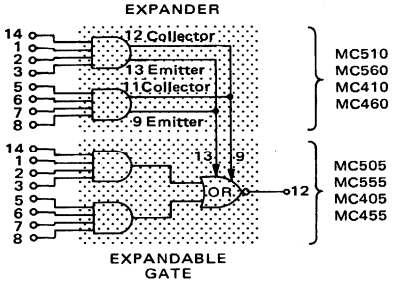
Δt_{pd} = +1.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = +1.0 ns/pF typ
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC510 MC560	1 (−1.33 mA)	−55°C to +125°C
MC410 MC460	1 (−1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

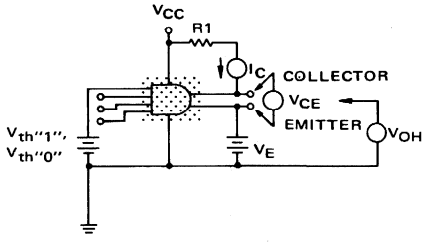
APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.



POSITIVE LOGIC

$$12 = \underbrace{\overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8)}}_{\text{EXPANDABLE GATE}} + \underbrace{\overline{(5 \cdot 6 \cdot 7 \cdot 8) + (14 \cdot 1 \cdot 2 \cdot 3)}}_{\text{EXPANDER}}$$

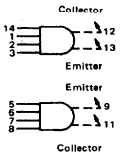
V_{CE}, V_{OH} TEST CIRCUIT



R1 = 1.3 k ohms for V_{OH} test. Adjustable to obtain I_C on V_{CE} test.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



	@ Test Temperature	TEST CONDITIONS mA I_C	mA I_{in}	Volts V_R	V_{E1}	V_{E2}	V_{E3}	V_{th1}	V_{th0}	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}
MC510 , MC560	−55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	-
	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0
	+125°C	4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
MC410 , MC460	0°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0
	+75°C	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-

Characteristic	Symbol	Pin Under Test	MC510, MC560 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC410, MC460 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	V_R	V_{E1}	V_{E2}	V_{E3}	V_{th1}	V_{th0}	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}	Gnd†
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	2,3,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10
Breakdown Voltage	BV_{in}"0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV_{in}"1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																												
Output Voltage	V_{OH}	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	-	4	-	10
	V_{CE} ①	12	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max} ②	4	-	-	-	10	-	-	-	-	-	10	-	-	mAdc	-	-	-	-	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14
Power Supply Drain	I_{PDH}	4	-	2.5	-	2.5	-	2.5	-	3.0	-	3.0	-	3.0	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	I_{PDL}	4	-	3.0	-	3.0	-	3.0	-	3.5	-	3.5	-	3.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14

* Indicated pins tied to V_{CC} thru 1.3 k ohms ± 1.0% resistor.

** Indicated pins tied to V_{CCH} thru 1.3 k ohms ± 1.0% resistor.

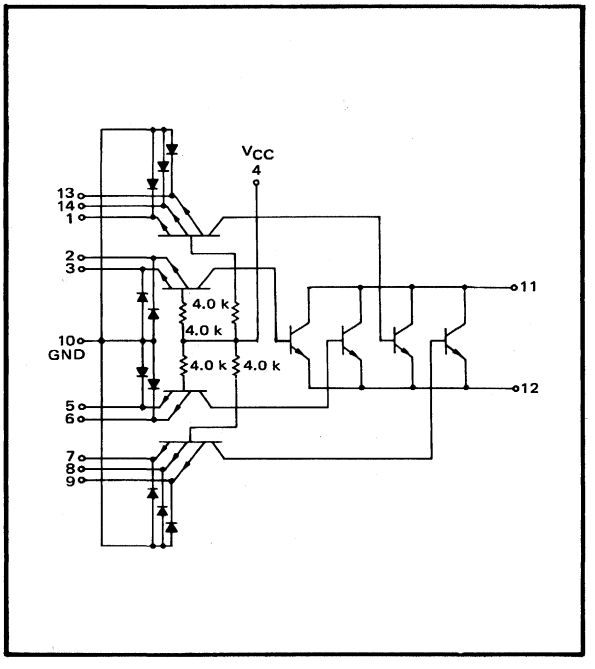
† Ground inputs to gate not under test during ALL tests, unless otherwise noted.

‡ The inputs of both gates must be ungrounded.

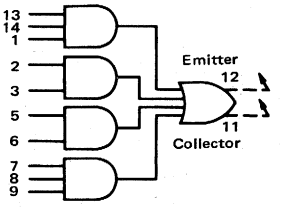
① V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).

② Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

MC509 · MC559
MC409 · MC459



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC509 series or the MC510 series expander package.



Total Power Dissipation = 20 mW/pkg.

Propagation Delay Time:

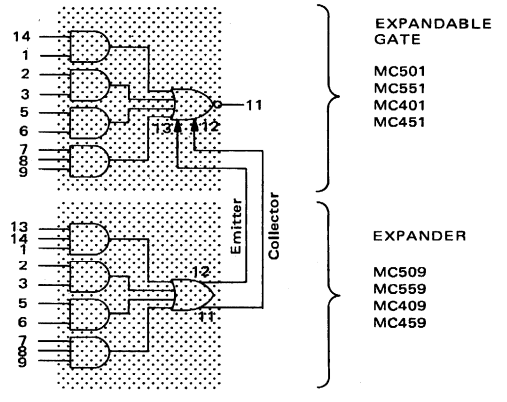
Δt_{pd} = +4.0 ns typ (1.0 ns per ORed function) When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = 1.0 ns/pF typ Caused by additional capacitance at expansion points.

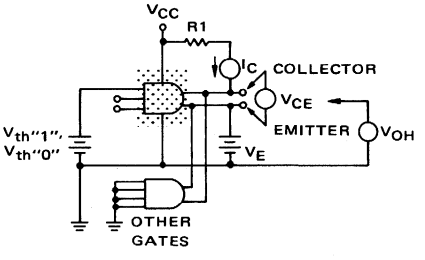
SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC509 MC559	1 (−1.33 mA)	−55°C to +125°C
MC409 MC459	1 (−1.66 mA)	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT" GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.



V_{CE}, V_{OH} TEST CIRCUIT



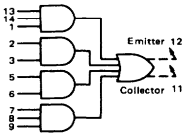
R1 = 1.3 k ohms for V_{OH} test. Adjustable to obtain I_C on V_{CE} test.

POSITIVE LOGIC:

$$12 = \underbrace{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9)}_{\text{EXPANDABLE GATE}} + \underbrace{(13 \cdot 14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9)}_{\text{EXPANDER}}$$

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.

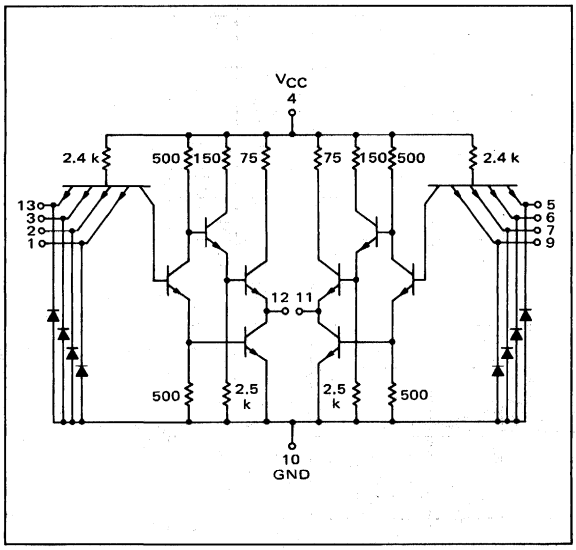


@ Test Temperature		TEST CONDITIONS mA I_C	mA I_{in}	Volts V_R	V_{E1}	V_{E2}	V_{E3}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}
MC509, MC559	−55°C	4.0	1.0	4.5	1.00	0.90	0.8	2.0	1.0	5.5	*	-	5.0	-
	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.7	1.2	5.5	*	**	5.0	8.0
	+125°C	4.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
MC409, MC459	0°C	4.0	1.0	4.5	0.90	0.80	0.8	1.9	1.1	5.5	*	-	5.0	-
	+25°C	4.0	1.0	4.5	0.85	0.75	0.8	1.8	1.2	5.5	*	**	5.0	7.0
	+75°C	4.0	1.0	4.5	0.75	0.65	0.8	1.7	1.1	5.5	*	-	5.0	-

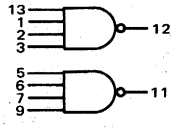
Characteristic	Symbol	Pin Under Test	MC509, MC559 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC409, MC459 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	V_R	V_{E1}	V_{E2}	V_{E3}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}	Gnd
Input																												
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	2,3,5,6,7, 8,9,13,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9, 10,13,14
Output																												
Output Voltage	V_{OH}	11	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10
	V_{CE} ①	11	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	11	-	-	12	-	-	1	-	-	-	-	4	-	2,3,5,6,7,8,9,10
Leakage Current	I_{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	20	-	-	-	-	-	20	-	-	mAdc	-	-	-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I_{PDH}	4	-	5.0	-	5.0	-	5.0	-	6.0	-	6.0	-	6.0	mAdc	-	-	-	-	-	12	-	-	-	-	-	4	-	10
	I_{PDL}	4	-	6.0	-	6.0	-	6.0	-	7.0	-	7.0	-	7.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14

* Indicated pins tied to V_{CC} thru 1.3 kohms ± 1.0% resistor.
** Indicated pins tied to V_{CCH} thru 1.3 kohms ± 1.0% resistor.
① V_{CE} is referenced to the emitter Voltage (Pin 12).

MC507 • MC557
MC407 • MC457



Each of the two independent drivers in the package consists of a 4-input AND gate driving an output inverter. The output inverter is capable of supplying twice the drive of the basic gates. The line driver is especially useful for driving high capacitive loads or for driving large fan-outs such as the numerous clock inputs of large counters.



Positive Logic:
$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

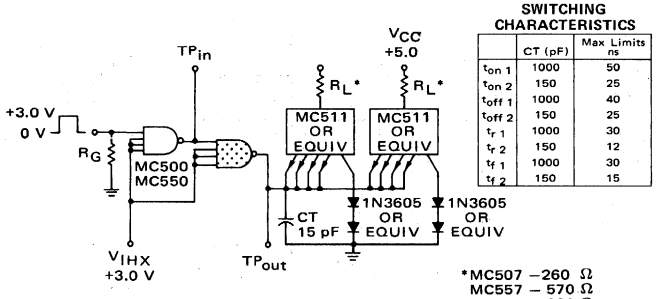
Negative Logic:
$12 = \overline{1 + 2 + 3 + 13}$

Total Power Dissipation = 60 mW typ/pkg
Propagation Delay Time = 25 ns typ @ 1000 pF Load

SERIES	INPUT LOADING FACTOR (I_F)	OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
MC507 MC557	1.5 (-2.0 mA)*	30 MC500 series Gates (40 mA) 15 MC500 series Gates (20 mA)	−55°C to +125°C
MC407 MC457	1.5 (-2.5 mA)*	24 MC400 series Gates (40 mA) 12 MC400 series Gates (20 mA)	0°C to +75°C

*Use I_F value of gate being driven (-1.33 or -1.66) to calculate output drive capability of line driver.

SWITCHING TIME TEST CIRCUIT



SWITCHING CHARACTERISTICS

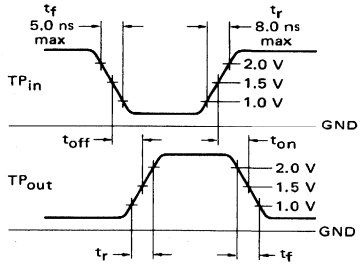
	CT (pF)	Max Limits ns
$t_{on\ 1}$	1000	50
$t_{on\ 2}$	150	25
$t_{off\ 1}$	1000	40
$t_{off\ 2}$	150	25
$t_{r\ 1}$	1000	30
$t_{r\ 2}$	150	12
$t_{f\ 1}$	1000	30
$t_{f\ 2}$	150	15

*MC507 −260 Ω
MC557 − 570 Ω
MC407 − 330 Ω
MC457 − 660 Ω

PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns max
t_f = 5.0 ns max

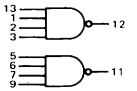
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one device. The other device is tested in the same manner. Further, test procedures are shown for only one input of the device under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	$V_{out\,1}$	$V_{out\,2}$	V_{OL}	V_{CC}	V_{CCH}	V_{IHX}
MC507*, MC557	−55°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	2.0	1.0	5.5	-	-	5.0	-	-
	+25°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.7	1.2	5.5	6.5	8.0	5.0	8.0	3.0
	+125°C	40	20	-3.0	-1.5	1.0	0.45	2.8	4.5	1.4	0.9	5.5	-	-	5.0	-	-
MC407*, MC457	0°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.9	1.1	5.5	-	-	5.0	-	-
	+25°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.8	1.2	5.5	6.5	8.0	5.0	7.0	3.0
	+75°C	40	20	-2.4	-1.2	1.0	0.45	3.0	4.5	1.7	1.1	5.5	-	-	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC507, MC557 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC407, MC457 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	$V_{out\,1}$	$V_{out\,2}$	V_{OL}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																													
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3,13	-	-	-	-	-	4	-	-	1,10
Input Leakage Current	I_R	1	-	200	-	200	-	200	-	200	-	200	-	200	μAdc	-	-	-	-	-	1	-	-	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	I_L	1	-	200	-	200	-	200	-	200	-	200	-	200	μAdc	-	-	-	-	-	1	-	-	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	-	-	2,3,10,13
Output																													
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	-	-	4	-	-	10
Low Current MC507/407	I_{OL}	12	-	-	100	-	-	-	-	-	100	-	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	12	4	-	-	10
MC557/457		12	-	-	60	-	-	-	-	-	60	-	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	12	4	-	-	10
Breakdown Current	I_O	12	-	-	-	1.0	-	-	-	-	-	1.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	12	-	4	-	-	1,2,3,10,13
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	-	-	4	-	-	1,2,3,10,13
Short-Circuit Current	I_{SC}	12	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	-50	-150	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10,12,13
Output Voltage	V_{OH}	12	2.8	-	3.2	-	3.35	-	3.0	-	3.1	-	3.15	-	Vdc	-	12	-	1	-	-	-	-	-	-	-	4	-	-	10
	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device)																													
Maximum Power Supply Current	I_{max}	4	-	-	-	15	-	-	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I_{PDH}	4	-	28	-	28	-	28	-	34	-	34	-	34	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	9	-	9	-	9	-	11	-	11	-	11	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10
Switching Parameters																Pulse In	Pulse Out												
Turn-On Delay	t_{on} ①	1,12	-	-	-	50 ①	-	-	-	-	-	50 ①	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10
Turn-Off Delay	t_{off} ①	1,12	-	-	-	40 ①	-	-	-	-	-	40 ①	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10
Rise Time	t_r ①	1,12	-	-	-	30 ①	-	-	-	-	-	30 ①	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10
Fall Time	t_f ①	1,12	-	-	-	30 ①	-	-	-	-	-	30 ①	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	4	-	2,3,13	10

* Prime Fan-Out.
† Ground inputs to gates not under test during ALL tests, unless otherwise noted.
‡ The inputs to all gates must be ungrounded.
①Values @ 1000 pF load.

MTTL II

INTEGRATED CIRCUITS
MC2100/MC2000 SERIES

MTTL II

INTEGRATED CIRCUITS

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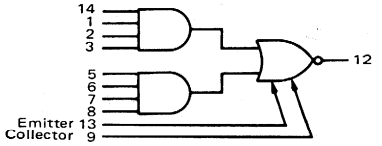
NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 5.0 Vdc, T_A = 25°C

Function	Type		Output Loading Factor Each Output		Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
	Case 609, 93 0 to +75°C	Case 609 -55 to +125°C	MC2000 Series	MC2100 Series			
Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2000 MC2050	MC2100 MC2150	9 5	11 6	7.0	27	4-66
Quad 2-Input NAND Gate	MC2001 MC2051	MC2101 MC2151	9 5	11 6	6.0	88	4-68
4-Wide 3-2-2-3 Input Expander for AND-OR-INVERT Gates	MC2002 MC2052	MC2102 MC2152	9 5	11 6	—	28	4-87
Dual 4-Input NAND Gate	MC2003 MC2053	MC2103 MC2153	9 5	11 6	6.0	44	4-64
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2004 MC2054	MC2104 MC2154	9 5	11 6	7.0	36	4-70
Single 8-Input NAND Gate	MC2005 MC2055	MC2105 MC2155	9 5	11 6	8.0	22	4-62
Dual 4-Input Expander for AND-OR-INVERT Gates	MC2006 MC2056	MC2106 MC2156	9 5	11 6	—	14	4-85
Triple 3-Input NAND Gate	MC2007 MC2057	MC2107 MC2157	9 5	11 6	6.0	66	4-72
AND J-K Flip-Flop	MC2009 MC2059	MC2109 MC2159	9 5	11 6	f = 30 MHz	40	4-76
OR J-K Flip-Flop	MC2010 MC2060	MC2110 MC2160	9 5	11 6	f = 30 MHz	50	4-81
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2013 MC2063	MC2113 MC2163	9 5	11 6	8.0	58	4-74

GATES

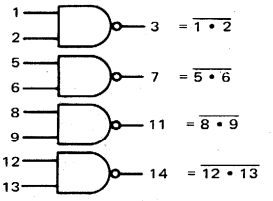
MC2000/MC2050
MC2100/MC2150
Expandable 2-Wide 4-Input AND-OR-INVERT Gate



$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8) + \ldots}$

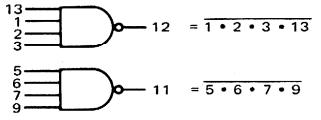
t_{pd} = 7.0 ns typ
P_D = 27 mW typ/Pkg

MC2001/MC2051
MC2101/MC2151
Quad 2-Input NAND Gate



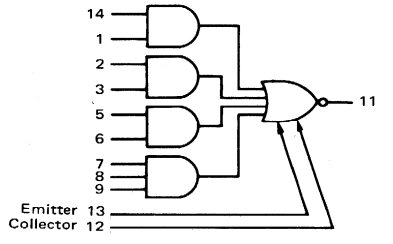
t_{pd} = 6.0 ns typ
P_D = 88 mW typ/Pkg

MC2003/MC2053
MC2103/MC2153
Dual 4-Input NAND Gate



t_{pd} = 6.0 ns typ
P_D = 44 mW typ/Pkg

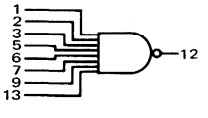
MC2004/MC2054
MC2104/MC2154
Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate



$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + \ldots}$

t_{pd} = 7.0 ns typ
P_D = 36 mW typ/Pkg

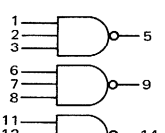
MC2005/MC2055
MC2105/MC2155
Single 8-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

t_{pd} = 8.0 ns typ
P_D = 22 mW typ/Pkg

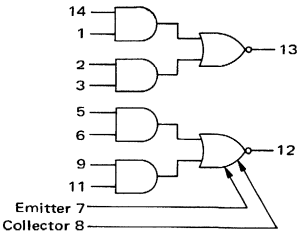
MC2007/MC2057
MC2107/MC2157
Triple 3-Input NAND Gate



$5 = \overline{1 \cdot 2 \cdot 3}$

t_{pd} = 6.0 ns typ
P_D = 66 mW typ/Pkg

MC2013/MC2063
MC2113/MC2163
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate

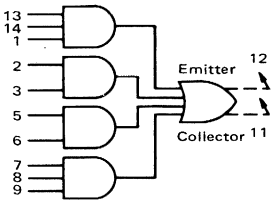


$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$
$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + \ldots}$

t_{pd} = 8.0 ns typ P_D = 58 mW typ/Pkg

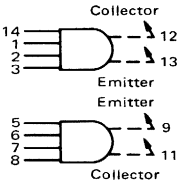
EXPANDERS

MC2002/MC2052
MC2102/MC2152
4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates



P_D = 28 mW typ/Pkg

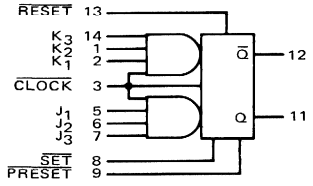
MC2006/MC2056
MC2106/MC2156
Dual 4-Input Expander For AND-OR-INVERT Gates



P_D = 14 mW typ/Pkg

FLIP-FLOPS

MC2009/MC2059
MC2109/MC2159
AND J-K Flip-Flop

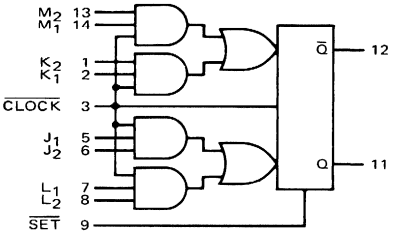


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

f = 30 MHz
P_D = 40 mW

MC2010/MC2060
MC2110/MC2160
OR J-K Flip-Flop



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care
Where $J = J_1 \cdot J_2$
$L = L_1 \cdot L_2$
$K = K_1 \cdot K_2$
$M = M_1 \cdot M_2$

f = 30 MHz
P_D = 50 mW

MTTL II

GENERAL INFORMATION SECTION

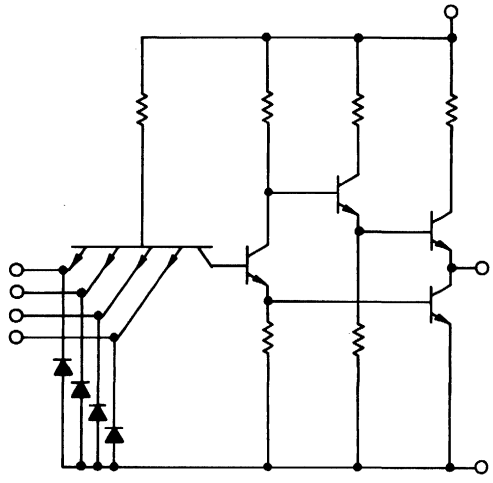
INTRODUCTION

MTTL II transistor-transistor logic is a high-speed, high-noise-immunity family of saturating integrated logic circuits.

The MTTL II family provides a speed extension of the medium-speed MTTL family. The circuits in the MTTL II family are identified by a multiple emitter input transistor and a two-stage active "pull-up" in the upper output network as shown in Figure 1.

The multiple emitter input configuration offers the maximum amount of logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The two-stage output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allow high-speed operation while driving large capacitive loads.

FIGURE 1 – TYPICAL MTTL II CIRCUIT



MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage – Continuous MC2100 Series MC2000 Series	+8.0 +7.0	Vdc
Supply Operating Voltage Range	4.5 to 6.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range MC2100 Series MC2000 Series	-55 to +125 0 to +75	°C
Storage Temperature Range Flat Package Plastic Package	-65 to +200 -55 to +125	°C
Maximum Junction Temperature MC2100 Series MC2000 Series	 +175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Ceramic Flat Package Plastic Dual-In-Line	 0.09 0.15	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Ceramic Flat Package Plastic Dual-In-Line	 0.26 0.30	°C/mW

TYPICAL CHARACTERISTICS

The following summary presents the typical operating characteristics of the MTTL II family. Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.

Supply Voltage Operating Range = 4.5 to 6.0 volts

Operating Temperature Range:
MC2100/2150 Series = −55 to +125°C
MC2000/2050 Series = 0 to +75°C

Output Drive Capability
Other Gates (Output Loading Factor):
MC2100 Series = 11 MC2100 or MC2150 Series Gates.
MC2150 Series = 6 MC2100 or MC2150 Series Gates.
MC2000 Series = 9 MC2000 or MC2050 Series Gates.
MC2050 Series = 5 MC2000 or MC2050 Series Gates.

Capacitance = 600 pF

Output Impedance
High State = 10 ohms (unsaturated) nominal
Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
+5.5 volts maximum
−0.5 volt minimum

Switching Threshold = 1.5 volts nominal

Input Impedance
High State = 400 k ohms nominal
Low State = 2.5 k ohms nominal

Worst-Case DC Noise Margin
High State — MC2100/2150 series 0.700 volt minimum
MC2000/2050 series 0.600 volt minimum
Low State — MC2100/2150 series 0.650 volt minimum
MC2000/2050 series 0.650 volt minimum

Power Dissipation
22 mW per gate typical
40-50 mW per flip-flop typical

Switching Speeds(1)
Average Propagation Delay = 6.0 ns per gate typical
15 ns per flip-flop typical

Rise Time = 1.0 ns typical
Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC2109/MC2110 Series) = 30 MHz maximum.

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL, the designer must continually be aware of the fact that he is working with the fastest form of saturating logic available in the industry today. The switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions have been included to help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rate of change of currents and voltages for a single MTTL II gate is in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL II circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every five packages throughout a breadboard is adequate to supress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The standard supply voltage of the MTTL II logic circuits is +5.0 Vdc.The typical average dc power dissipation is given for each MTTL II circuit.(2) It should be noted that the totem pole output common to all high level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.7 mW/MHz/output for a 15 pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL II circuits.

Unused Inputs and Unused Gates

The unused inputs of any MTTL II logic circuit should not be left open, and can either be tied to the used inputs or returned to the supply voltage. This will reduce any potential problems resulting from external noise. If the inputs are returned to the supply voltage, care should be taken to insure that the supply voltage does not exceed the maximum rated input voltage of 5.5 volts. If the supply can exceed 5.5 volts, the unused inputs must be returned to a lower voltage. The total number of inputs that can be tied to the output of any driving gate is 50. (This is defined as high state output loading factor.) It should be noted that the low state output loading rules must still be maintained. The minimum logical "1" level for the high state output loading is summarized for V_{CC} = 5.0 V, V_{IL} = 0.45 V and I_{OH} = −5.0 mA:

MC2100/2150 Series — V_{OH} = 2.7 volts minimum @ −55°C
MC2000/2050 Series — V_{OH} = 2.9 volts minimum @ 0°C

The unused inputs of the various flip-flops may be tied back to their associated outputs. To determine which outputs are related to each set of inputs by internal feedback, refer to the circuit schematics.

The inputs of any unused gate in a package should be grounded. This places the gate in its lowest power condition and will help to eliminate unnecessary power drain.

Expanders and Expander Nodes

The ORing nodes of all the MTTL II AND-OR-INVERT gates are made available for expanding the number of AND gates to 10. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 0.7 ns/pF.

Output OR (AND) Function

Unlike the MDTL family of logic circuits, the outputs of the MTTL II logic circuits cannot be tied together to perform the output OR, or more correctly, the output AND function. If the outputs of the MTTL II family devices are tied together, it would be possible for the lower output transistor of one circuit and the upper output transistor of another circuit to be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground and the current that flows (approximately I_{SC}) exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

Operating Characteristics of Flip-Flops

The general operating characteristics and restrictions for the MC2109/MC2110 series J-K flip-flops are as follows:

The clocked inputs are inhibited when the clock is in the low state, and data should be applied and allowed to settle. The clocked inputs are enabled when the clock goes high and data enters the flip-flop. The data is temporarily stored in the charge-storage section (temporary memory) while the clock is in the high state. This data is transferred to the bistable section on the negative clock transition.

The data on the clocked inputs should not be changed while the clock is in the high state. Data changes during this clock condition require 300 ns settling time.

The direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs do not directly affect the charge-storage section and therefore should not be used while the clock is high. On the negative transition of the clock, previously stored data may override the asynchronous set output state. Further, the direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs do not override the clock and will not control the state of the flip-flop until 100 ns after the negative transition of the clock. The clock signal must conform to the following boundary conditions at +125°C.

Maximum guaranteed clock frequency	= 30 MHz
Maximum clock fall time	= 100 ns
Minimum clock pulse width	= 15 ns
Minimum clock pulse amplitude	= 1.8 V
Maximum negative clock voltage	= −0.5 V

Note: These boundary conditions for operation are not defined as occuring simultaneously.

The transfer of data from the charge storage section to the bistable section is essentially an ac operation and thus results in the restriction of the clock fall time. If the clock fall time is greater than 100 ns, the information retained in the charge-storage section may not be transferred to the bistable section. The flip-flop will operate from very low frequencies to 30 MHz as long as the clock fall time is less than or equal to 100 ns.

Large negative clock excursions may cause incorrect data transfers to the bistable section during the transfer cycles. Therefore, the most negative clock signal should be limited to −0.5 volt.

---

(1) The switching characteristics of the MTTL II family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns.}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative transition of the output from the 2.0 V to the 1.0 V level.

(2)
$$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical dc current drains at V_{CC} = +5.0 V.

MC2000/2050 and 2100/2150 MTTL II* series integrated circuits are electrically interchangeable with SUHL II† series logic circuits as shown in the cross reference below.

SG SF NUMBER	Description	−55 to +125°C		0 to +75°C	
		Fan-Out = 11	Fan-Out = 6	Fan-Out = 9	Fan-Out = 5
SG210-213	Expandable 2-Wide 4-Input AND-OR-INVERT Gate	MC2100	MC2150	MC2000	MC2050
SG220-223	Quad 2-Input NAND Gate	MC2101	MC2151	MC2001	MC2051
SG230-233	4-Wide 3-2-2-3 Input Expander For AND-OR-INVERT Gates	MC2102	MC2152	MC2002	MC2052
SG240-243	Dual 4-Input NAND Gate	MC2103	MC2153	MC2003	MC2053
SG250-253	Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate	MC2104	MC2154	MC2004	MC2054
SG260-263	Single 8-Input NAND Gate	MC2105	MC2155	MC2005	MC2055
SG270-273	Dual 4-Input Expander For AND-OR-INVERT Gates	MC2106	MC2156	MC2006	MC2056
–	Triple 3-Input NAND Gate	MC2107	MC2157	MC2007	MC2057
SF250-253	AND J-K Flip-Flop	MC2109	MC2159	MC2009	MC2059
SF260-263	OR J-K Flip-Flop	MC2110	MC2160	MC2010	MC2060
SG310-313	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC2113	MC2163	MC2013	MC2063

*Trademark of Motorola Inc.
†Trademark of Sylvania Electric Products, Inc.

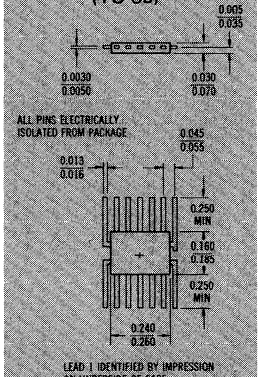
DEFINITIONS

BV_{in} "0"	Input breakdown voltage (ON level)
BV_{in} "1"	Input breakdown voltage (OFF level)
f_{Tog}	Toggle frequency
I_C	Collector current
I_F	Input forward current
I_{FC}	Forward current of clock input
I_{in}	Input current
$2\ I_{in}$	2-times the Input Current
$4\ I_{in}$	4-times the Input Current
I_L	Inverse beta current
I_{LC}	Inverse beta current of the clock input
I_{max}	Maximum rated power supply current with V_{max} applied
I_O	Output breakdown current
I_{OH}	Output high current
I_{OL}	Output low current
I_{OLK}	Output leakage current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input reverse current with V_R applied
I_{RC}	Reverse current of clock input
I_{SC}	Short circuit current obtained from device output when one or more inputs are low
Pr	Prime Fan-Out
PRF	Pulse repetition frequency
PW	Pulse width
Std	Standard fan-out
t_f	Fall time
t_{off}	Turn-off delay time
t_{on}	Turn-on delay time
t_{Post}	The minimal time necessary before the $\overline{SET}$, $\overline{PRESET}$, or $\overline{RESET}$ inputs can control the flip-flop after the negative clock edge
t_r	Rise time
Δt_{pd}	Average increase in propagation delay per AND gate of expander when connected to an AND-OR-INVERT gate.
$\Delta t_{pd}/pF$	Increased propagation delay caused by additional capacitance at expansion points.
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
V_{Amp}	Voltage amplitude
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CE}	Collector-emitter voltage
V_{CR}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CC}.
V_{CRH}	Collector voltage obtained thru 1.3 k ohm resistor from V_{CCH}.
V_{E1}, V_{E2}, V_{E3}	Emitter voltage
V_{EN}	Enable voltage level
V_{IH}	Voltage for high input voltage state
V_{IHX}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Voltage for low input voltage state
V_{INH}	Inhibit voltage level
V_{max}	Maximum rated power supply voltage (V_{CC})
V_{OH}	Output high voltage with I_{OH} flowing out of pin
V_{OL}	Output low voltage with I_{OL} flowing into pin
V_{out} "0"	Output low voltage with V_{th} "1" applied
V_{out} "1"	Output high voltage with V_{th} "0" applied
V_R	Input reverse voltage
V_{th} "0"	Input logic "0" threshold voltage
V_{th} "1"	Input logic "1" threshold voltage

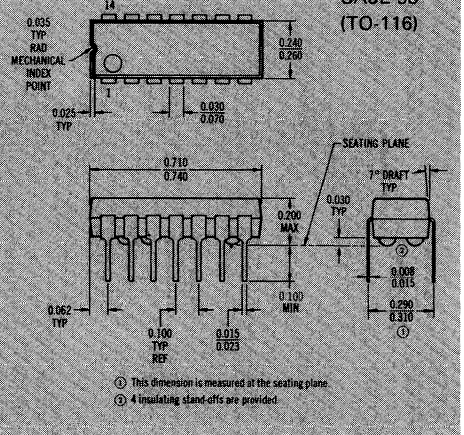
PACKAGING

All MTTL II integrated circuits are available in the TO-85, 14-lead flat package. MC2000 series is also available in the 14-lead dual in-line plastic package. To order the flat package, add suffix "F" to the basic type number; to order plastic package, add suffix "P".

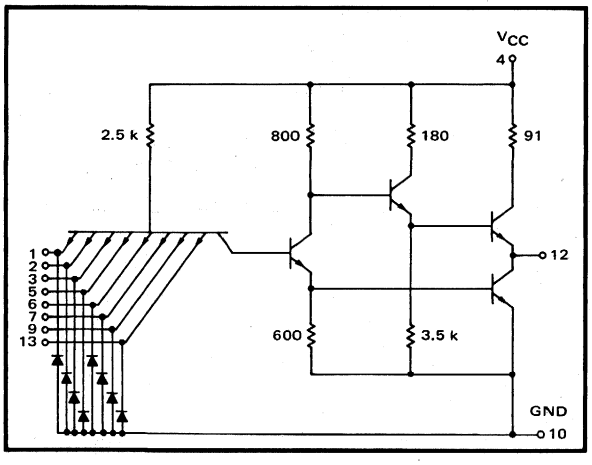
CASE 609
(TO-85)



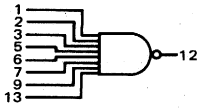
CASE 93
(TO-116)



MC2105 • MC2155
MC2005 • MC2055



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



Positive Logic:

$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$

Negative Logic:

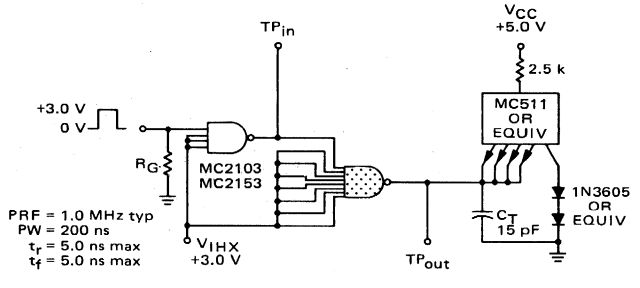
$12 = \overline{1 + 2 + 3 + 5 + 6 + 7 + 9 + 13}$

Total Power Dissipation = 22 mW typ/Pkg

Propagation Delay Time = 8.0 ns typ

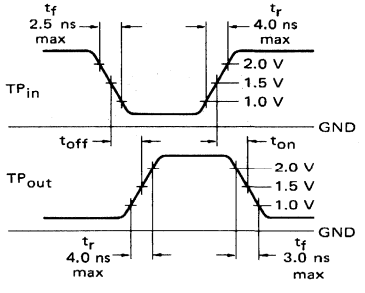
SERIES	INPUT LOADING FACTOR (I_F)		OUTPUT DRIVE (I_{OL})			TEMPERATURE RANGE
MC2105 MC2155	1	−2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	−55°C to +125°C
MC2005 MC2055	1	−2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



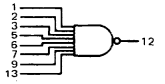
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.

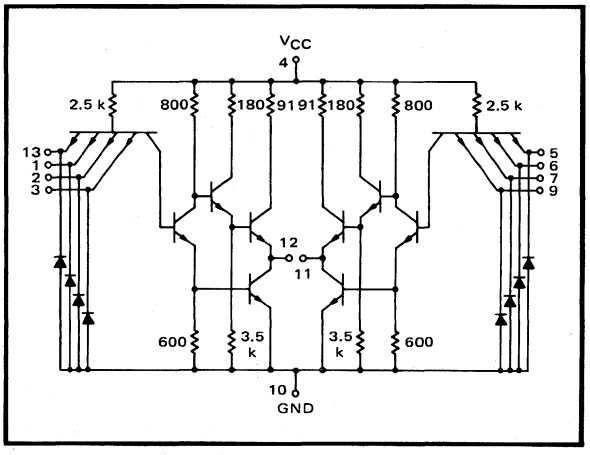


@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2105*, MC2155	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2005*, MC2055	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

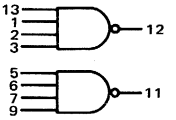
Characteristic	Symbol	Pin Under Test	MC2105, MC2155 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2005, MC2055 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3,5,6 7,9,13	-	-	-	4	-	-	1, 10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7, 9,10,13
Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6,7, 9,10,13
Short-Circuit Current	I_{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7, 9,10,12,13
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	12	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	6.50	-	-	-	-	-	6.75	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1, 10
Power Supply Drain	I_{PDH}	4	-	7.5	-	7.5	-	7.5	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	3.75	-	3.75	-	3.75	-	5.0	-	5.0	-	5.0	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1, 10
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1, 12	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Turn-Off Delay	t_{off}	1, 12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Rise Time	t_r	1, 12	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10
Fall Time	t_f	1, 12	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,5,6, 7,9,13	10

* Prime Fan-Out.

MC2103 • MC2153
MC2003 • MC2053



This device consists of two 4-input NAND gates. The gates can be cross coupled to form a multiple-input R-S flip-flop or a circuit for eliminating contact bounce.



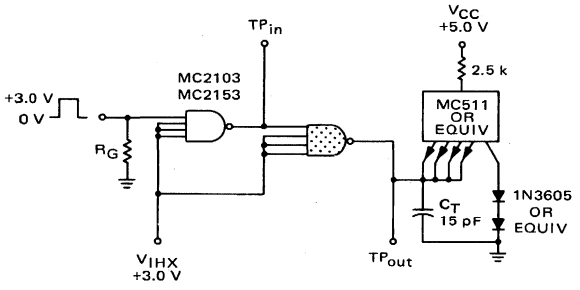
Positive Logic:
$12 = \overline{1 \cdot 2 \cdot 3 \cdot 13}$

Negative Logic:
$12 = \overline{1 + 2 + 3 + 13}$

Total Power Dissipation = 44 mW typ/Pkg
Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR (I_F)		OUTPUT DRIVE (I_{OL})		TEMPERATURE RANGE
MC2103 MC2153	1	−2.0 mA	11 MC2100 series Gates 6 MC2100 series Gates	22 mA 12 mA	−55°C to +125°C
MC2003 MC2053	1	−2.5 mA	9 MC2000 series Gates 5 MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

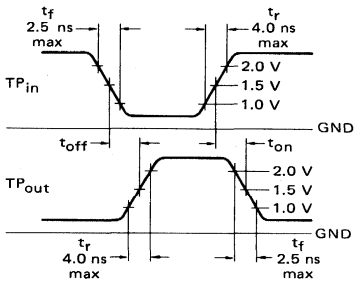
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns max
t_f = 5.0 ns max

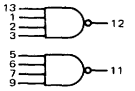
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. To complete testing, sequence through remaining inputs.

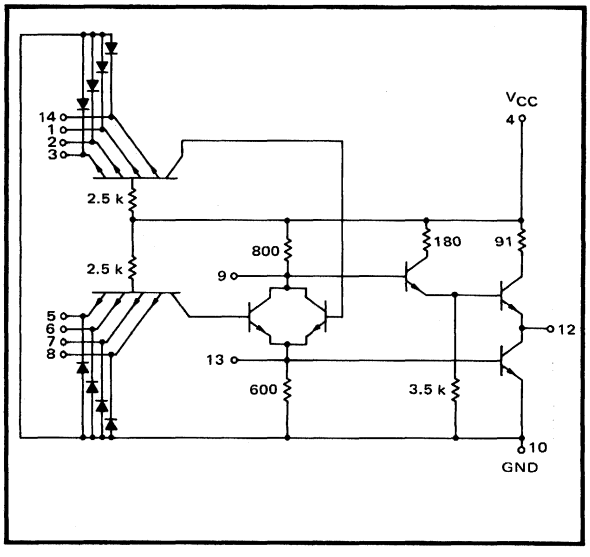


@ Test Temperature		TEST CONDITIONS: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2103*, MC2153	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2003*, MC2053	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

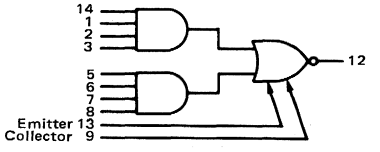
Characteristic	Symbol	Pin Under Test	MC2103, MC2153 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2003, MC2053 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3,13	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,13
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,13
Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	12	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3, 10,13
Short-Circuit Current	I_{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 10,12,13
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	12	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	13	-	-	-	-	-	13.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,5,10
Power Supply Drain	I_{PDH}	4	-	15	-	15	-	15	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	7.5	-	7.5	-	7.5	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,5,10
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Turn-Off Delay	t_{off}	1,12	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Rise Time	t_r	1,12	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10
Fall Time	t_f	1,12	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,13	10

* Prime Fan-Out.
† Ground inputs to gate not under test during ALL tests unless otherwise noted.
‡ The inputs of both gates must be ungrounded.

MC2100 • MC2150
MC2000 • MC2050



This device consists of two 4-input AND gates ORed together and driving an output inverter. The ORing nodes are available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds. This gate is usable for construction of half adders and other applications where the exclusive OR function is required.



Positive Logic:

$12 = \overline{(1 \cdot 2 \cdot 3 \cdot 14) + (5 \cdot 6 \cdot 7 \cdot 8) + (\text{Expanders})}$

Negative Logic:

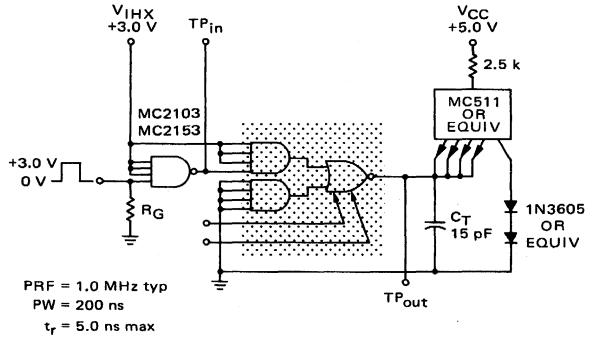
$12 = \overline{(1 + 2 + 3 + 14) \cdot (5 + 6 + 7 + 8) \cdot (\text{Expanders})}$

Total Power Dissipation = 27 mW typ/Pkg

Propagation Delay Time = 7.0 ns typ

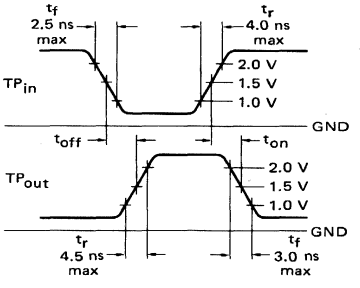
SERIES	INPUT LOADING FACTOR (I_F)		OUTPUT DRIVE (I_{OL})			TEMPERATURE RANGE
MC2100 MC2150	1	−2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	−55°C to +125°C
MC2000 MC2050	1	−2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns max
t_f = 5.0 ns max

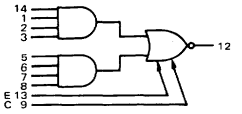
VOLTAGE WAVEFORMS AND DEFINITIONS



NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.

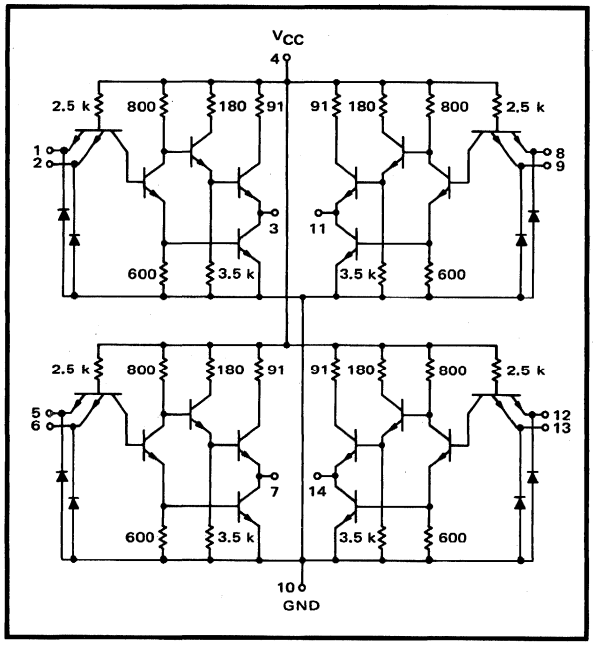


@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2100*, MC2150	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2000*, MC2050	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

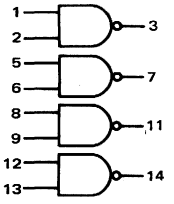
Characteristic	Symbol	Pin Under Test	MC2100, MC2150 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2000, MC2050 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3,14	-	-	-	4	-	-	1,5,6,7,8,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	5,6,7,8,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	5,6,7,8,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,10,14,
Output																												
Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	1	-	-	4	-	-	5,6,7,8,10
	V_{out} "1"	12	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	1	-	4	-	-	5,6,7,8,10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	12	4	-	-	1,2,3,5,6,7,8,10,14
Short-Circuit Current	I_{SC}	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,10,12,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	1	-	-	-	-	4	-	-	5,6,7,8,10
	V_{OH}	12	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	12	-	1	-	-	-	-	-	4	-	-	5,6,7,8,10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	10	-	-	-	-	-	11	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,10,14
Power Supply Drain	I_{PDH}	4	-	9.0	-	9.0	-	9.0	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	6.0	-	6.0	-	6.0	-	7.5	-	7.5	-	7.5	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,12	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Turn-Off Delay	t_{off}	1,12	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Rise Time	t_r	1,12	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10
Fall Time	t_f	1,12	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	12	-	-	-	-	-	-	-	4	-	2,3,14	5,6,7,8,10

*Prime Fan-Out.

MC2101 • MC2151
MC2001 • MC2051



This device consists of four 2-input NAND gates. The four gates in a single package represent increased functional flexibility. For example, a dual set-reset flip-flop may be obtained if each pair of gates is externally cross-coupled.



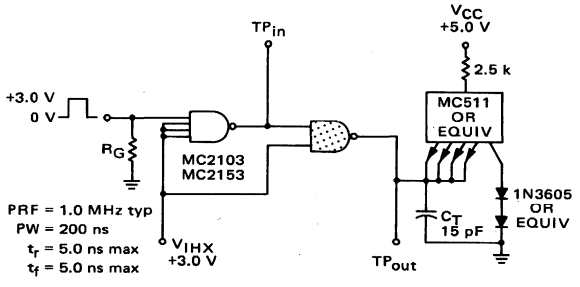
Positive Logic:
$3 = \overline{1 \cdot 2}$

Negative Logic:
$3 = \overline{1 + 2}$

Total Power Dissipation = 88 mW typ/Pkg
Propagation Delay Time = 6.0 ns typ

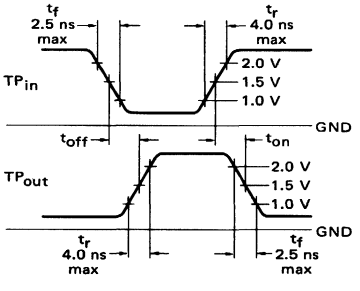
SERIES	INPUT LOADING FACTOR (I_F)		OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC2101 MC2151	1	−2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	−55°C to +125°C
MC2001 MC2051	1	−2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

SWITCHING TIME TEST CIRCUIT



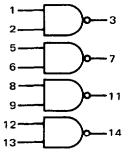
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in a similar manner. Further, test procedures are shown for only one input of the gate being tested. The other input is tested in the same manner.

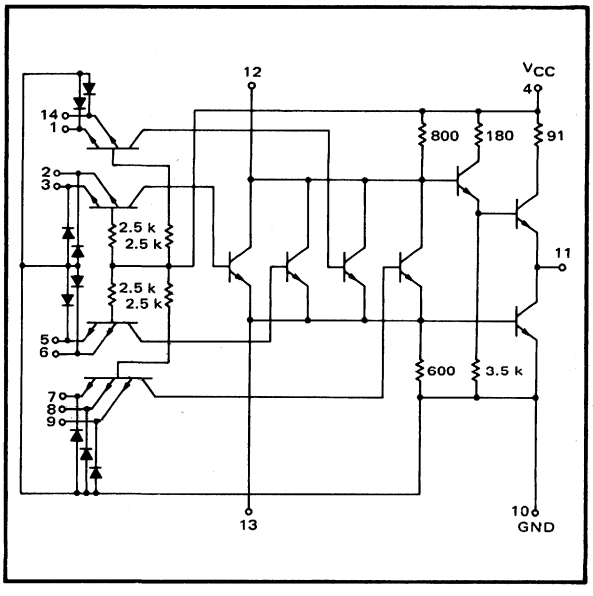


@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2101*, MC2151	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2001*, MC2051	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

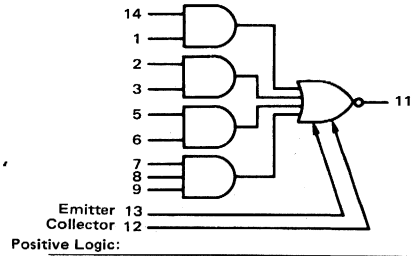
Characteristic	Symbol	Pin Under Test	MC2101, MC2151 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2001, MC2051 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,10
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,10
Output																												
Output Voltage	V_{out} "0"	3	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	3	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	3	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	3	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	3	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	1,2,10
Short-Circuit Current	I_{SC}	3	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	3	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	3	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	3	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	26	-	-	-	-	-	27	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,5,8, 10,12
Power Supply Drain	I_{PDH}	4	-	30	-	30	-	30	-	40	-	40	-	40	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	15	-	15	-	15	-	20	-	20	-	20	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,5,8, 10,12
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Turn-Off Delay	t_{off}	1,3	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Rise Time	t_r	1,3	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10
Fall Time	t_f	1,3	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns	1	3	-	-	-	-	-	-	-	4	-	2	10

*Prime Fan-Out
†Ground inputs to gates not under test during ALL tests unless otherwise noted.
‡The inputs of all gates must be ungrounded.

MC2104 • MC2154
MC2004 • MC2054



This device consists of three 2-input and one 3-input AND gates ORed together and driving an output inverter. The ORing nodes are made available for expansion, and up to 10 AND gates can be ORed together using the MC2102 or the MC2106 series expanders. Since switching speed is affected by the amount of capacitance on the expander nodes, care should be taken to minimize this capacitance to maintain switching speeds.



Positive Logic:

$$11 = \overline{(14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (\text{Expanders})}$$

Negative Logic:

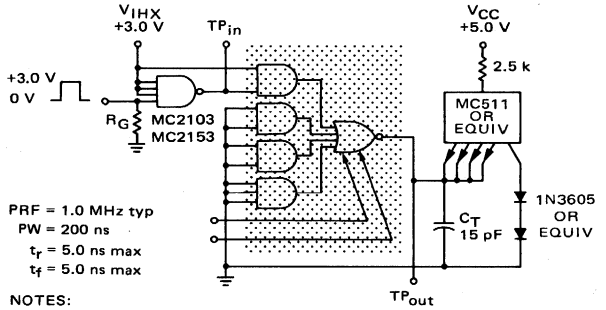
$$11 = \overline{(14 + 1) \cdot (2 + 3) \cdot (5 + 6) \cdot (7 + 8 + 9) \cdot (\text{Expanders})}$$

Total Power Dissipation = 36 mW typ/Pkg

Propagation Delay Time = 7.0 ns typ

SERIES	INPUT LOADING FACTOR (I_F)		OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC2104 MC2154	1	−2.0 mA	11 6	MC2100 series Gates MC2100 series Gates	22 mA 12 mA	−55°C to +125°C
MC2004 MC2054	1	−2.5 mA	9 5	MC2000 series Gates MC2000 series Gates	22.5 mA 12.5 mA	0°C to +75°C

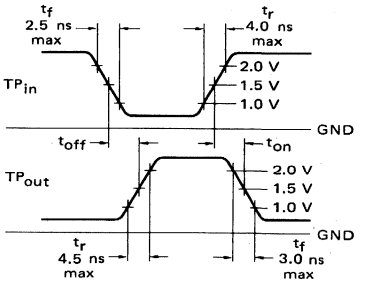
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns max
t_f = 5.0 ns max

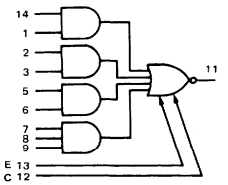
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Expander pins should be left open when measuring switching times.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.

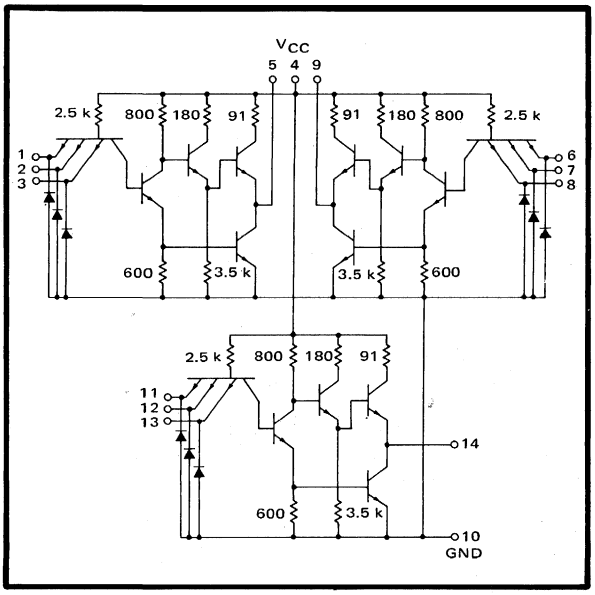


@ Test Temperature		I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts	V_{CCH} Volts	V_{IHX} Volts
MC2104*, MC2154	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2004*, MC2054	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

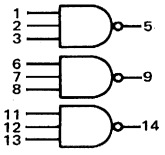
Characteristic	Symbol	Pin Under Test	MC2104, MC2154 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2004, MC2054 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10,14
Output																												
Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	1	-	-	4	-	-	2,3,5,6,7,8,9,10
	V_{out} "1"	11	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	1	-	4	-	-	2,3,5,6,7,8,9,10
Leakage Current	I_{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	11	4	-	-	1,2,3,5,6,7,8,9,10,14
Short-Circuit Current	I_{SC}	11	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,11,14
Output Voltage	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	1	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
	V_{OH}	11	2.70	-	3.10	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	11	-	1	-	-	-	-	-	4	-	-	2,3,5,6,7,8,9,10
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max}	4	-	-	-	17	-	-	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,14
Power Supply Drain	I_{PDH}	4	-	12	-	12	-	12	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10
	I_{PDL}	4	-	10	-	10	-	10	-	13	-	13	-	13	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,6,7,8,9,10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,11	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Turn-Off Delay	t_{off}	1,11	-	-	-	12	-	-	-	-	-	12	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Rise Time	t_r	1,11	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10
Fall Time	t_f	1,11	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	11	-	-	-	-	-	-	-	4	-	14	2,3,5,6,7,8,9,10

* Prime Fan-Out.

MC2107 • MC2157
MC2007 • MC2057



This device consists of three 3-Input AND gates driving output inverters. These gates can be used to build a pulse shaping network for interfacing with discrete component circuits.

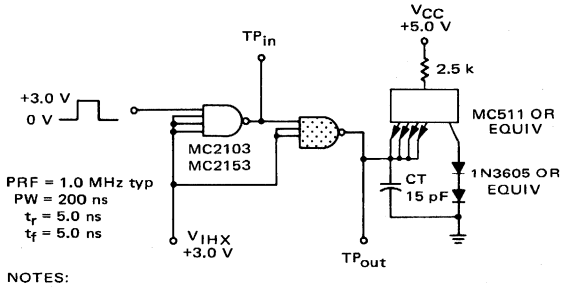


Positive Logic: $5 = \overline{1 \cdot 2 \cdot 3}$
Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC2107 MC2157	1	(-2.0 mA)	11 6	MC2100 series Gates MC2100 series Gates	(22 mA) (12 mA)	−55°C to +125°C
MC2007 MC2057	1	(-2.5 mA)	9 5	MC2000 series Gates MC2000 series Gates	(22.5 mA) (12.5 mA)	0° to +75°C

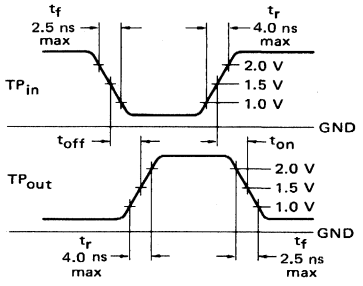
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

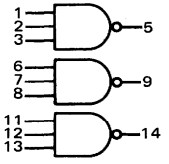
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

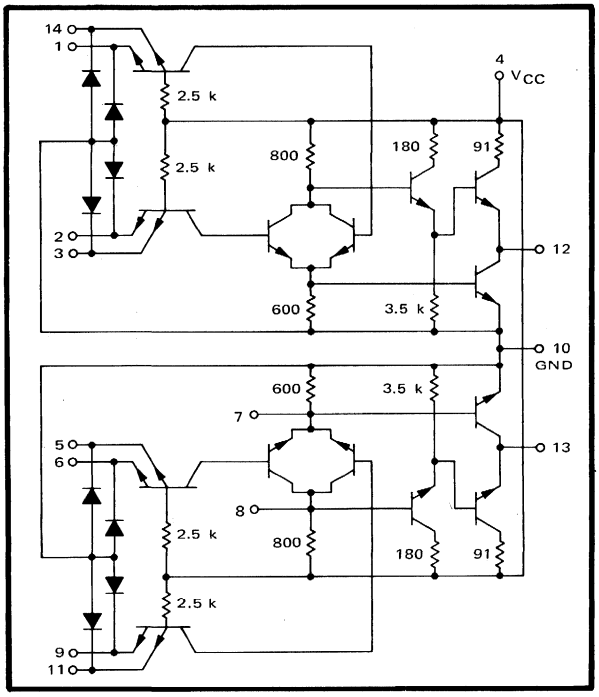


@ Test Temperature		TEST CONDITIONS mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2107*, MC2157	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2007*, MC2057	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

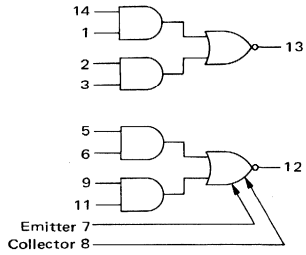
Characteristic	Symbol	Pin Under Test	MC2107, MC2157 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2007, MC2057 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	2,3	-	-	-	4	-	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
Output																												
Output Voltage	V_{out} "0"	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	5	-	-	-	-	-	1	-	-	4	-	-	10
	V_{out} "1"	5	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	5	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	5	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10
Short-Circuit Current	I_{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 5,10
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	5	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	5	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	5	-	1	-	-	-	-	-	4	-	-	10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	19.5	-	-	-	-	-	20.25	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11
Power Supply Drain	I_{PDH}	4	-	22.5	-	22.5	-	22.5	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10 ‡
	I_{PDL}	4	-	11.25	-	11.25	-	11.25	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,6,10,11
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,5	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Turn-Off Delay	t_{off}	1,5	-	-	-	10	-	-	-	-	-	10	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Rise Time	t_r	1,5	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Fall Time	t_f	1,5	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns	1	5	-	-	-	-	-	-	-	4	-	2,3	10

* Prime Fan-Out †Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

MC2113 • MC2163
MC2013 • MC2063



One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together and driving an output inverter with the ORing nodes made available for expansion. Up to 10 AND gates can be ORed together using the MC2102 or MC2106 expanders series. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

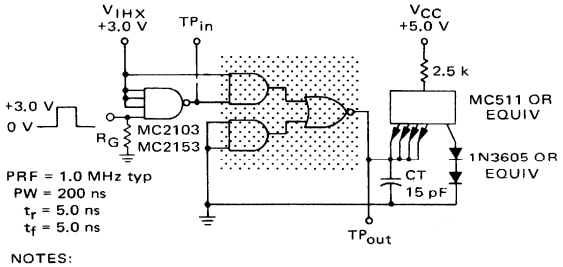
$13 = \overline{(1 \cdot 14) + (2 \cdot 3)}$

$12 = \overline{(5 \cdot 6) + (9 \cdot 11) + (\text{Expander})}$

Total Power Dissipation = 58 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

SERIES	INPUT LOADING FACTOR	(I_F)		OUTPUT DRIVE	(I_{OL})	TEMPERATURE RANGE
MC2113 MC2163	1	(-2.0 mA)	11 6	MC2100 series Gates MC2100 series Gates	(22 mA) (12 mA)	−55°C to +125°C
MC2013 MC2063	1	(-2.5 mA)	9 5	MC2000 series Gates MC2000 series Gates	(22.5 mA) (12.5 mA)	0° to +75°C

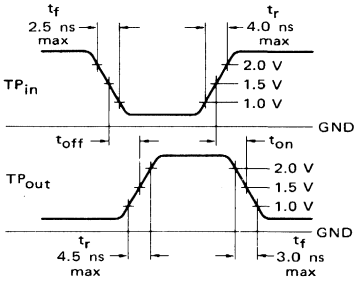
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_r = 5.0 ns
t_f = 5.0 ns

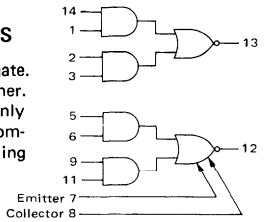
NOTES:
R_G = 50 ohms
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
When checking expander side, expander pins should be open.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@ Test Temperature		TEST CONDITIONS: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	Volts V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2113*, MC2163	−55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2013*, MC2063	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

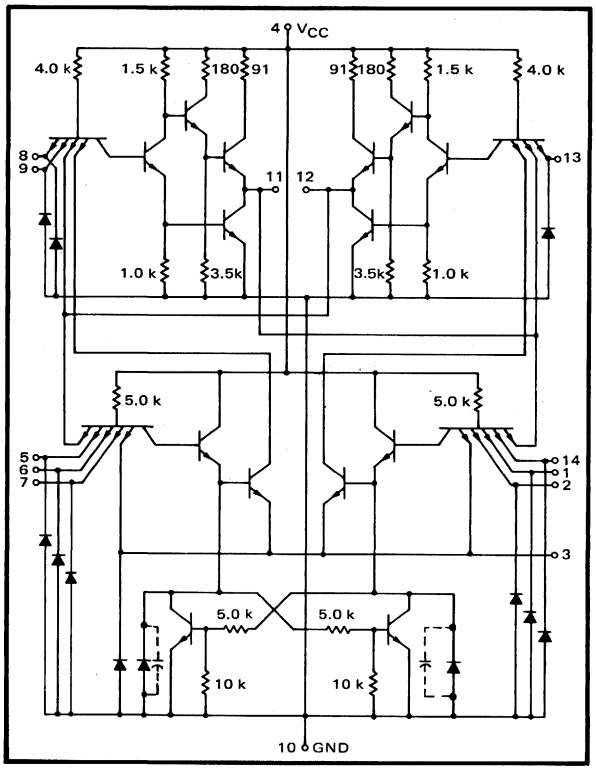
Characteristic	Symbol	Pin Under Test	MC2113, MC2163 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2013, MC2063 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	14	-	-	-	4	-	-	1,2,3,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10,14
Output																												
Output Voltage	V_{out} "0"	13	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	13	-	-	-	-	-	1	-	-	4	-	-	2,3,10
	V_{out} "1"	13	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	13	-	-	-	-	-	1	-	4	-	-	2,3,10
Leakage Current	I_{OLK}	13	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	-	-	-	13	4	-	-	1,2,3, 10,14
Short-Circuit Current	I_{SC}	13	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,10, 13,14
Output Voltage	V_{OL}	13	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	13	-	-	-	1	-	-	-	-	4	-	-	2,3,10
	V_{OH}	13	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc	-	13	-	1	-	-	-	-	-	4	-	-	2,3,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	20	-	-	-	-	-	22	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3, 10,14
Power Supply Drain	I_{PDH}	4	-	18	-	18	-	18	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	10‡
	I_{PDL}	4	-	12	-	12	-	12	-	15	-	15	-	15	mAdc	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3, 10,14
Switching Parameters																Pulse In	Pulse Out											
Turn-On Delay	t_{on}	1,13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Turn-Off Delay	t_{off}	1,13	-	-	-	11	-	-	-	-	-	11	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Rise Time	t_r	1,13	-	-	-	4.5	-	-	-	-	-	4.5	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10
Fall Time	t_f	1,13	-	-	-	3.0	-	-	-	-	-	3.0	-	-	ns	1	13	-	-	-	-	-	-	-	4	-	14	2,3,10

* Prime Fan-Out

† Ground inputs to gates not under test during ALL tests unless otherwise noted.

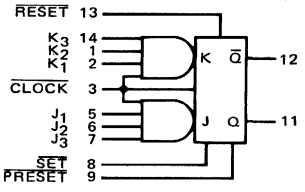
‡ The inputs to all gates must be ungrounded.

MC2109 • MC2159
MC2009 • MC2059

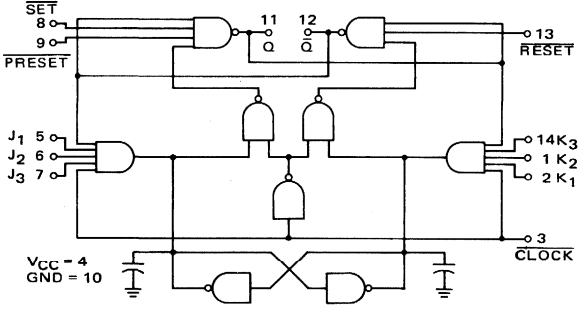


The MC2009, MC2059, MC2109, and MC2159 are clocked flip-flops that trigger on the negative edge and perform the J-K logic junction. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gates in counters and certain other applications. A direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ are also available.

In normal operation, information is changed on the J and K inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in a high state. When the clock returns low, the information is transferred to the bistable section and the Q and $\bar{Q}$ outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is high. Each flip-flop can be set or reset directly by the direct $\overline{SET}$, $\overline{PRESET}$, or $\overline{RESET}$ inputs. Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



EQUIVALENT CIRCUIT



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

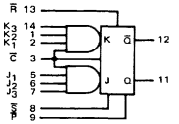
Where $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

Total Power Dissipation = 40 mW typ/Pkg
Switching Times:
t_{on} = 20 ns typ
t_{off} = 13 ns typ

SERIES	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC2109 MC2159	1.00	0.66	(−2.0 mA)	(−1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	−55°C to +125°C
MC2009 MC2059	1.00	0.66	(−2.5 mA)	(−1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



@ Test Temperature		I_{OL} mA		I_{OH} mA		I_{in} mA	$2\ I_{in}$ mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,0}$ Volts	$V_{th\,1}$ Volts	V_{out} Volts	V_{CC} Volts
		Pr*	Std	Pr*	Std									
MC2109*, MC2159	−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
	+25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
MC2009*, MC2059	0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
	+25°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

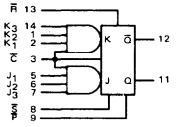
Characteristic	Symbol	Pin Under Test	MC2109, MC2159 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2009, MC2059 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,0}$	$V_{th\,1}$	V_{out}	V_{CC}	Gnd
Input																											
Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-		5,10,13
		8	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
		9	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,10,11,14
		5	-		-		-		-		-		-			-	-	-	-	-	-	5	-	-	-		1,2,3,6,7,10,12,14
		8	-		-		-		-		-		-			-	-	-	-	-	-	8	-	-	-		1,2,3,5,6,7,9,10,12,14
		9	-		-		-		-		-		-			-	-	-	-	-	-	9	-	-	-		1,2,3,5,6,7,8,10,12,14
		13	-		-		-		-		-		-			-	-	-	-	-	-	13	-	-	-		1,2,3,5,6,7,10,11,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	8	-	1	-	-	-	4	10
		5	-		-		-		-		-		-			-	-	-	-	13	-	5	-	-	-		
		8	-		-		-		-		-		-			-	-	-	-		-	8	-	-	-		
		9	-		-		-		-		-		-			-	-	-	-		-	9	-	-	-		
		13	-		-		-		-		-		-			-	-	-	-	8	-	13	-	-	-		
Breakdown Voltage	BV_{in}"0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	8	-	-	-	-	-	4	10
		5		-		-		-		-		-		-		-	-	5	-	13	-	-	-	-	-		
		8		-		-		-		-		-		-		-	-	8	-		-	-	-	-	-		
		9		-		-		-		-		-		-		-	-	9	-		-	-	-	-	-		
		13		-		-		-		-		-		-		-	-	13	-	8	-	-	-	-	-		
	BV_{in}"1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	4	2,3,5,6,7,10,11,14
		5		-		-		-		-		-		-		-	-	5	-	-	-	-	-	-	-		1,2,3,6,7,10,12,14
		8		-		-		-		-		-		-		-	-	8	-	-	-	-	-	-	-		1,2,3,5,6,7,9,10,12,14
		9		-		-		-		-		-		-		-	-	9	-	-	-	-	-	-	-		1,2,3,5,6,7,8,10,12,14
		13		-		-		-		-		-		-		-	-	13	-	-	-	-	-	-	-		1,2,3,5,6,7,10,11,14

* Prime Fan-Out.

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	@ Test Temperature	I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	2 I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,0}$	$V_{th\,1}$	V_{out}	V_{CC}
		TEST CONDITIONS												
		mA						Volts						
MC2109*, MC2159	−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.0	2.0	5.5	5.0
	+25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.2	1.7	5.5	5.0
	+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	0.9	1.4	5.5	5.0
MC2009*, MC2059	0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.9	5.5	5.0
	+25°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.2	1.8	5.5	5.0
	+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.1	1.7	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC2109, MC2159 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2009, MC2059 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	2 I_{in}	V_{IL}	V_{IH}	V_R	$V_{th\,0}$	$V_{th\,1}$	V_{out}	V_{CC}	Gnd
Clock Input Forward Current	I_F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	I_L	3	-	200	-	200	-	200	-	200	-	200	-	200	μAdc	-	-	-	-	13	-	3	-	-	-	4	10
		3	-	200	-	200	-	200	-	200	-	200	-	200	μAdc	-	-	-	-	8	-	3	-	-	-	4	10
Breakdown Voltage	BV_{in} "0"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	13	-	-	-	-	-	4	10
		3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	8	-	-	-	-	-	4	10
	BV_{in} "1"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	-	-	-	-	-	-	4	1,2,5,6,7,10,14
Output Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	-	13	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	-	9	-	↓	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	-	8	-	↓	3,10,13
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	13	-	-	4	8,10
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	9	-	-	↓	10,13
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	8	-	-	↓	10,13
Leakage Current	I_{OLK}	12	-	225	-	225	-	225	-	225	-	225	-	225	μAdc	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,9,10,13,14
		11	-	225	-	225	-	225	-	225	-	225	-	225	μAdc	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I_{SC}	12	-	-	-30	-70	-	-	-	-	-30	-70	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14
		11	-	-	-30	-70	-	-	-	-	-30	-70	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	-	13	-	-	-	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	9	-	-	-	-	↓	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	8	-	-	-	-	↓	3,10,13
	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	12	-	-	13	-	-	-	-	-	4	8,10
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	9	-	-	-	-	-	↓	10,13
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	8	-	-	-	-	-	↓	10,13
Power Requirements (Total Device) Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,10,13
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,8,10

* Prime Fan-Out.

OPERATING CHARACTERISTICS

Clock fall time $\leq$ 100 ns.

Triggers on clock pulse widths $\geq$ 15 ns.

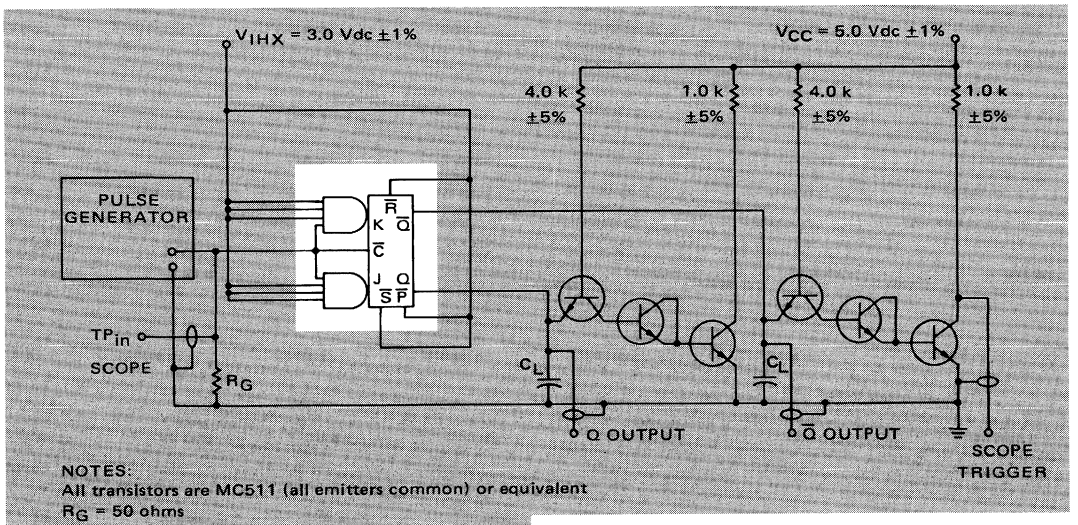
Provides direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop will require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{Q}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

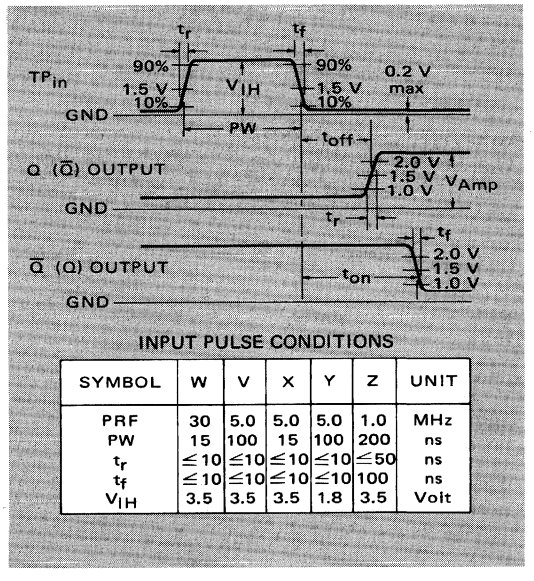
Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{PRESET}$ and $\overline{SET}$ are tied to $\overline{Q}$; $\overline{RESET}$ is tied to Q.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

VOLTAGE WAVEFORMS AND DEFINITIONS



SWITCHING TIMES

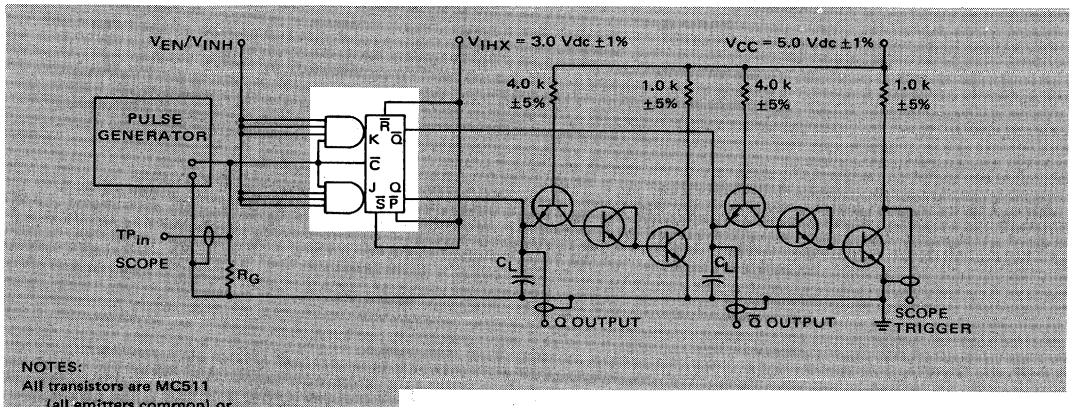
TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		25	ns
Rise Time	t_r	V		6.0	ns
Fall Time	t_f	V		4.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

WORST-CASE TESTS (Device must toggle with each clock pulse)			
TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	30 MHz max	W
Pulse Width	PW	15 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	100 ns max	Z

INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	30	5.0	5.0	5.0	1.0	MHz
PW	15	100	15	100	200	ns
t_r	$\leq$10	$\leq$10	$\leq$10	$\leq$10	$\leq$50	ns
t_f	$\leq$10	$\leq$10	$\leq$10	$\leq$10	100	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance

Enable Mode Test:
The device under test shall toggle when V_{EN} = 1.8 Vdc ±1% is applied.

Inhibit Mode Test:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ±1% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

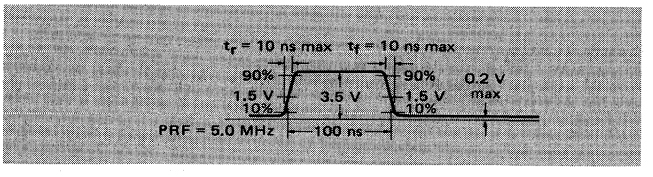
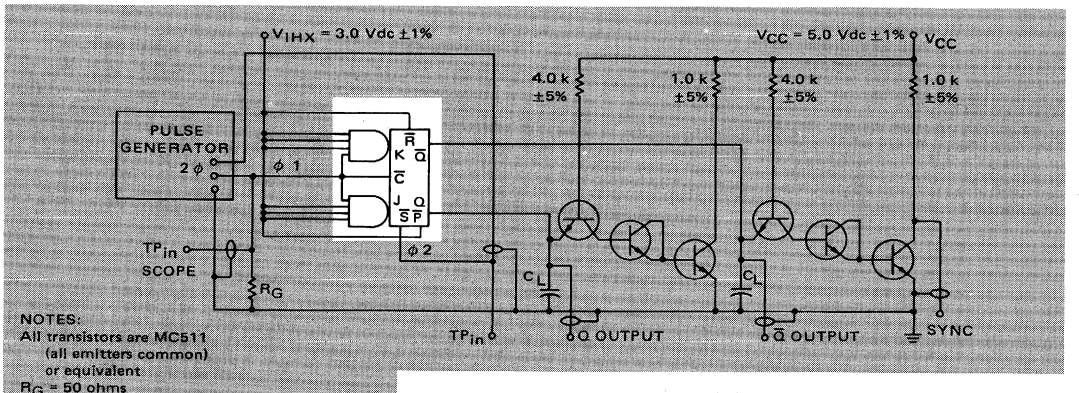


FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



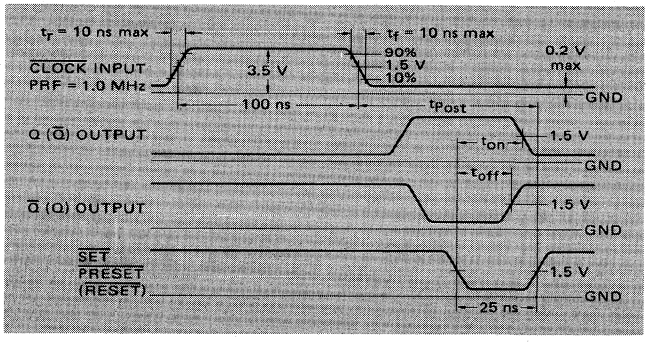
NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance
t_{Post} = Post Time

TEST PARAMETERS

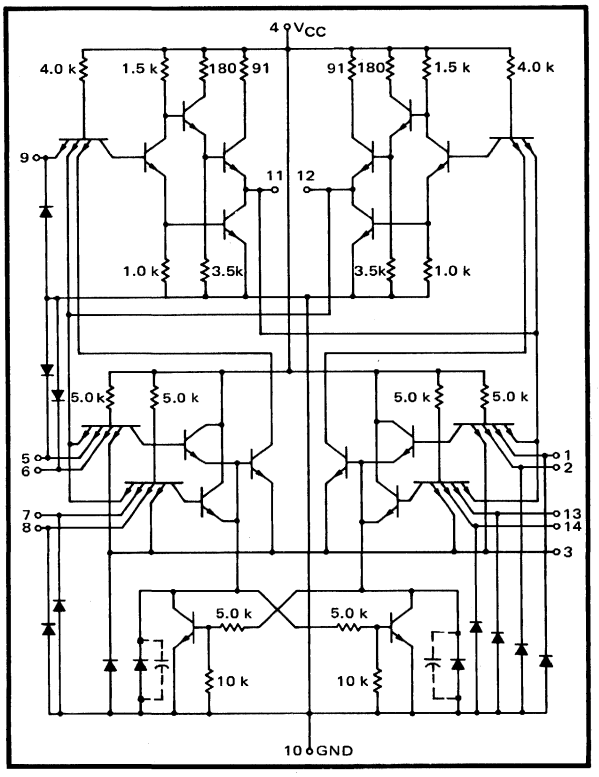
SYMBOL	VALUE	UNIT
t_{Post}	100	ns min
t_{on}	25	ns max
t_{off}	20	ns max

NOTE:
When t_{Post} is 100 ns, SET, PRESET or RESET pulses must actuate the device.
SET, PRESET, and RESET pulse cannot return to the high state before the required post time.
Connections shown for measuring times related to SET terminal only. To measure times at PRESET terminal apply input pulse to Pin 9 in place of Pin 8. To measure times at RESET terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS



MC2110 • MC2160
MC2010 • MC2060

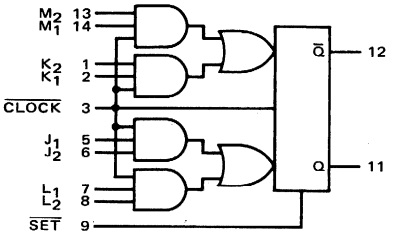


The MC2110, MC2160, MC2010, and MC2060 are clocked flip-flops that trigger on the negative edge and are internally wired to perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and the L inputs are ORed together and the K and the M inputs are ORed together. A direct $\overline{SET}$ is also available.

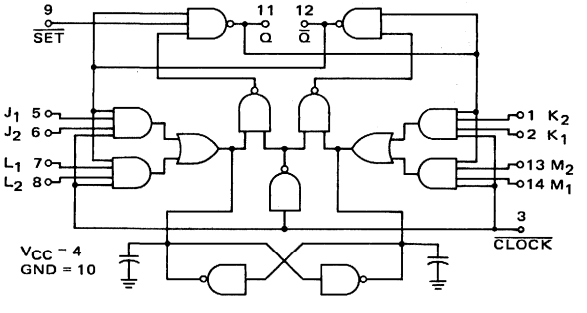
In normal operation, information is changed on the clocked inputs while the clock is in a low state, since the inputs are inhibited in this condition. Information is read into a temporary memory through the AND-OR input gating when the clock is in the high state. When the clock returns low the information in the temporary memory is transferred to the bistable section and the Q and the $\overline{Q}$ outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

Each flip-flop can be set directly by applying a low state to the direct $\overline{SET}$ input. Since each flip-flop is a charge storage device there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it very useful for shift right/shift left registers and for up/down counters.



EQUIVALENT CIRCUIT



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

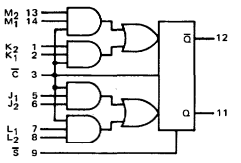
X = Don't Care
Where $J = J_1 \cdot J_2$
$L = L_1 \cdot L_2$
$K = K_1 \cdot K_2$
$M = M_1 \cdot M_2$

Total Power Dissipation = 50 mW typ/Pkg
Switching Times:
t_{on} = 20 ns typ
t_{off} = 13 ns typ

SERIES	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC2110 MC2160	2.00	0.66	(−4.0 mA)	(−1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	−55°C to +125°C
MC2010 MC2060	2.00	0.66	(−5.0 mA)	(−1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J, one K, and the $\overline{SET}$ input. The remaining J, K, L, M inputs are tested in the same manner.



	@ Test Temperature	I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	$2\ I_{in}$ mA	$4\ I_{in}$ mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts
MC2110*, MC2160	−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	22.0	12.0	-1.5	-0.7	1.0	2.0	4.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC2010*, MC2060	0°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	22.5	12.5	-1.2	-0.6	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC2110, MC2160 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2010, MC2060 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	$4\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
Input Forward Current	I_F	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	-	2,3,5,6,7, 8,13,14	-	-	-	4	1,9,10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	1,2,3,6,7, 8,13,14	-	-	-	↓	5,10,11
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	↓	3,9,10,11
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,8,10,11,13,14
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	9	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	1	-	-	-	4	9,10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	5	-	-	-	↓	10,11
		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	9	-	-	-	↓	10,11
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	9,10
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	10,11
		9		-		-		-		-		-		-	↓	-	-	9	-	-	-	-	-	-	-	-	↓	10,11
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	4	2,3,5,6,7,8,10,11,13,14
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	-	-	-	-	-	↓	1,2,3,6,7,8,9,10,12,13,14
		9		-		-		-		-		-		-	↓	-	-	9	-	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,8,10,12,13,14
Clock Input Forward Current	I_F	3	-	-4.0	-	-4.0	-	-4.0	-	-5.0	-	-5.0	-	-5.0	mAdc	-	-	-	-	-	-	-	1,2,5,6,7, 8,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	300	-	300	-	300	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,8,10,13,14
Inverse Beta Current	I_L	3	-	400	-	400	-	400	-	400	-	400	-	400	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	9,10
		3	-	400	-	400	-	400	-	400	-	400	-	400	μAdc	-	-	-	-	-	-	-	3	-	-	-	4	10,11
Breakdown Voltage	BV_{in} "0"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	4	10, 11
		3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	4	10, 12
	BV_{in} "1"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	-	-	-	-	-	-	-	4	1,2,5,6,7,8,10,13,14
Output (For Set Only) Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11①	-	-	-	-	-	-	-	9	-	-	4	3, 10
	V_{out} "1"	11	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	-	-	9	-	4	3,10
Leakage Current	I_{OLK}	12	-	650	-	650	-	650	-	650	-	650	-	650	μAdc	-	-	-	-	-	-	-	12	-	-	-	4	1,2,3,5,6,7,8,10,11,13,14
		11	-	650	-	650	-	650	-	650	-	650	-	650	μAdc	-	-	-	-	-	-	-	11	-	-	-	4	1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I_{SC}	12	-	-	-30	-70	-	-	-	-	-30	-70	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,10,11,12,13,14
		11	-	-	-30	-70	-	-	-	-	-30	-70	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	12	-	-	-	-	-	-	-	-	-	4	3,10,11
		11	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	11	-	-	-	-	-	-	-	-	-	4	3,10,12
	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12①	-	-	-	-	-	9	-	-	-	-	4	3,10
		11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11①	-	-	-	-	-	9	-	-	-	-	4	3,10
Breakdown Voltage	I_O	12	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	mAdc	-	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,10,11,13,14
		11	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	-	4.25	mAdc	-	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14
Power Requirements (Total Device) Power Supply Drain	I_{PD}	4	-	15	-	15	-	15	-	18	-	18	-	18	Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,12
	I_{PD}	4	-	15	-	15	-	15	-	18	-	18	-	18	Vdc	-	-	-	-	-	-	-	-	-	-	-	4	3,10,11

* Prime Fan-Out ① Momentarily ground pin prior to taking measurement at terminal.

OPERATING CHARACTERISTICS

Clock fall time $\leq$ 100 ns.

Triggers on clock pulse widths $\geq$15 ns.

The application of a "0" state to the $\overline{SET}$ will cause Q to go to the "1" state. The clock must be in the low state when this function is performed.

Data at the clocked inputs must be present before the clock goes to a high state. If the information on the clocked inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state change. The flip-flop will also require typically 6.0 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state, the information in the temporary storage section is transferred; and the Q and $\overline{Q}$ outputs will change accordingly. While the clock is in a low state, the J, K, L, and M terminals are inhibited.

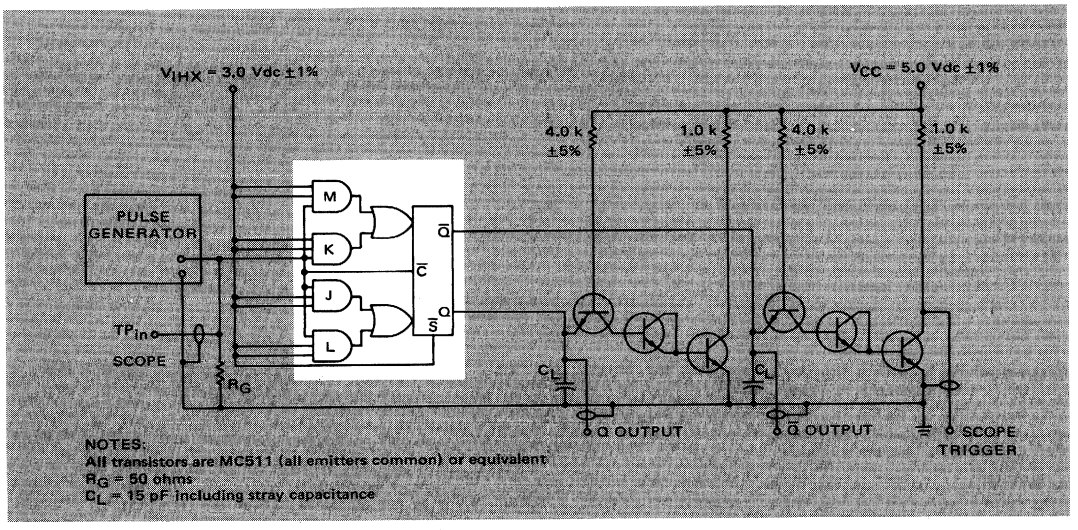
Unused Inputs:

Single unused J, K, L, and M inputs should be tied to the used input, to the clock input, or to 2.0 to 5.0 Vdc.

If both J, K, L, or M inputs are unused, they MUST be tied to ground.

Unused $\overline{SET}$ is tied to $\overline{Q}$.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



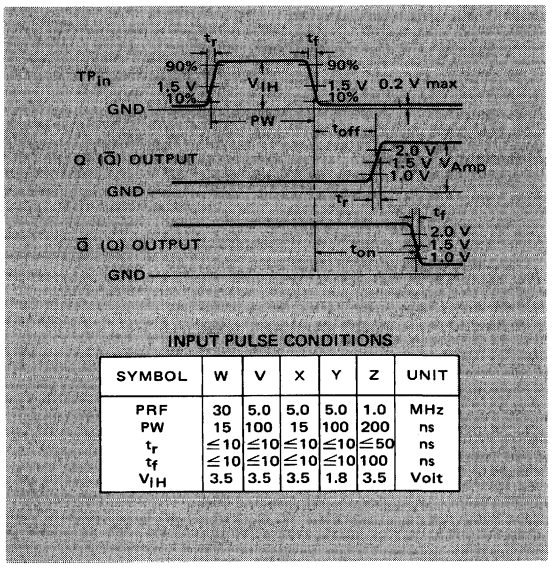
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{off}	V		20	ns
Delay Time On	t_{on}	V		25	ns
Rise Time	t_r	V		6.0	ns
Fall Time	t_f	V		4.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	30 MHz max	W
Pulse Width	PW	15 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	100 ns max	Z

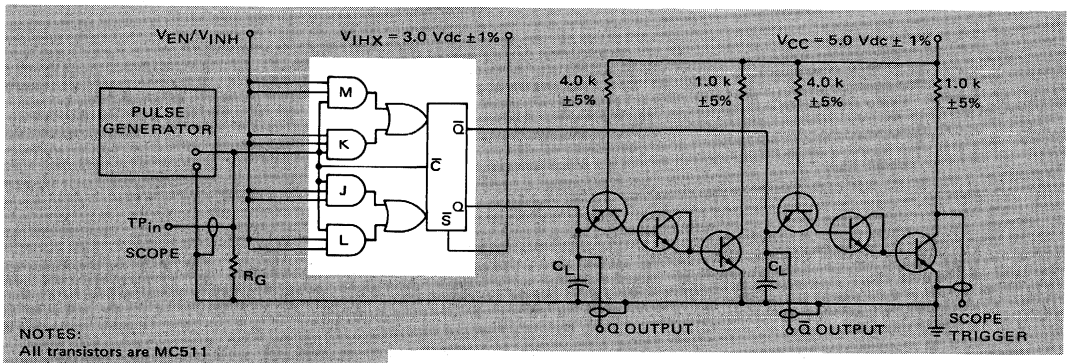
VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	30	5.0	5.0	5.0	1.0	MHz
PW	15	100	15	100	200	ns
t_r	$\leq$10	$\leq$10	$\leq$10	$\leq$10	$\leq$50	ns
t_f	$\leq$10	$\leq$10	$\leq$10	$\leq$10	100	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K-L-M TERMINAL CHARACTERISTICS TEST CIRCUIT



NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance
Enable Mode Test:
The device under test shall toggle when V_{EN} = 1.8 Vdc ±1% is applied.
Inhibit Mode Test:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ±1% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

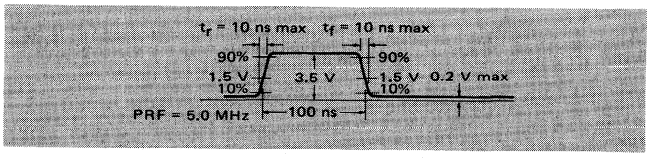
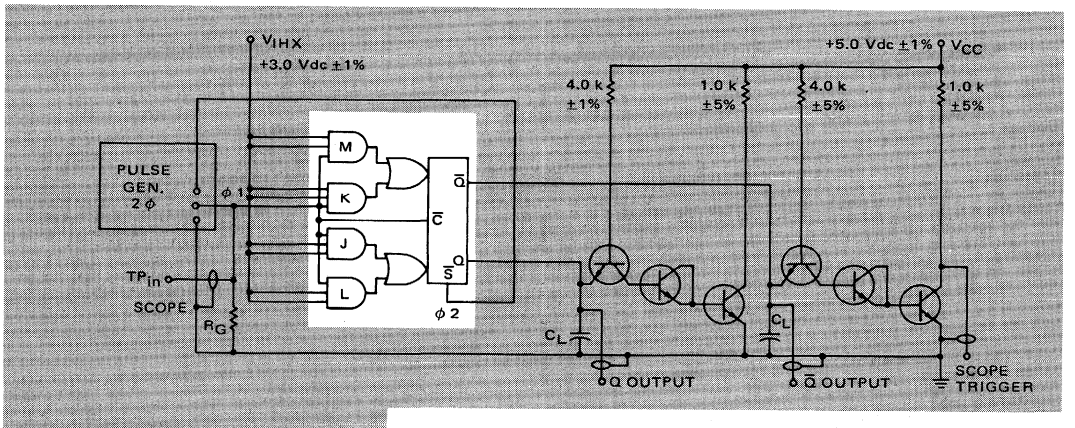


FIGURE 3 – $\overline{SET}$ TERMINAL CHARACTERISTICS TEST CIRCUIT



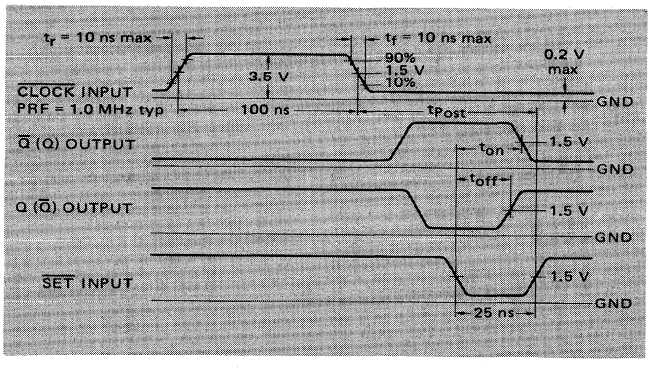
NOTES:
All transistors are MC511 (all emitters common) or equivalent
R_G = 50 ohms
C_L = 15 pF including stray capacitance capacitance
t_{Post} = Post Time

TEST PARAMETERS

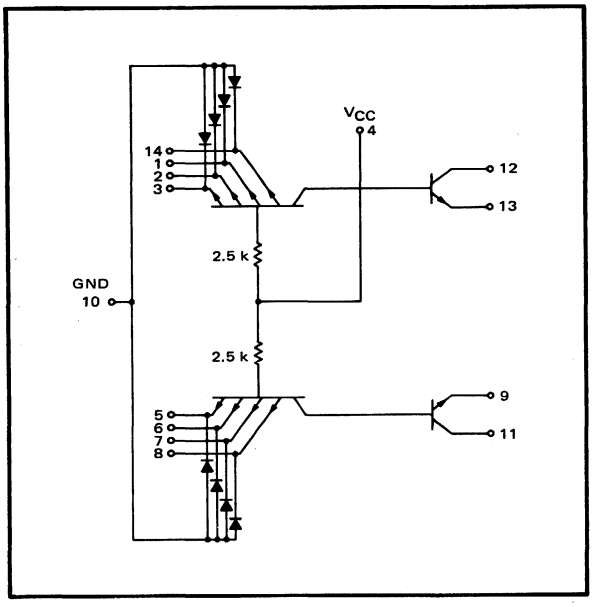
SYMBOL	VALUE	UNIT
t_{Post}	100	ns min
t_{on}	25	ns max
t_{off}	20	ns max

NOTE:
When t_{Post} is 100 ns, $\overline{SET}$ pulse must actuate the device. $\overline{SET}$ pulse cannot return to the high state before the required post time.

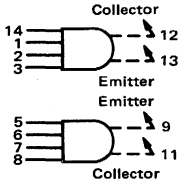
VOLTAGE WAVEFORMS AND DEFINITIONS



MC2106 • MC2156
MC2006 • MC2056



This device consists of two independent 4-input AND gates. The outputs of each gate are made available as ORing nodes. Using the MC2102 series and the MC2106 series with any one of the basic expandable gates, up to 10 AND gates can be ORed together.



Total Power Dissipation = 14 mW typ/Pkg.

Propagation Delay Times:

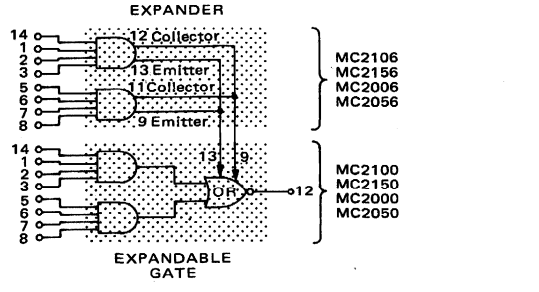
Δt_{pd} = +1.0 ns typ
When added to the expandable AND-OR-INVERT gates.

$\Delta t_{pd}/pF$ = +0.7 ns/pF typ
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR (I_F)		TEMPERATURE RANGE
MC2106 MC2156	1	−2.0 mA	−55°C to +125°C
MC2006 MC2056	1	−2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

APPLICATION: EXPANDABLE 2-WIDE 4-INPUT, "AND-OR-INVERT" GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED.

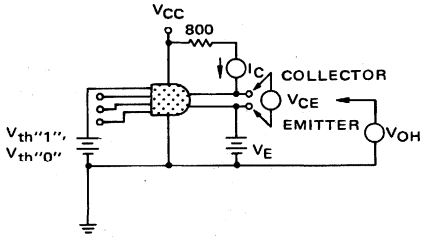


POSITIVE LOGIC

$12 = \overline{(14 \cdot 1 \cdot 2 \cdot 3) + (5 \cdot 6 \cdot 7 \cdot 8)} + \overline{(5 \cdot 6 \cdot 7 \cdot 8) + (14 \cdot 1 \cdot 2 \cdot 3)}$

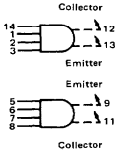
EXPANDABLE GATE — EXPANDER

V_{CE}, V_{OH} TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.

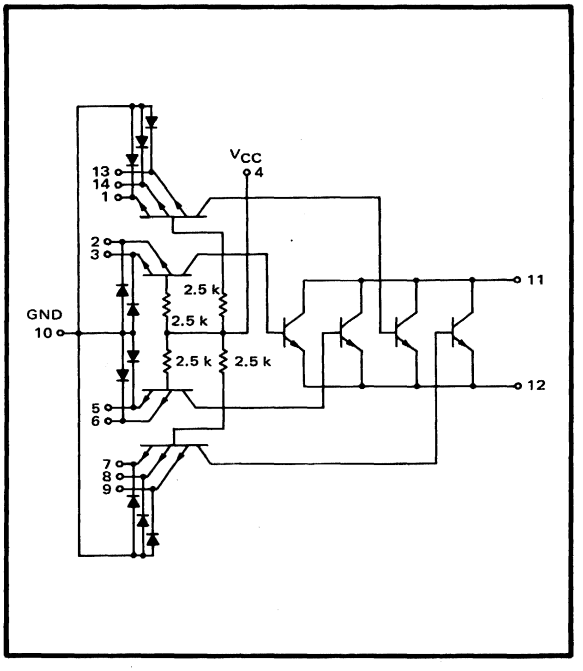


	@ Test Temperature	I_C (mA)	I_{in} (mA)	V_R (Volts)	V_{E1} (Volts)	V_{E2} (Volts)	V_{E3} (Volts)	$V_{th\,1}$ (Volts)	$V_{th\,0}$ (Volts)	V_{out} (Volts)	V_{CR} (Volts)	V_{CRH} (Volts)	V_{CC} (Volts)	V_{CCH} (Volts)
MC2106, MC2156	−55°C	6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0
	+125°C	6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
MC2006, MC2056	0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0
	+75°C	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-

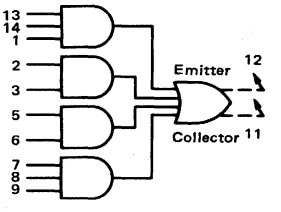
Characteristic	Symbol	Pin Under Test	MC2106, MC2156 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2006, MC2056 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	V_R	V_{E1}	V_{E2}	V_{E3}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}	Gnd†
Input																												
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	2,3,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	13	-	-	-	-	-	12	-	4	-	10
Breakdown Voltage	BV_{in} "0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	13	-	-	-	-	-	12	-	4	-	10
	BV_{in} "1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,10,14
Output																												
Output Voltage	V_{OH}	12	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	13	-	-	1	-	12	-	4	-	10
	V_{CE} ①	12	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	12	-	-	13	-	-	1	-	-	-	-	4	-	10
Leakage Current	I_{OLK}	12	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	13	-	-	12	-	-	4	-	1,2,3,10,14
Power Requirements (Total Device)																												
Maximum Power Supply Current	I_{max} ②	4	-	-	-	7.0	-	-	-	-	-	7.5	-	-	mAdc	-	-	-	-	-	9,13	-	-	-	-	11, 12	-	4	1,2,3,10,14
Power Supply Drain	I_{PDH}	4	-	3.0	-	3.0	-	3.0	-	3.6	-	3.6	-	3.6	mAdc	-	-	-	-	-	9,13	-	-	-	-	-	4	-	10‡
	I_{PDL}	4	-	4.25	-	4.25	-	4.25	-	5.25	-	5.25	-	5.25	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,10,14

* Indicated pins tied to V_{CC} thru 800 ohms ± 1.0% resistor.
** Indicated pins tied to V_{CCH} thru 800 ohms ± 1.0% resistor.
† Ground inputs to gate not under test during ALL tests, unless otherwise noted.
‡ The inputs of both gates must be ungrounded.
① V_{CE} is referenced to the emitter voltage (Pin 13). The other gate is referenced to (Pin 9).
② Pin 9 ties to Pin 13. Pin 12 ties to Pin 11.

MC2102 • MC2152
MC2002 • MC2052



This device consists of two 2-input and two 3-input AND gates ORed together with the common ORing nodes made available as the output. The basic expandable gate can be expanded up to 10 AND gates by using the MC2102 series or the MC2106 series expander package.



Total Power Dissipation = 28 mW typ/Pkg.

Propagation Delay Times:

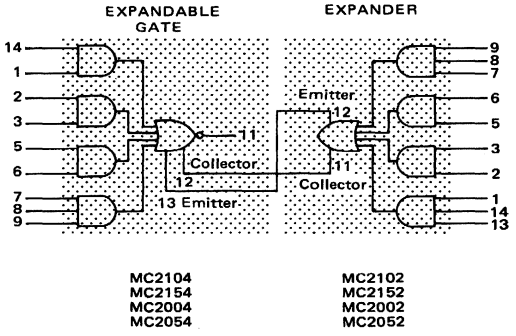
Δt_{pd} = +2.0 ns typ
When added to the expandable AND-OR-INVERT gates.

$\Delta t_{pd}/pF$ = +0.7 ns/pF typ
Caused by additional capacitance at expansion points.

SERIES	INPUT LOADING FACTOR (I_F)	TEMPERATURE RANGE
MC2102 MC2152	1 −2.0 mA	−55°C to +125°C
MC2002 MC2052	1 −2.5 mA	0°C to +75°C

Full output loading factor of the expandable gate is maintained.

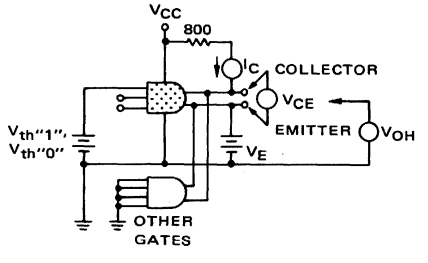
APPLICATION: EXPANDABLE 4-WIDE "AND-OR-INVERT" GATE WITH A 4-WIDE 3-2-2-3 INPUT EXPANDER CONNECTED.



MC2104
MC2154
MC2004
MC2054

MC2102
MC2152
MC2002
MC2052

V_{CE}, V_{OH} TEST CIRCUIT



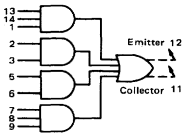
EXPANDER (MC2102)
POSITIVE LOGIC

$$11 = \overline{(13 \cdot 14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9) + (14 \cdot 1) + (2 \cdot 3) + (5 \cdot 6) + (7 \cdot 8 \cdot 9)}$$

EXPANDER — EXPANDABLE GATE

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



@ Test Temperature		TEST CONDITIONS												
		mA		Volts										
		I_C	I_{in}	V_R	V_{E1}	V_{E2}	V_{E3}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}
MC2102 , MC2152	−55°C	6.0	1.0	4.5	1.00	0.90	0.8	2.0	0.9	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.7	1.1	5.5	*	**	5.0	8.0
	+125°C	6.0	1.0	4.5	0.65	0.55	0.8	1.4	0.9	5.5	*	-	5.0	-
MC2002 , MC2052	0°C	6.0	1.0	4.5	0.90	0.80	0.8	1.9	1.0	5.5	*	-	5.0	-
	+25°C	6.0	1.0	4.5	0.85	0.75	0.8	1.8	1.1	5.5	*	**	5.0	7.0
	+75°C	6.0	1.0	4.5	0.75	0.65	0.8	1.7	1.0	5.5	*	-	5.0	-

Characteristic	Symbol	Pin Under Test	MC2102, MC2152 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2002, MC2052 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	V_R	V_{E1}	V_{E2}	V_{E3}	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CR}	V_{CRH}	V_{CC}	V_{CCH}	Gnd
Input																													
Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	2,3,5,6,7, 8,9,13,14	-	-	-	-	-	-	-	-	4	-	1,10
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8, 9,10,13,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	1	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
Breakdown Voltage	BV_{in}"0"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	12	-	-	-	-	-	11	-	4	-	2,3,5,6,7,8,9,10
	BV_{in}"1"	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	4	-	2,3,5,6,7,8,9, 10,13,14
Output																													
Output Voltage	V_{OH}	11	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	4.8	-	Vdc	-	-	-	-	12	-	-	1	-	11	-	4	-	2,3,5,6,7,8,9,10
	V_{CE} ①	11	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	-	0.65	Vdc	11	-	-	12	-	-	1	-	-	-	-	4	-	2,3,5,6,7,8,9,10
Leakage Current	I_{OLK}	11	-	250	-	250	-	250	-	250	-	250	-	250	μAdc	-	-	-	-	-	12	-	-	11	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	14	-	-	-	-	-	15	-	-	mAdc	-	-	-	-	-	12	-	-	-	-	11	-	4	1,2,3,5,6,7,8, 9,10,13,14
Power Supply Drain	I_{PDH}	4	-	6.0	-	6.0	-	6.0	-	7.2	-	7.2	-	7.2	mAdc	-	-	-	-	-	12	-	-	-	-	-	4	-	10
	I_{PDL}	4	-	8.5	-	8.5	-	8.5	-	10.5	-	10.5	-	10.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8, 9,10,13,14

* Indicated pins tied to V_{CC} thru 800 ohms ± 1.0% resistor.
** Indicated pins tied to V_{CCH} thru 800 ohms ± 1.0% resistor.
① V_{CE} is referenced to the emitter Voltage (Pin 12).

MTTL III

INTEGRATED CIRCUITS

MC3000 SERIES

MTTL III

INTEGRATED CIRCUITS

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DEVICE SPECIFICATIONS

GATES

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MC3030	Dual 4-Input Expander for AND-OR-INVERT Gates	4-122

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MC3050	AND J-K Flip-Flop	4-128
MC3052	AND Input $J\bar{J}$-$K\bar{K}$ Flip-Flop	4-133
MC3060	Dual Type D Flip-Flop	4-138
MC3061	Dual J-K Flip-Flop	4-141
MC3062	Dual J-K Flip-Flop	4-145

NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 5.0 V, T_A = 25°C

Function	Type	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg	Page No.
Quad 2-Input NAND Gate	MC3000	10	6.0	88	4-112
Quad 2-Input AND Gate	MC3001	10	9.0	112	4-110
Quad 2-Input NOR Gate	MC3002	10	6.0	122	4-114
Quad 2-Input OR Gate	MC3003	10	9.0	150	4-116
Triple 3-Input NAND Gate	MC3005	10	6.0	66	4-108
Dual 4-Input NAND Gate	MC3010	10	6.0	44	4-104
Single 8-Input NAND Gate	MC3015	10	8.0	22	4-102
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	MC3020	10	6.0	62.5	4-106
Dual 4-Input NAND Power Gate	MC3025	20	6.0	70	4-120
Dual 4-Input AND Power Gate	MC3026	20	9.0	90	4-118
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	*	9.0	56	4-124
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	*	6.0	44	4-126
Dual 4-Input Expander for AND-OR-INVERT Gates	MC3030	**	***	15	4-122
AND J-K Flip-Flops	MC3050	10	f = 40 MHz	80	4-128
AND Input $J\bar{J}$-$K\bar{K}$ Flip-Flop	MC3052	10	f = 40 MHz	75	4-133
Dual Type D Flip-Flop	MC3060	10	f = 30 MHz	120	4-138
Dual J-K Flip-Flop	MC3061	10	f = 50 MHz	100	4-141
Dual J-K Flip-Flop	MC3062	10	f = 50 MHz	100	4-145

*Direct Output = 10 minus the number of resistor-terminated outputs being used.

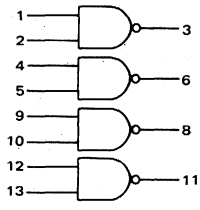
**Full output loading factor of the expandable gate is maintained.

***Δt_{pd} = +1.0 ns typ when added to the expandable AND-OR-INVERT Gate.

Δt_{pd}/pF = +1.0 ns pF typ caused by additional capacitance at expansion points.

GATES

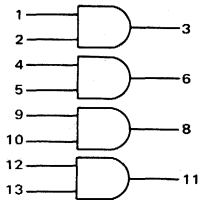
MC3000
Quad 2-Input NAND Gate



$3 = \overline{1 \cdot 2}$

t_{pd} = 6.0 ns typ
P_D = 88 mW typ/pkg

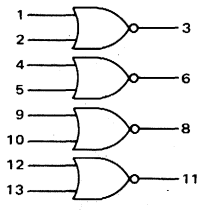
MC3001
Quad 2-Input AND Gate



$3 = 1 \cdot 2$

t_{pd} = 9.0 ns typ
P_D = 112 mW typ/pkg

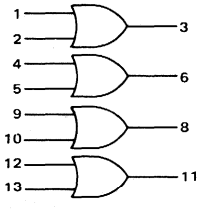
MC3002
Quad 2-Input NOR Gate



$3 = \overline{1 + 2}$

t_{pd} = 6.0 ns typ
P_D = 122 mW typ/pkg

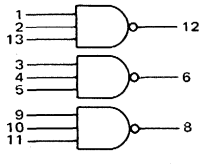
MC3003
Quad 2-Input OR Gate



$3 = 1 + 2$

t_{pd} = 9.0 ns typ
P_D = 150 mW typ/pkg

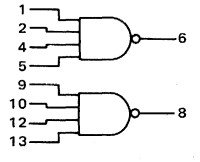
MC3005
Triple 3-Input NAND Gate



$12 = \overline{1 \cdot 2 \cdot 13}$

t_{pd} = 6.0 ns typ
P_D = 66 mW typ/pkg

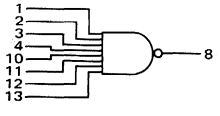
MC3010
Dual 4-Input NAND Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 6.0 ns typ
P_D = 44 mW typ/pkg

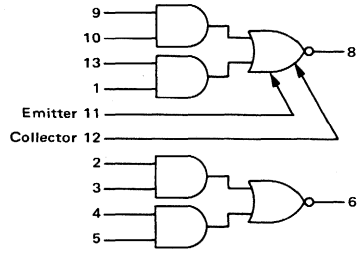
MC3015
Single 8-Input NAND Gate



$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$

t_{pd} = 8.0 ns typ
P_D = 22 mW typ/pkg

MC3020
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate



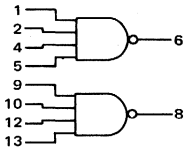
$8 = \overline{(9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$

t_{pd} = 6.0 ns typ
P_D = 62.5 mW typ/pkg

LOGIC DIAGRAMS (continued)

POWER GATES

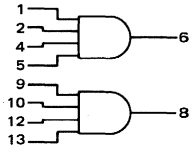
MC3025
Dual 4-Input NAND Power Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

t_{pd} = 6.0 ns typ
P_D = 70 mW typ/pkg

MC3026
Dual 4-Input AND Power Gate

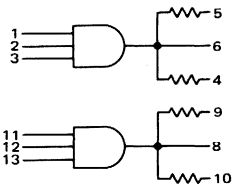


$6 = 1 \cdot 2 \cdot 4 \cdot 5$

t_{pd} = 9.0 ns typ
P_D = 90 mW typ/pkg

LINE DRIVERS

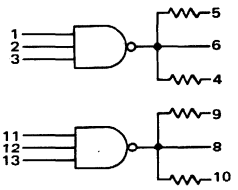
MC3028
Dual 3-Input 3-Output AND
Series Terminated Line Driver



4, 5, 6, = 1 • 2 • 3

t_{pd} = 9.0 ns typ
P_D = 56 mW typ/pkg

MC3029
Dual 3-Input 3-Output NAND
Series Terminated Line Driver

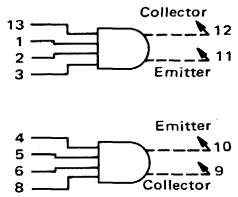


$4, 5, 6 = \overline{1 \cdot 2 \cdot 3}$

t_{pd} = 6.0 ns typ
P_D = 44 mW typ/pkg

EXPANDER

MC3030
Dual 4-Input Expander for
AND-OR-INVERT Gates



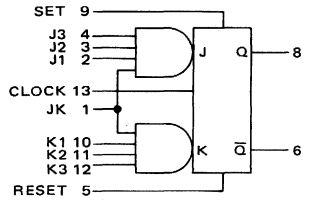
Δt_{pd} = +1.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = +1.0 ns pF typ
Caused by additional capacitance at expansion points.

P_D = 15 mW typ/pkg

FLIP-FLOPS

MC3050
AND J-K Flip-Flop

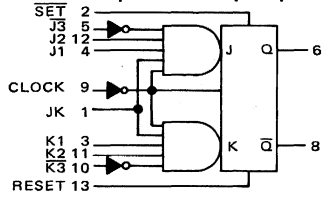


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where:
J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

f = 40 MHz
P_D = 80 mW typ/pkg

MC3052
AND Input $J\overline{J}$-$K\overline{K}$ Flip-Flop

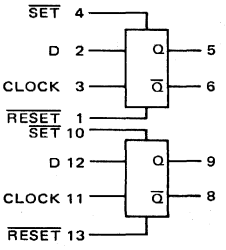


J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where:
J = J1 • J2 • $\overline{J3}$ • JK
K = K1 • K2 • $\overline{K3}$ • JK

f = 40 MHz
P_D = 75 mW typ/pkg

MC3060
Dual Type D Flip-Flop

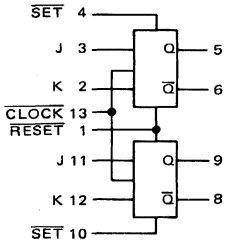


D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$

f = 30 MHz
P_D = 120 mW typ/pkg

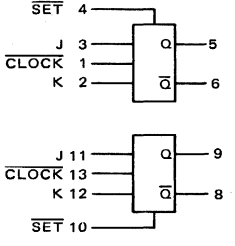
MC3061
Dual J-K Flip-Flop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

f = 50 MHz
P_D = 100 mW typ/pkg

MC3062
Dual J-K Flip-Flop



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

f = 50 MHz
P_D = 100 mW typ/pkg

MTTL III

GENERAL INFORMATION SECTION

INTRODUCTION

MTTL III integrated circuits are designed with speed approaching the limit for saturated logic and for good load driving capability. This line includes all the characteristics that have made transistor-transistor logic so popular. The major advantage of MTTL III over other TTL lines is the square transfer characteristic (Figure 1) that exists only for the MTTL III family. Because of this "ideal" transfer characteristic, the MTTL III family is the only TTL line that is truly compatible with MDTL. Another advantage of this family over competitive TTL lines is that it is designed to minimize problems associated with ringing.

The circuits in the MTTL III family are distinguished by a multiple-emitter input transistor, a darlington active "pull-up" in the upper output network, and an active bypass network in the base of the output pull-down transistor as shown in Figure 2.

The multiple-emitter input configuration offers the maximum logic capability in the minimum physical area and provides improved switching characteristics during turnoff. Clamp diodes are provided at each of the inputs to limit undershoot that occurs in typical system applications such as driving long interconnect wiring. The Darlington output configuration provides very low output impedances in each of the two output states. These low impedances result in excellent ac noise immunity and allows high-speed operation while driving large capacitive loads.

The active bypass shown in the dotted area of Figure 2 holds the phase inverter transistor "off" until gate threshold is reached. This circuit operation provides the squared transfer characteristic shown in Figure 1.

In addition to improving the transfer characteristic, the bypass network offers a number of advantages compared to a simple resistor that can be traced to a much smaller impedance variation with temperature.

1. *Lower bypass impedance for the reverse current of the output transistor at elevated temperatures, provides faster turn-off.*
2. *A lower current spike during the turn-off transient causes a lower ac power factor resulting in a lower total power consumption. This advantage is even more pronounced at higher temperatures.*
3. *Faster turn-on at low temperature.*

FIGURE 1 – COMPARISON OF CONVENTIONAL TRANSISTOR-TRANSISTOR LOGIC AND MTTL III

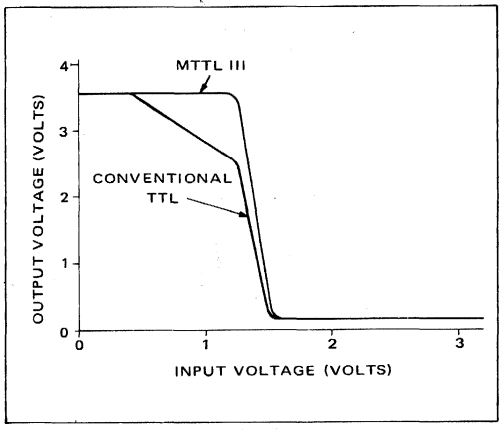
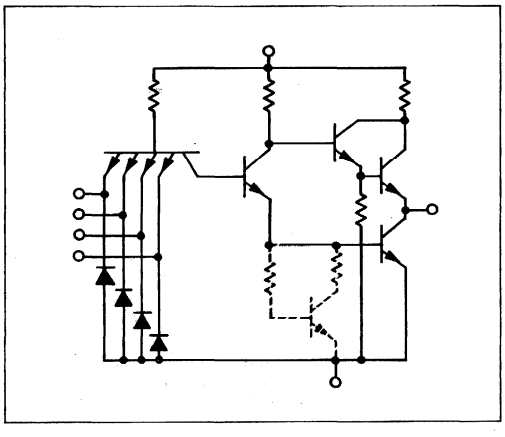


FIGURE 2 – TYPICAL MTTL III CIRCUIT



TYPICAL CHARACTERISTICS

Typical operating characteristics of the MTTL III family include: (Unless otherwise indicated, the parameters are defined for V_{CC} = +5.0 volts and T_A = +25°C.)

Supply Voltage Operating Range = 4.5 to 5.5 volts

Operating Temperature Range: MC3000 Series
0 to +75°C

Output Drive Capability
Gates (Output Loading Factor):
MC3000 Series = 10 Gates.

Capacitance = 600 pF

Output Impedance
High State = 10 ohms nominal (unsaturated)
Low State = 10 ohms nominal

Output Voltage Swing = 0.2 to 3.5 volts typical

Input Voltage Limits
+5.5 volts maximum
-1.5 volts minimum (1)

Switching Threshold = 1.5 volts nominal

Input Impedance
High State = 400 k ohms nominal
Low State = 2.4 k ohms nominal

Worst-Case dc Noise Margin
High State = 0.700 volt minimum
Low State = 0.700 volt minimum

Power Dissipation
22 mW per gate typical
50-80 mW per flip-flop typical

Switching Speeds (2)
Average Propagation Delay = 6.0 ns per gate typical
13 ns per flip-flop typical
Rise Time = 1.0 ns typical
Fall Time = 1.3 ns typical

Flip-Flop Clock Frequency (MC3061) = 50 MHz maximum.

(1) Assuming unused inputs are returned to voltage not greater than 4.0 Vdc.

(2) The switching characteristics of the MTTL III family are defined with respect to the associated transitions of the voltage waveforms. The average propagation delay is defined as the average of the turn-on delay and the turn-off delay measured from the 1.5 V point of the input to the 1.5 V point of the associated output transition or:

$$t_{pd} = \frac{t_{on} + t_{off}}{2} \text{ ns}$$

Rise time is defined as the positive going transition of the output from the 1.0 V to the 2.0 V level. Fall time is defined as the negative output transition from the 2.0 V to the 1.0 V level.

"NAND" GATES

The basic gate of the MTTL III logic family is the positive logic NAND gate. This gate is characterized by high speed, good load driving capability, superior transfer characteristic, and freedom from ringing problems. Representative of the various NAND gates presently available in the MTTL III family is the 4-input NAND gate (½ of the MC3010) shown in Figure 3.

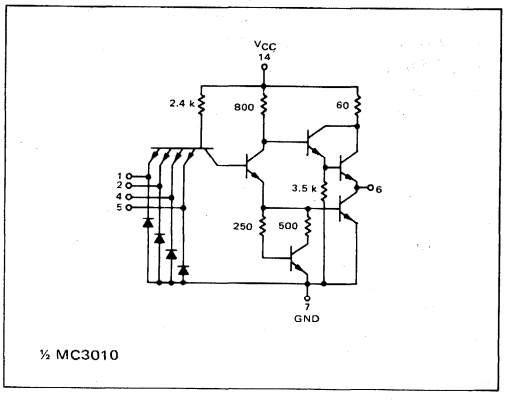
"AND" GATES

While it is possible to design a complete logic system with NAND logic, it is often desirable to use other logic forms to save circuits, power dissipation, and propagation delay. Therefore, the positive logic AND function has been added to the MTTL III family.

Examples of the AND function are the standard quad 2-input gate, dual 4-input gate, dual 4-input power gate and a dual 3-input, 3-output line driver.

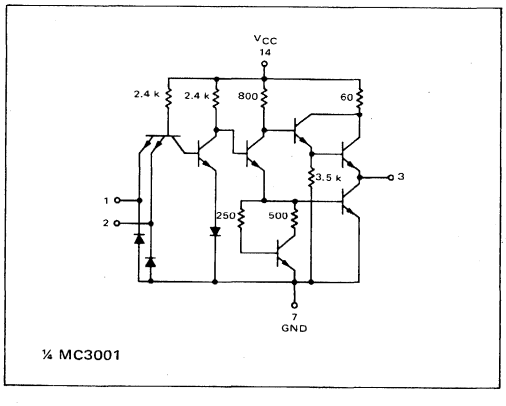
The technique used to form the AND function is the addition of an inverter to the basic NAND circuit. As shown in Figure 4, the inverter transistor with a collector resistor and an offset diode connected to its emitter is inserted between the multiple-emitter input transistor and the basic circuit phase-splitter transistor. The extra inversion adds only 3.0 ns propagation delay and about 6.0 mW additional power dissipation.

FIGURE 3 – MTTL III POSITIVE LOGIC "NAND" GATE CIRCUIT



½ MC3010

FIGURE 4 – MTTL III POSITIVE LOGIC "AND" GATE CIRCUIT



¼ MC3001

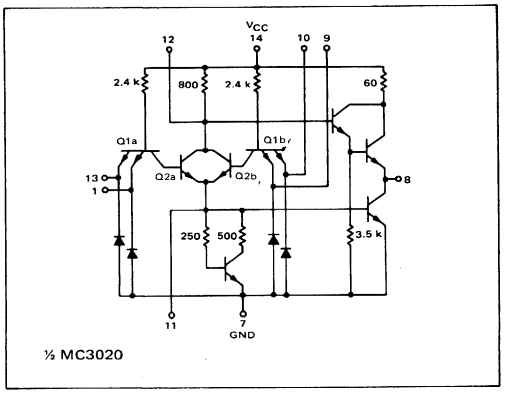
"AND-OR-INVERT" GATES

Unlike the MDTL family of logic circuits, the outputs of MTTL logic circuits cannot be tied together to perform the "Implied AND", often called the "Wired OR" function. If the outputs of the MTTL family devices are tied together, the lower output transistor of one circuit and the upper output transistor of another circuit can be "on" simultaneously. This condition provides a low-impedance path from V_{CC} to ground, and due to excessive current flow, the saturated output state cannot be maintained and the desired logic function is not satisfied.

To retain the logical advantages offered by the "Implied AND" with the speed and load driving capability of an active pull-up, the MTTL III family offers an AND-OR-INVERT Gate. The gate in Figure 5 incorporates two 2-input AND functions with outputs that are ORed and inverted. The AND function is provided by two multiple-emitter input transistors (Q1a and Q1b). The OR and INVERT operation is accomplished by two paralleled transistors (Q2a and Q2b) sharing a single collector resistor and a single bypass network. These paralleled transistors in turn drive the standard output.

The common collector and emitter nodes of one gate in each package are available externally to permit expansion.

FIGURE 5 – MTTL III "AND-OR-INVERT" GATE CIRCUIT



EXPANDER AND EXPANDER NODES

The ORing nodes of ½ the MC3020 dual AND-OR-INVERT Gate (Figure 5) are available for expanding the number of AND gates to four. Since these are comparatively high-impedance nodes, care should be taken to minimize capacitive loading on the expander terminals if switching speed is to be maintained. When an expander is to be used with an expandable AND-OR-INVERT gate, it should be placed as close as possible to the gate being expanded. The increase in the average propagation delay per AND gate added to an expandable AND-OR-INVERT gate is typically 1.0 ns/AND gate. The increase in average propagation delay as a function of capacitance added to the expander nodes is typically 1.0 ns/pF.

"NOR" GATES

To save inverters, the system designer often needs the positive logic NOR function as well as the negative logic NOR available with the standard NAND gate. This capability is incorporated in the MTTL III line in the form of the MC3002, quad 2-input NOR Gate. The NOR gate is a modified AND-OR-INVERT gate with only a single emitter on each input transistor, as shown in Figure 6.

"OR" GATES

To provide the system designer with still another tool for optimum design, the MTTL III Series also offers the positive logic OR function. As shown in Figure 7, the OR is essentially a NOR gate with an additional inverter.

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In most systems, however, there are a few applications that exceed the capability of a standard gate. The MTTL III power gates, shown in Figure 8, are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates: 20 standard gate loads instead of 10.

FIGURE 6 – MTTL III POSITIVE LOGIC "NOR" GATE CIRCUIT

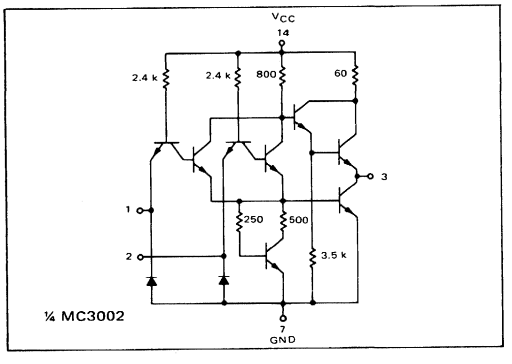
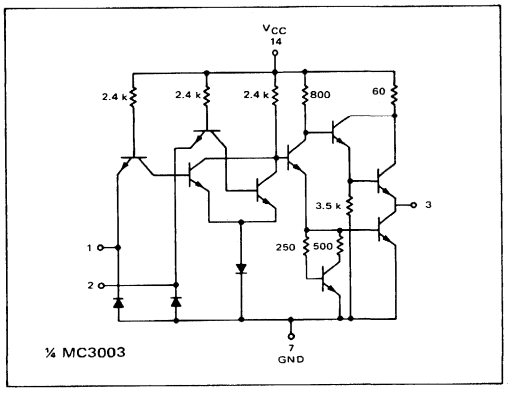


FIGURE 7 – MTTL III POSITIVE LOGIC "OR" GATE CIRCUIT



LINE DRIVERS

To minimize switching transients on long lines, the MTTL III family includes dual 3-input/3-output series-terminated line drivers. Two outputs have 75-ohm resistors in series with the standard output node, and one is connected directly to the node. A good match can be made at the output of each resistor when driving 93-ohm coax or 120-ohm twisted pair. For loads of 50 to 93 ohms, the two resistive outputs are paralleled for impedance matching. The non-resistive output can be used to drive adjacent loads in a normal fashion. The total number of output loads connected to the direct output (non-resistive output) is the standard fan-out of 10, minus the number of resistor terminated outputs being used.

Figure 9 shows 1/2 of the circuit of the MC3029, dual 3-input, 3-output series terminated NAND line driver. Figure 10 shows a typical application of this circuit and Figure 11 demonstrates the effects of series termination without a significant loss in high state noise immunity.

FIGURE 8 – MTTL III POWER GATE CIRCUIT (AND)

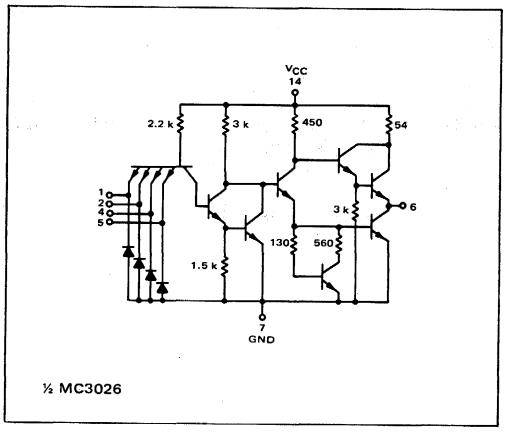


FIGURE 9 – MTTL III TERMINATED LINE DRIVER (NAND)

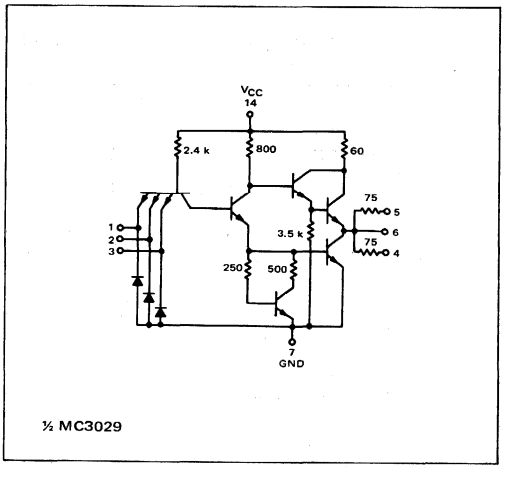


FIGURE 10 – TYPICAL APPLICATION OF THE LINE DRIVER

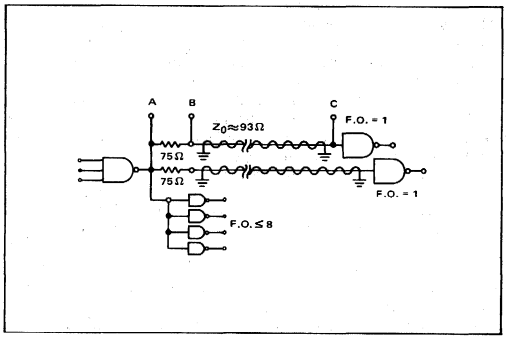
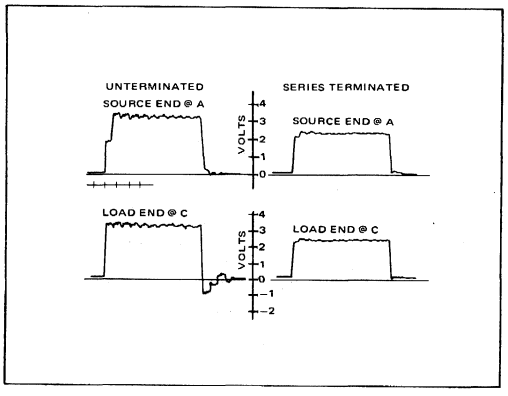


FIGURE 11 – EFFECTS OF SERIES TERMINATION WITH A MTTL III GATE DRIVING A 93-OHM LINE



OPERATING CHARACTERISTICS OF FLIP-FLOPS

The cornerstone of any modern logic family is the capability of its storage elements. The MTTL III flip-flops are designed to give maximum logic performance with fewer system restrictions than their predecessors. Three basic designs are typified by the MC3050, MC3060 and MC3061/MC3062. Common to all designs are:

1. Edge clocking.

   The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25°C).

2. Overriding asynchronous inputs.

   The direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock or the information on synchronous inputs.

3. Short set-up times.

   Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Therefore data may be applied anytime in the clock period except during the time interval between the Set-up and Hold times. This characteristic permits higher clock frequencies or eliminates the necessity for critical control of clock pulse width.

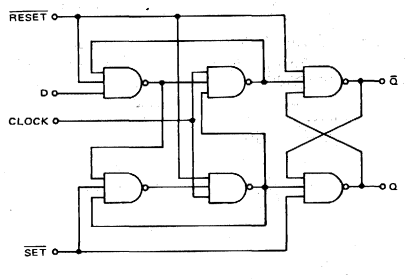
4. All inputs to the storage elements including the clock input have inputs that are compatible with all three MTTL families.

The MC3050 and MC3060 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3061 and MC3062 dual flip-flops are negative edge triggered devices and therefore operate in precisely the opposite manner. That is, data is stored on the negative edge of the clock.

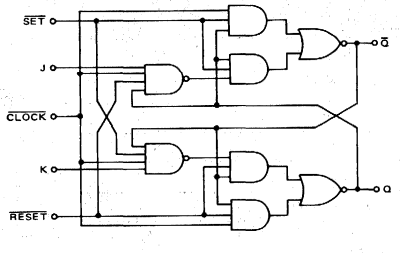
In addition to the previously mentioned storage elements. The MC3052 Master-Slave flip-flop is also available. Data is stored in the Master flip-flop when the clock is low and transferred to the Slave flip-flop when the clock goes high.

Detailed discussion of each of the MTTL III flip-flops is provided on the individual data sheets.

FIGURE 12 – LOGIC DIAGRAMS OF EDGE-CLOCKED MTTL III FLIP-FLOPS

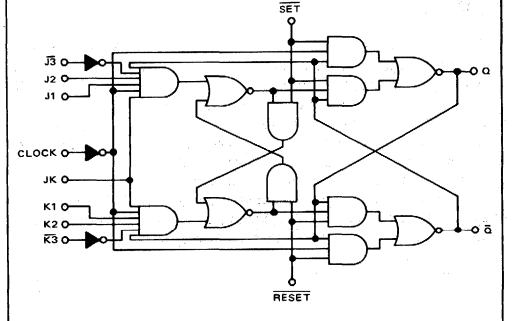


MC3060

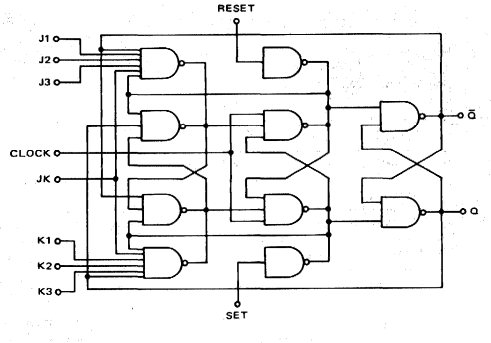


MC3061

FIGURE 13 – LOGIC DIAGRAM OF MTTL III MASTER-SLAVE J-K FLIP-FLOP



MC3052



MC3050

BREADBOARDING SUGGESTIONS

When breadboarding with any form of high-speed, high-performance TTL circuit, the designer must always be aware of the problems caused by very high switching speeds. These switching speeds, especially the frequencies associated with the very fast rise and fall times of the circuits, are in the upper RF range and good high-frequency layout techniques should be used. The following breadboarding suggestions will help the designer in his initial circuit layout. In many cases the breadboarding suggestions will have to be modified to meet the requirements of the designer's specific application.

Power and Ground Distribution

Special care should be taken to insure adequate distribution of power and ground systems. The typical rates of change of current and voltage for a single MTTL III gate are in the range of 10^7 A/s and 10^8 V/s respectively. These figures reflect the necessity for a low-impedance power supply and ground distribution system, if transients are to be minimized and noise margins maintained. The use of AWG No. 20 wire or larger is often required. For printed circuitry, line widths of 100 mils or more are often necessary. A ground plane is desirable when using a large number of units.

Bypassing

To reduce supply transients, the breadboard should be bypassed at the point where power is supplied to the board and at intervals throughout the board. The use of a single bypass capacitor at the output terminal of the power supply is not adequate in a breadboard utilizing the fast rise and fall time MTTL III circuits. A comparatively large, low-inductance type capacitor (in the 1.0 μF range) is suggested at the point where power and ground enter the board. In many cases it has been found that distributing 0.01 μF capacitors for every five packages throughout a breadboard is adequate to suppress normal switching transients. It is also suggested that a bypass capacitor be placed in close proximity to any circuit driving a large capacitive load.

Power Dissipation

The typical average dc power dissipation is given for each MTTL III device (3). It should be noted that the totem-pole output common to all high-level MTTL circuits has an associated ac power dissipation factor. This factor results from the timing overlap of the upper and lower output transistors during the normal switching operation and is typically 0.4 mW/MHz/output for a 15-pF load. This ac power dissipation should be added when calculating the total power requirements of the MTTL III circuits.

Unused Inputs and Unused Gates

To minimize potential problems resulting from external noise, the unused inputs of any MTTL III logic circuit should not be left open, but should either be tied to the used inputs or returned to a voltage between 2.0 and 5.5 Vdc. (For flip-flops, see appropriate data sheet for additional detail.) If the unused inputs are returned to a voltage, care should be exercised to insure that the absolute voltage between the most negative input level and that voltage does not exceed +5.5 volts. The total number of inputs that can be tied to the output of any driving gate is 25. (This is defined as high-state output loading factor.) It should be noted that the low-state output loading rules must still be maintained. The minimum logical "1" level for the high-state output loading is summarized for V_{CC} = 5.0 V, V_{IL} = 1.1 V, and I_{OH} = -2.0 mA: V_{OH} = 2.5 volts minimum @ 0^oC.

To minimize power drain, the inputs of any unused gate in a package should be maintained at the level that would place the outputs in the high state (the low power dissipation state).

(3) $$P_D = \frac{I_{PDL} + I_{PDH}}{2} (V_{CC})$$

where I_{PDL} and I_{PDH} are the typical current drains at V_{CC} = +5.0 V.

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage — Continuous	+7.0	Vdc
Supply Operating Voltage Range	4.5 to 5.5	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range — Flat Package Plastic Package	−65 to +175 −55 to +125	°C °C

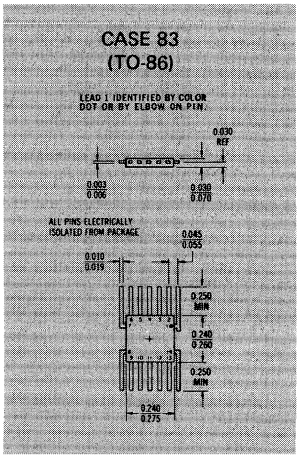
DEFINITIONS

BV_{in}	Input breakdown voltage
C_T	Total parasitic capacitance, which includes probe, wiring, and load capacitances
I_C	Collector current
I_{CO}	Expander collector leakage current
I_D	Input diode current with negative voltage applied
I_E	Emitter current
I_{EO}	Expander emitter leakage current
I_{EXE}	Expander drive current at emitter node of AND-OR-INVERT gate
I_F	Input forward current with V_{CC} applied
I_{F1}	Input forward current with V_{CCL} applied
I_{F2}	Input forward current with V_{CCH} applied
I_{FC}	Clock input forward current
I_{FD}	D input forward current
I_{FJ}	J input forward current
I_{FK}	K input forward current
I_{FJK}	JK input forward current
I_{FR}	RESET input forward current
I_{FS}	SET input forward current
I_{in}	Input current
I_{max}	Maximum rated power supply current with V_{max} applied
I_{OH}	Output high state current
I_{OHA}	Unterminated output high state current
$I_{OHB, C}$	Terminated output high state current
I_{OL}	Output low state current
I_{OL1}	Output low state current with V_{CCL} applied
I_{OL1A}	Unterminated output low state current with V_{CCL} applied
I_{OL2}	Output low state current with V_{CCH} applied
I_{OL2A}	Unterminated output low state current with V_{CCH} applied
$I_{OL1B, 1C}$	Terminated output low state current with V_{CCL} applied
$I_{OL2A, 2C}$	Terminated output low state current with V_{CCH} applied
I_{PD}	Flip-flop power supply drain current
I_{PDH}	Power supply drain with inputs high
I_{PDL}	Power supply drain with inputs low
I_R	Input leakage current
I_{RC}	Clock input leakage current
I_{RD}	D input leakage current
I_{RJ}	J input leakage current
I_{RK}	K input leakage current
I_{RJK}	JK input leakage current
I_{RR}	RESET input leakage current
I_{RS}	SET input leakage current
I_{SC}	Short-circuit current
P_1	Pulse used to set flip-flop state
PRF	Pulse repetition frequency
PW	Pulse width
t_f	Fall time
$t_{Hold\ "0"}$	Minimum time that low state data must be maintained after the clocking edge
$t_{Hold\ "1"}$	Minimum time that high state data must be maintained after the clocking edge
Δt_{pd}	Average increase in propagation delay per expander AND gate when connected to an AND-OR-INVERT gate
$\Delta t_{pd}/pF$	Increased propagation delay caused by additional capacitance at expansion points
$t_{pd\ "0"}$	Turn-on delay
$t_{pd\ "1"}$	Turn-off delay
t_r	Rise time
$t_{sd\ "0"}$	Turn-on delay from asynchronous input
$t_{sd\ "1"}$	Turn-off delay from asynchronous input
$t_{Set\ "0"}$	Minimum time that low state data must be applied prior to the clocking edge
$t_{Set\ "1"}$	Minimum time that high state data must be applied prior to the clocking edge
TP_{in}	Test point at input of device under test
TP_{out}	Test point at output of device under test
$V_{BE\ max}$	Emitter node threshold voltage for logic "0" output level
$V_{BE\ min}$	Emitter node threshold voltage for logic "1" output level
V_{CC}	Power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_D	Diode clamp voltage
V_{EE1}	Voltage applied to expander emitter for V_{OL} test
V_{EE2}	Voltage applied to expander emitter node for I_{CO} test
V_F	Maximum logic "0" level output voltage
V_{IH}	Logic "1" threshold voltage
V_{IHX}	Reduced supply voltage to hold input above threshold and to prevent noise from entering the device
V_{IL}	Logic "0" threshold voltage
V_{max}	Maximum rated power supply voltage
V_{OH}	Output high voltage with I_{OH} source current
V_{OL}	Output low voltage with I_{OL} source current
V_{OL1}	Maximum output low voltage with V_{CCL} applied
V_{OL2}	Maximum output low voltage with V_{CCH} applied
V_{OL3}	Maximum output low voltage on terminated output with V_{CCL} applied
V_{OL4}	Maximum output low voltage on terminated output with V_{CCH} applied
V_R	Logic "1" minimum reverse voltage
V_{RH}	Logic "1" maximum reverse voltage

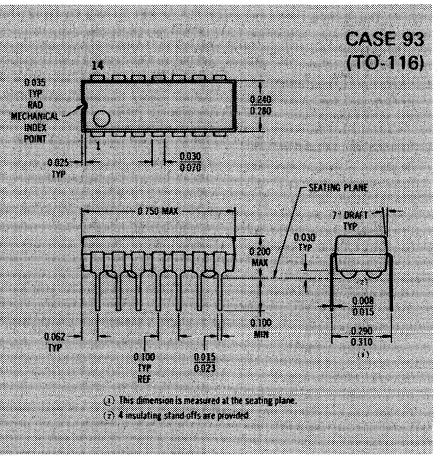
PACKAGING

All MTTL III integrated circuits are available in the TO-85 14 lead flat package and TO-116 dual in-line plastic package. Suffix "F" to the basic type number; to order plastic package, add Suffix "P".

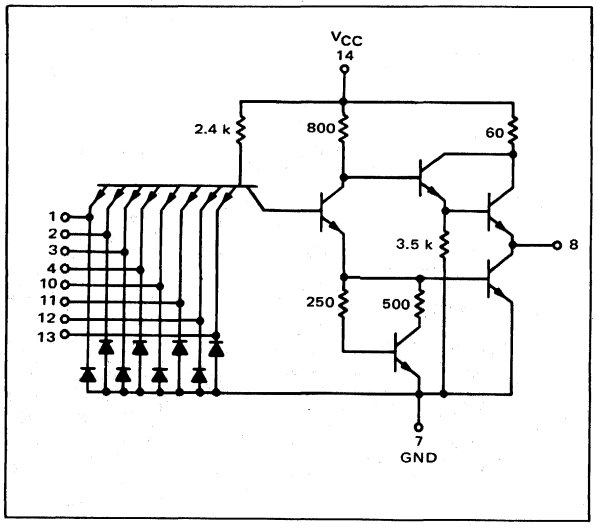
CASE 83
(TO-86)



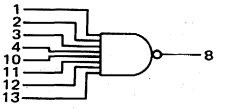
CASE 93
(TO-116)



MC3015



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders and decoders.



Positive Logic:

$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$

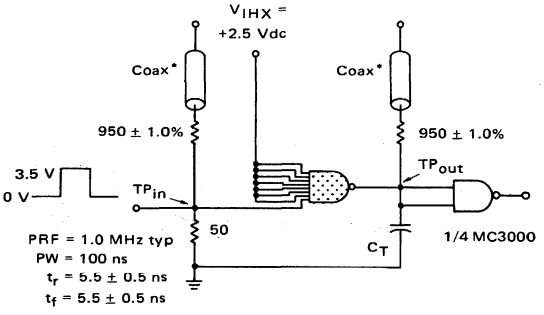
Negative Logic:

$8 = \overline{1 + 2 + 3 + 4 + 10 + 11 + 12 + 13}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 22 mW typ/pkg
Propagation Delay Time = 8.0 ns typ

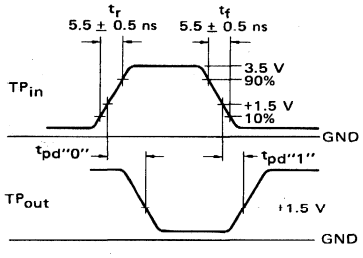
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

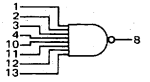
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of this device. To complete testing, sequence through remaining inputs in the same manner.

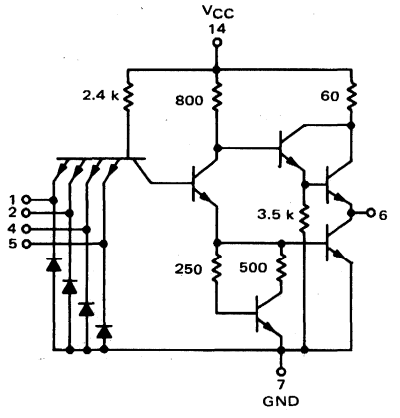


@Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

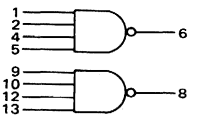
Characteristic	Symbol	Pin Under Test	MC3015 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2, 3, 4, 10, 11, 12, 13	-	-	-	14	-	7
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 3, 4, 7, 10, 11, 12, 13
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7
Output Output Voltage	V_{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	14	-	-	7
	V_{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	1	-	-	2, 3, 4, 10 11, 12, 13	-	-	-	14	-	7
	V_{OH}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	1	-	-	-	2, 3, 4, 10, 11, 12, 13	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	8	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7,8, 10, 11, 12,13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	6.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Power Supply Drain	I_{PDH}	14	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 10, 11, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	4.3	-	4.3	-	4.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13
Switching Parameters Turn-On Delay	$t_{pd"0"}$	1, 8	-	-	-	12	-	-	ns	Pulse In: 1	Pulse Out: 8	-	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13,	7
Turn-Off Delay	$t_{pd"1"}$	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 10, 11, 12, 13	7

MC3010

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND gates. These gates may be cross-coupled to form a set-reset flip-flop.

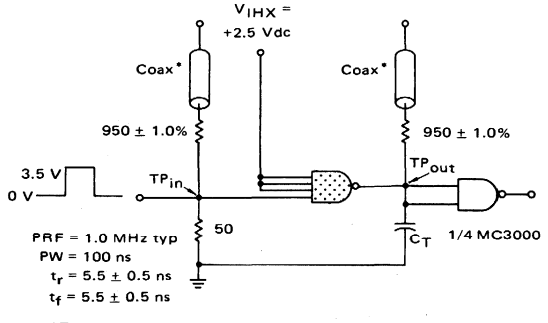


Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 44 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

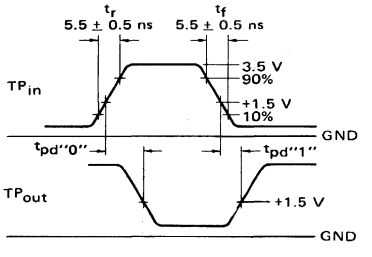
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

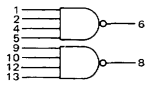
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES															
	mA					Volts										
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5	
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-	

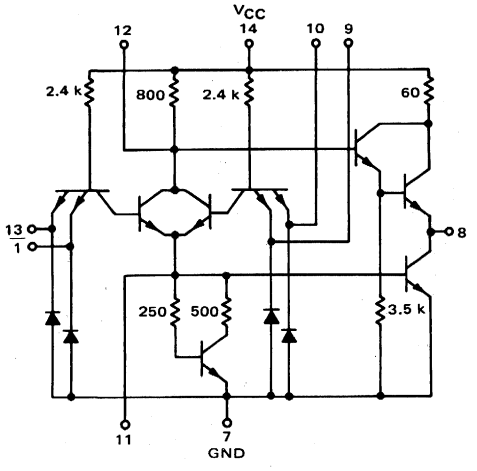
Characteristic	Symbol	Pin Under Test	MC3010 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																									
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7
Output																									
Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V_{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 6, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	9.0	-	9.0	-	9.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0}$	1, 6	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	$t_{pd"1"}$	1, 6	-	-	-	10	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

EXPANDABLE DUAL 2-WIDE 2-INPUT "AND-OR-INVERT" GATE

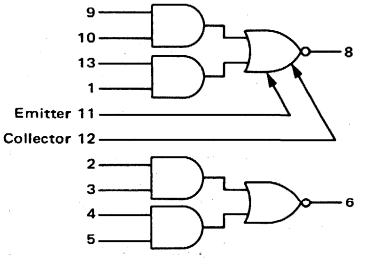
MC3020

1/2 OF CIRCUIT SHOWN †



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$8 = \overline{(9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$

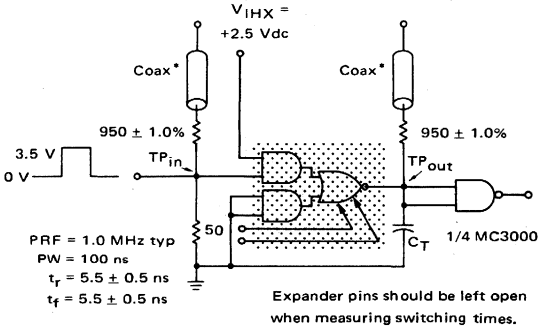
Negative Logic:

$8 = \overline{(9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})}$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 62.5 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

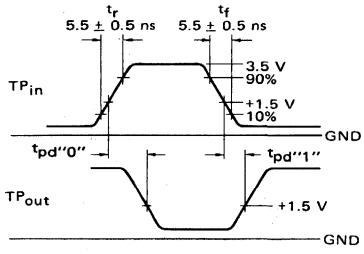


Expander pins should be left open when measuring switching times.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

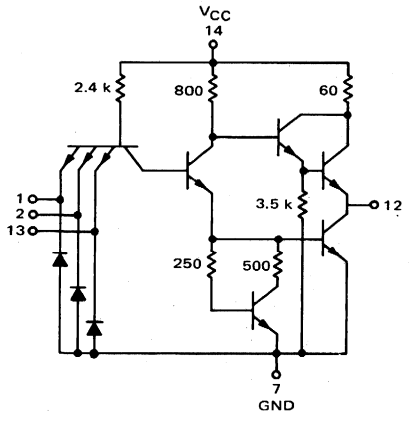
@Test Temperature	TEST CURRENT/VOLTAGE VALUES																
	mA							Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	I_E	I_{EXE}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	19	23	-2.0	-	-	0.3	0.50	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	0.3	0.55	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	19	23	-2.0	-	-	0.3	0.70	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

Characteristic	Symbol	Pin Under Test	MC3020 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	I_E	I_{EXE}	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																											
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	-	-	1	-	13	-	-	14	-	-	7, 9, 10*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	-	-	1	-	13	-	-	-	14	-	7, 9, 10*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	7, 9, 10, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	14	-	7, 9, 10, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	-	7, 9, 10*
Output																											
Output Voltage	V_{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	-	-	1	-	-	13	-	-	14	-	-	7, 9, 10*
	V_{OL1}	8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1,7,9,10,13
	V_{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	11, 12	-	-	-	-	-	-	-	-	14	-	1,7,9,10,13*
	V_{OL2}	8	-	0.4	-	0.4	-	0.4	Vdc	-	8	-	-	-	-	-	-	1	-	-	13	-	-	-	14	-	7, 9, 10*
	V_{OH}	8	2.5	-	2.5	-	2.5	-	Vdc	-	-	8	-	-	-	-	1	-	-	-	13	-	-	14	-	-	1, 7, 10*
Short-Circuit Current	I_{SC}	8	-	-	-30	-100	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 7, 8, 9, 10, 13*
Base-Emitter Voltage	$V_{BE\ max}$	11	-	1.010	-	0.975	-	0.935	Vdc	8	-	-	-	-	-	11, 12	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 13*
	$V_{BE\ min}$	11	0.70	-	0.65	-	0.55	-	Vdc	-	-	-	-	-	11	-	-	-	-	-	-	-	-	14	-	-	1, 9, 10, 12, 13*
Power Requirements (Total Device)																											
Maximum Power Supply Current	I_{max}	14	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9,10, 13
Power Supply Drain	I_{PDH}	14	-	22	-	22	-	22	mAdc	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 13	-	14	-	-	-	7
	I_{PDL}	14	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5,7, 9,10,13
Switching Parameters										Pulse In	Pulse Out																
Turn-On Delay	$t_{pd"0"}$	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*
Turn-Off Delay	$t_{pd"1"}$	1, 8	-	-	-	12	-	-	ns	1	8	-	-	-	-	-	-	-	-	-	-	-	14	-	-	13	7, 9, 10*

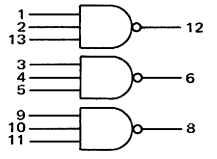
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3005

1/3 OF CIRCUIT SHOWN



This package consists of three 3-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $12 = \overline{1 \cdot 2 \cdot 13}$

Negative Logic: $12 = \overline{1 + 2 + 13}$

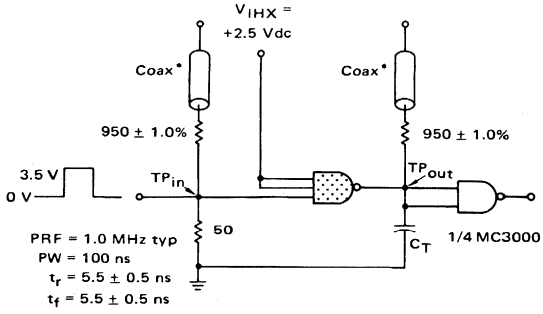
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 66 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

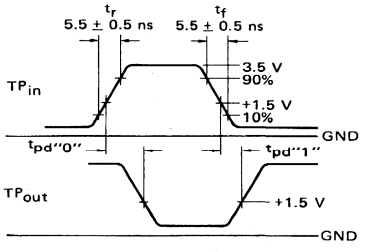
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

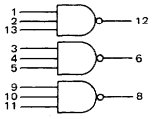
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

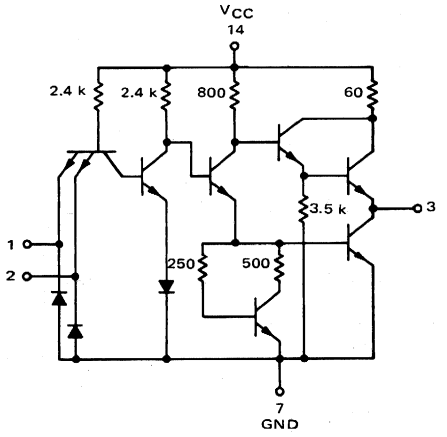
Characteristic	Symbol	Pin Under Test	MC3005 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2, 13	-	-	14	-	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2, 13	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output Output Voltage	V_{OL1}	12	-	0.4	-	0.4	-	0.4	Vdc	12	-	-	-	-	-	1	-	-	2, 13	-	-	14	-	-	7*
	V_{OL2}	12	-	0.4	-	0.4	-	0.4	Vdc	-	12	-	-	-	-	1	-	-	2, 13	-	-	-	14	-	7*
	V_{OH}	12	2.5	-	2.5	-	2.5	-	Vdc	-	-	12	-	-	1	-	-	-	2, 13	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	12	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 7,* 12, 13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7, 9, 10, 11, 13
Power Supply Drain	I_{PDH}	14	-	27	-	27	-	27	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 3, 4, 5, 9, 10, 11, 13	-	14	-	-	-	7
	I_{PDL}	14	-	12.5	-	12.5	-	12.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5,7, 9,10,11,13
Switching Parameters Turn-On Delay	$t_{pd"0"}$	1, 12	-	-	-	10	-	-	ns	Pulse In 1	Pulse Out 12	-	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*
Turn-Off Delay	$t_{pd"1"}$	1, 12	-	-	-	10	-	-	ns	1	12	-	-	-	-	-	-	-	-	-	14	-	-	2, 13	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

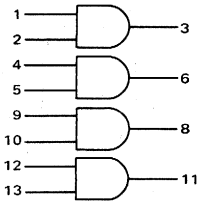
QUAD 2-INPUT "AND" GATE

MC3001

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

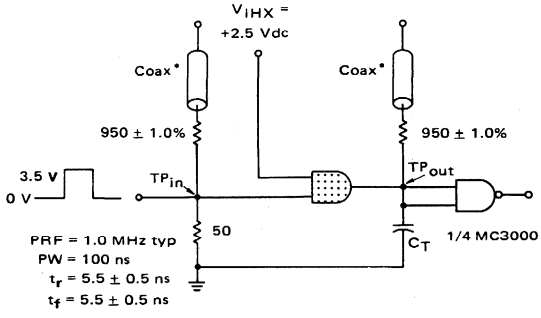


Positive Logic: 3 = 1 · 2
Negative Logic: 3 = 1 + 2

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 112 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

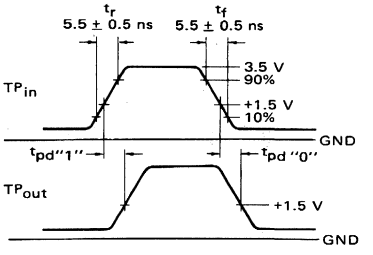
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

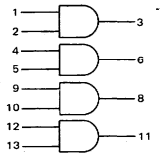
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



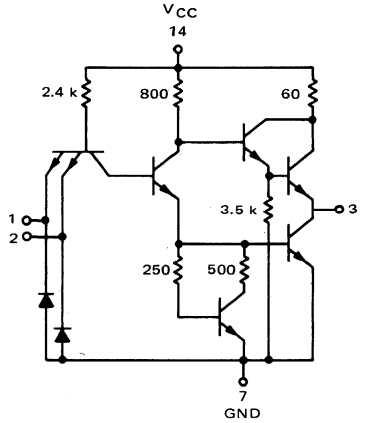
@Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

Characteristic	Symbol	Pin Under Test	MC3001 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																									
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2*	-	-	14	-	-	7
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2*	-	-	-	14	-	7
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output																									
Output Voltage	V_{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	-	2*	-	-	14	-	-	7
	V_{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	1	-	-	-	2*	-	-	-	14	-	7
	V_{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	-	1	-	-	2*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2*	-	14	-	-	-	3,7
Power Requirements (Total Device)																									
Maximum Power Supply Current	I_{max}	14	-	-	-	34	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	14	-	-	-	7
	I_{PDL}	14	-	48	-	48	-	48	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,7, 9,10,12,13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0"}$	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7
Turn-Off Delay	$t_{pd"1"}$	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7

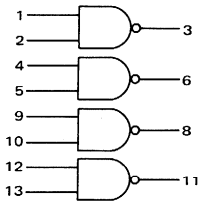
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

MC3000

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NAND gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$

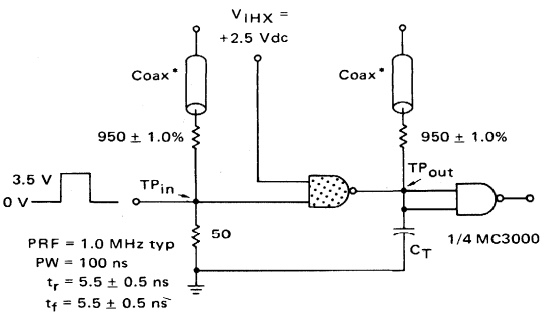
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 88 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

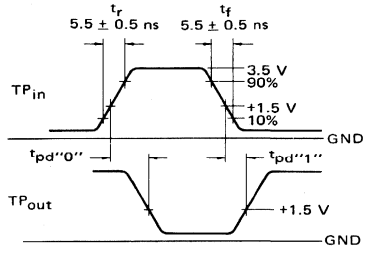
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

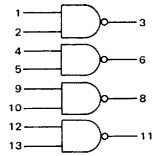
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



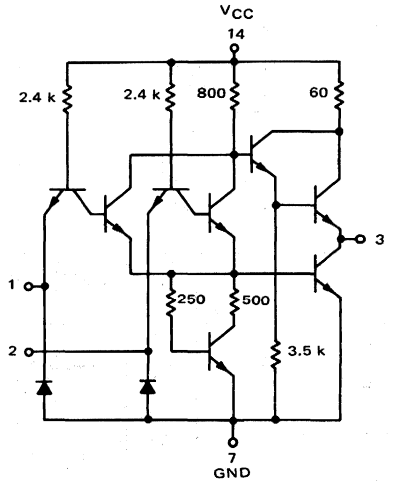
@Test Temperature	TEST CURRENT / VOLTAGE VALUES															
	mA					Volts										
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5	
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-	

Characteristic	Symbol	Pin Under Test	MC3000 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																									
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2	-	-	14	-	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2,7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	2,7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output																									
Output Voltage	V_{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	2	-	-	14	-	-	7*
	V_{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	2	-	-	-	14	-	7*
	V_{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	2	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	36	-	36	-	36	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	17.5	-	17.5	-	17.5	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0"}$	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2	7*
Turn-Off Delay	$t_{pd"1"}$	1,3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2	7*

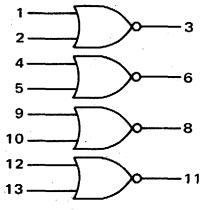
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3002

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input NOR gates. Each gate may be used as an inverter, or two gates may be cross-coupled to form bistable circuits.



Positive Logic: $3 = \overline{1 + 2}$

Negative Logic: $3 = \overline{1 \bullet 2}$

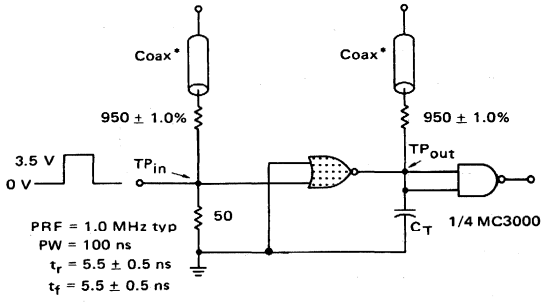
Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 122 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

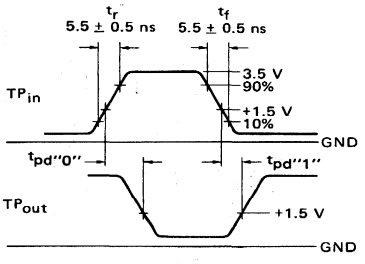
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

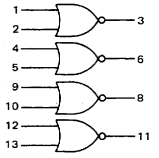
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



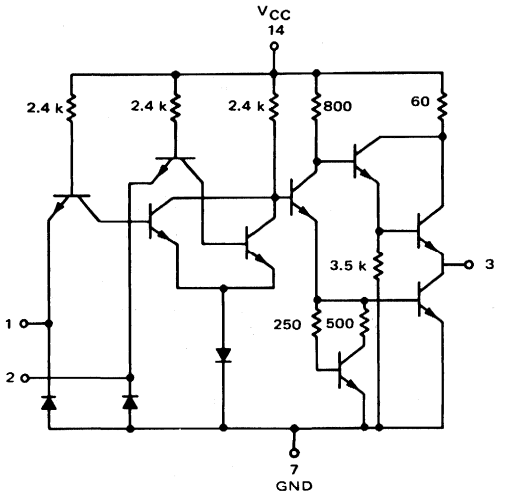
@Test Temperature	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
	mA					Volts								
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3002 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																								
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2	-	-	14	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2	-	-	-	14	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	2, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	7*
Output																								
Output Voltage	V_{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	-	1	-	-	-	-	-	14	-	2, 7*
	V_{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	-	1	-	-	-	-	-	-	14	2, 7*
	V_{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	1	-	-	-	-	-	-	14	-	2, 7*
Short-Circuit Current	I_{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 3, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	38	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Power Supply Drain	I_{PDH}	14	-	43	-	43	-	43	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	7
	I_{PDL}	14	-	27	-	27	-	27	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters										Pulse In	Pulse Out													
Turn-On Delay	$t_{pd"0"}$	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2, 7*
Turn-Off Delay	$t_{pd"1"}$	1, 3	-	-	-	10	-	-	ns	1	3	-	-	-	-	-	-	-	-	-	14	-	-	2, 7*

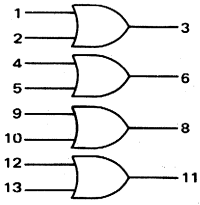
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

MC3003

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

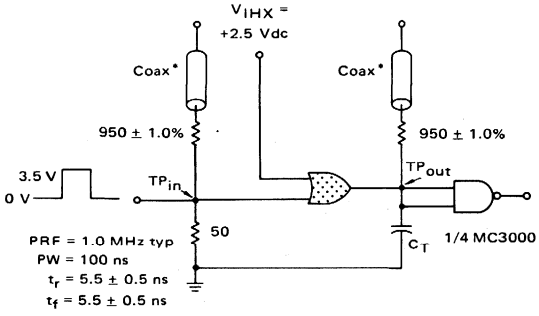


Positive Logic: 3 = 1 + 2
Negative Logic: 3 = 1 · 2

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

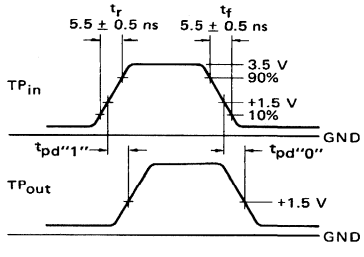
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

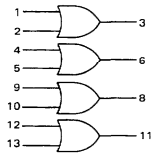
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



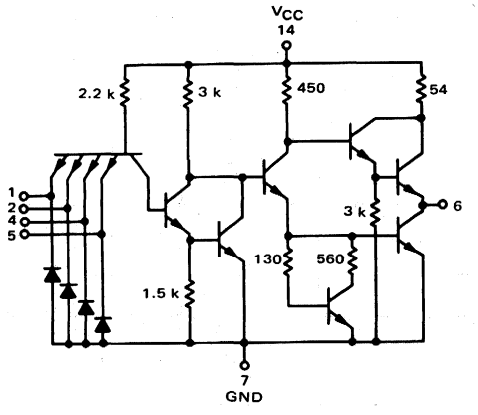
@Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	19	23	-2.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	19	23	-2.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	19	23	-2.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

Characteristic	Symbol	Pin Under Test	MC3003 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																									
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	1	-	2*	-	-	14	-	-	7
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	1	-	2*	-	-	-	14	-	7
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output																									
Output Voltage	V_{OL1}	3	-	0.4	-	0.4	-	0.4	Vdc	3	-	-	-	-	1	-	-	-	2*	-	-	14	-	-	7
	V_{OL2}	3	-	0.4	-	0.4	-	0.4	Vdc	-	3	-	-	-	1	-	-	-	2*	-	-	-	14	-	7
	V_{OH}	3	2.5	-	2.5	-	2.5	-	Vdc	-	-	3	-	-	-	1	-	-	2*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	3	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	1, 2*	-	14	-	-	-	3,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	45	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1,2,4,5,9, 10,12,13	-	14	-	-	-	7
	I_{PDL}	14	-	55	-	55	-	55	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,7, 9,10,12,13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0"}$	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7
Turn-Off Delay	$t_{pd"1"}$	1, 3	-	-	-	12	-	-	ns	1	3	-	-	-	-	-	-	-	*	-	14	-	-	2	7

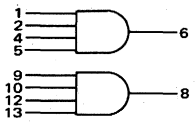
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}

MC3026

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).

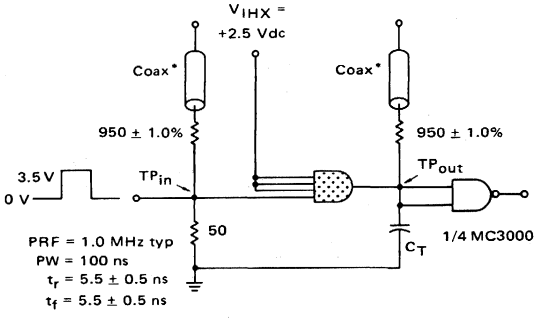


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

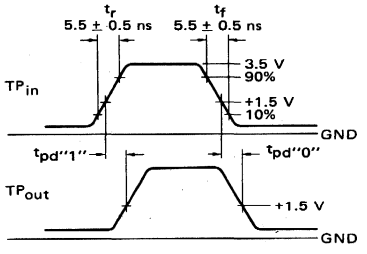
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

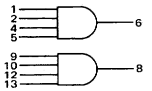
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

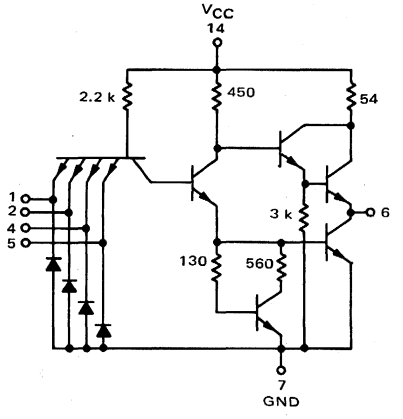


Characteristic	Symbol	Pin Under Test	MC3026 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	@Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
										0°C	38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
										+25°C	38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5	
										+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
											TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:															
Input																										
Forward Current	I_{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAdc		-	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	14	-	-	7
	I_{F2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc		-	-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc		-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc		-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc		-	-	-	-	I	-	-	-	-	*	-	-	14	-	-	7
Output																										
Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc		6	-	-	-	-	1	-	-	-	2, 4, 5 *	-	-	14	-	-	7
	V_{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc		-	6	-	-	-	1	-	-	-	2, 4, 5 *	-	-	-	14	-	7
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc		-	-	6	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-	-50	-125	-	-	mAdc		-	-	-	-	-	-	-	-	-	1, 2, 4, 5 *	-	14	-	-	-	6, 7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	22	-	-	mAdc		-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	14	-	14	-	14	mAdc		-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	38	-	38	-	38	mAdc		-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Switching Parameters											Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0"}$	1, 6	-	-	-	15	-	-	ns		1	6	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7
Turn-Off Delay	$t_{pd"1"}$	1, 6	-	-	-	15	-	-	ns		1	6	-	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

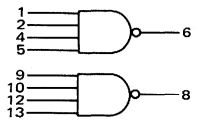
*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

MC3025

1/2 OF CIRCUIT SHOWN



This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).



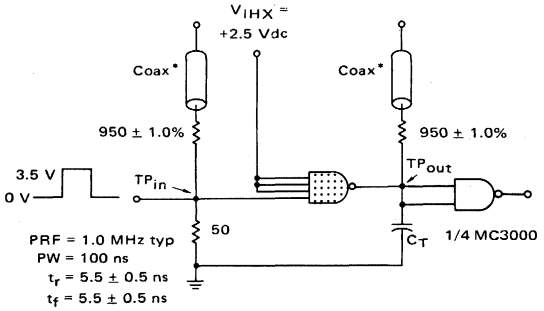
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1.1
Output Loading Factor = 20

Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

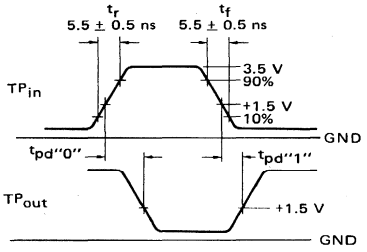
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

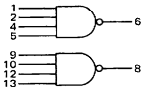
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



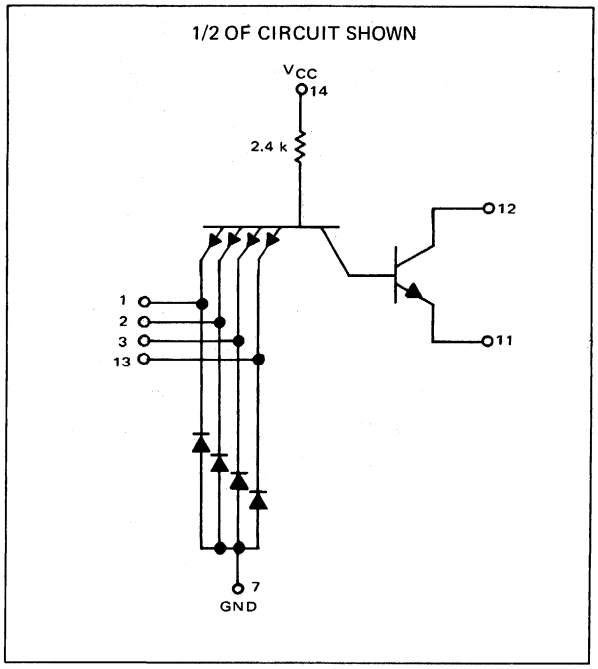
@Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
0°C	38	46	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-
+25°C	38	46	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5
+75°C	38	46	-4.0	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-

Characteristic	Symbol	Pin Under Test	MC3025 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																									
Forward Current	I_{F1}	1	-	-2.1	-	-2.1	-	-2.1	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	14	-	-	7*
	I_{F2}	1	-	-2.6	-	-2.6	-	-2.6	mAdc	-	-	-	-	-	-	-	1	-	2, 4, 5	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 4, 5, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 4, 5, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output																									
Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	-	1	-	-	2, 4, 5	-	-	14	-	-	7*
	V_{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	6	-	-	-	-	1	-	-	2, 4, 5	-	-	-	14	-	7*
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	6	-	-	1	-	-	-	2, 4, 5	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-	-50	-125	-	-	mA	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,4,5,6,7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 4, 5, 7 9,10, 12, 13
Power Supply Drain	I_{PDH}	14	-	32	-	32	-	32	mAdc	-	-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	10	-	10	-	10	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7 9,10, 12, 13
Switching Parameters										Pulse In	Pulse Out														
Turn-On Delay	$t_{pd"0"}$	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*
Turn-Off Delay	$t_{pd"1"}$	1,6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	14	-	-	2, 4, 5	7*

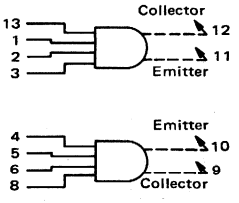
*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

DUAL 4-INPUT EXPANDER FOR "AND-OR-INVERT" GATES

MC3030



This device consists of two independent 4-input AND gates. The outputs of each gate are available as ORing nodes. Using the MC3030 expander, with the MC3020 expandable gate, up to four AND gates can be ORed together.



Input Loading Factor = 1
Full output loading factor of the expandable gate is maintained.

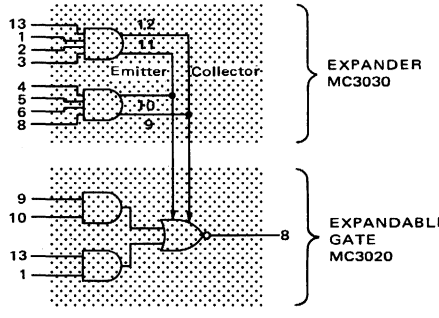
Total Power Dissipation = 15 mW typ/pkg

Propagation Delay Time:

Δt_{pd} = +1.0 ns typ
When added to the expandable "AND-OR-INVERT" gate.

$\Delta t_{pd}/pF$ = +1.0 ns pF typ
Caused by additional capacitance at expansion points.

APPLICATION: EXPANDABLE 2-WIDE 2-INPUT AND-OR-INVERT GATE WITH A DUAL 4-INPUT EXPANDER CONNECTED



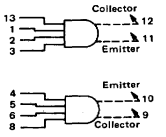
Positive Logic:

$$8 = \overline{(9 \bullet 10) + (13 \bullet 1)} + \overline{(13 \bullet 1 \bullet 2 \bullet 3) + (4 \bullet 5 \bullet 6 \bullet 8)}$$

Expandable Gate — Expander

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in a similar manner. Further, test procedures are shown for only one input of the expander being tested. To complete testing, sequence through remaining inputs.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA													
	I_C	I_{in}	I_D	V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	6.0	-	-	2.5	4.0	0.4	1.010	0.70	2.0	1.1	-	5.0	4.5	5.5
+25°C	6.0	1.0	-10	2.5	4.0	0.4	0.975	0.65	1.8	1.1	7.0	5.0	4.5	5.5
+75°C	6.0	-	-	2.5	4.0	0.4	0.935	0.55	1.8	0.9	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3030 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_C	I_{in}	I_D	V_R	V_{RH}	V_F	V_{EE1}	V_{EE2}	V_{IH}	V_{IL}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																								
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	2, 3, 13	1	-		-	-	-	-	14	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	2, 3, 13	1	-	-	-	-	-	-	-	14	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	1	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	1	-	-	-	-	-	-	-	-	-	-	-	14	2, 3, 7, 13*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	-	-	-	-	-	-	14	-	7*
Output																								
Output Voltage	V_{OL}	12	-	1.41	-	1.38	-	1.34	Vdc	12	-	-	-	-	-	11	-	1	-	-	-	14	-	7*
Emitter Current	I_{EO}	11	-	-300	-	-300	-	-300	μAdc	-	-	-	-	-	-	-	11	-	1	-	-	12, 14	-	7**
Collector Current	I_{CO}	12	-	300	-	300	-	300	μAdc	-	-	-	-	-	-	-	11	1	-	-	-	12, 14	-	7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	7.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,3,4,5, 6,7,8,13
Power Supply Drain	I_{PDL}	14	-	5.0	-	5.0	-	5.0	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,5, 6,7,8,13

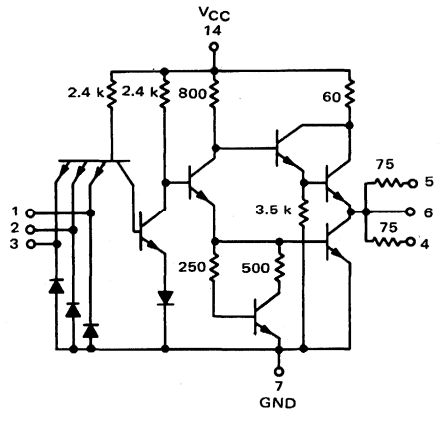
* Ground inputs to gates not under test unless otherwise noted.

** The inputs to both gates are ungrounded.

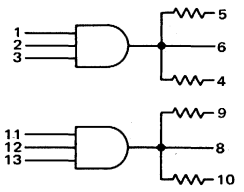
DUAL 3-INPUT 3-OUTPUT "AND" SERIES TERMINATED LINE DRIVER

MC3028

1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated AND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6, = 1 · 2 · 3

Negative Logic: 4, 5, 6, = 1 + 2 + 3

Input Loading Factor = 1

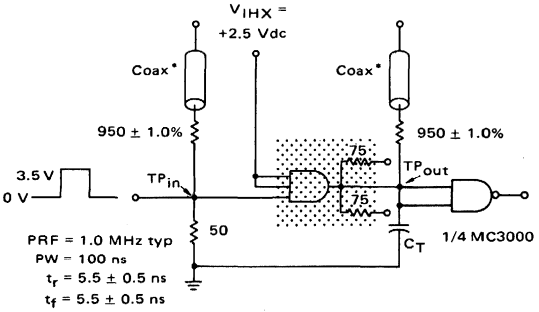
Output Loading Factor, Direct Output (Pins 6 & 8) = 10 minus the number of resistor-terminated outputs being used.

Output Loading Factor, Resistors (Pins 4, 5, 9, & 10) = 1

Total Power Dissipation = 56 mW typ/pkg

Propagation Delay Time = 9.0 ns typ

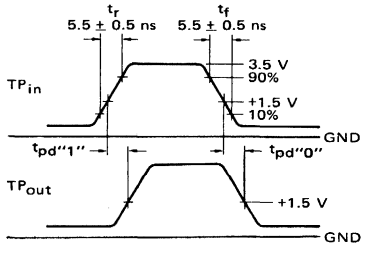
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

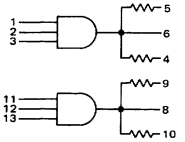
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procedures are shown for only one input of the line driver being tested. To complete testing, sequence through remaining inputs.



@Test Temperature	TEST CURRENT/VOLTAGE VALUES																							
	mA											Volts												
	$I_{OL\,1A}$	$I_{OL\,1B}$	$I_{OL\,1C}$	$I_{OL\,2A}$	$I_{OL\,2B}$	$I_{OL\,2C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}			
0°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-			
+25°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5			
+75°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-			

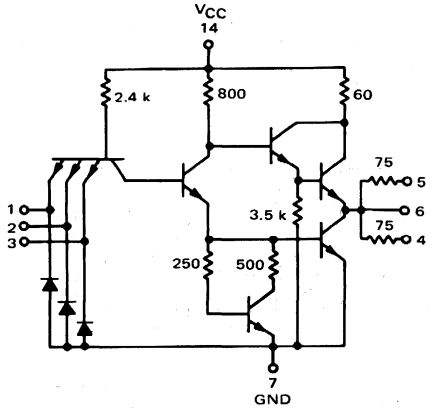
Characteristic	Symbol	Pin Under Test	MC3028 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL\,1A}$	$I_{OL\,1B}$	$I_{OL\,1C}$	$I_{OL\,2A}$	$I_{OL\,2B}$	$I_{OL\,2C}$	$I_{OH\,A}$	$I_{OH\,B}$	$I_{OH\,C}$	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3*	-	-	14	-	-	7
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3*	-	-	-	14	-	7
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	*	-	-	-	14	-	2,3,7
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	*	-	-	-	14	-	2,3,7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
Output Output Voltage	$V_{OL\,1}$	6	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2,3*	-	-	14	-	-	7
	$V_{OL\,2}$	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	-	6	5	4	-	-	-	-	-	1	-	-	-	2,3*	-	-	-	14	-	7
	$V_{OL\,3}$	5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	-	-	1	-	-	-	2,3*	-	-	14	-	-	7
	$V_{OL\,4}$	5	-	0.5	-	0.5	-	0.5	Vdc	-	-	-	6	5	4	-	-	-	-	-	1	-	-	-	2,3*	-	-	-	14	-	7
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	5	4	-	-	-	1	-	-	2,3*	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1,2,3*	-	14	-	-	-	6,7
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	14	-	-	-	-	7
Power Supply Drain	I_{PDH}	14	-	12	-	12	-	12	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	24	-	24	-	24	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7 11, 12, 13
Switching Parameters										Pulse In	Pulse Out																				
Turn-On Delay	$t_{pd"0"}$	1, 6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2,3	7
Turn-Off Delay	$t_{pd"1"}$	1, 6	-	-	-	12	-	-	ns	1	6	-	-	-	-	-	-	-	-	-	-	-	-	-	*	-	14	-	-	2,3	7

*Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

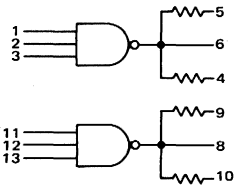
DUAL 3-INPUT 3-OUTPUT "NAND" SERIES TERMINATED LINE DRIVER

MC3029

1/2 OF CIRCUIT SHOWN



This device is a dual 3-input/3-output series-terminated NAND line driver that minimizes switching transients on long lines by approximating line impedance. Two outputs are provided through 75-ohm resistors for use when driving 93 to 120-ohm lines. These outputs should be paralleled when driving 50 to 93-ohm lines. In addition, an output is provided directly at the gate output node for driving adjacent gates.



Positive Logic: 4, 5, 6 = $\overline{1 \cdot 2 \cdot 3}$

Negative Logic: 4, 5, 6 = $\overline{1 + 2 + 3}$

Input Loading Factor = 1

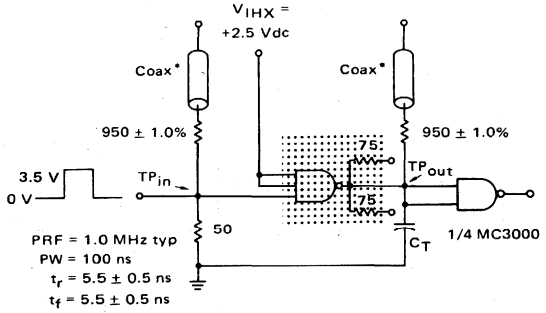
Output Loading Factor, Direct Output (Pins 6 and 8) = 10 Minus The Number of Resistor-Terminated Outputs Being Used.

Output Loading Factor, Resistors (Pins 4, 5, 9 and 10) = 1

Total Power Dissipation = 44 mW typ/pkg

Propagation Delay Time = 6.0 ns typ

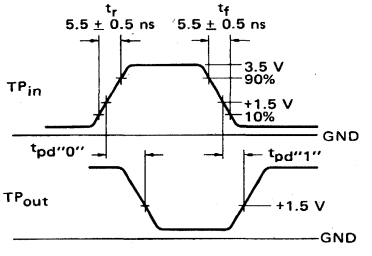
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

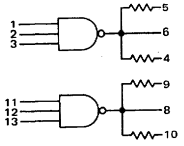
C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line driver. The other line driver is tested in the same manner. Further, test procecures are shown for only one input of the line driver under test. To complete testing sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3029 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES @Test Temperature	mA I_{OL1A}	I_{OL1B}	I_{OL1C}	I_{OL2A}	I_{OL2B}	I_{OL2C}	I_{OHA}	I_{OHB}	I_{OHC}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
										0°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
										+25°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	2.5	
										+75°C	15.2	1.9	1.9	18.4	2.3	2.3	-1.8	-0.1	-0.1	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	-	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:	I_{OL1A}	I_{OL1B}	I_{OL1C}	I_{OL2A}	I_{OL2B}	I_{OL2C}	I_{OHA}	I_{OHB}	I_{OHC}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																															
Forward Current	I_{F1}	1	-	-1.9	-	-1.9	-	-1.9	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	14	-	-	7*
	I_{F2}	1	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*
Leakage Current	I_R	1	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	14	-	2, 3, 7*
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	Vdc	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	14	-	2, 3, 7*
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	14	-	-	7*
Output																															
Output Voltage	V_{OL1}	6	-	0.4	-	0.4	-	0.4	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	14	-	-	7*
	V_{OL2}	6	-	0.4	-	0.4	-	0.4	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*
	V_{OL3}	5	-	0.5	-	0.5	-	0.5	Vdc	6	5	4	-	-	-	-	-	-	-	-	-	-	1	-	2,3	-	-	14	-	-	7*
	V_{OL4}	5	-	0.5	-	0.5	-	0.5	Vdc	-	-	-	6	4	5	-	-	-	-	-	-	-	1	-	2,3	-	-	-	14	-	7*
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	-	-	-	-	-	6	4	5	-	-	1	-	-	-	2,3	-	-	14	-	-	7*
Short-Circuit Current	I_{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 6, 7*
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	12	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1, 2, 3, 7, 11, 12, 13
Power Supply Drain	I_{PDH}	14	-	18	-	18	-	18	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1, 2, 3, 11, 12, 13	-	14	-	-	-	7
	I_{PDL}	14	-	9	-	9	-	9	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 3, 7, 11, 12, 13
Switching Parameters										Pulse In / Pulse Out																					
Turn-On Delay	$t_{pd"0"}$	1, 6	-	-	-	10	-	-	ns	1 / 6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*
Turn-Off Delay	$t_{pd"1"}$	1, 6	-	-	-	10	-	-	ns	1 / 6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14	-	-	2, 3	7*

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.

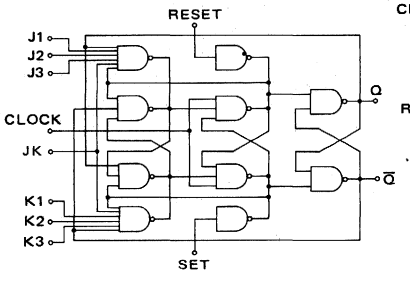
"AND" J-K FLIP-FLOP

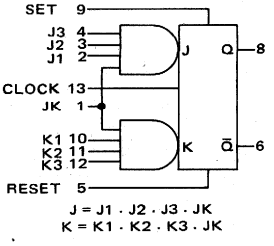
MC3050

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data, such as initial conditions into the flip-flop. The direct SET and RESET fully override the clock; i.e., the direct SET and RESET control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is high; data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the high state to the SET or RESET inputs.

LOGIC DIAGRAM





$J = J1 \cdot J2 \cdot J3 \cdot JK$

$K = K1 \cdot K2 \cdot K3 \cdot JK$

TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
J, K, SET, RESET = 0.6
CLOCK, JK = 1.2

Output Loading Factor = 10

Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C)

Total Power Dissipation = 80 mW/pkg

Toggle Frequency = 40 MHz

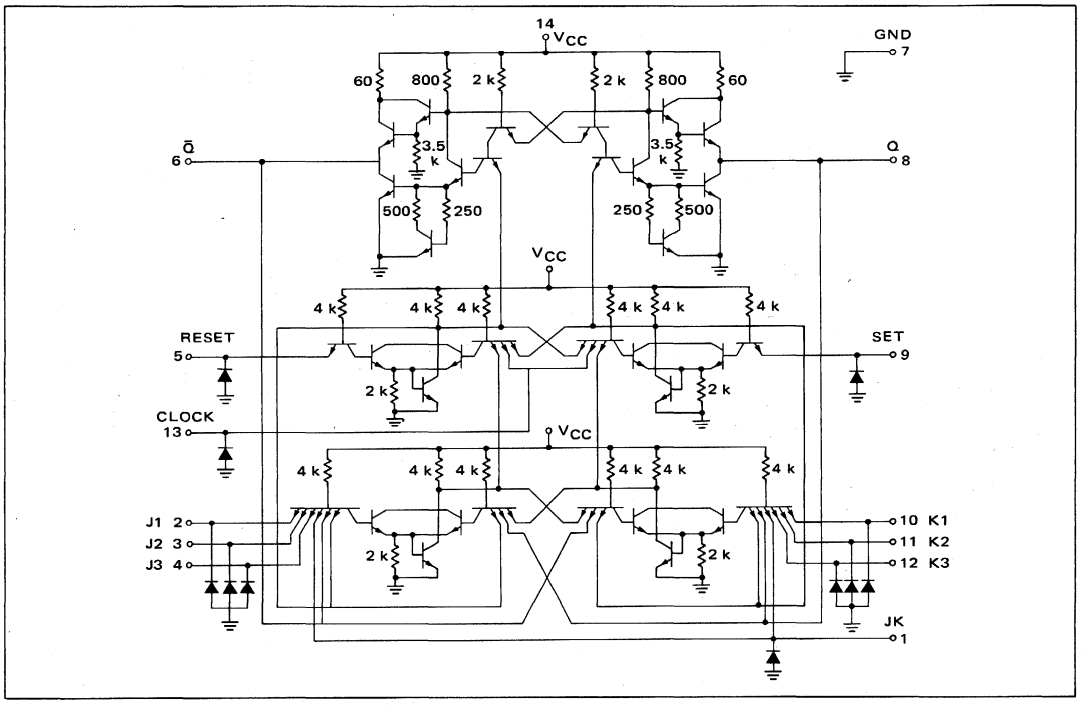
Logical "1" Setup Time = 10 ns

Logical "0" Setup Time = 5.0 ns

Logical "1" and "0" Hold Time = 5.0 ns

t_{pd} "0" = 12 ns

t_{pd} "1" = 14 ns



OPERATING CHARACTERISTICS

High state data must be present 17 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

Positive edge triggering: When the clock goes from the low state to the high state, the information in the input steering section is transferred to the bistable section.

The direct SET and RESET inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED TO GROUND.

Unused Inputs:

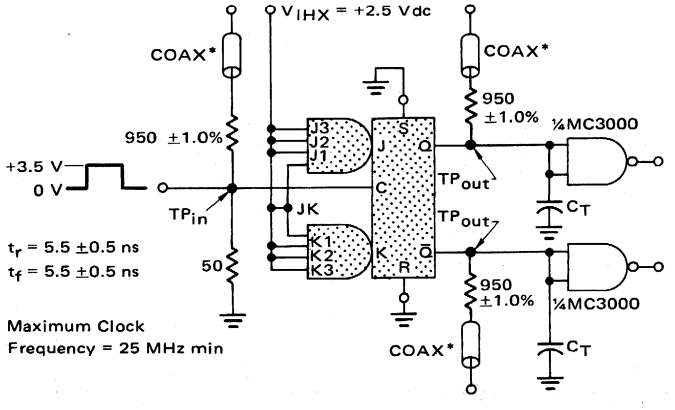
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, $\overline{Q}$, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused SET and RESET inputs MUST be tied to ground.

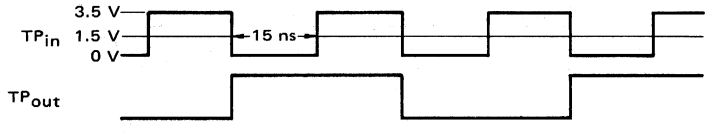
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



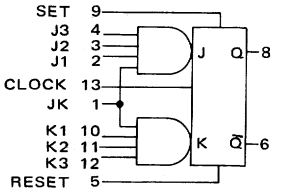
*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3050 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																								
Forward Current	I_{FJ}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,3,4,5	-	-	-	14	7,9,13
		3	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	3	-	1,2,4,5	-	-	-	↓	↓
		4	-		-		-			-	-	-	-	-	-	-	4	-	1,2,3,5	-	-	-		
	I_{FK}	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	10	-	1,9,11,12	-	-	-	14	5,7,13
		11	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	11	-	1,9,10,12	-	-	-	↓	↓
		12	-		-		-			-	-	-	-	-	-	-	12	-	1,9,10,11	-	-	-		
	I_{FC}	13	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	13	-	-	-	-	-	14	1,5,7,9
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	2,3,4,10,11,12	-	-	-	14	5,7,9,13
	I_{FS}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	9	-	5	-	-	-	14	7
	I_{FR}	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	5	-	9	-	-	-	14	7
Leakage Current	I_{RJ}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	2	9	-	-	-	14	1,3,4,5,7
		3	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	-	3	↓	-	-	-	↓	1,2,4,5,7
		4	-		-		-			-	-	-	-	-	-	-	-	4		-	-	-		1,2,3,5,7
	I_{RK}	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	10	5	-	-	-	14	1,7,9,11,12
		11	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	-	-	11	↓	-	-	-	↓	1,7,9,10,12
		12	-		-		-			-	-	-	-	-	-	-	-	12		-	-	-		1,7,9,10,11
	I_{RC}	13	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	13	1,2,3,4,5,10,11,12	-	-	-	14	7,9
	I_{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	1	9	-	-	-	14	2,3,4,5,7,10,11,12
	I_{RS}	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	9	-	-	-	-	14	7
	I_{RR}	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	7

ELECTRICAL CHARACTERISTICS (continued)

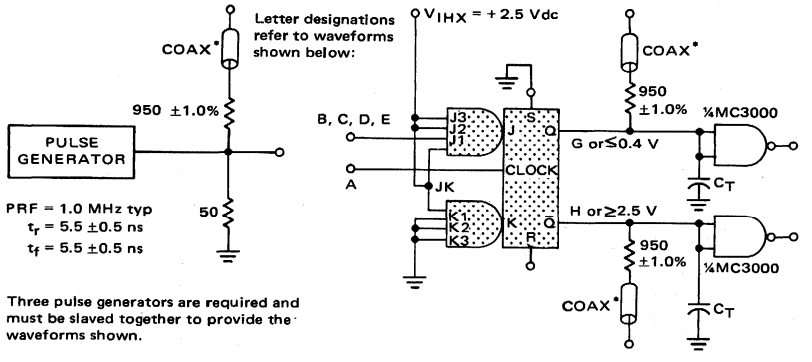
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3050 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	9	-	-	-	14	1,3,4,5,7
		3	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	-	↓	-	-	-	↓	1,2,4,5,7
		4	-	-		-	-	-		-	-	4	-	-	-	-	-	-		-	-	-		1,2,3,5,7
		10	-	-		-	-	-		-	-	10	-	-	-	-	-	-	5	-	-	-		1,7,9,11,12
		11	-	-		-	-	-		-	-	11	-	-	-	-	-	-	↓	-	-	-		1,7,9,10,12
		12	-	-		-	-	-		-	-	12	-	-	-	-	-	-		-	-	-		1,7,9,10,11
		13	-	-		-	-	-		-	-	-	13	-	-	-	-	-	1,2,3,4,5,10,11,12	-	-	-		7,9
		1	-	-		-	-	-		-	-	-	1	-	-	-	-	-	9	-	-	-		2,3,4,5,7,10,11,12
		9	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-	-	-		7
		5	-	-	↓	-	-	-	↓	-	-	5	-	-	-	-	-	-	-	-	-	-	↓	7
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	Vdc	-	-	-	-	2	-	-	-	-	-	-	-	14	-	7
		3	-	-	-	↓	-	-	↓	-	-	-	-	3	-	-	-	-	-	-	-	↓	-	↓
		4	-	-	-		-	-		-	-	-	-	4	-	-	-	-	-	-	-		-	
		10	-	-	-		-	-		-	-	-	-	10	-	-	-	-	-	-	-		-	
		11	-	-	-		-	-		-	-	-	-	11	-	-	-	-	-	-	-		-	
		12	-	-	-		-	-		-	-	-	-	12	-	-	-	-	-	-	-		-	
		13	-	-	-		-	-		-	-	-	-	13	-	-	-	-	-	-	-		-	
		1	-	-	-		-	-		-	-	-	-	1	-	-	-	-	-	-	-		-	
		9	-	-	-		-	-		-	-	-	-	9	-	-	-	-	-	-	-		-	
		5	-	-	-	↓	-	-	↓	-	-	-	-	5	-	-	-	-	-	-	-	↓	-	↓
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	5	9	-	-	-	-	-	-	14	7,13
		8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	9	5	-	-	-	-	-	-	14	7,13
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	9	5	-	-	-	-	-	14	-	7,13
		8	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	5	9	-	-	-	-	-	14	-	7,13
Short-Circuit Current	I_{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	5	-	14	-	-	6,7,9
		8	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	9	-	14	-	-	5,7,8
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	35	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,5,7,13
Power Supply Drain	I_{PD}	14	-	26	-	26	-	26	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	1,5,7,13

OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

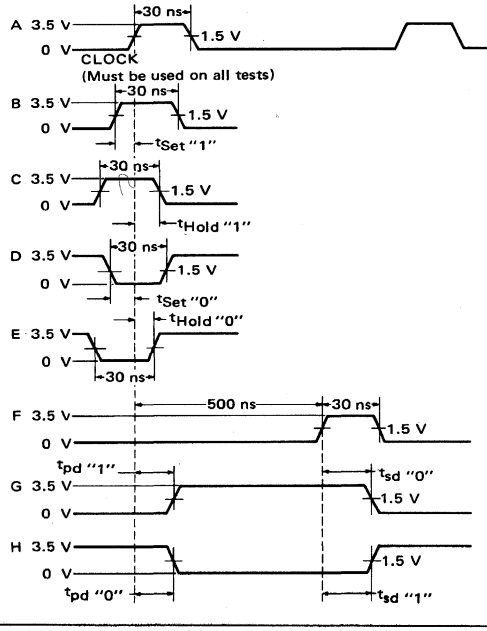
(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J**	INPUT SET**	INPUT RESET**	INPUT K**	Q**	$\overline{Q}$**	LIMITS (ns) Min	LIMITS (ns) Max
t_{Set} "1" J	B	Gnd	F	Gnd	G	H	-	17
t_{Hold} "1" J	C	Gnd	F	Gnd	G	H	-	0†
t_{Set} "0" J	D	Gnd	F	Gnd	≤0.4 V	≥2.5 V	-	5.0
t_{Hold} "0" J	E	Gnd	F	Gnd	≤0.4 V	≥2.5 V	-	0†
t_{Set} "1" K	Gnd	F	Gnd	B	H	G	-	17
t_{Hold} "1" K	Gnd	F	Gnd	C	H	G	-	0†
t_{Set} "0" K	Gnd	F	Gnd	D	≥ 2.5 V	≤0.4 V	-	5.0
t_{Hold} "0" K	Gnd	F	Gnd	E	≥ 2.5 V	≤0.4 V	-	0†
t_{pd} "1"	Delay from clock to Q during t_{Set} "1" J test. Delay from clock to $\overline{Q}$ during t_{Set} "1" K test.						8.0	30
t_{pd} "0"	Delay from clock to $\overline{Q}$ during t_{Set} "1" J test. Delay from clock to Q during t_{Set} "1" K test.						8.0	30
t_{sd} "1"	Delay from SET to Q during t_{Set} "1" K test. Delay from RESET to $\overline{Q}$ during t_{Set} "1" J test.						7.0	23
t_{sd} "0"	Delay from SET to $\overline{Q}$ during t_{Set} "1" K test. Delay from RESET to Q during t_{Set} "1" J test.						7.0	23

**Letters shown in these columns refer to waveforms at the left.
†t_{Hold} is typically a negative number.

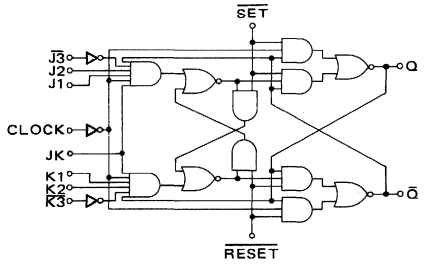
"AND" INPUT JJ̄-KK̄ FLIP-FLOP

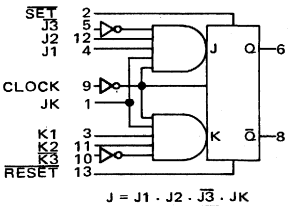
MC3052

The MC3052 is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a J̄-input ANDed together and two K-inputs and a K̄-input ANDed together. An enable input (JK) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, J̄, K and K̄) or an additional logic input (JK) for use in counters or certain other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to enable presetting data into the flip-flop such as initial conditions. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state, since the inputs are inhibited under this condition. Information may be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked inputs. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

LOGIC DIAGRAM





J = J1 · J2 · J3 · JK
K = K1 · K2 · K3 · JK

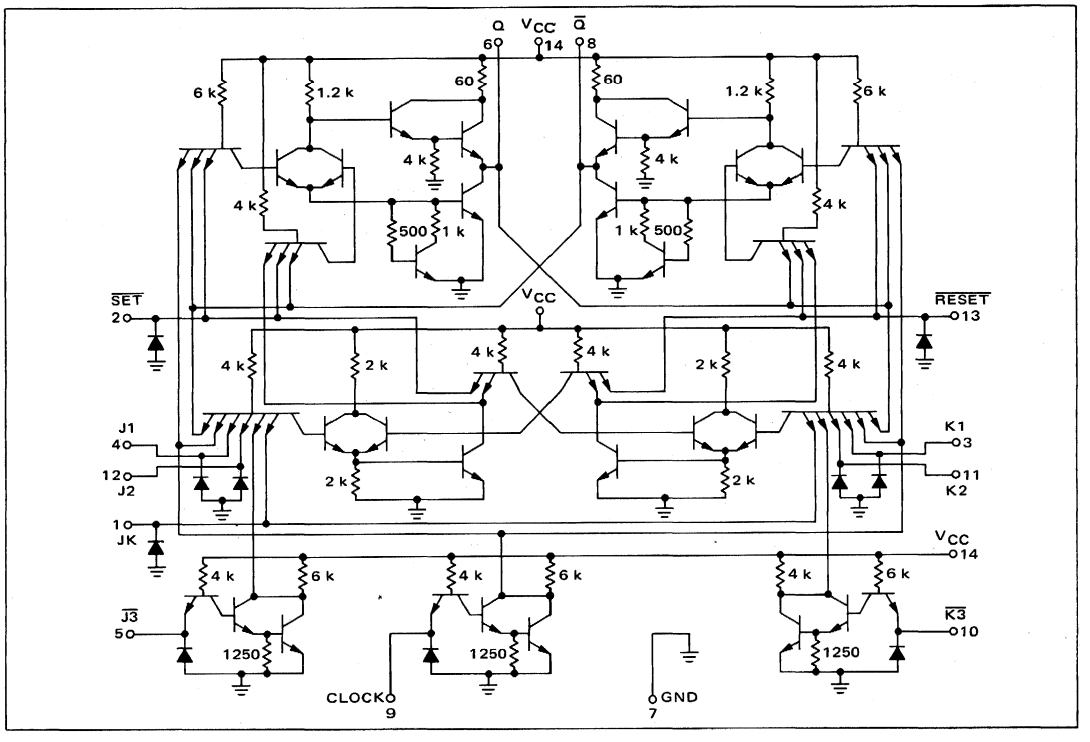
TRUTH TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

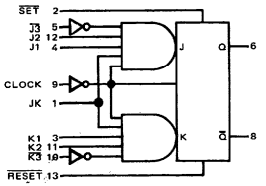
Input Loading Factors:
JK = 1.3
J, K, CLOCK = 0.6
$\overline{SET}$, $\overline{RESET}$ = 2.0

Output Loading Factor = 10

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)
Total Power Dissipation = 75 mW/pkg
Toggle Frequency = 40 MHz
Logical "1" Setup Time = 10 ns
Logical "0" Hold Time = 8.0 ns
t_{pd} "0" = 20 ns
t_{pd} "1" = 12 ns



ELECTRICAL CHARACTERISTICS



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	

Characteristic	Symbol	Pin Under Test	MC3052 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																									
Forward Current	I_{FJ}	4	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	4	-	1,12	-	-	-	14	-	5,7,9,13
		12	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	12	-	1,4	-	-	-	14	-	5,7,9,13
	I_{FK}	3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	3	-	1,11	-	-	-	14	-	2,7,9,10
		11	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	11	-	1,3	-	-	-	14	-	2,7,9,10
	$I_{F\bar{J}}$	5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	5	-	-	-	-	-	14	-	7
	$I_{F\bar{K}}$	10	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	10	-	-	-	-	-	14	-	7
	I_{FC}	9	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	9	-	-	-	-	-	14	-	7
	I_{FJK}	1	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	1	-	3,4,11,12	-	-	-	14	-	2,5,7,9,10,13
	$I_{F\bar{S}}$	2	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	2	-	-	-	-	-	14	-	7,9,13
	$I_{F\bar{R}}$	13	-	-4.5	-	-4.5	-	-4.5	mAdc	-	-	-	-	-	-	-	13	-	-	-	-	-	14	-	2,7,9
Leakage Current	I_{RJ}	4	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	4	5,9	-	-	-	14	-	1,2,7,12
		12	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	12	5,9	-	-	-	14	-	1,2,4,7
	I_{RK}	3	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	3	9,10	-	-	-	14	-	1,7,11,13
		11	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	11	9,10	-	-	-	14	-	1,3,7,13
	$I_{R\bar{J}}$	5	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	5	-	-	-	-	14	-	7
	$I_{R\bar{K}}$	10	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	10	-	-	-	-	14	-	7
	I_{RC}	9	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	9	-	-	-	-	14	-	7
	I_{RJK}	1	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	1	5,9,10	-	-	-	14	-	3,4,6,7,8,11,12
	$I_{R\bar{S}}$	2	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	2	1,4,10,12,13	-	-	-	14	9	3,5,7,11
	$I_{R\bar{R}}$	13	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	13	1,2,3,5,11	-	-	-	14	9	4,7,10,12

*Pulse is used to set flip-flop in desired state. P_1 = 4.0 V (V_{RH}), 0 V

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3052 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Breakdown Voltage	BV_{in}	4	-	-	5.5	-	-	-	Vdc	-	-	4	-	-	-	-	-	-	5,9	-	-	-	14	-	1,2,7,12
		12	-	-	↓	-	-	-	↓	-	-	12	-	-	-	-	-	-	5,9	-	-	-	↓	-	1,2,4,7
		3	-	-		-	-	-		-	-	3	-	-	-	-	-	-	9,10	-	-	-		-	1,7,11,13
		11	-	-		-	-	-		-	-	11	-	-	-	-	-	-	9,10	-	-	-		-	1,3,7,13
		1	-	-		-	-	-		-	-	-	1	-	-	-	-	-	2,5,9,10,13	-	-	-		-	3,4,6,7,8,11,12
		2	-	-		-	-	-		-	-	-	2	-	-	-	-	-	1,4,10,12,13	-	-	-		9	3,5,7,11
		13	-	-		-	-	-		-	-	-	13	-	-	-	-	-	1,2,3,5,11	-	-	-		9	4,7,10,12
		5	-	-		-	-	-		-	-	5	-	-	-	-	-	-	-	-	-	-		-	7
		9	-	-		-	-	-		-	-	9	-	-	-	-	-	-	-	-	-	-		-	7
		10	-	-	↓	-	-	-	↓	-	-	10	-	-	-	-	-	-	-	-	-	-	↓	-	7
Clamp Voltage	V_D	4	-	-	-	-1.5	-	-	Vdc	-	-	-	-	4	-	-	-	-	-	-	-	14	-	-	7
		12	-	-	-	↓	-	-	↓	-	-	-	-	12	-	-	-	-	-	-	-	↓	-	-	↓
		3	-	-	-		-	-		-	-	-	-	3	-	-	-	-	-	-	-		-	-	
		11	-	-	-		-	-		-	-	-	-	11	-	-	-	-	-	-	-		-	-	
		5	-	-	-		-	-		-	-	-	-	5	-	-	-	-	-	-	-		-	-	
		10	-	-	-		-	-		-	-	-	-	10	-	-	-	-	-	-	-		-	-	
		9	-	-	-		-	-		-	-	-	-	9	-	-	-	-	-	-	-		-	-	
		1	-	-	-		-	-		-	-	-	-	1	-	-	-	-	-	-	-		-	-	
		2	-	-	-		-	-		-	-	-	-	2	-	-	-	-	-	-	-		-	-	
		13	-	-	-	↓	-	-	↓	-	-	-	-	13	-	-	-	-	-	-	-	↓	-	-	↓
Output																									
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	13	2	-	-	-	-	-	-	14	-	7,9
		8	-	0.4	-	0.4	-	0.4	Vdc	8	-	-	-	-	2	13	-	-	-	-	-	-	14	-	7,9
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	2	13	-	-	-	-	-	14	-	-	7,9
		8	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	13	2	-	-	-	-	-	14	-	-	7,9
Short-Circuit Current	I_{SC}	6	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	2,6,7
		8	-	-	-30	-100	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	7,8,13
Power Requirements (Total Device)																									
Maximum Power Current	I_{max}	14	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	1,2,3,4,5,7,9,10,11,12,13
Power Supply Drain	I_{PD}	14	-	30	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,2,5,7,9,10

*Pulse is used to set flip-flop in desired state. P_1 = 4.0 V (V_{RH}), 0 V

OPERATING CHARACTERISTICS

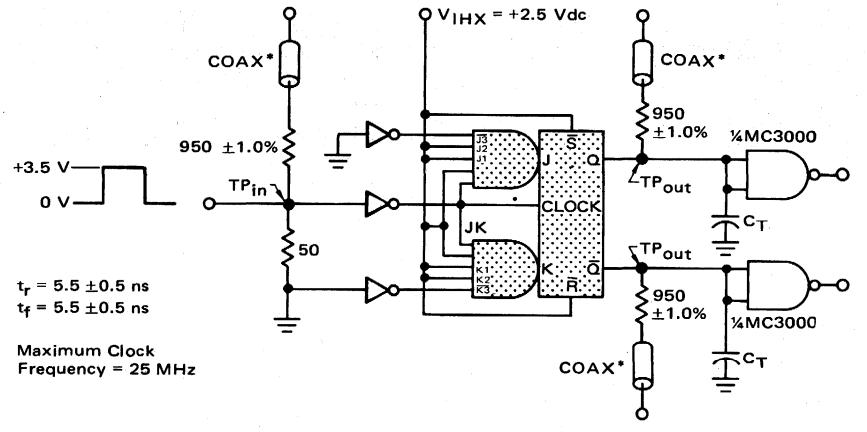
Data should be present prior to the negative clock transition. If data is changed from a "1" to a "0" while the clock is in the low state, the flip-flop will not recognize this new data state.

The application of a low level to the $\overline{SET}$ input sets Q high and low level on the $\overline{RESET}$ input resets Q low. These functions may be performed at any time without regard to the clock area.

Positive edge triggering – When the clock goes from the low to the high state, the information stored in the master flip-flop section is transferred to the slave flip-flop section thus appearing at the outputs. When the clock is in the high state, the inputs are inhibited.

Unused J, K, and JK inputs should be tied together with used inputs, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc. The unused $\overline{J}$ and $\overline{K}$ inputs must be tied to ground. The unused $\overline{SET}$ and $\overline{RESET}$ inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

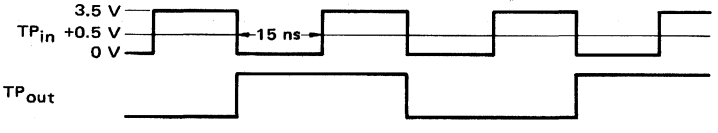
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

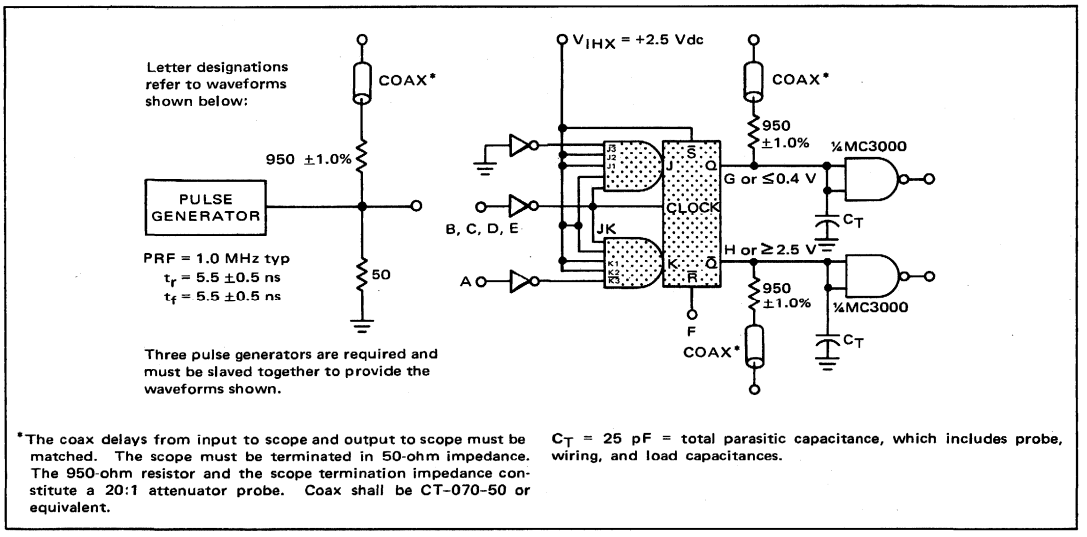
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

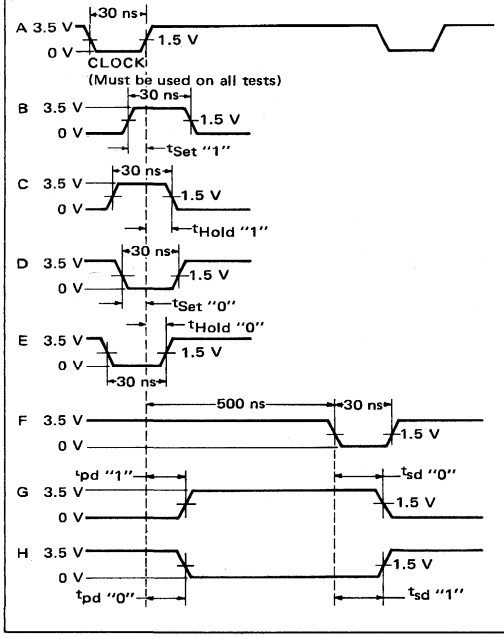
(For J inputs and $\overline{\text{RESET}}$ input; to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



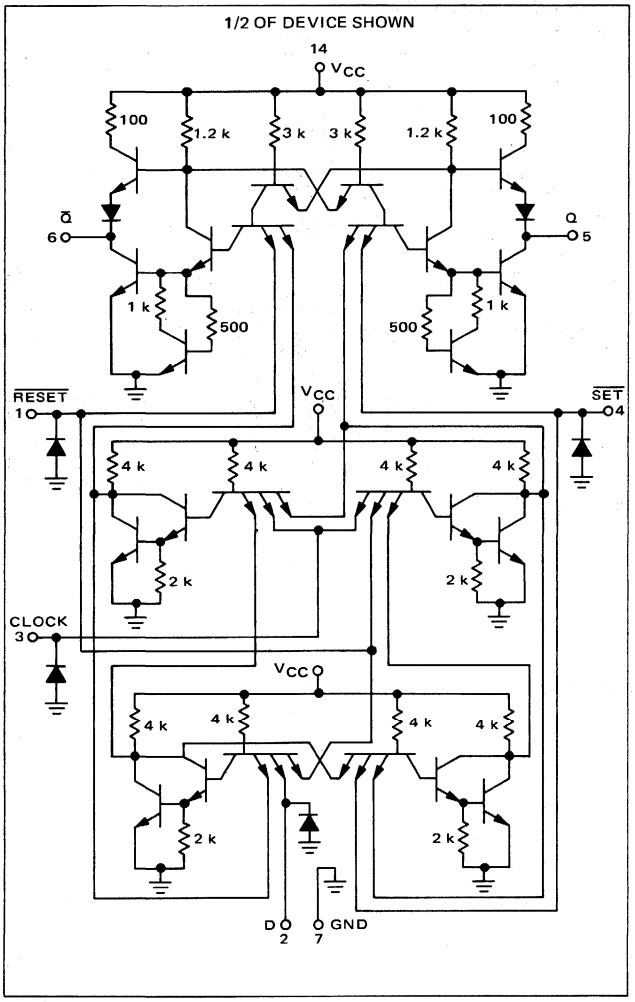
TEST PROCEDURES CHART

TEST	INPUT J*	INPUT $\overline{J}$*	INPUT $\overline{SET}$*	INPUT $\overline{RESET}$*	INPUT K*	INPUT $\overline{K}$*	Q*	$\overline{Q}$*	LIMITS (ns) Min	LIMITS (ns) Max
t_{Set} "1" J	C	Gnd	2.5 V	F	Gnd	Gnd	G	H	–	15
t_{Hold} "0" J	B	Gnd	2.5 V	F	Gnd	Gnd	≤0.4 V	≥2.5 V	–	–3.0
t_{Set} "1" K	Gnd	Gnd	F	2.5 V	C	Gnd	H	G	–	15
t_{Hold} "0" K	Gnd	Gnd	F	2.5 V	B	Gnd	≥2.5 V	≤0.4 V	–	–3.0
t_{Set} "1" $\overline{J}$	2.5 V	E	2.5 V	F	2.5 V	Gnd	G	H	–	15
t_{Hold} "0" $\overline{J}$	2.5 V	D	2.5 V	F	2.5 V	Gnd	≤0.4 V	≥2.5 V	–	–3.0
t_{Set} "1" $\overline{K}$	2.5 V	Gnd	F	2.5 V	2.5 V	E	H	G	–	15
t_{Hold} "0" $\overline{K}$	2.5 V	Gnd	F	2.5 V	2.5 V	D	≥2.5 V	≤0.4 V	–	–3.0
t_{pd} "1"	Delay from clock to Q during t_{Set} "1" J test. Delay from clock to $\overline{Q}$ during t_{Set} "1" K test.								8	20
t_{pd} "0"	Delay from clock to $\overline{Q}$ during t_{Set} "1" J test. Delay from clock to Q during t_{Set} "1" K test.								14	28
t_{sd} "1"	Delay from $\overline{SET}$ to Q during t_{Set} "1" K test. Delay from $\overline{RESET}$ to $\overline{Q}$ during t_{Set} "1" J test.								–	18
t_{sd} "0"	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Set} "1" K test. Delay from $\overline{RESET}$ to Q during t_{Set} "1" J test.								–	25

*Letters shown in these columns refer to waveforms.

DUAL TYPE D FLIP-FLOP

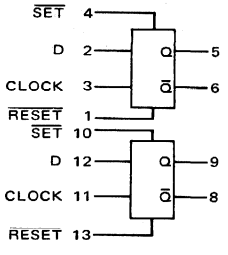
MC3060



The MC3060 dual flip-flop triggers on the positive edge of the clock and performs the Type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct $\overline{SET}$ and $\overline{RESET}$ inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Set-up and Hold times. The clocked inputs are inhibited when the clock is high and data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Set-up and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\overline{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.



TRUTH TABLE

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

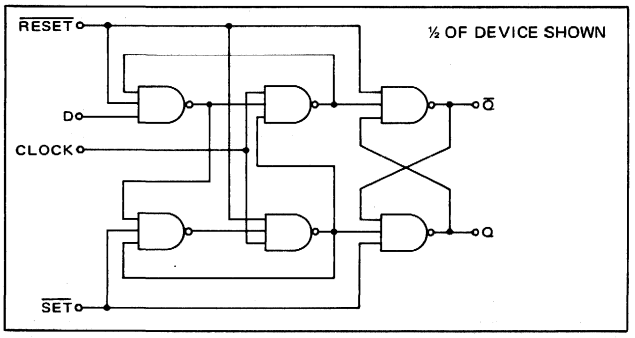
$Q^{n+1} = D^n$

Input Loading Factors:
- $\overline{SET}$ = 1.0
- $\overline{RESET}$ = 1.5
- CLOCK= 1.4
- D = 0.6

Output Loading Factor = 10

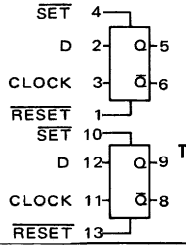
Typical Characteristics: (V_{CC} = 5.0 V, T_A = 25°C)
- Total Power Dissipation = 120 mW/pkg
- Toggle Frequency = 30 MHz
- Logical "1" Setup Time = 10 ns
- Logical "0" Setup Time = 5.0 ns
- Logical "1" and "0" Hold Times = 5.0 ns
- t_{pd} "0" = 17 ns
- t_{pd} "1" = 15 ns

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES														
	mA					Volts									
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5	
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5	
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5	

Characteristic	Symbol	Pin Under Test	MC3060 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																									
Forward Current	I_{FC}	3	-	-3.0	-	-3.0	-	-3.0	mAdc	-	-	-	-	-	-	-	3	-	1	-	-	-	14	-	2,4,7,11
	I_{FD}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,4	-	-	-	14	-	3,7,11
	I_{FS}	4	-	-2.3	-	-2.3	-	-2.3	mAdc	-	-	-	-	-	-	-	4	-	1	-	-	-	14	-	2,3,7,11
	I_{FR}	1	-	-3.4	-	-3.4	-	-3.4	mAdc	-	-	-	-	-	-	-	1	-	2,4	-	-	-	14	-	3,7,11
Leakage Current	I_{RC}	3	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	3	4	-	-	-	14	-	1,2,7,11
	I_{RD}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	2	3,4	-	-	-	14	-	1,7,11
	I_{RS}	4	-	110	-	110	-	110	μAdc	-	-	-	-	-	-	-	-	4	1,2	-	-	-	14	3	7,11
	I_{RR}	1	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	1	4	-	-	-	14	3	2,7,11
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	Vdc	-	-	-	3	-	-	-	-	-	4	-	-	-	14	-	1,2,7,11
		2	-	-	↓	-	-	-	↓	-	-	2	-	-	-	-	-	-	3,4	-	-	-	↓	-	1,7,11
		4	-	-		-	-	-		-	-	-	4	-	-	-	-	-	1,2	-	-	-		3	7,11
		1	-	-		-	-	-		-	-	-	1	-	-	-	-	-	4	-	-	-		3	2,7,11
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	-	14	-	-	7,11
		2	-	-	-	↓	-	-	↓	-	-	-	-	2	-	-	-	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-		-	-	-	-	4	-	-	-	-	-	-	-		-	-	
		1	-	-	-	↓	-	-	↓	-	-	-	-	1	-	-	-	-	-	-	-	↓	-	-	↓
Output																									
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	4	1	-	-	-	-	-	-	14	-	2,3,7,11
		5	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	1	4	-	-	-	-	-	-	14	-	2,3,7,11
	V_{OH}	6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	1	4	-	-	-	-	-	14	-	-	2,3,7,11
		5	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	-	4	1	-	-	-	-	-	14	-	-	2,3,7,11
Short-Circuit Current	I_{SC}	6	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	4	1	-	-	-	14	-	-	-	6,7,11
		5	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	1	4	-	-	-	14	-	-	-	5,7,11
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	1,13	14	-	-	-	-	3,4,7,10,11
Power Supply Drain	I_{PD}	14	-	29	-	29	-	29	mAdc	-	-	-	-	-	-	-	-	-	4,10	-	14	-	-	-	1,3,7,11,13

* Pulse is used to set flip-flop in desired state. P_1 = 4.0 V (V_{RH}), 0 V. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

OPERATING CHARACTERISTICS

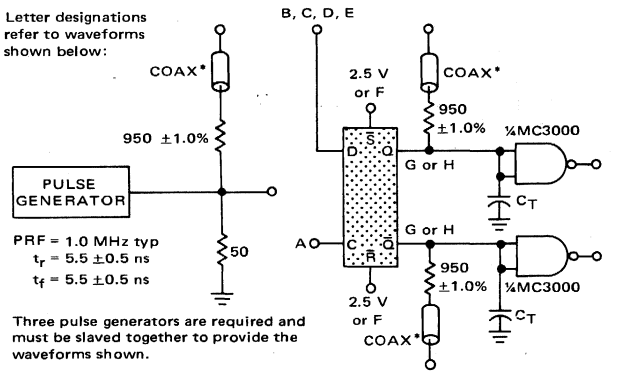
Data must be present 15 ns prior to the rise of the clock and remain 5.0 ns after the clock signal rises.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs may be used at any time as they completely override the clock.

Positive edge triggering: When the clock goes from the low to the high state, the information in the input steering section is transferred to the bistable section.

Unused inputs should be tied to a voltage between 2.0 and 5.5 Vdc.

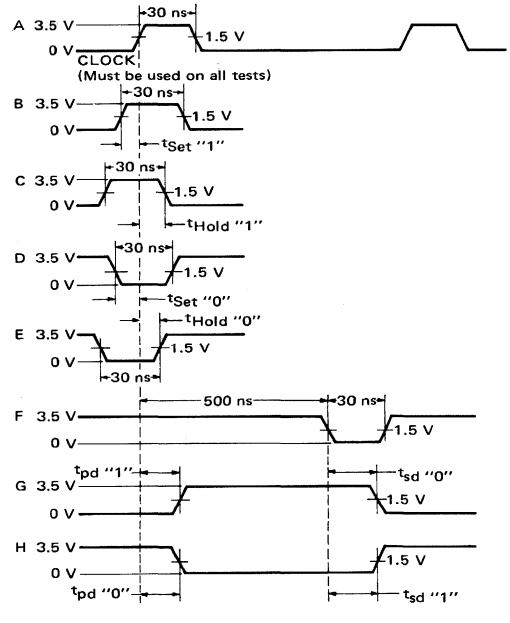
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT D*	INPUT $\overline{SET}$*	INPUT $\overline{RESET}$*	Q*	$\overline{Q}$*	LIMITS (ns) Min	LIMITS (ns) Max
t_{Set} "1" D	B	2.5 V	F	G	H	–	15
t_{Hold} "1" D	C	2.5 V	F	G	H	–	5.0
t_{Set} "0" D	D	F	2.5 V	H	G	–	15
t_{Hold} "0" D	E	F	2.5 V	H	G	–	5.0
t_{pd} "1"	Delay from clock to Q during t_{Set} "1" D test. Delay from clock to $\overline{Q}$ during t_{Set} "0" D test.					10	25
t_{pd} "0"	Delay from clock to Q during t_{Set} "0" D test. Delay from clock to $\overline{Q}$ during t_{Set} "1" D test.					10	25
t_{sd} "1"	Delay from $\overline{SET}$ to Q during t_{Set} "0" D test. Delay from $\overline{RESET}$ to $\overline{Q}$ during t_{Set} "1" D test.					5.0	20
t_{sd} "0"	Delay from $\overline{SET}$ to $\overline{Q}$ during t_{Set} "0" D test. Delay from $\overline{RESET}$ to Q during t_{Set} "1" D test.					5.0	20

*Letters shown in these columns refer to waveforms at left.

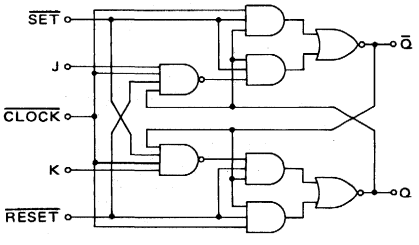
MC3061

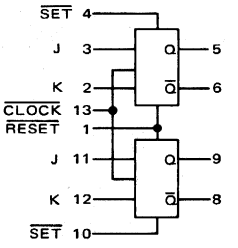
The MC3061 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input in addition to the common direct $\overline{RESET}$ input. These direct inputs provide a means of resetting a group of flip-flops such as a register which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops, making it particularly useful in registers or other common clock applications.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the $\overline{SET}$ input. In addition, both flip-flops may be reset simultaneously by using the common $\overline{RESET}$ in a similar manner.

LOGIC DIAGRAM

1/2 OF DEVICE SHOWN,
$\overline{RESET}$ AND $\overline{CLOCK}$ COMMON TO BOTH





Input Loading Factors:
$\overline{SET}$ = 1.6
$\overline{RESET}$, $\overline{CLOCK}$ = 3.2
J, K = 0.6

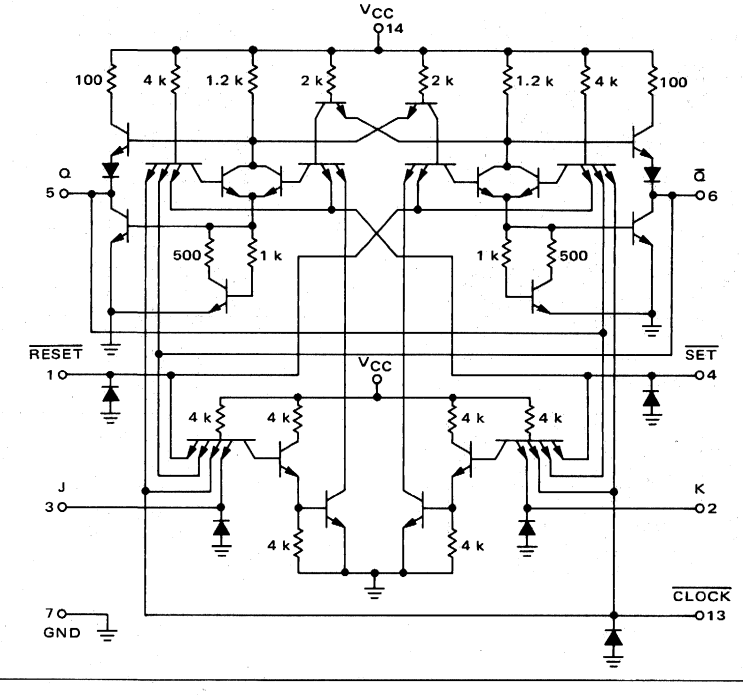
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics
(V_{CC} = 5.0 V; T_A = 25°C)

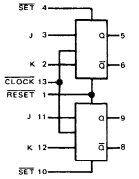
Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd} "0" = 12 ns
t_{pd} "1" = 12 ns



1/2 OF CIRCUIT
SHOWN ($\overline{RESET}$ AND $\overline{CLOCK}$
COMMON TO BOTH)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop plus the inputs common to both flip-flops. To complete testing, sequence through the remaining inputs in the same manner.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
	mA					Volts								
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}
0°C	23	-2.0	-	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.5	5.5
+25°C	23	-2.0	1.0	2.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.5	5.5
+75°C	23	-2.0	-	-	-	0.9	1.8	0.4	2.5	4.0	-	5.0	4.5	5.5

Characteristic	Symbol	Pin Under Test	MC3061 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																									
Forward Current	I_{FJ}	3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	3	-	1,4,13	-	-	-	14	1	2,7,10
	I_{FK}	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	-	-	2	-	1,4,13	-	-	-	14	4	3,7,10
	$I_{F\overline{R}}$	1	-	-3.5	-	-3.5	-	-3.5	mAdc	-	-	-	-	-	-	-	1	-	3,4,13	-	-	-	14	-	2,7,10
	$I_{F\overline{S}}$	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	-	-	4	-	1,2,13	-	-	-	14	-	3,7,10
	$I_{F\overline{C}}$	13	-	-5.7	-	-5.7	-	-5.7	mAdc	-	-	-	-	-	-	-	13	-	1,2,3,11,12	-	-	-	14	4,10	7
Leakage Current	I_{RJ}	3	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	3	2,4	-	-	-	14	-	1,7,10,13
	I_{RK}	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	-	-	2	1,3	-	-	-	14	-	4,7,10,13
	$I_{R\overline{R}}$	1	-	230	-	230	-	230	μAdc	-	-	-	-	-	-	-	-	1	2	-	-	-	14	1	3,4,7,11,13
	$I_{R\overline{S}}$	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	-	-	4	3	-	-	-	14	4	1,2,7,10,13
	$I_{R\overline{C}}$	13	-	290	-	290	-	290	μAdc	-	-	-	-	-	-	-	-	13	-	-	-	-	14	-	1,2,3,4,7,10,11,12
Breakdown Voltage	BV_{in}	3	-	-	5.5	-	-	-	Vdc	-	-	3	-	-	-	-	-	-	2,4	-	-	-	14	-	1,7,10,13
		2	-	-	↓	-	-	-	↓	-	-	2	-	-	-	-	-	-	1,3	-	-	-	↓	-	4,7,10,13
		1	-	-	↓	-	-	-	↓	-	-	-	1	-	-	-	-	-	2	-	-	-	↓	1	3,4,7,11,13
		4	-	-	↓	-	-	-	↓	-	-	-	4	-	-	-	-	-	3	-	-	-	↓	4	1,2,7,10,13
		13	-	-	↓	-	-	-	↓	-	-	-	13	-	-	-	-	-	-	-	-	-	↓	-	1,2,3,4,7,10,11,12
Clamp Voltage	V_D	3	-	-	-	-1.5	-	-	Vdc	-	-	-	-	3	-	-	-	-	-	-	-	14	-	-	7,10
		2	-	-	-	↓	-	-	↓	-	-	-	-	2	-	-	-	-	-	-	-	↓	-	-	↓
		1	-	-	-	↓	-	-	↓	-	-	-	-	1	-	-	-	-	-	-	-	↓	-	-	↓
		4	-	-	-	↓	-	-	↓	-	-	-	-	4	-	-	-	-	-	-	-	↓	-	-	↓
		13	-	-	-	↓	-	-	↓	-	-	-	-	13	-	-	-	-	-	-	-	↓	-	-	↓
Output																									
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	1	4	-	-	-	-	-	-	14	1	7,10
		6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	4	1	-	-	-	-	-	-	14	4	7,10
	V_{OH}	5	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	-	4	1	-	-	-	-	-	14	-	4	7,10
		6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	1	4	-	-	-	-	-	14	-	1	7,10
Short-Circuit Current	I_{SC}	5	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	4,5,7,10
		6	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,6,7,10
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	42	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	30	-	30	-	30	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,7

*Momentarily ground pin prior to taking measurement. (If pin is also in another column, the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

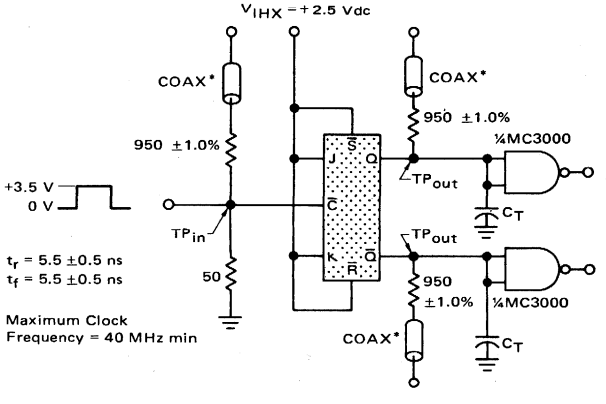
High state data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The direct $\overline{SET}$ (individual) inputs and $\overline{RESET}$ (common) inputs may be used at any time without regard to the clock state. The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input or reset to the Q = 0 state by applying a low level to the $\overline{RESET}$ input. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering — The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

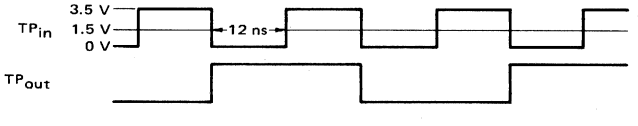
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

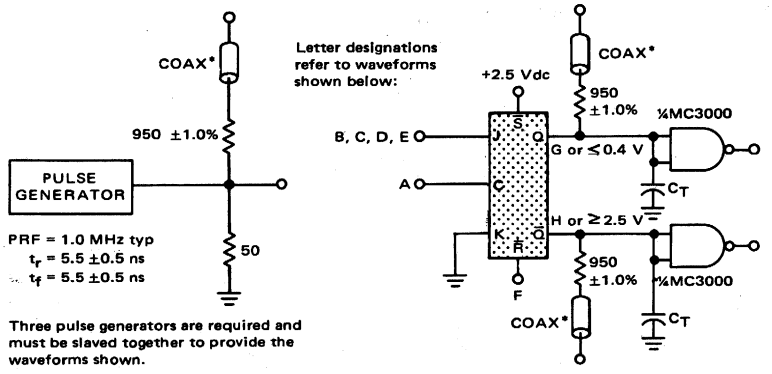
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

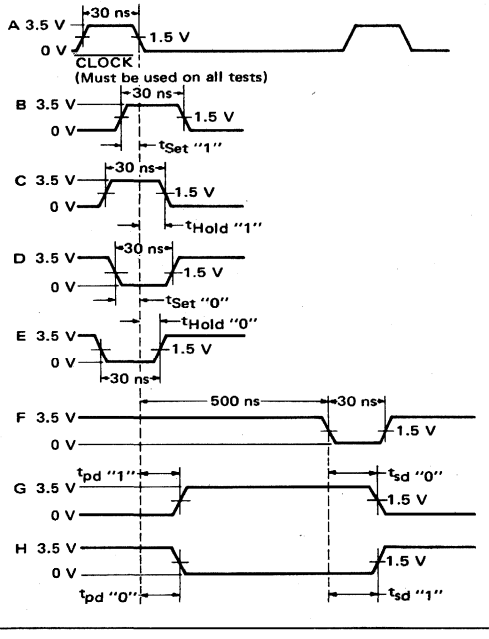
(For J Inputs and $\overline{\text{RESET}}$ Input; to test other inputs, refer to Test Procedures Chart)



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT J*	INPUT $\overline{\text{SET}}$*	INPUT $\overline{\text{RESET}}$*	INPUT K*	Q*	$\overline{Q}$*	LIMITS (ns) Max
t_{Set} "1" J	B	2.5 V	F	Gnd	G	H	15
t_{Hold} "1" J	C	2.5 V	F	Gnd	G	H	0**
t_{Set} "0" J	D	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	15
t_{Hold} "0" J	E	2.5 V	F	Gnd	≤0.4 V	≥2.5 V	0**
t_{Set} "1" K	Gnd	F	2.5 V	B	H	G	15
t_{Hold} "1" K	Gnd	F	2.5 V	C	H	G	0**
t_{Set} "0" K	Gnd	F	2.5 V	D	≥2.5 V	≤0.4 V	15
t_{Hold} "0" K	Gnd	F	2.5 V	E	≥2.5 V	≤0.4 V	0**
t_{pd} "1"	Delay from clock to Q during t_{Set} "1" J test. Delay from clock to $\overline{Q}$ during t_{Set} "1" K test.						18
t_{pd} "0"	Delay from clock to $\overline{Q}$ during t_{Set} "1" J test. Delay from clock to Q during t_{Set} "1" K test.						18
t_{sd} "1"	Delay from $\overline{\text{SET}}$ to Q during t_{Set} "1" K test. Delay from $\overline{\text{RESET}}$ to $\overline{Q}$ during t_{Set} "1" J test.						18
t_{sd} "0"	Delay from $\overline{\text{SET}}$ to $\overline{Q}$ during t_{Set} "1" K test. Delay from $\overline{\text{RESET}}$ to Q during t_{Set} "1" J test.						18

*Letters shown in these columns refer to waveforms shown at the left.
**t_{Hold} is typically a negative number.

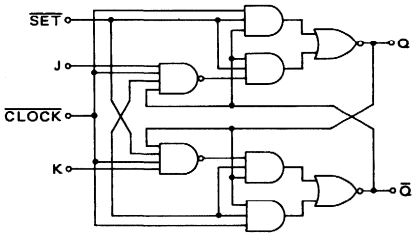
DUAL J-K FLIP-FLOP

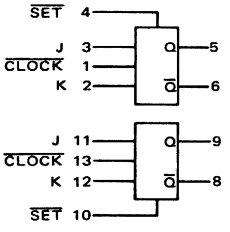
MC3062

The MC3062 dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Set-up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set-up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the $\overline{SET}$ input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN





Input Loading Factors:
$\overline{CLOCK}$, $\overline{SET}$ = 1.6
J, K, = 0.6

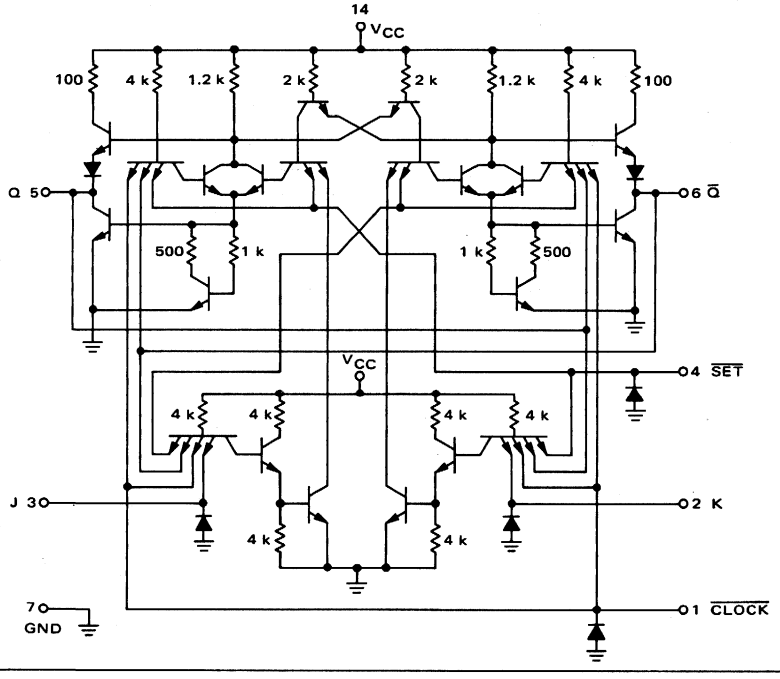
Output Loading Factor = 10

J-K TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Typical Characteristics:
(V_{CC} = 5.0 V; T_A = 25°C)

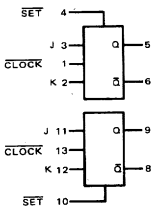
Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd} "1" = 12 ns
t_{pd} "0" = 12 ns



1/2 OF DEVICE SHOWN

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES												
	mA					Volts							
	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	
0°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5	
+25°C	23	-2.0	1.0	2.0	-10	0.4	2.5	4.0	7.0	5.0	4.5	5.5	
+75°C	23	-2.0	-	-	-	0.4	2.5	4.0	-	5.0	4.5	5.5	

Characteristic	Symbol	Pin Under Test	MC3062 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	I_D	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	P_1*	Gnd
Input																							
Forward Current	I_F	2	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	2	-	1,4	-	-	-	14	-	3,6,7,13
		3	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	-	3	-	1,4	-	-	-	14	-	2,5,7,13
	$I_{F\overline{S}}$	4	-	-1.8	-	-1.8	-	-1.8	mAdc	-	-	-	-	-	4	-	1,2	-	-	-	14	-	3,7,13
	$I_{F\overline{C}}$	1	-	-2.9	-	-2.9	-	-2.9	mAdc	-	-	-	-	-	1	-	2,3	-	-	-	14	4	7,13
		1	-	-2.9	-	-2.9	-	-2.9	mAdc	-	-	-	-	-	1	-	2,3,4	-	-	-	14	5	7,13
Leakage Current	I_R	2	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	2	3	-	-	-	14	-	1,4,7,13
		3	-	80	-	80	-	80	μAdc	-	-	-	-	-	-	3	2	-	-	-	14	-	1,4,7,13
	$I_{R\overline{S}}$	4	-	140	-	140	-	140	μAdc	-	-	-	-	-	-	4	3	-	-	-	14	-	1,2,7,13
	$I_{R\overline{C}}$	1	-	170	-	170	-	170	μAdc	-	-	-	-	-	-	1	-	-	-	-	14	-	2,3,4,7,13
Breakdown Voltage	BV_{in}	2	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	-	-	-	14	-	1,4,7,13
		3	-	-	↓	-	-	-	↓	-	-	3	-	-	-	-	-	-	-	-	↓	-	1,4,7,13
		4	-	-		-	-	-		-	-	-	4	-	-	-	-	-	-	-		-	1,2,7,13
		1	-	-		-	-	-		-	-	-	1	-	-	-	-	-	-	-		-	2,3,4,7,13
Clamp Voltage	V_D	2	-	-	-	-1.5	-	-	Vdc	-	-	-	-	2	-	-	-	-	-	14	-	-	7,13
		3	-	-	-	↓	-	-	↓	-	-	-	-	3	-	-	-	-	-	↓	-	-	↓
		4	-	-	-		-	-		-	-	-	-	4	-	-	-	-	-		-	-	
		1	-	-	-		-	-		-	-	-	-	1	-	-	-	-	-		-	-	
Output																							
Output Voltage	V_{OL}	5	-	0.4	-	0.4	-	0.4	Vdc	5	-	-	-	-	-	-	-	-	-	-	14	5	1,7,13
		6	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	4	-	-	-	-	-	14	4	1,7,13
	V_{OH}	5	2.5	-	2.5	-	2.5	-	Vdc	-	5	-	-	-	4	-	-	-	-	14	-	4	7
		6	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	-	-	4	-	-	14	-	5	1,7,13
Short-Circuit Current	I_{SC}	5	-	-	-20	-60	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	4,5,7,13
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	41	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	-	4,7,10
Power Supply Drain	I_{PD}	14	-	29	-	29	-	29	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	4,7,10

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

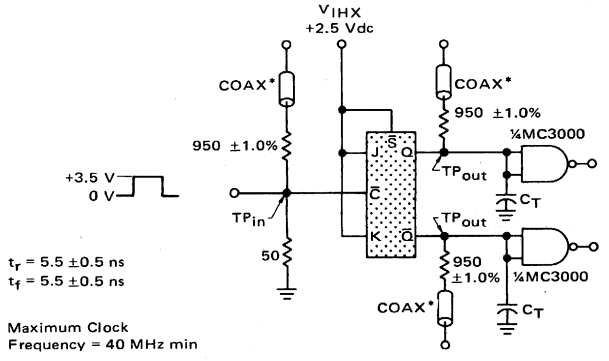
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the $\overline{SET}$ input. The direct $\overline{SET}$ inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



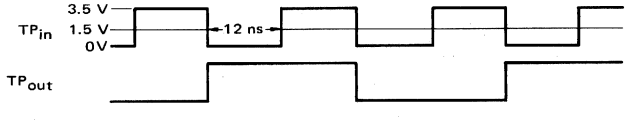
t_r = 5.5 ±0.5 ns
t_f = 5.5 ±0.5 ns

Maximum Clock Frequency = 40 MHz min

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

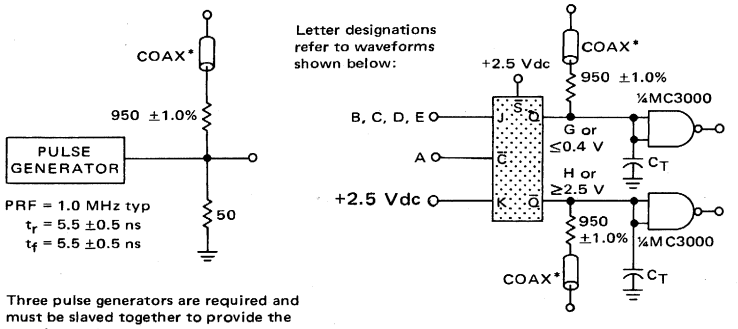
VOLTAGE WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)

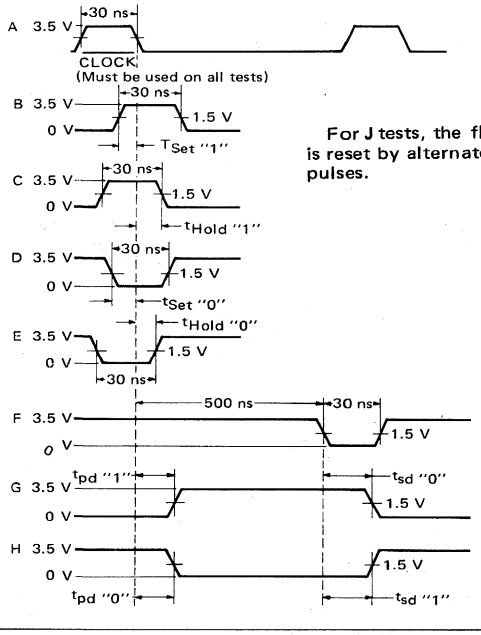


Three pulse generators are required and must be slaved together to provide the waveforms shown.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



For J tests, the flip-flop is reset by alternate clock pulses.

TEST PROCEDURES CHART

TEST	INPUT J*	INPUT $\overline{SET}$*	INPUT K*	Q*	$\bar{Q}$*	LIMITS (ns) Max
t_{Set} "1" J	B	2.5 V	2.5 V	G	H	15
t_{Hold} "1" J	C	2.5 V	2.5 V	G	H	0**
t_{Set} "0" J	D	2.5 V	2.5 V	≤0.4 V	≥2.5 V	15
t_{Hold} "0" J	E	2.5 V	2.5 V	≤0.4 V	≥2.5 V	0**
t_{Set} "1" K	Gnd	F	B	H	G	15
t_{Hold} "1" K	Gnd	F	C	H	G	0**
t_{Set} "0" K	Gnd	F	D	≥2.5 V	≤0.4 V	15
t_{Hold} "0" K	Gnd	F	E	≥2.5 V	≤0.4 V	0**
t_{pd} "1"	Delay from $\overline{clock}$ to Q during t_{Set} "1" J test. Delay from $\overline{clock}$ to $\bar{Q}$ during t_{Set} "1" K test.					18
t_{pd} "0"	Delay from $\overline{clock}$ to $\bar{Q}$ during t_{Set} "1" J test. Delay from $\overline{clock}$ to Q during t_{Set} "1" K test.					18
t_{sd} "1"	Delay from $\overline{SET}$ to Q during t_{Set} "1" K test.					18
t_{sd} "0"	Delay from $\overline{SET}$ to $\bar{Q}$ during t_{Set} "1" K test.					18

*Letters shown in test columns refer to waveforms shown at the left.
**t_{Hold} is typically a negative number.

MDTL

INTEGRATED CIRCUITS
MC930/MC830 SERIES

MDTL

INTEGRATED CIRCUITS

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NUMERICAL INDEX

(Functions and Characteristics)

V_{CC} = 5.0 Vdc, T_A = 25°C

Function	Type ① 0 to +75°C	Case	Type ① −55 to +125°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
Expandable Dual 4-Input NAND Gate	MC830	83,93	MC930	83	8	30	22	5-12
Expandable Dual 3-2 Input NAND Gate	MC830	96A	MC930	96A	8	30	22	5-12
Clocked Flip-Flop	MC831	83,93,96A	MC931	83,96A	7	40	55	5-28
Expandable Dual 4-Input Buffer	MC832	83,93	MC932	83	25	35	85	5-24
Expandable Dual 3-2 Input Buffer	MC832	96A	MC932	96A	25	35	85	5-24
Dual 4-Input Expander	MC833	83,93	MC933	83	–	–	–	5-52
Dual 4-3 Input Expander	MC833	96A	MC933	96A	–	–	–	5-52
Hex Inverter	MC834	83,93	MC934	83	8	30	66	5-18
Hex Inverter	MC836	83,93	MC936	83	8	30	66	5-20
Hex Inverter	MC837	83,93	MC937	83	7	25	90	5-20
Decade Counter	MC838	83,93	MC938	83	8	30 MHz ③	150	5-44
Divide-by-Sixteen Counter	MC839	83,93	MC939	83	8	30 MHz ③	150	5-48
4-Input AND Driver with NOR Strobe	MC843	96A	MC943	96A	250 mA	80	50	5-26
Expandable Dual 4-Input Power Gate	MC844	83,93	MC944	83	27	30	65	5-22
Expandable Dual 3-2 Input Power Gate	MC844	96A	MC944	96A	27	30	65	5-22
Clocked Flip-Flop	MC845	83,93,96A	MC945	83,96A	12/10 ②	40	60	5-31
Quad 2-Input NAND Gate	MC846	83,93	MC946	83	8	30	44	5-16
Quad Inverter	MC846	96A	MC946	96A	8	30	44	5-16
Clocked Flip-Flop	MC848	83,93,96A	MC948	83,96A	11/9 ②	40	70	5-31
Quad 2-Input NAND Gate (2 kΩ pullup resistor)	MC849	83,93	MC949	83	7	25	66	5-16
Quad Inverter (2 kΩ pullup resistor)	MC849	96A	MC949	96A	7	25	60	5-16
Pulse Triggered Binary	MC850	83,93,96A	MC950	83,96A	10/8 ②	15	50	5-39
Monostable Multivibrator	MC851	83,93,96A	MC951	83,96A	10	40	30	5-42
Dual J-K Flip-Flop (common clock and C_D, separate S_D)	MC852	83,93	MC952	83	12/10 ②	40	120	5-34
Dual J-K Flip-Flop (separate clock and S_D, no C_D)	MC853	83,93	MC953	83	12/10 ②	40	120	5-34
Dual J-K Flip-Flop (common clock and C_D, separate S_D, 2 kΩ pullup resistor)	MC855	83,93	MC955	83	11/9 ②	40	140	5-34
Dual J-K Flip-Flop (separate clock and S_D, no C_D, 2 kΩ pullup resistor)	MC856	83,93	MC956	83	11/9 ②	40	140	5-34
Expandable Dual 4-Input NAND Gate (2 k pullup resistor)	MC861	83,93	MC961	83	7	25	33	5-12
Expandable Dual 3-2 Input NAND Gate (2 k pullup resistor)	MC861	96A	MC961	96A	7	25	33	5-12
Triple 3-Input NAND Gate	MC862	83,93	MC962	83	8	30	33	5-14
Dual 2-Input NAND Gate plus Inverter	MC862	96A	MC962	96A	8	30	30	5-14
Triple 3-Input NAND Gate (2 kΩ pullup resistor)	MC863	83,93	MC963	83	7	25	50	5-14
Dual 2-Input NAND Gate plus Inverter (2 kΩ pullup resistor)	MC863	96A	MC963	96A	7	25	45	5-14

① G suffix denoted Metal Can, F suffix denotes Flat Package, P suffix denotes Plastic Package. (i.e., MC830G = Metal Can, MC830F = Flat Package, MC830 P = Plastic Package)

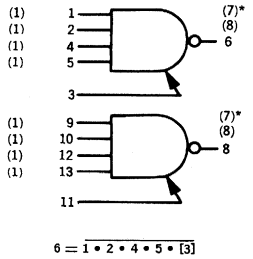
② Fan-out for MC830 series type / Fan-out for MC930 series type.

③ Maximum Counting Frequency

Numbers at ends of terminals represent pin numbers. Numbers in parenthesis indicate loading.
"G" Package: V_{CC} = pin 10, Gnd = pin 5 unless otherwise noted.
"F" and "P" Packages: V_{CC} = pin 14, Gnd = pin 7 unless otherwise noted.

GATES

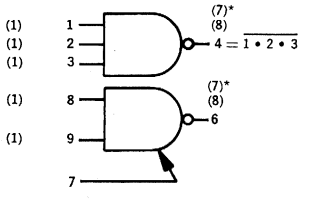
MC830F, MC830P, MC930F MC861F, MC861P, MC961F Expandable Dual 4-Input Gate



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

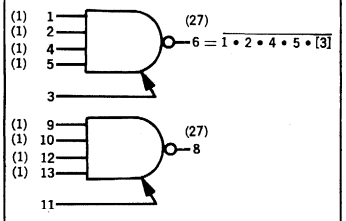
*APPLIES TO MC861F, MC861P, MC961F

MC830G, MC930G MC861G, MC961G Expandable Dual 3-2 Input Gate

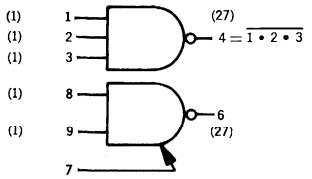


*APPLIES TO MC861G, MC961G

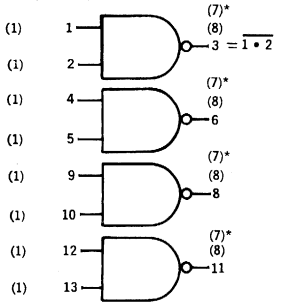
MC844F, MC844P, MC944F Expandable Dual 4-Input Power Gate



MC844G, MC944G Expandable Dual 3-2 Input Power Gate

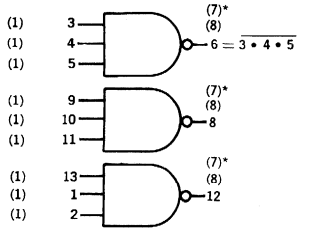


MC846F, MC846P, MC946F MC849F, MC849P, MC949F Quad 2-Input Gate



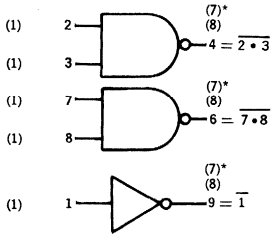
*APPLIES TO MC849F, MC849P, MC949F

MC862F, MC862P, MC962F MC863F, MC863P, MC963F Triple 3-Input Gate



*APPLIES TO MC863F, MC863P, MC963F

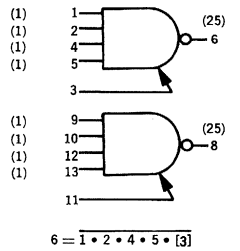
MC862G, MC962G MC863G, MC963G Dual 2-Input Gate Plus Inverter



*APPLIES TO MC863G, MC963G

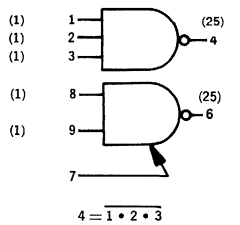
BUFFERS

MC832F, MC832P, MC932F Expandable Dual 4-Input Buffer



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

MC832G, MC932G Expandable Dual 3-2 Input Buffer

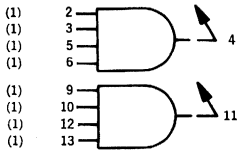


$4 = \overline{1 \cdot 2 \cdot 3}$

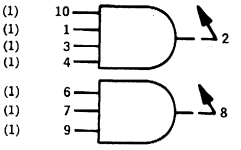
LOADING DIAGRAMS (continued)

EXPANDERS

MC833F, MC833P, MC933F
Dual 4-Input Expander

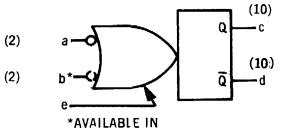


MC833G, MC933G
Dual 4-3 Input Expander



MULTIVIBRATOR

MC851F, MC851G, MC851P
MC951F, MC951G
Monostable Multivibrator



*AVAILABLE IN
"F" & "P" Pkgs. ONLY

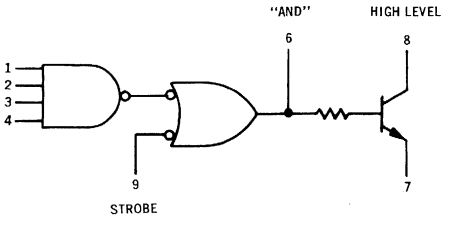
"F" & "P" Pkgs.: V_{CC} = pin 14, Gnd = pin 7
"G" Pkg.: V_{CC} = pin 6, Gnd = pin 1

Pin Connections

Letter	a	b	c	d	e
"F" & "P" Pkgs.	3	4	6	1	2
"G" Pkg.	9	—	10	7	8

DRIVERS

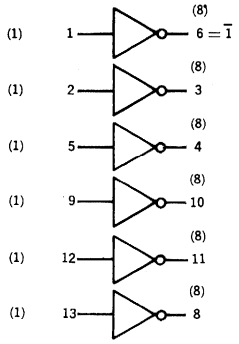
MC843G, MC943G
4-Input AND Driver with NOR Strobe



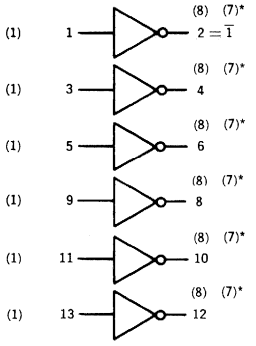
$\bar{8} = 1 \cdot 2 \cdot 3 \cdot 4 + \bar{9}$

INVERTERS

MC834F, MC834P, MC934F
Hex Inverter

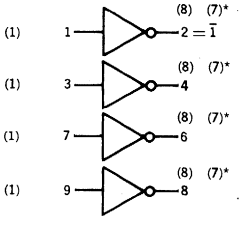


MC836F, MC836P, MC936F
MC837F, MC837P, MC937F
Hex Inverter



*APPLIES TO MC837F, MC837P, MC937F

MC846G, MC946G
MC849G, MC949G
Quad Inverter



*APPLIES TO MC849G, MC949G

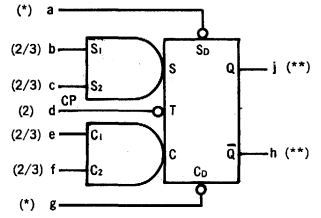
FLIP-FLOPS

MC831F, MC831G, MC831P
MC931F, MC931G

MC845F, MC845G, MC845P
MC945F, MC945G

MC848F, MC848G, MC848P
MC948F, MC948G

Clocked Flip-Flop



*SD and CD loading factor: ¾ for MC831/MC931 types
2 for other clocked flip-flops

**Q and Q̄ loading factor: 7 for MC831/MC931 types
12 for MC845 types
10 for MC945 types
11 for MC848 types
9 for MC948 types

Pin Connections

Letter	a	b	c	d	e	f	g	h	j
"F" & "P" Pkgs.	10	3	4	2	12	11	5	9	6
"G" Pkg.	7	2	3	1	9	8	—	6	4

SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 — Low State (more negative)
1 — High State (more positive)
X — State of the input does not affect the state of the circuit.
U — Indeterminate State

J-K TRUTH TABLE
(Connect S_2 to $\bar{Q}$, C_2 to Q)

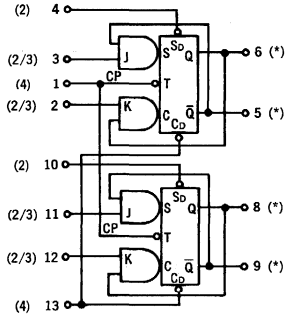
t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

MC852F, MC852P, MC952F
MC855F, MC855P, MC955F
Dual J-K Flip-Flop



*Q and Q̄ loading factor:

12 — MC852
10 — MC952
11 — MC855
9 — MC955

ASYNCHRONOUS TRUTH TABLE
MC952/MC852 and MC955/MC855

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

ASYNCHRONOUS TRUTH TABLE
MC953/MC853 and MC956/MC856

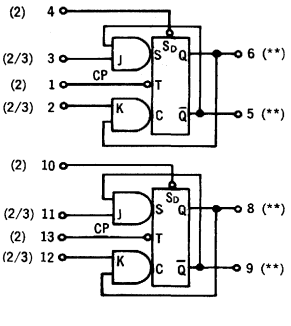
S_D	Q	$\bar{Q}$
1	NC	NC
0	1	0

J-K TRUTH TABLE
All Types

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs: they are independent of all other inputs.

MC853F, MC853P, MC953F
MC856F, MC856P, MC956F
Dual J-K Flip-Flop



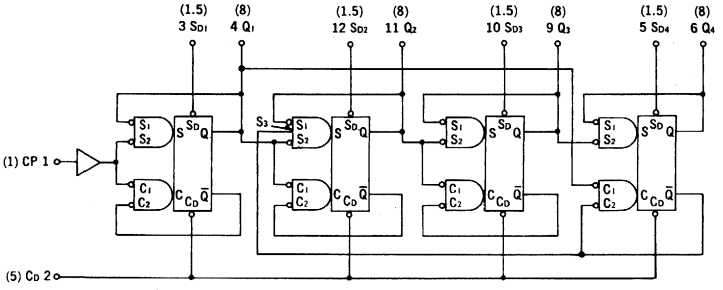
**Q and Q̄ loading factor:

12 — MC853
10 — MC953
11 — MC856
9 — MC956

LOADING DIAGRAMS (continued)

COUNTERS

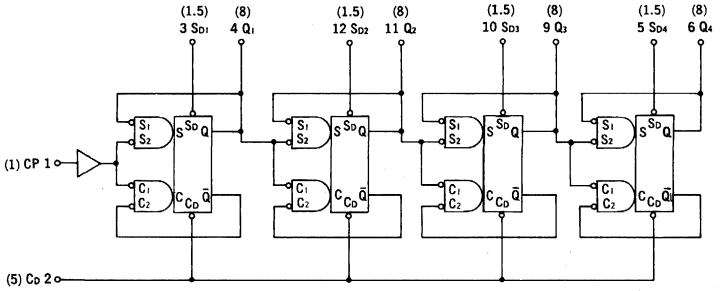
MC838F, MC838P, MC938F
Decade Counter



DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	
3	Q_1	Q_2	$\bar{Q}_3$	
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	
5	Q_1	$\bar{Q}_2$	Q_3	
6	$\bar{Q}_1$	Q_2	Q_3	
7	Q_1	Q_2	Q_3	
8	$\bar{Q}_1$	Q_4		
9	Q_1	Q_4		

MC839F, MC839P, MC939F
Divide-by-Sixteen Counter

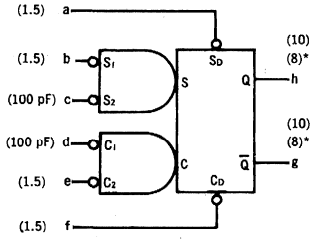


DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
3	Q_1	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
5	Q_1	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
6	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
7	Q_1	Q_2	Q_3	$\bar{Q}_4$
8	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
9	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
10	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	Q_4
11	Q_1	Q_2	$\bar{Q}_3$	Q_4
12	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	Q_4
13	Q_1	$\bar{Q}_2$	Q_3	Q_4
14	$\bar{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

PULSE TRIGGERED BINARY

MC850F, MC850G, MC850P, MC950F, MC950G
Pulse Triggered Binary



* APPLIES TO MC950F, MC950G

SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	0	0	0	U
1	X	1	X	Q_n
X	1	X	1	Q_n
0	1	1	0	Q_n
0	0	X	1	1
0	0	1	X	1
1	X	0	0	0
X	1	0	0	0

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

SINGLE TRIGGER TRUTH TABLE
(Pins S_2 and C_1 tied together)

t_n		t_{n+1}
S_1	C_2	Q
0	0	U
1	0	0
0	1	1
1	1	Q_n

0 = low state (more negative) 1 = high state (more positive)

X = don't care U = indeterminate state NC = no change

Pin Connections

Letter	a	b	c	d	e	f	g	h
"F" & "P" Pkgs.	13	4	5	6	10	1	11	3
"G" Pkg.	9	3	4	5	7	1	8	2

MDTL

GENERAL INFORMATION SECTION

INTRODUCTION

The MDTL line of diode transistor logic is a general purpose logic family offering moderate speed, good noise immunity, low noise generation, a high degree of logic flexibility, and economy.

GATE FUNCTIONS

The MDTL family offers positive-logic NAND gates with the capability of tying together the outputs of two or more elements. This not only allows greater logic flexibility, but also reduces required inventory stocking levels since AND-OR-INVERT functions (Wired OR) are readily obtained without special gates.

Buffer elements and power gates are available for driving large capacitive loads and/or where fan-out requirements are high. The buffer has an active pullup configuration, therefore the AND-OR-INVERT function can not be implemented with the buffer. Outputs of two or more buffer elements (or multiple buffer and power gate arrays) may be paralleled to achieve higher fan-out providing the inputs are also paralleled.

PROPAGATION DELAY

The typical propagation delay through an MDTL gate is 30 ns with nominal loading, providing the gate utilizes 6.0 k ohm pullup resistors. (Gates with 2.0 k ohm pullup resistors, approximately 25% faster, are also available.) The propagation delay is asymmetrical; t_{pd+} (propagation delay with the output transistor turning off) is normally double the value of t_{pd-} (propagation delay with the output transistor turning on). It will also be found that the value of t_{pd-} is affected very little by output loading, while t_{pd+} is quite dependent on the capacitive load seen by the output.

FLIP-FLOP OPERATING CHARACTERISTICS

There are two generic types of flip-flops within the MDTL family- – an ac binary and master-slave configuration. The ac binary is useful in high-speed systems (it will toggle at a rate typically greater than 40 MHz) and is also useful in control sections where its unique truth table is often advantageous.

FLIP-FLOP TRUTH TABLES

The synchronous truth tables, specified for the single clocked flip-flops (MC931/831, MC945/845, MC948/848) and the dual J-K flip-flops, relate the state the output will attain after a negative transition of the toggle input to the state of the output and the steering inputs (J-K or S-C) during the period when the toggle input is high. The complete truth table is valid only when the steering inputs are not allowed to change while the toggle input is high.

For applications which require changing the steering inputs while the clock input is high, a determination of the divergence from the truth table may be obtained from Figure 1. Note that the first four states do not affect the master section while the remaining five may. A general rule for this type of flip-flop (MC931/831, MC945/845, MC948/848 operated in the synchronous R-S mode) is that if one or more conditions that affect the master section are present while the clock is high, the flip-flop will respond to the last condition present prior to the negative transition of the clock.

Figure 2 shows a next-state table for J-K flip-flops, useful in determining the response of J-K flip-flops to a negative clock transition under conditions that involve changing the steering inputs while the clock input is high. Simply stated, satisfying either of the last two conditions in the table at any time while the clock input is high will cause the flip-flop to toggle when the clock goes low. The above discussion and next-state table apply to the MC931/831, MC945/845, and MC948/848 when operated in the J-K mode as well as to the dual J-K devices in the MDTL family.

FIGURE 1 – SINGLE CLOCKED FLIP-FLOP TRUTH TABLE

t_n				t_{n+1}	
S_1	S_2	C_1	C_2	Q	
0	x	0	x	Q_n	These Conditions Have No Effect On Master Section
0	x	x	0	Q_n	
x	0	0	x	Q_n	
x	0	x	0	Q_n	
0	x	1	1	0	These Conditions May Affect The Master Section
x	0	1	1	0	
1	1	0	x	1	
1	1	x	0	1	
1	1	1	1	U	

0 – Low State (more negative)
1 – High State (more positive)
x – State of the input does not affect the state of the circuit.
U – Indeterminate State

FIGURE 2 – J-K NEXT-STATE TABLE

J	K	Q_n	Q_{n+1}
0	x	0	Q_n
x	0	1	Q_n
1	x	0	$\overline{Q}_n$
x	1	1	$\overline{Q}_n$

POWER SUPPLY REQUIREMENTS

Normal operating voltage for the MDTL series is 5.0 volts ±10%. Typical power dissipation is given for each circuit, assuming a supply voltage of 5.0 volts. Also specified is a maximum worst-case current drain at the operating voltage. It should be noted that the specification of maximum current at 8.0 volt supply is primarily to guarantee reliability of the product under adverse conditions. It is not meant to infer that 8.0 volts is a normal operating condition.

Since power dissipation of an MDTL gate or flip-flop changes little with changes in the output state, bypassing of the power supply leads is not critical; however, a 1.0 μF capacitor where the supply connections enter the board is recommended. This is generally sufficient if the system is composed of gates and flip-flops with passive pullup elements, but smaller capacitors (approximately 0.01 μF) should be distributed on the board with a ratio of one capacitor for each eight packages if the board has a high density of circuits with active pullup elements (i.e., buffers, ac-coupled binaries, decade counters, etc.). It is also advisable to bypass the supply with a single 0.01 μF capacitor in close proximity to any MC951/851 used in the system.

MAXIMUM RATINGS

Characteristic	Rating	Unit
Supply Voltage — Continuous Pulsed, < 1 second	8.0 12	Vdc
Output Current (into outputs) — MC932/832, MC944/844 — Continuous Pulsed, < 30 ms MC951/851, MC950/850 — Continuous MC950/850 — Pulsed, < 30 ms All other types	 150 300 50 100 30	mAdc
Input Forward Current	−10	mAdc
Input Reverse Current — MC932/832, MC944/844, MC950/850 All other types	 5.0 1.0	mAdc
Operating Temperature Range — MC930 Series MC830 Series	 −55 to +125 0 to + 75	°C
Storage Temperature Range — Metal Can and Flat Package Plastic Package	 −65 to +150 −55 to +125	°C

GENERAL RULES

- The number of load circuits that may be driven from an output is determinated by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
- With the exception of the buffer elements, the outputs of all MDTL gates and inverters may be tied together to form the Wired-OR function. For each added gate which has a 6 k ohm pullup resistor, subtract 0.83 unit load. The addition of a gate with a 2 k ohm pullup resistor reduces the available fan-out by 2.5 unit loads. No reduction in fan-out is required when wiring collectors of gates or inverters which have no internal pullup resistor.
- The outputs of the Dual Buffer may not be tied together.
- The outputs of the Dual Power Gate may be tied together to perform the Wired-OR function.
- An external load resistor should be utilized with the Dual Power Gate. At V_{CC} = 5.0 ± 0.5 V, subtract the following output loads:

  R
  2kΩ — 2 loads
  1kΩ — 4 loads
  510Ω — 8 loads

- For increased current capability, the inputs and outputs of ½ MC932 and ½ MC944 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

DEFINITIONS

C_P Clock pulse

f_C Counting frequency

I_{CE} Test current for measuring LV_{CE}

I_{CEX} Collector-to-emitter leakage of the output transistor

I_F Forward current of input diodes for unit input load. Also shown are 0.5 I_F, 2/3 I_F, 2 I_F, etc., which indicate input loading factor times I_F.

I_2, I_{12} Forward current of pins 2 and 12 of the pulse triggered binary

I_9 Forward current of pin 9 of the monostable multivibrator

I_{FCP} Forward current of clock input diodes. Shown as 2 I_{FCP} for inputs with loading factor of 2.

I_{FD} Forward current of dual expander diodes

I_{FS} Forward current of SET and CLEAR input diodes. Shown as 2 I_{FS} for inputs with loading factor of 2.

I_{max} Maximum rated power supply current with V_{max} applied

I_{OH} Output high current

I_{OL} Output low current

I_{OLB} Output low current of buffer stage of 4-Input AND Driver

I_{PDH} Power supply drain with the inputs high

I_{PDL} Power supply drain with the inputs low

I_R Reverse current of input diodes with V_R applied. Also shown are 2 I_R, 4 I_R, 5 I_R, etc., which indicate input loading factor times I_R.

I_{RCP} Reverse current of clock input diodes. Shown as 2 I_{RCP} for inputs with loading factor of 2.

I_{SC} Short circuit current obtained from device output when one or more inputs are low

LV_{CE} Output latch voltage

PW Pulse Width

t_f Fall time

t_r Rise time

t_{pd+} Propagation delay time with the output transistor turning off

t_{pd-} Propagation delay time with the output transistor turning on

TP_{in} Test point at input of unit under test

TP_{out} Test point at output of unit under test

V_{CC} Power supply voltage

V_{CCH} High power supply voltage

V_{CCL} Low power supply voltage

V_{CEX} Output transistor collector-to-emitter voltage

V_{CPTH} Clock threshold voltage

V_F Forward voltage test condition when testing forward current of input diodes

V_{FD} Forward voltage drop limit for expander diodes

V_{IH} Voltage for high input voltage state

V_{IL} Voltage for low input voltage state

V_{max} Maximum rated power supply voltage (V_{CC})

V_{OH} Output high voltage with I_{OH} flowing out of pin

V_{OHB} Output high voltage of buffer stage of 4-Input AND Driver

V_{OL} Output low voltage with I_{OL} flowing into pin

V_{OLB} Output low voltage of buffer stage of 4-Input AND Driver

V_{OX} Output voltage test condition when testing I_{CEX} for 4-Input AND Driver

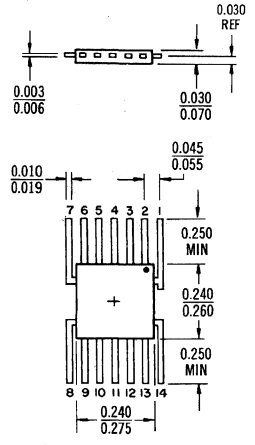
V_R Reverse voltage for input diode leakage test

V_X Low voltage utilized in testing expander inputs

PACKAGING

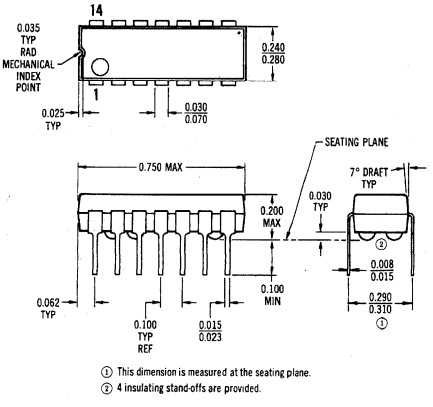
Devices with "F" suffix to the type number are in the TO-86 flat package (case 83); those with "G" suffix are in the TO-100 metal can (case 96A); those with "P" suffix are in the dual in-line plastic package (case 93).

CASE 83 (TO-86)

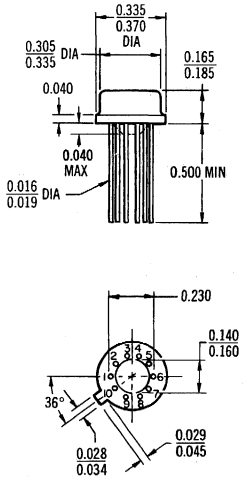


Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

CASE 93 (TO-116)



CASE 96A (TO-100)



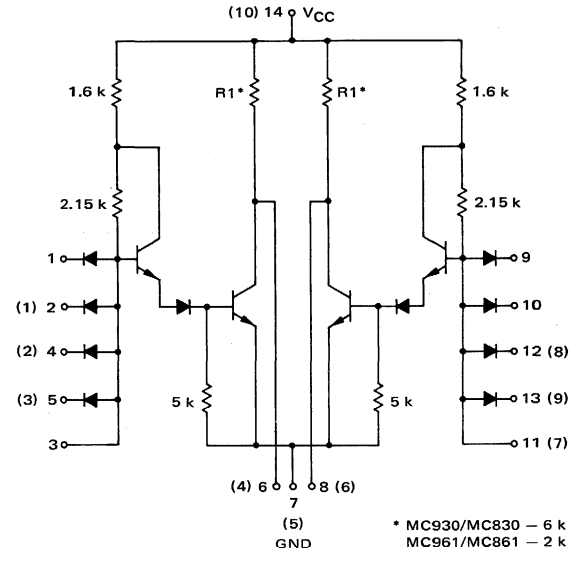
EXPANDABLE DUAL 4-INPUT GATES

MC930F · MC830F, P
MC961F · MC861F, P

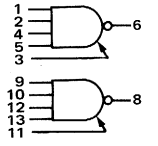
EXPANDABLE DUAL 3-2 INPUT GATES

MC930G · MC830G
MC961G · MC861G

This gate element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input NAND gate circuits. Since the metal can (G suffix) has only 10 pins, that circuit consists of one 3-input and one 2-input expandable gate. The elements may be cross-coupled to form a bistable multivibrator, or the outputs may be connected in parallel to perform the logic "OR" function.



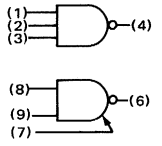
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC930F/MC830F, P
MC961F/MC861F, P

Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5 + [3]}$



MC930G/MC830G
MC961G/MC861G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

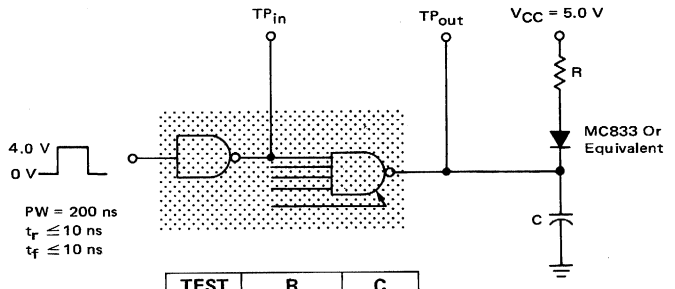
Input Loading Factor = 1

Output Loading Factor:
MC930/MC830 = 8
MC961/MC861 = 7

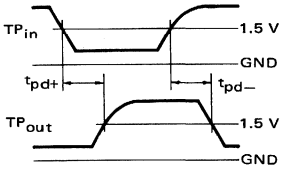
Total Power Dissipation:
MC930/MC830 = 22 mW typ/pkg
MC961/MC861 = 33 mW typ/pkg

Propagation Delay Time
MC930/MC830 = 30 ns typ
MC961/MC861 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

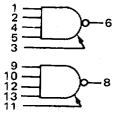


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	–	1	–	2	3	4	5	6	–	–	7	8	9	10



@ Test Temperature		I_{OL} mA		I_{OH} mA		V_{IL} Volts	V_{IH} Volts	V_X Volts	V_F Volts	V_R Volts	V_{CEX} Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{max} Volts
		MC930	MC961	MC930	MC961										
MC930, MC961	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-
		MC830	MC861	MC830	MC861										
MC830, MC861	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC930, MC961 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC830, MC861 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	1	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		2	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		4	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		5	-	-	-	-	-	-		-	-	
				-		-		-			-		-		-		-		-	-	3	-	-	-	-		-	-	
Short-Circuit Current																													
MC930/MC830	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
MC961/MC861		6	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-	-		-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-		-		-			-		-		-			-	-	-	-	-	2	1,4,5	-	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,5	-	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	5	1,2,4	-	-	-		-	
Power Drain Current (Total Device)																													
MC930/MC830	I_{PDH}	14	-	-	-	6.5	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
MC961/MC861	I_{PDH}	14	-	-	-	10.7	-	-		-	-	-	13.1	-	-		-	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	5.5	-	-		-	-	-	8.0	-	-		-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
MC930/MC830	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-	-		-	-	-	
MC961/MC861	t_{pd+}	1,6	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-	-		-	-	-	
	t_{pd-}	1,6	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-	-		-	-	-	

Pins not listed are left open.

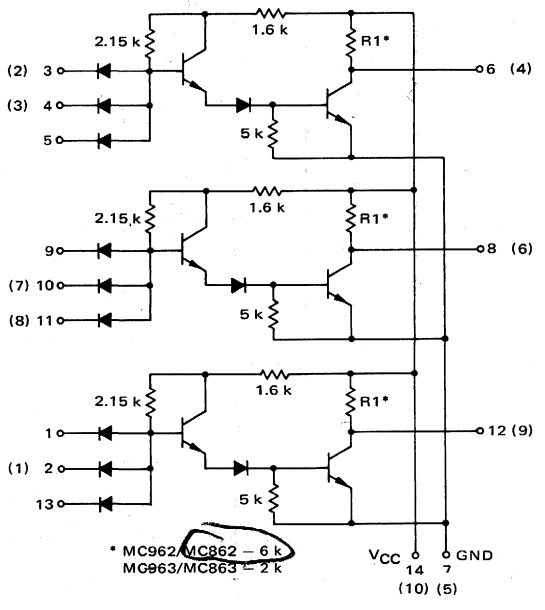
TRIPLE 3-INPUT GATES

MC962F · MC862F, P
MC963F · MC863F, P

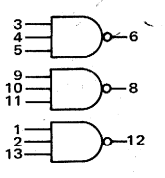
DUAL 2-INPUT GATES PLUS INVERTER

MC962G · MC862G
MC963G · MC863G

This gate element, in the 14-pin flat and dual in-line packages, consists of three 3-input NAND gate circuits. Since the metal can (G suffix) has only 10 pins, that circuit consists of two 2-input gates and one inverter.



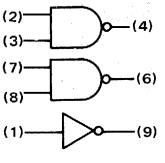
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC962F/MC862F,P
MC963F/MC863F,P

Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Negative Logic: $6 = \overline{3 + 4 + 5}$



MC962G/MC862G
MC963G/MC863G

Positive Logic: $4 = \overline{2 \cdot 3}$

Negative Logic: $4 = \overline{2 + 3}$

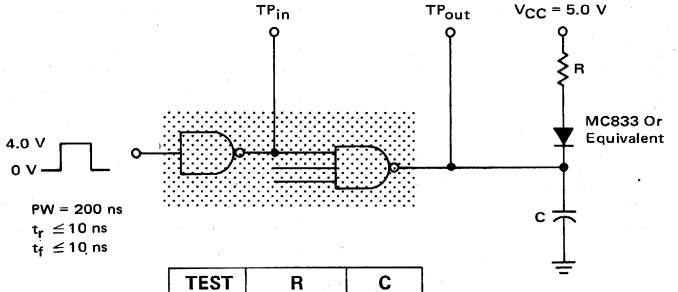
Input Loading Factor = 1

Output Loading Factor:
- MC962/MC862 = 8
- MC963/MC863 = 7

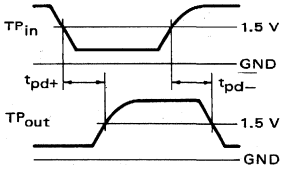
Total Power Dissipation:
- MC962F/MC862F, P = 33 mW typ/pkg
- MC962G/MC862G = 30 mW typ/pkg
- MC963F/MC863F, P = 50 mW typ/pkg
- MC963G/MC863G = 45 mW typ/pkg

Propagation Delay Time
- MC962/MC862 = 30 ns typ
- MC963/MC863 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

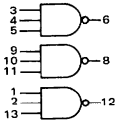


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	–	1	2	3	–	4	5	6	–	7	8	9	–	10



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES														
		mA				Volts										
		I_{OL}		I_{OH}												
		MC962	MC963	MC962	MC963	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}		
MC962, MC963	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-		
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00		
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-		
		MC862	MC863	MC862	MC863											
MC862, MC863	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-		
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00		
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-		

Characteristic	Symbol	Pin Under Test	MC962, MC963 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC862, MC863 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	3,4,5	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	3	-	-	-	-	-		-	-	
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	↓	4	-	-	-	-	-	↓	-	-	↓
				-		-		-			-		-		-		-		5	-	-	-	-	-		-	-	
Short-Circuit Current																												
MC962/MC862	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	3,6,7
MC963/MC863		6	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	3,6,7
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	-	14	-	4,5,7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	-	↓	-	3,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-	-		-	3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	6,14	-	-	-	-	3,7
Forward Current	I_F	3	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	3	4,5	-	-	-	14	-	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	4	3,5	-	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5	3,4	-	-	-		-	
Power Drain Current (Total Device)																												
MC962/MC862	I_{PDH}	14	-	-	-	9.75	-	-	mAdc	-	-	-	12	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC963/MC863	I_{PDH}	14	-	-	-	16	-	-	↓	-	-	-	19.6	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	8.25	-	-	↓	-	-	-	12	-	-	↓	-	-	-	-	-	-	-	-	-	-	14	3,7,9,13
Switching Times																	Pulse In	Pulse Out										
MC962/MC862	t_{pd+}	3,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	3	6	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	3,6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC963/MC863	t_{pd+}	3,6	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-		-	-	-	
	t_{pd-}	3,6	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓

Pins not listed are left open.

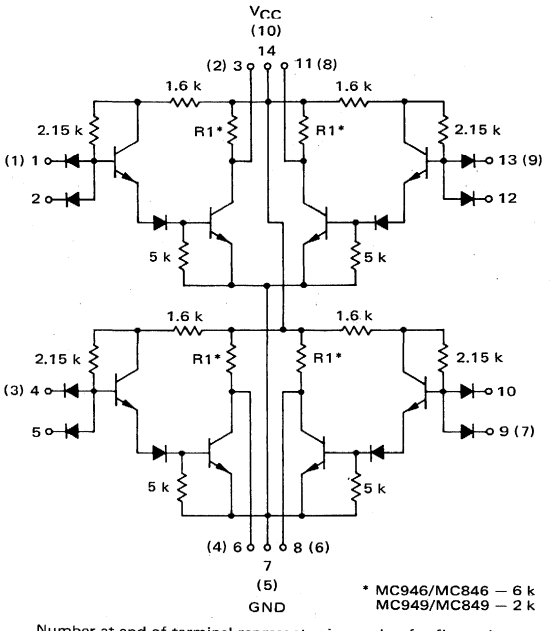
QUAD 2-INPUT GATES

MC946F · MC846F, P
MC949F · MC849F, P

QUAD INVERTERS

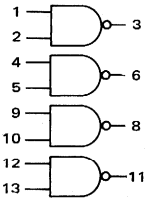
MC946G · MC846G
MC949G · MC849G

This gate element, in the 14-pin flat and dual in-line packages, consists of four 2-input NAND gate circuits. This circuit can be used as a dual 2-input non-inverting gate, or as two bistable circuits when two dual 2-input gates are cross-coupled. Since the metal can (G suffix) has only 10 pins, that circuit consists of four inverters.



* MC946/MC846 — 6 k
MC949/MC849 — 2 k

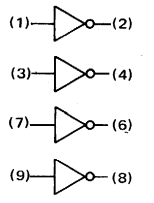
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC946F/MC846F, P
MC949F/MC849F, P

Positive Logic: $3 = \overline{1 \cdot 2}$

Negative Logic: $3 = \overline{1 + 2}$



MC946G/MC846G
MC949G/MC849G

Positive Logic: $2 = \overline{1}$

Negative Logic: $2 = \overline{1}$

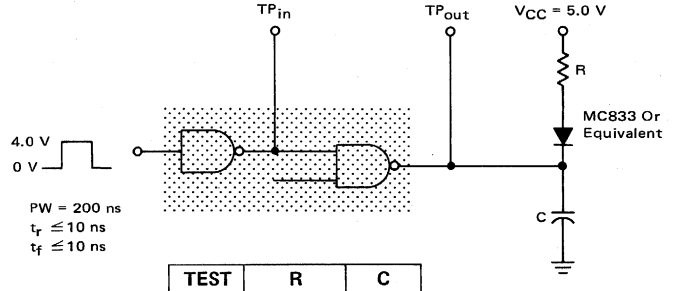
Input Loading Factor = 1

Output Loading Factor:
MC946/MC846 = 8
MC949/MC849 = 7

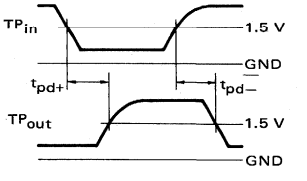
Total Power Dissipation:
MC946/MC846 = 44 mW typ/pkg
MC949F/MC849F, P = 66 mW typ/pkg
MC949G/MC849G = 60 mW typ/pkg

Propagation Delay Time:
MC946/MC846 = 30 ns typ
MC949/MC849 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

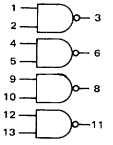


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	–	2	3	–	4	5	6	7	–	8	–	9	10

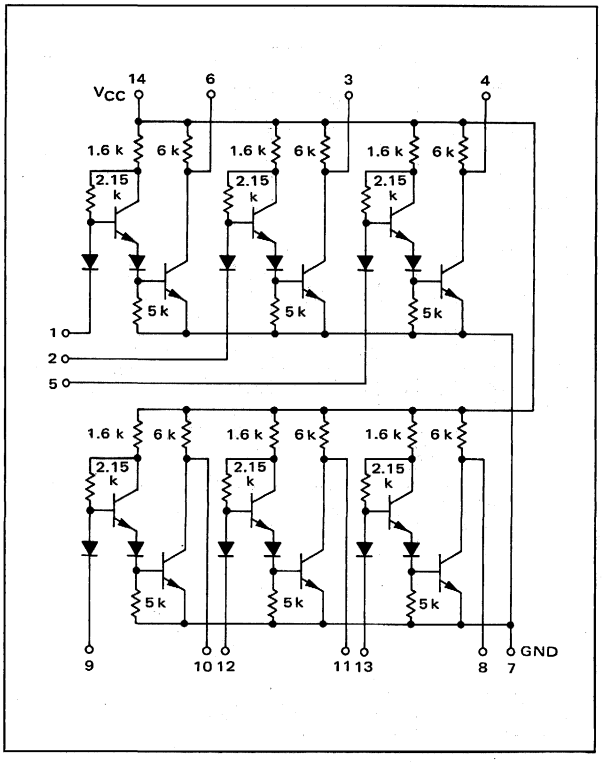


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
		mA				Volts									
		I_{OL}		I_{OH}											
		MC946	MC949	MC946	MC949	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC946, MC949	−55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-	
	+25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-	
		MC846	MC849	MC846	MC849										
MC846, MC849	0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-	

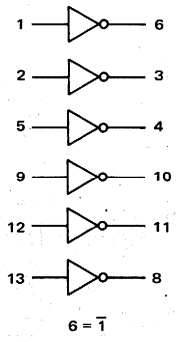
Characteristic	Symbol	Pin Under Test	MC946, MC949 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC846, MC849 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	-	1,2	-	-	-	-	14	-	-	7
	V_{OH}	3	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	3	1	-	-	-	-	-	↓	-	-	↓
		3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	2	-	-	-	-	-		-	-	
Short-Circuit Current																												
MC946/MC846	I_{SC}	3	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,3,7
MC949/MC849		3	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,3,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,7
		2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	2	-	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	3,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	2	-	-	-	14	-	7
		2	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	2	1	-	-	-	14	-	7
Power Drain Current (Total Device)																												
MC946/MC846	I_{PDH}	14	-	-	-	13	-	-	mAdc	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC949/MC849	I_{PDH}	14	-	-	-	21.4	-	-	↓	-	-	-	26.2	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	11	-	-		-	-	-	16	-	-		-	-	-	-	-	-	-	-	-	-	14	1,4,7,9,12
Switching Times																	Pulse In	Pulse Out										
MC946/MC846	t_{pd+}	1,3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	3	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,3	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC949/MC849	t_{pd+}	1,3	-	-	15	60	-	-		-	-	15	60	-	-				-	-	-	-	-		-	-	-	
	t_{pd-}	1,3	-	-	10	30	-	-		-	-	10	30	-	-				-	-	-	-	-		-	-	-	

Pins not listed are left open.

MC934F · MC834F, P

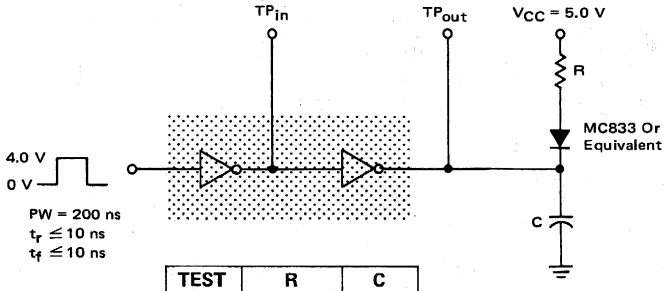


This element consists of six inverter circuits.

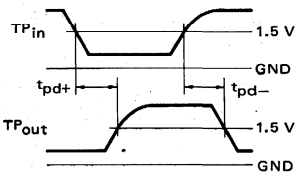


Input Loading Factor = 1
Output Loading Factor = 8
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 30 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

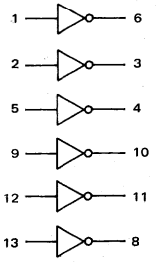


TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

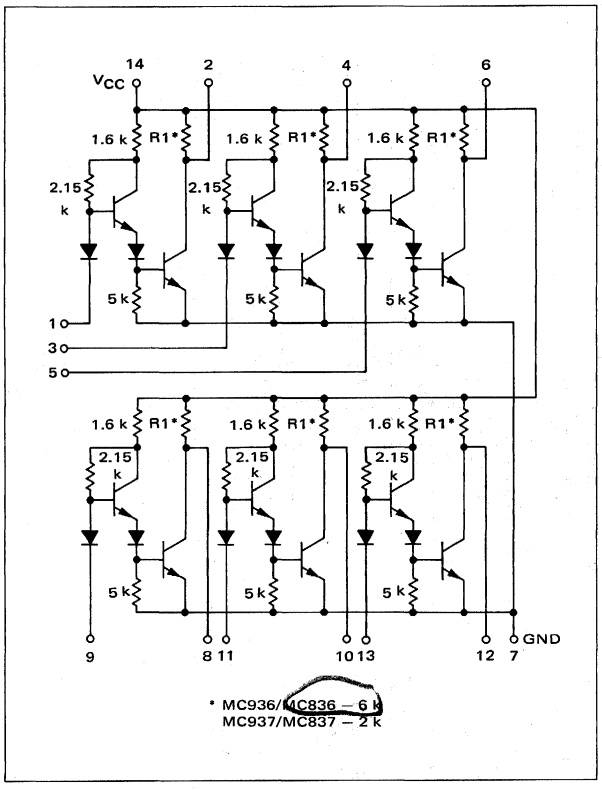


@ Test Temperature		TEST CURRENT / VOLTAGE VALUES											
		mA		Volts									
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC934	−55°C	11.4	-0.12	1.40	2.10	0	4.00	-	-	4.50	5.50	-	
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	-	-	4.50	5.50	-	
MC834	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-	

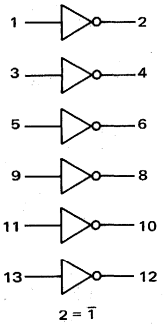
Characteristic	Symbol	Pin Under Test	MC934 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC834 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-	Vdc	2.60	-	2.60	-	2.50	-	Vdc	-	6	1	-	-	-	-	-	14	-	-	7
Short-Circuit Current	I_{SC}	6	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	19.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	16.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,2,5,7, 9,12,13
Switching Times																	Pulse In	Pulse Out										
	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	30	-	-	ns	-	-	10	30	-	-	ns	1	6	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

MC936F · MC836F, P
MC937F · MC837F, P



This element consists of six inverter circuits.



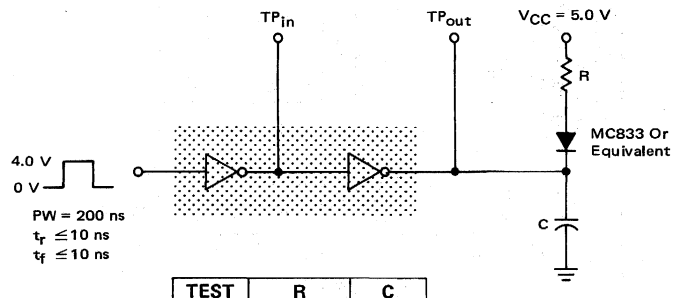
Input Loading Factor = 1

Output Loading Factor:
MC936/MC836 = 8
MC937/MC837 = 7

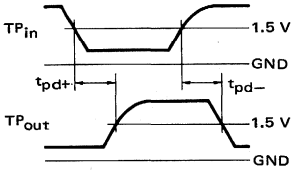
Total Power Dissipation
MC936/MC836 = 66 mW typ/pkg
MC937/MC837 = 90 mW typ/pkg

Propagation Delay Time
MC936/MC836 = 30 ns typ
MC937/MC837 = 25 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

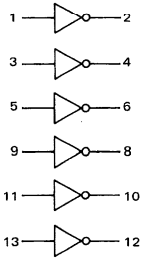


TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



@ Test Temperature	TEST CURRENT / VOLTAGE VALUES												
	mA				Volts								
	I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
	MC936	MC937	MC936	MC937									
MC936, MC937 −55°C	11.4	10.4	-0.12	-0.5	1.40	2.10	0	4.00	-	-	4.50	5.50	-
MC936, MC937 +25°C	12.0	11.0	-0.12	-0.5	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
MC936, MC937 +125°C	10.8	9.8	-0.12	-0.5	0.80	2.00	0	4.00	-	-	4.50	5.50	-
	MC836	MC837	MC836	MC837									
MC836, MC837 0°C	12.0	11.0	-0.12	-0.5	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
MC836, MC837 +25°C	12.0	11.0	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
MC836, MC837 +75°C	11.4	10.4	-0.12	-0.5	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC936, MC937 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC836, MC837 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	2	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	2	-	-	1	-	-	-	-	14	-	-	7
	V_{OH}	2	2.50	-	2.60	-	2.50	-	Vdc	2.60	-	2.60	-	2.50	-	Vdc	-	2	1	-	-	-	-	-	14	-	-	7
Short-Circuit Current																												
MC936/MC836	I_{SC}	2	-	-1.34	-	-1.34	-	-1.30	mAdc	-	-1.30	-	-1.30	-	-1.25	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,7
MC937/MC837		2	-	-4.00	-	-4.00	-	-3.90	mAdc	-	-3.90	-	-3.90	-	-3.75	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	2,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)																												
MC936/MC836	I_{PDH}	14	-	-	-	19.5	-	-	mAdc	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
MC937/MC837	I_{PDH}	14	-	-	-	32.0	-	-	↓	-	-	-	39	-	-	↓	-	-	-	-	-	-	-	14	-	-	-	7
All Types	I_{max}	14	-	-	-	16.5	-	-	↓	-	-	-	24	-	-	↓	-	-	-	-	-	-	-	-	-	-	14	1,3,5,7, 9,11,13
Switching Times																	Pulse In	Pulse Out										
MC936/MC836	t_{pd+}	1,2	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	2	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,2	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
MC937/MC837	t_{pd+}	1,2	-	-	15	60	-	-	↓	-	-	15	60	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓
	t_{pd-}	1,2	-	-	10	30	-	-	↓	-	-	10	30	-	-	↓	↓	↓	-	-	-	-	-	↓	-	-	-	↓

Pins not listed are left open.

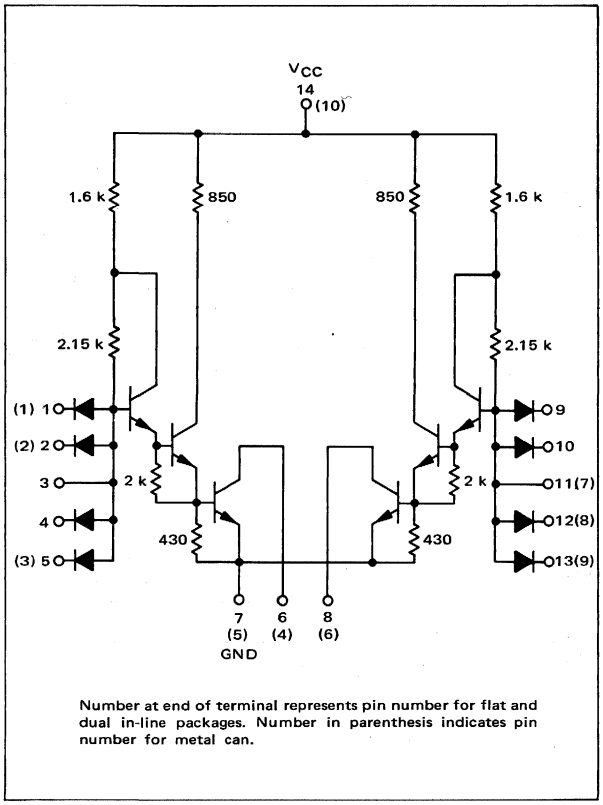
EXPANDABLE DUAL 4-INPUT POWER GATES

MC944F • MC844F, P

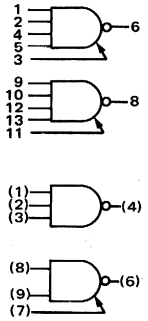
EXPANDABLE DUAL 3-2 INPUT POWER GATES

MC944G • MC844G

The MC944/MC844 is a dual NAND power gate with an output transistor capable of sinking more current than standard gate elements. It is useful as a high fan-out gate (with an external pull-up resistor), and as a line, relay, or lamp driver. Each output of the MC944/MC844 is capable of sinking up to 100 mA individually (90 mA if both outputs are conducting simultaneously) provided that temperature extremes are limited to 0°C to +100°C for MC944, and +15°C to +55°C for MC844. The typical breakdown voltage of the output transistor is greater than 12 V.



Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC944F/MC844F, P

Positive Logic:

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic:

$6 = \overline{1 + 2 + 4 + 5 + [3]}$

MC944G/MC844G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

Input Loading Factor = 1
Output Loading Factor = 27
Total Power Dissipation = 65 mW typ/pkg
Propagation Delay Time = 30 ns typ

OPERATING RULES

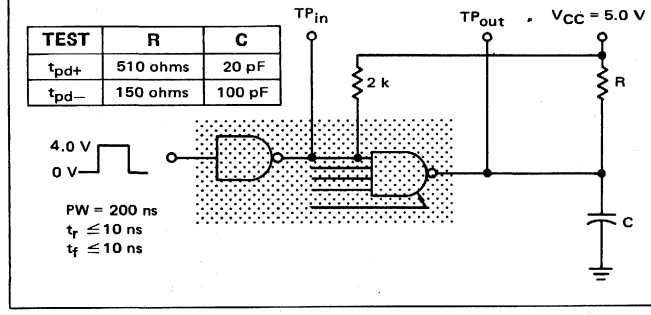
- The outputs of the Dual Power Gate may be tied together to perform the wired-collector OR function.
- An external load resistor should be utilized with the Dual Power Gate. At V_{CC} = 5.0 ±0.5 V, subtract the following output loads:

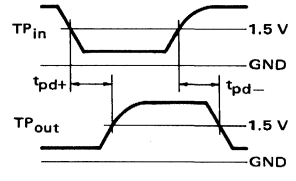
R
2 kΩ – 2 loads
1 kΩ – 4 loads
510 Ω – 8 loads

- For increased current capability, the inputs and outputs of ½MC944 and ½MC932 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	510 ohms	20 pF
t_{pd-}	150 ohms	100 pF



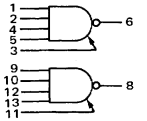


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate.
The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	-	-	3	4	5	6	-	-	7	8	9	10



@ Test Temperature		I_{OL} (mA)	I_{CE} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_X (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	V_{max} (Volts)
MC944	−55°C	36	-	-	2.10	-	0	4.00	-	-	4.50	5.50	-
	+25°C	40	5.00	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	36	-	-	2.00	-	0	4.00	-	-	4.50	5.50	-
MC844	0°C	40	-	-	2.00	-	0.45	4.00	-	-	5.00	5.00	-
	+25°C	40	5.00	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	36	-	-	1.80	-	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC944 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC844 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{CE}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
Output Breakdown Voltage	LV_{CE}	6	-	-	6.0	-	-	-	Vdc	-	-	6.0	-	-	-	Vdc	-	6	-	-	-	-	-	-	-	-	14	-	1,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	2	-	-	-	↓	-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	µAdc	-	-	-	100	-	-	µAdc	-	-	1	-	-	-	-	6	-	-	14	-	7
			-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	-	-	2	-	-	-	-	↓	-	-	↓	-	↓
			-	-	-		-	-		-	-	-		-	-		-	-	4	-	-	-	-		-	-		-	
			-	-	-		-	-		-	-	-		-	-		-	-	5	-	-	-	-		-	-		-	
			-	-	-		-	-		-	-	-		-	-		-	-	-	-	3	-	-		-	-		-	
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	2	1,4,5	-	-	-	↓	-	↓
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,5	-	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	5	1,2,4	-	-	-		-	
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	20	-	-	mAdc	-	-	-	22.5	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
	t_{pd+}	1,6	-	-	15	50	-	-	ns	-	-	15	50	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	10	35	-	-	ns	-	-	10	35	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

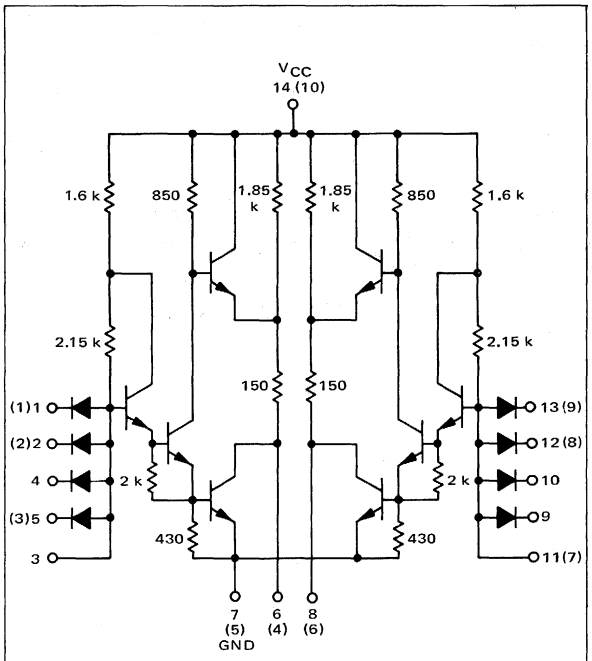
EXPANDABLE DUAL 4-INPUT BUFFERS

MC932F • MC832F, P

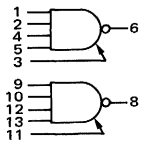
EXPANDABLE DUAL 3-2 INPUT BUFFERS

MC932G • MC832G

This buffer element, in the 14-pin flat and dual in-line packages, consists of two expandable 4-input inverting drivers. Since the metal can (G suffix) has only 10 pins, this circuit consists of one 3-input and one 2-input expandable inverting driver. These units are designed especially for driving large capacitive loads at high speeds. An output emitter follower in series with a 150-ohm resistor drives the output to the high voltage level. A low saturation resistance transistor is turned on, pulling the output down to the low voltage level, and providing rapid discharge of capacitive loads.



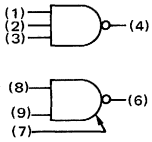
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.



MC932F/MC832F, P

Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Negative Logic: $6 = \overline{1 + 2 + 4 + 5 + [3]}$



MC932G/MC832G

Positive Logic: $4 = \overline{1 \cdot 2 \cdot 3}$

Negative Logic: $4 = \overline{1 + 2 + 3}$

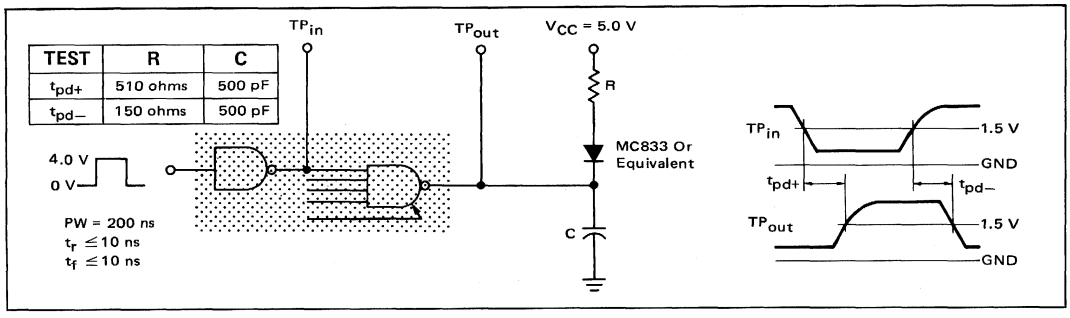
Input Loading Factor = 1
Output Loading Factor = 25
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 35 ns typ

OPERATING RULES

- The outputs of the Dual Buffer may not be tied together.
- For increased current capability, the inputs and outputs of ½MC932 and ½MC944 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	510 ohms	500 pF
t_{pd-}	150 ohms	500 pF

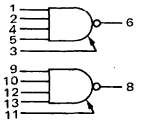


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER													
Flat/Dual In-Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Metal Can	1	2	–	–	3	4	5	6	–	–	7	8	9	10

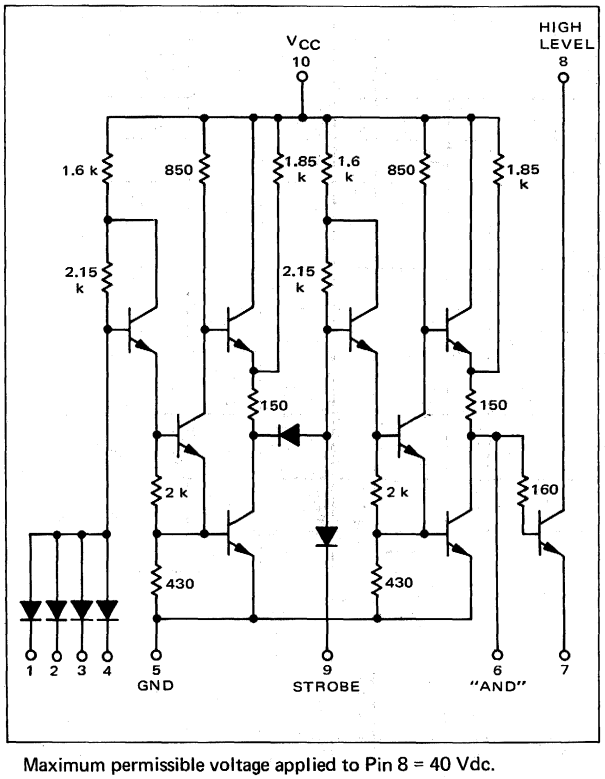


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES													
		mA		Volts											
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC932	−55°C	34	-2.00	1.40	2.10	-	0	4.00	-	-	4.50	5.50	-	
	+25°C	36	-2.50	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	8.00	
	+125°C	32	-4.00	0.80	2.00	-	0	4.00	-	-	4.50	5.50	-	
MC832	0°C	36	-2.00	1.20	2.00	-	0.45	4.00	-	-	5.00	5.00	-	
	+25°C	36	-2.50	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	34	-3.00	0.95	1.80	-	0.50	4.00	-	-	5.00	5.00	-	

Characteristic	Symbol	Pin Under Test	MC932 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC832 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_X	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	-	7
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	1	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		2	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		4	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		5	-	-	-	-	-	-	-	-	-	
				-		-		-			-		-		-		-		-	-	3	-	-	-	-	-	-	-	
Short-Circuit Current	I_{SC}	6	-16	-	-18	-	-16	-	mAdc	-15	-	-16	-	-14	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	1,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	-	14	-	2,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-	-		-	1,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-	-		-	1,2,5,7
		5	-		-		-			-		-		-			-	-	-	-	-	-	5	-	-	-		-	1,2,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,4,5	-	-	-	14	-	7
		2	-		-		-			-		-		-			-	-	-	-	-	2	1,4,5	-	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,5	-	-	-		-	
		5	-		-		-			-		-		-			-	-	-	-	-	5	1,2,4	-	-	-		-	
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	26.6	-	-	mAdc	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	1,7,9
Switching Times																	Pulse In	Pulse Out											
	t_{pd+}	1,6	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,6	-	-	15	40	-	-	ns	-	-	15	40	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	-	7

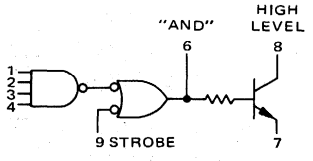
Pins not listed are left open.

MC943G • MC843G



Maximum permissible voltage applied to Pin 8 = 40 Vdc.

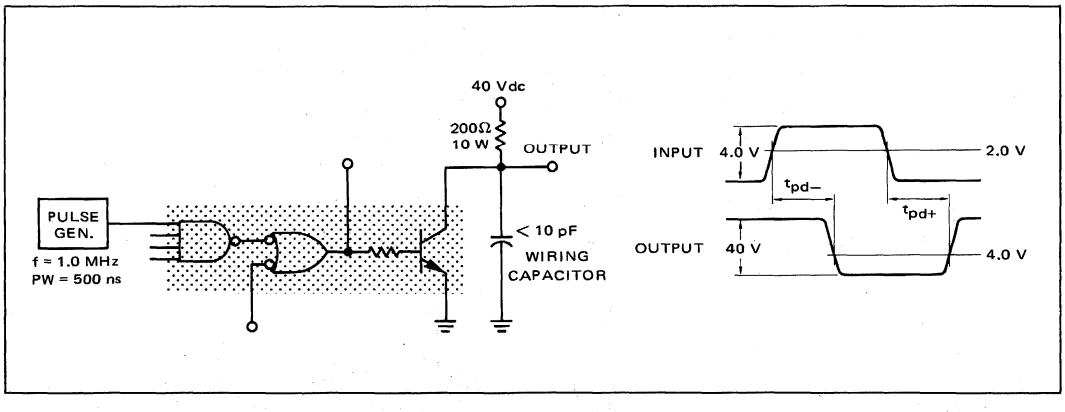
This device is a monolithic dual buffer element in a hybrid configuration with a high performance NPN silicon transistor to allow the output stage to operate to 40 volts with sink current capability of 250 mA. The device may also be used in conjunction with other saturated logic forms.



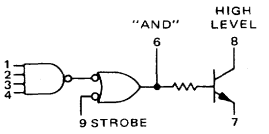
Positive Logic: $\overline{8} = 1 \cdot 2 \cdot 3 \cdot 4 + \overline{9}$
Negative Logic: $\overline{8} = (1 + 2 + 3 + 4)\overline{9}$

Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 80 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

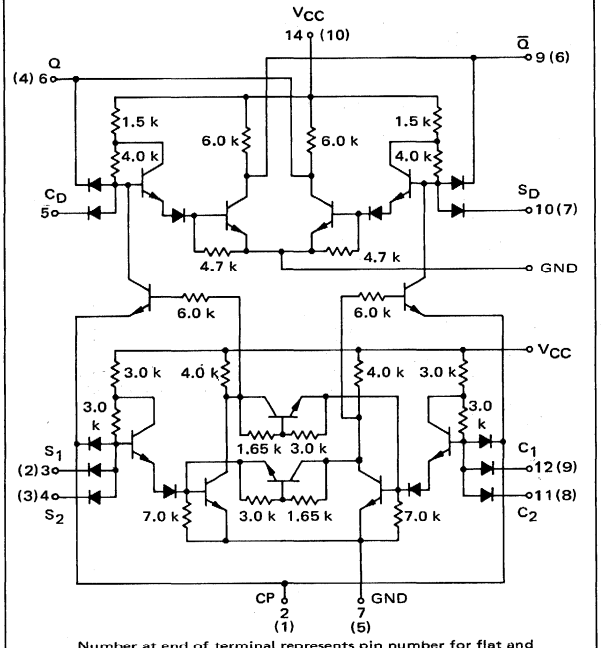


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES											
		mA		Volts									
		I_{OL}	I_{OLB}	V_{IL}	V_{IH}	V_{OX}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
MC943	−55°C	250	34	1.40	2.10	40	0	4.00	-	5.00	5.50	-	
MC943	+25°C	250	36	1.10	2.00	40	0	4.00	5.00	5.00	5.50	8.00	
MC943	+125°C	250	32	0.80	2.00	40	0	4.00	-	5.00	5.50	-	
MC843	0°C	250	36	1.20	2.00	40	0.45	4.00	-	5.00	5.00	-	
MC843	+25°C	250	36	1.10	.90	40	0.45	4.00	5.00	5.00	5.00	8.00	
MC843	+75°C	250	34	0.95	1.80	40	0.50	4.00	-	5.00	5.00	-	

Characteristic	Symbol	Pin Under Test	MC943 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC843 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OLB}	V_{IL}	V_{IH}	V_{OX}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	8	-	0.50	-	0.50	-	0.50	Vdc	-	0.50	-	0.50	-	0.50	Vdc	8	-	-	1,2,3,4	-	-	-	-	10	-	-	5,7
		8	-	0.50	-	0.50	-	0.50		-	0.50	-	0.50	-	0.50		8	-	1,2,3,4,9	-	-	-	-	-		-	-	
	V_{OLB}	6	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		-	6	1	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		2	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		3	-	-	-	-	-		-	-	
			-		-		-			-		-		-			-		4	-	-	-	-	-		-	-	
	V_{OHB}	6	2.20	-	2.00	-	1.80	-		2.00	-	2.00	-	1.90	-		-	-	-	1,2,3,4	-	-	-	-		-	-	
		6	2.20	-	2.00	-	1.80	-		2.00	-	2.00	-	1.90	-		-	-	1,2,3,4,9	-	-	-	-	-		-	-	
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	-	1	-	-	10	-	2,3,4,5,7
		2	-		-		-			-		-		-			-	-	-	-	-	-	2	-	-		-	1,3,4,5,7
		3	-		-		-			-		-		-			-	-	-	-	-	-	3	-	-		-	1,2,4,5,7
		4	-		-		-			-		-		-			-	-	-	-	-	-	4	-	-		-	1,2,3,5,7
		9	-		-		-			-		-		-			-	-	-	-	-	-	9	-	-		-	5,7
Output Leakage Current	I_{CEX}	8	-	5.0	-	5.0	-	200	μAdc	-	10	-	10	-	200	μAdc	-	-	-	-	8	-	-	-	10	-	-	1,5,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	-	1	2,3,4	-	-	10	-	5,7
		2	-		-		-			-		-		-			-	-	-	-	-	2	1,3,4	-	-		-	
		3	-		-		-			-		-		-			-	-	-	-	-	3	1,2,4	-	-		-	
		4	-		-		-			-		-		-			-	-	-	-	-	4	1,2,3	-	-		-	
		9	-		-		-			-		-		-			-	-	-	-	-	9	-	-	-		-	
Power Drain Current	I_{PDH}	10	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	10	-	-	-	5,7
	I_{max}	10	-	-	-	6.0	-	-	mAdc	-	-	-	8.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	10	1,5,9
Switching Times																	Pulse In	Pulse Out										
	t_{pd-}	1, 8	-	-	-	100	-	-	ns	-	-	-	140	-	-	ns	1	8	-	-	-	-	-	10	-	-	-	5,7
	t_{pd+}	1, 8	-	-	-	150	-	-	ns	-	-	-	230	-	-	ns	1	8	-	-	-	-	-	10	-	-	-	5,7

Pins not listed are left open.

MC931F, G · MC831F, P, G

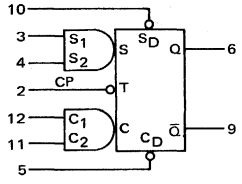


Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

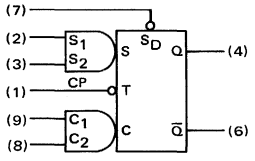
This clocked flip-flop consists of two directly coupled flip-flops, operating on the "master-slave" principle. Operation depends only on voltage levels, and the shape of the input clock becomes unimportant in determining the state of this flip-flop. The input information is stored in the "master" flip-flop when the clock voltage is high, and is transferred to the "slave" when the clock voltage is low.

This clocked flip-flop can be operated in either the R-S or J-K mode. For J-K operation the Q output is connected to a clear input, and the $\overline{Q}$ output is connected to a set input. Direct set (S_D) and direct clear (C_D) inputs are available.

MC931F/MC831F, P



MC931G/MC831G



SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)

1 – High State (more positive)

X – State of the input does not affect the state of the circuit.

U – Indeterminate State

J-K TRUTH TABLE

(Connect S_2 to $\overline{Q}$, C_2 to Q)

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

Input Loading Factor:
S and C = 2/3
S_D and C_D = 3/4
T = 2

Output Loading Factor = 7

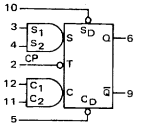
Total Power Dissipation = 55 mW typ/pkg

Propagation Delay Time = 40 ns typ

ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBERS												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	–	14
Metal Can	–	1	2	3	–	4	5	–	6	7	8	9	–	10



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC931	−55°C	10.0	-0.12	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	10.6	-0.12	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	9.5	-0.12	0.80	2.00	0	4.00	-	4.50	5.50	-
MC831	0°C	10.5	-0.12	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	10.5	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	10.2	-0.12	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC931 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC831 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	CP_c§	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	-	-	-	-	14	-	-	-	2	-	3,7,9‡
		9	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		9	-	-	-	-	-	-		-	-	-	2	-	6‡,7,12
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6†	11	3,4	-	-	-		-	-	2	-	-	7
				-		-		-			-		-		-		-	6†	12	3,4	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	6	10	5	-	-	-		-	-		-	-	3,4,7
		9		-		-		-			-		-		-		-	9†	3	11,12	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	9†	4	11,12	-	-	-		-	-		-	-	7
				-		-		-			-		-		-		-	9	5	10	-	-	-		-	-		-	-	7,11,12
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	14	-	-	-	-	2,7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	-	2,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-		-	2	-	-	3,4,7
		10	-		-		-			-		-		-			-	-	-	-	-	10	-	-		-	2	-	-	7,11,12
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	-	2,7
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	-	2,7
	I_{RCP}	2	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	-	-	2	-	-		-	-	-	-	3,4,7,11,12
Forward Current	2/3 I_F	3	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	-	3	-	-	14	-	-	-	-	7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	-	
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	-	
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	-	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	4	-	-	-	-	-		-	-	-	2	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	11	-	-	-	-	-		-	-	-	2	
	I_{FS}	5	-	-1.20	-	-1.20	-	-1.10		-	-1.05	-	-1.05	-	-1.00		-	-	-	-	5	-	-	-		-	-	-	-	4,7,9,10
	I_{FS}	10	-	-1.20	-	-1.20	-	-1.10		-	-1.05	-	-1.05	-	-1.00		-	-	-	-	10	-	-	-		-	-	-	-	5,6,7,11
Power Drain Current	I_{PDH}	14	-	-	-	11	-	-	mAdc	-	-	-	14	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	-	7
	I_{max}	14	-	-	-	14.5	-	-	mAdc	-	-	-	18	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	-	-	2,3,4,7, 11,12
Switching Times																	Pulse In	Pulse Out												
	t_{pd+}	2, 6	-	-	25	75	-	-	ns	-	-	25	75	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	-	7
	t_{pd-}	2, 6	-	-	35	75	-	-	ns	-	-	35	75	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	-	7

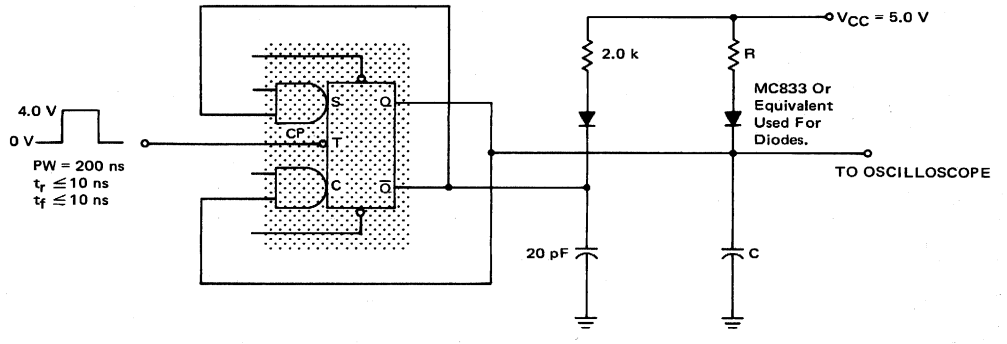
Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
CP_c = Clock Pulse c
} See Clock Pulse Waveforms.

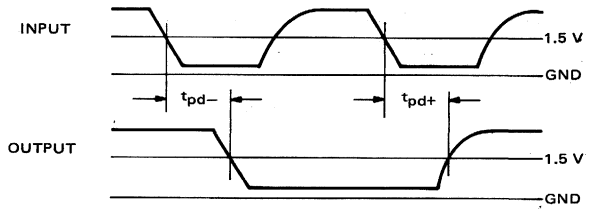
† Momentarily ground this terminal before applying -0.12 mA.

‡ Momentarily ground this terminal before applying I_{OL} to complementary terminal, i.e., terminal of opposite function.

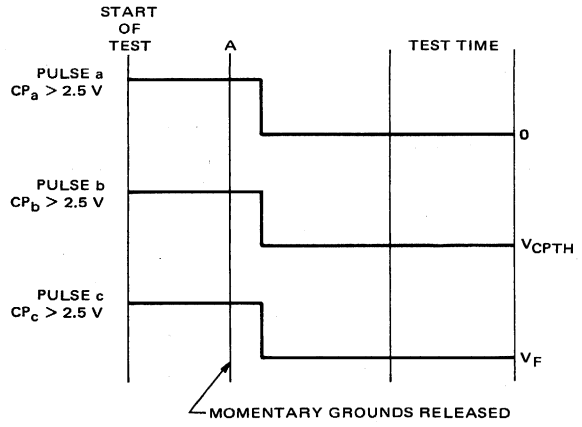
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



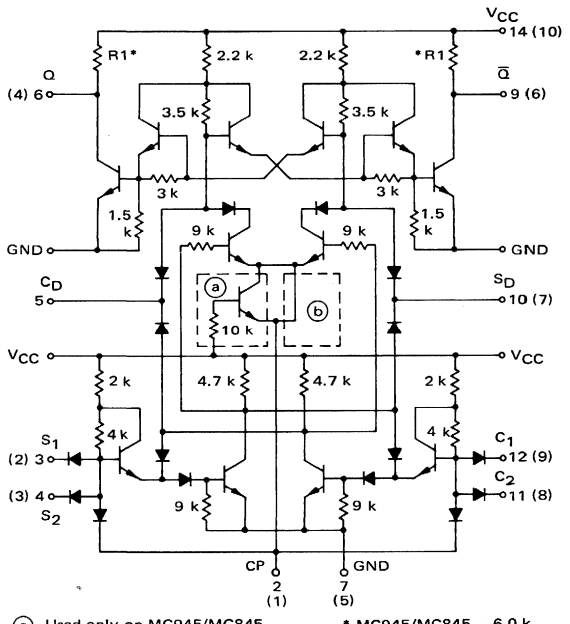
CLOCK PULSE WAVEFORMS
($t_f < 1.0\ \mu s$)



TEST CONDITIONS

	V_{CPTH}
	MC931
−55°C	1.10 V
+25°C	0.95 V
+125°C	0.75 V
	MC831
0°C	1.00 V
+25°C	0.95 V
+75°C	0.85 V

MC945F, G · MC845F, P, G
MC948F, G · MC848F, P, G



(a) Used only on MC945/MC845

(b) Used only on MC948/MC848

* MC945/MC845 – 6.0 k
MC948/MC848 – 2.0 k

Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

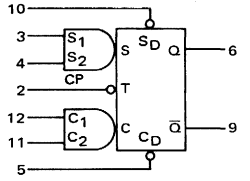
These clocked flip-flops consist of two directly coupled flip-flops, operating on the "master-slave" principle. The input information is stored in the "master" flip-flop when the clock voltage is high, and is transferred to the "slave" when the clock voltage is low.

This clocked flip-flop can be operated in either the R-S or J-K mode. For J-K operation the Q output is connected to a clear input, and the $\overline{Q}$ output is connected to a set input. Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs. No matter what other inputs are applied to the flip-flop, the direct set and clear inputs prevail.

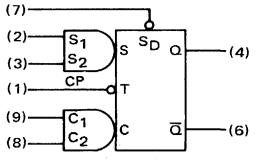
The outputs are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

The output pull-up resistor of the MC948/MC848 has been changed from that utilized in the MC945/MC845 in order to improve the propagation delay-versus-capacitance characteristics.

MC945F/MC845F, P
MC948F/MC848F, P



MC945G/MC845G
MC948G/MC848G



SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

0 – Low State (more negative)

1 – High State (more positive)

X – State of the input does not affect the state of the circuit.

U – Indeterminate State

J-K TRUTH TABLE

(Connect S_2 to $\overline{Q}$, C_2 to Q)

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

Input Loading Factor:
S and C = 2/3
S_D, C_D, T = 2

Output Loading Factor:
MC945 = 10
MC845 = 12
MC948 = 9
MC848 = 11

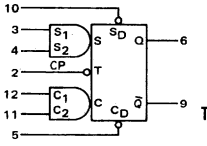
Total Power Dissipation:
MC945/MC845 = 60 mW typ/pkg
MC948/MC848 = 70 mW typ/pkg

Propagation Delay Time = 40 ns typ

ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	–	14
Metal Can	–	1	2	3	–	4	5	–	6	7	8	9	–	10



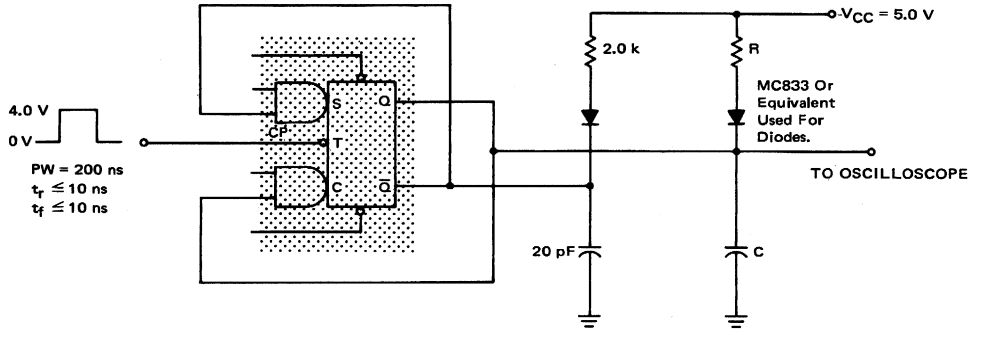
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES												
	mA				Volts								
	I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	
	MC945	MC948	MC945	MC948									
MC945, MC948 −55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-	
MC945, MC948 +25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00	
MC945, MC948 +125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-	
	MC845	MC848	MC845	MC848									
MC845, MC848 0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-	
MC845, MC848 +25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00	
MC845, MC848 +75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-	

Characteristic	Symbol	Pin Under Test	MC945, MC948 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC845, MC848 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	6	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	6	-	-	-	-	-	-	14	-	-	-	2	3,7
		9	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		9	-	-	-	-	-	-		-	-	-	2	7,12
	V_{OH}	6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	11	3,4	-	-	-		-	-	2	-	7
		↓		-		-		-			-		-		-		-	↓	12	3,4	-	-	-		-	-		-	7
				-		-		-			-		-		-		-		10	5	-	-	-		-	-		-	3,4,7
		9		-		-		-			-		-		-		-	9	3	11,12	-	-	-		-	-		-	7
		↓		-		-		-			-		-		-		-	↓	4	11,12	-	-	-		-	-		-	7
				-		-		-			-		-		-		-		5	10	-	-	-		-	-		-	7,11,12
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	3	-	-	14	-	-	-	2,7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	↓	-	-	-	2,7
		5	-		-		-			-		-		-			-	-	-	-	-	5	-	-		-	2	-	3,4,7
		10	-		-		-			-		-		-			-	-	-	-	-	10	-	-		-	2	-	7,11,12
		11	-		-		-			-		-		-			-	-	-	-	-	11	-	-		-	-	-	2,7
		12	-		-		-			-		-		-			-	-	-	-	-	12	-	-		-	-	-	2,7
	I_{RCP}	2	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	-	-	2	-	-		-	-	-	3,4,7,11,12
Forward Current	2/3 I_F	3	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	3	-	-	-	14	-	-	-	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	4	-	-	-	↓	-	-	-	↓
		11	-		-		-			-		-		-			-	-	-	-	11	-	-	-		-	-	-	
		12	-		-		-			-		-		-			-	-	-	-	12	-	-	-		-	-	-	
	I_{FCP}	2	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	5	-	2	-	-	-		-	-	-	7
	I_{FCP}	2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	10	-	2	-	-	-		-	-	-	7
	I_{FS}	5	-		-		-			-		-		-			-	-	-	-	5	-	-	-		-	-	-	3,7,10,12
	I_{FS}	10	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	10	-	-	-	↓	-	-	-	4,5,7,11
Power Drain Current																													
MC945/MC845	I_{PDH}	14	-	-	-	11	-	-	mAdc	-	-	-	14	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	14.5	-	-	↓	-	-	-	18	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	2,3,4,7,11,12
MC948/MC848	I_{PDH}	14	-	-	-	13.5	-	-		-	-	-	17	-	-		-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	19	-	-	↓	-	-	-	22.5	-	-	↓	-	-	-	-	-	-	-	-	-	14	-	-	2,3,4,7,11,12
Switching Times																	Pulse In	Pulse Out											
MC945/MC845	t_{pd+}	2,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	2	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	2,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓	↓	↓	-	-	-	-	↓	-	-	-	-	-	↓
MC948/MC848	t_{pd+}	2,6	-	-	25	75	-	-		-	-	25	75	-	-				-	-	-	-		-	-	-	-	-	
	t_{pd-}	2,6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓			-	-	-	-	↓	-	-	-	-	-	↓

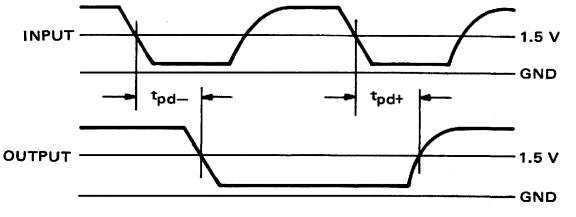
Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
} See Clock Pulse Waveforms.

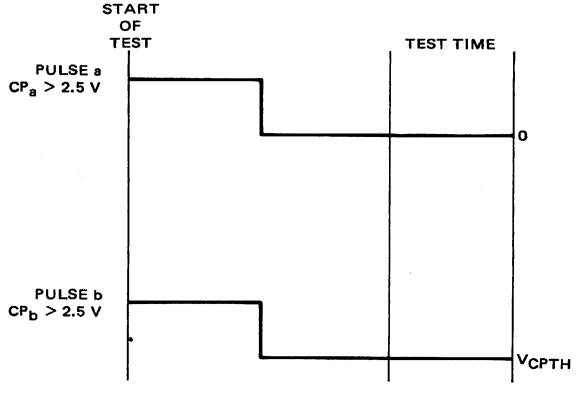
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



CLOCK PULSE WAVEFORMS
($t_f < 1.0\,\mu s$)



TEST CONDITIONS

	V_{CPTH}	
	MC945	MC948
−55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
	MC845	MC848
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V

MC952F · MC852F, P
MC953F · MC853F, P
MC955F · MC855F, P
MC956F · MC856F, P

Each section of the monolithic MC952/MC852 and MC953/MC853 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Operation depends only on voltage levels, so the rise and fall times of the input clock are unimportant in determining the state of the flip-flop. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

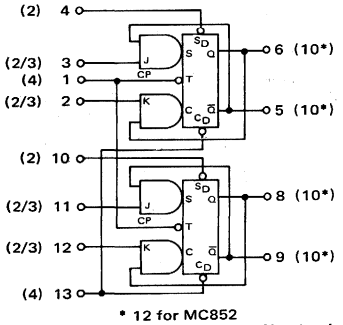
The MC952/MC852 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC953/MC853 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

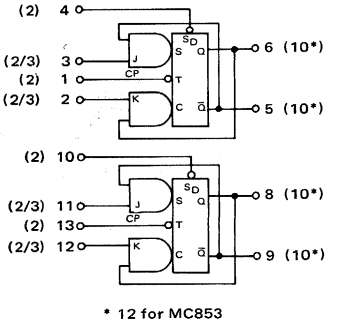
Total Power Dissipation
MC952/MC852, MC953/MC853
= 120 mW typ/pkg
MC955/MC855, MC956/MC856
= 140 mW typ/pkg
Propagation Delay Time = 40 ns typ

MC952/MC852



* 12 for MC852

MC953/MC853



* 12 for MC853

Number in parenthesis indicates loading.

ASYNCHRONOUS TRUTH TABLE
MC952/MC852 and MC955/MC855

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

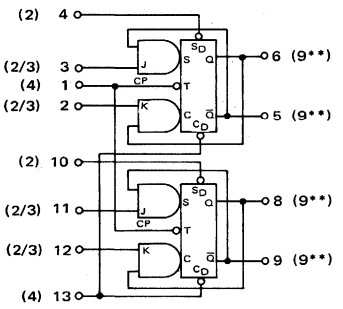
Each section of the monolithic MC955/MC855 and MC956/MC856 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the "master-slave" principle. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

The MC955/MC855 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC956/MC856 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

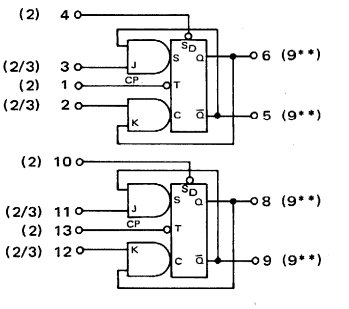
The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise. The output pull-up resistor has been changed from that utilized in the MC952/MC852 and MC953/MC853 in order to improve the propagation delay versus capacitance characteristics.

MC955/MC855



** 11 for MC855

MC956/MC856



** 11 for MC856

Number in parenthesis indicates loading.

ASYNCHRONOUS TRUTH TABLE
MC953/MC853 and MC956/MC856

S_D	Q	$\overline{Q}$
1	NC	NC
0	1	0

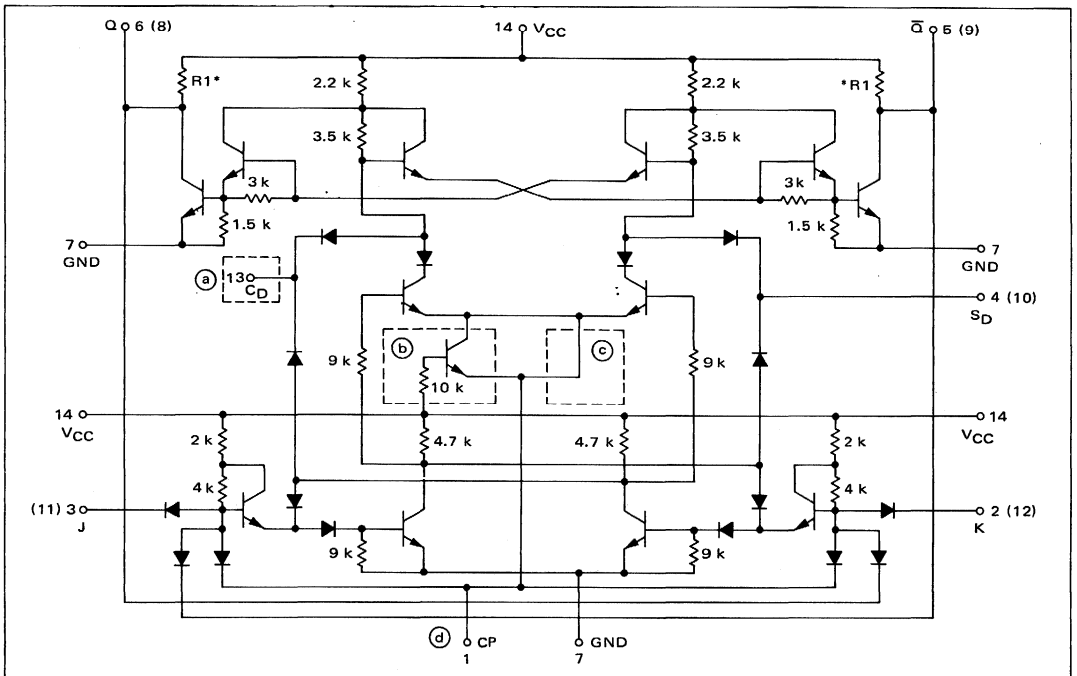
J-K TRUTH TABLE — All Types †

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs.

†Valid only when J and K inputs remain unchanged during period while CP is high.

CIRCUIT SCHEMATIC (½ of circuit shown)

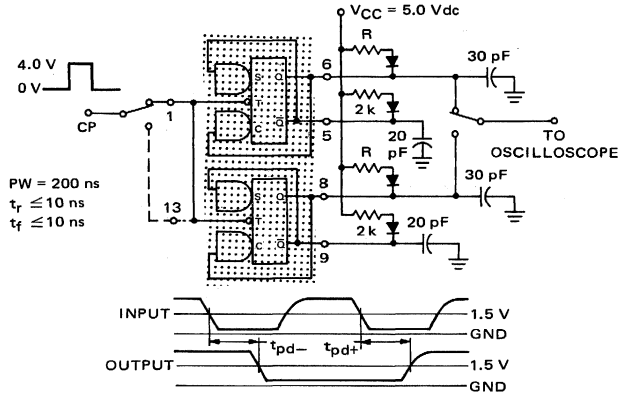


(a) Used only on MC952/MC852 and MC955/MC855
(b) Used only on MC952/MC852 and MC953/MC853
(c) Used only on MC955/MC855 and MC956/MC856
(d) Pin 13 used for other side of MC953/MC853 and MC956/MC856

NOTE: Number in parenthesis indicates pin number for other half of the schematic. Ground and V_{CC} pins are common to both sides.

* MC952/MC852 and MC953/MC853 — 6 k
MC955/MC855 and MC956/MC856 — 2 k

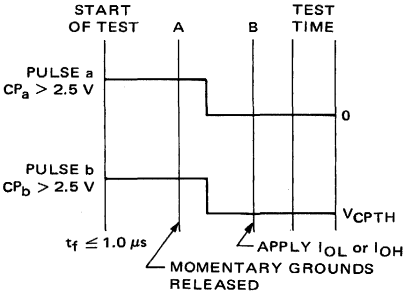
PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



Test circuit shown for MC952/MC852 and MC955/MC855.
Use dotted-line connection for MC953/MC853 and MC956/MC856, which have separate toggle inputs.
Ground pin 7. Only connected inputs are shown. All others are open.
MC833 or equivalent used for diodes.

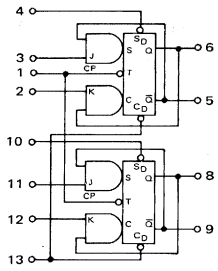
TEST	R
t_{pd+}	3.9 k ohms
t_{pd-}	400 ohms

CLOCK PULSE WAVEFORMS



TEST CONDITIONS

T_A	V_{CPTH}	
	MC952, MC953	MC955, MC956
−55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
	MC852, MC853	MC855, MC856
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V



MC952/MC852
MC955/MC855
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC952, MC955 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC852, MC855 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc
		6	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		8	-		-		-			-		-		-		
		9	-		-		-			-		-		-		
	V_{OH}	5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-	
		5	↓	-	↓	-	↓	-		↓	-	↓	-	↓	-	
		6		-		-		-			-		-		-	
		6		-		-		-			-		-		-	
		8		-		-		-			-		-		-	
		8		-		-		-			-		-		-	
		9		-		-		-			-		-		-	
		9		-		-		-			-		-		-	
Short-Circuit Current MC952/MC852	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
		6	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
		8														
		9														
MC955/MC855		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	
		6	↓	↓	↓	↓	↓	↓		↓	↓	↓	↓	↓	↓	
		8														
		9														
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		4	-		-		-			-		-		-		
		10	-		-		-			-		-		-		
		11	-		-		-			-		-		-		
		12	-		-		-			-		-		-		
All Types	$2\,I_R$	13	-	4.0	-	4.0	-	10		-	10	-	10	-	20	
MC952/MC852	$2\,I_{RCP}$	1	-	20	-	20	-	40		-	40	-	40	-	60	
MC955/MC855	$2\,I_{RCP}$	1	-	20	-	20	-	40		-	40	-	40	-	60	
Forward Current	$2/3\,I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	
		11	-		-		-			-		-		-		
		12	-		-		-			-		-		-		
	$2\,I_{FCP}$	1	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
		1	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67	
		10	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67	
	$2\,I_{FS}$	13	-	-6.40	-	-6.40	-	-6.00		-	-5.60	-	-5.60	-	-5.34	
Power Drain Current																
MC952/MC852	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc
	I_{max}	14	-	-	-	32	-	-	↓	-	-	-	36	-	-	↓
MC955/MC855	I_{PDH}	14	-	-	-	27	-	-		-	-	-	34	-	-	
	I_{max}	14	-	-	-	38	-	-	↓	-	-	-	45	-	-	↓
Switching Times																
MC952/MC852	t_{pd+}	1, 6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns
	t_{pd-}	1, 6	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓
	t_{pd+}	1, 8	-	-	25	100	-	-		-	-	25	100	-	-	
	t_{pd-}	1, 8	-	-	15	55	-	-		-	-	15	55	-	-	
MC955/MC855	t_{pd+}	1, 6	-	-	25	75	-	-		-	-	25	75	-	-	
	t_{pd-}	1, 6	-	-	15	55	-	-		-	-	15	55	-	-	
	t_{pd+}	1, 8	-	-	25	75	-	-		-	-	25	75	-	-	
	t_{pd-}	1, 8	-	-	15	55	-	-	↓	-	-	15	55	-	-	↓

Pins not listed are left open.

§ CP_a = Clock Pulse a, CP_b = Clock Pulse b } See Clock Pulse Waveforms.

† Applied after Clock Pulse.

‡ Momentary Ground.

		TEST CURRENT/VOLTAGE VALUES															
		mA				Volts											
@ Test Temperature		I_{OL}		I_{OH}		V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}				
		MC952	MC955	MC952	MC955												
MC952, MC955	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-				
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00				
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-				
		MC852	MC855	MC852	MC855												
MC852, MC855	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-				
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00				
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-				

Characteristic	Symbol	Pin Under Test	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	5†	-	2	-	-	-	-	14	-	-	-	1	7,13‡
		6	6†	-	3	-	-	-	-		-	-	-		4‡,7
		8	8†	-	11	-	-	-	-		-	-	-		7,10‡
		9	9†	-	12	-	-	-	-		-	-	-		7,13†
	V_{OH}	5		5†	3	2	-	-	-		-	-	1	-	4‡,7
		5		5	2,13	4	-	-	-		-	-		-	7
		6		6†	2	3	-	-	-		-	-		-	7,13‡
		6		6	3,4	13	-	-	-		-	-		-	7
		8		8†	12	11	-	-	-		-	-		-	7,13‡
		8		8	10,11	13	-	-	-		-	-		-	7
		9		9†	11	12	-	-	-		-	-		-	7,10‡
		9		9	12,13	10	-	-	-		-	-		-	7
Short-Circuit Current															
MC952/MC852	I_{SC}	5	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	-	-	-	-	-	-	-	-		-	-		6,7
		8	-	-	-	-	-	-	-	-		-	-		7,8
		9	-	-	-	-	-	-	-	-		-	-		7,9
MC955/MC855		5	-	-	-	-	-	-	-	-		-	-		5,7
		6	-	-	-	-	-	-	-	-		-	-		6,7
		8	-	-	-	-	-	-	-	-		-	-		7,8
		9	-	-	-	-	-	-	-	-		-	-		7,9
Reverse Current All Types	I_R	2	-	-	-	-	-	2	-	-	14	-	-	-	1,7
		3	-	-	-	-	-	3	-	-		-	-		1,7
		4	-	-	-	-	-	4	-	-		-	1	-	2,6,7
		10	-	-	-	-	-	10	-	-		-	1	-	7,8,12
		11	-	-	-	-	-	11	-	-		-	-	-	1,7
		12	-	-	-	-	-	12	-	-		-	-	-	1,7
All Types	$2\,I_R$	13	-	-	-	-	-	13	-	-		-	1	-	3,5,7,9,11
MC952/MC852	$2\,I_{RCP}$	1	-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7,8, 9,11,12
MC955/MC855	$2\,I_{RCP}$	1	-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7,8, 9,11,12
Forward Current	$2/3\,I_F$	2	-	-	-	-	2	-	-	-	14	-	-	1	7
		3	-	-	-	-	3	-	-	-		-	-		
		11	-	-	-	-	11	-	-	-		-	-		
		12	-	-	-	-	12	-	-	-		-	-		
	$2\,I_{FCP}$	1	-	-	4,10	-	1	-	-	-		-	-	-	
		1	-	-	13	-	1	-	-	-		-	-	-	
	I_{FS}	4	-	-	-	-	4	-	-	-		-	-	-	2,3,7,13
		10	-	-	-	-	10	-	-	-		-	-	-	7,11,12,13
	$2\,I_{FS}$	13	-	-	-	-	13	-	-	-		-	-	-	2,3,4,7, 10,11,12
Power Drain Current															
MC952/MC852	I_{PDH}	14	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7, 10,11,12
MC955/MC855	I_{PDH}	14	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7, 10,11,12
Switching Times			Pulse In	Pulse Out											
MC952/MC852	t_{pd+}	1,6	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd+}	1,8		8	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,8		8	-	-	-	-		-	-	-	-	-	
MC955/MC855	t_{pd+}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,6		6	-	-	-	-		-	-	-	-	-	
	t_{pd+}	1,8		8	-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,8		8	-	-	-	-		-	-	-	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
} See Clock Pulse Waveforms.

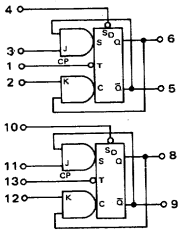
† Applied after Clock Pulse.

‡ Momentary Ground.

MC953/MC853
MC956/MC856

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



@ Test Temperature		I_{OL} mA MC953	I_{OL} mA MC956	I_{OH} mA MC953	I_{OH} mA MC956	V_{IL} Volts	V_{IH} Volts	V_F Volts	V_R Volts	V_{CC} Volts	V_{CCL} Volts	V_{CCH} Volts	V_{max} Volts
MC953, MC956	−55°C	14.6	13.0	-0.12	-0.5	1.40	2.10	0	4.00	-	4.50	5.50	-
	+25°C	15.2	13.6	-0.12	-0.5	1.10	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	13.8	12.3	-0.12	-0.5	0.80	2.00	0	4.00	-	4.50	5.50	-
		MC853	MC856	MC853	MC856								
MC853, MC856	0°C	16.8	15.4	-0.12	-0.5	1.20	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	16.8	15.4	-0.12	-0.5	1.10	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	16.0	14.6	-0.12	-0.5	0.95	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC953, MC956 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC853, MC856 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	CP_a§	CP_b§	Gnd
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	5	-	4	-	-	-	-	14	-	-	-	-	7
		6	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		6†	-	3	-	-	-	-		-	-	-	1.	4‡ 7
	V_{OH}	5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	5†	3	2	-	-	-		-	-	1	-	4‡,7
		6	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	6	3,4	-	-	-	-		-	-	1	-	7
Short-Circuit Current MC953/MC853	I_{SC}	5	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc	-	-	-	-	-	-	-	-	14	-	-	1	5,7
		6	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00		-1.25	-2.50	-1.15	-2.30	-1.05	-2.15		-	-	-	-	-	-	-	-		-	-		6,7
MC956/MC856		5	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-	-	5,7
		6	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10		-2.60	-5.20	-2.35	-4.75	-2.20	-4.40		-	-	-	-	-	-	-	-		-	-		6,7
Reverse Current All Types	I_R	2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	2	-	-	14	-	-	-	1,7
		3	-		-		-			-		-		-			-	-	-	-	-	3	-	-		-	-	-	1,7
		4	-		-		-			-		-		-			-	-	-	-	-	4	-	-		-	-	-	2,6,7
MC953/MC853	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1,14	-	-	-	-	-	-	2,3,5,6,7
MC956/MC856	I_{RCP}	1	-	10	-	10	-	20		-	20	-	20	-	30		-	-	-	-	-	1	-	-	14	-	-	-	2,3,5,6,7
Forward Current	$2/3\ I_F$	2	-	-1.07	-	-1.07	-	-1.00	mAdc	-	-0.95	-	-0.95	-	-0.90	mAdc	-	-	-	-	2	-	-	-	14	-	-	1	7
	$2/3\ I_F$	3	-	-1.07	-	-1.07	-	-1.00		-	-0.95	-	-0.95	-	-0.90		-	-	-	-	3	-	-	-		-	-	1	
	I_{FCP}	1	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	4	-	1	-	-	-		-	-	-	
	I_{FS}	4	-	-3.20	-	-3.20	-	-3.00		-	-2.80	-	-2.80	-	-2.67		-	-	-	-	4	-	-	-		-	-	-	3,7
Power Drain Current (Total Device) MC953/MC853	I_{PDH}	14	-	-	-	22	-	-	mAdc	-	-	-	28	-	-	mAdc	-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	32	-	-		-	-	-	36	-	-		-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
MC956/MC856	I_{PDH}	14	-	-	-	27	-	-		-	-	-	34	-	-		-	-	-	-	-	-	14	-	-	-	-	-	7
	I_{max}	14	-	-	-	38	-	-		-	-	-	45	-	-		-	-	-	-	-	-	-	-	-	14	-	-	1,2,3,4,7,10, 11,12,13
Switching Times																	Pulse In	Pulse Out											
MC953/MC853	t_{pd+}	1,6	-	-	25	100	-	-	ns	-	-	25	100	-	-	ns	1	6	-	-	-	-	14	-	-	-	-	-	7
	t_{pd-}	1,6	-	-	15	55	-	-		-	-	15	55	-	-				-	-	-	-		-	-	-	-	-	
MC956/MC856	t_{pd+}	1,6	-	-	25	75	-	-		-	-	25	75	-	-				-	-	-	-		-	-	-	-	-	
	t_{pd-}	1,6	-	-	15	55	-	-		-	-	15	55	-	-				-	-	-	-		-	-	-	-	-	

Pins not listed are left open.

§ CP_a = Clock Pulse a
CP_b = Clock Pulse b
} See Clock Pulse Waveforms.

† Applied after Clock Pulse.
‡ Momentary ground.

MC950F, G • MC850F, P, G

The MC950/MC850 high-speed gated flip-flop utilizes capacitive coupling of the pulse-triggered set and clear inputs. Directly coupled set and clear inputs are available as well as direct set and clear inputs that respond to dc levels and override the clocked inputs. Separate clock signals may be applied to the capacitively coupled inputs or they may be tied together to obtain single-channel triggering operation. Maximum toggle frequency is typically 40 MHz at 25°C with power dissipation on the order of 30 mW.

Typical applications include binary ripple counters, shift registers, and similar applications. It may be used to advantage in high-speed portions of digital systems that are presently using MDTL circuitry.

SYNCHRONOUS TRUTH TABLE

t_n				$t_n + 1$
S_1	S_2	C_1	C_2	Q
0	0	0	0	U
1	X	1	X	Q_n
X	1	X	1	Q_n
0	1	1	0	Q_n
0	0	X	1	1
0	0	1	X	1
1	X	0	0	0
X	1	0	0	0

SINGLE TRIGGER TRUTH TABLE

(Pins S_2 and C_1 tied together)

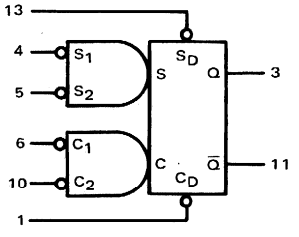
t_n		$t_n + 1$
S_1	C_2	Q
0	0	U
1	0	0
0	1	1
1	1	Q_n

ASYNCHRONOUS TRUTH TABLE

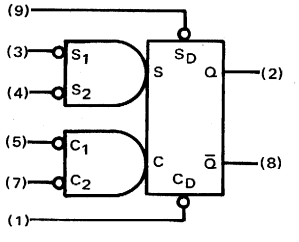
S_D	C_D	Q	$\bar{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

0 = low state (more negative)
1 = high state (more positive)
X = don't care
U = indeterminate state
NC = no change

MC950F/MC850F, P



MC950G/MC850G

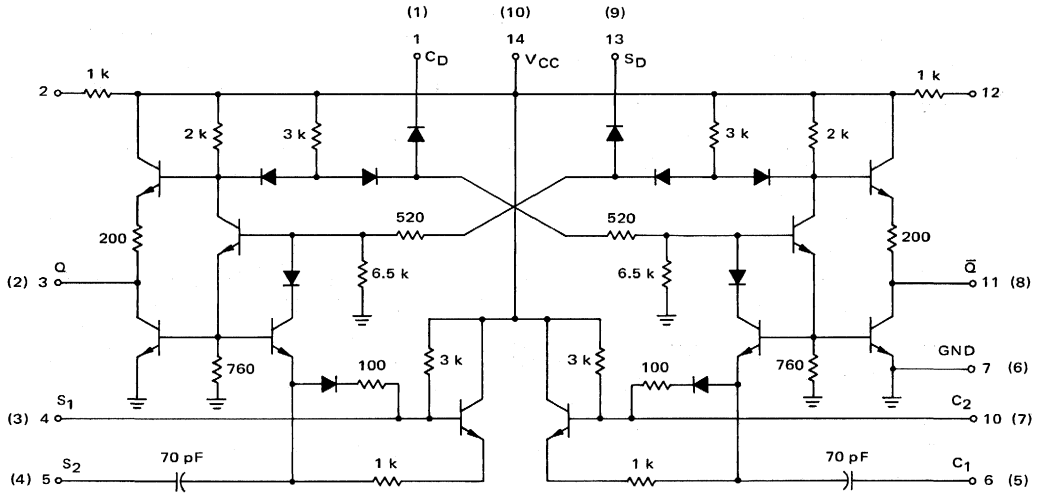


Input Loading Factor
S_D, S_1, C_D, C_2 = 1.5
S_2, C_1 = 100 pF

Output Loading Factor
MC950 = 8
MC850 = 10

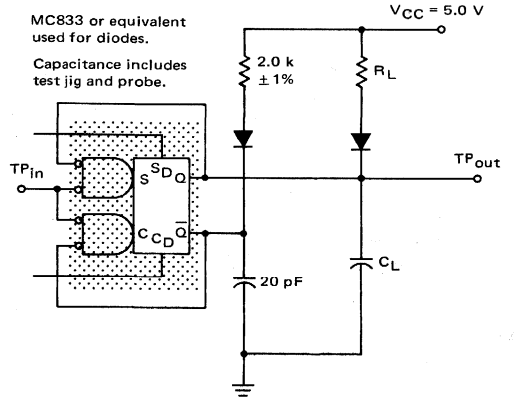
Total Power Dissipation = 50 mW typ/pkg
Propagation Delay Time = 15 ns typ

CIRCUIT SCHEMATIC

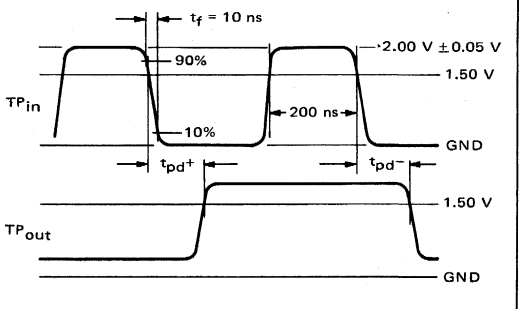


Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



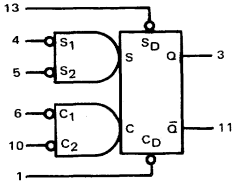
TEST	R_L	C_L
t_{pd^+}	3.9 k ohms	30 pF
t_{pd^-}	400 ohms	50 pF



ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	–	–	10	11	12	13	14
Metal Can	1	–	2	3	4	5	6	–	–	7	8	–	9	10

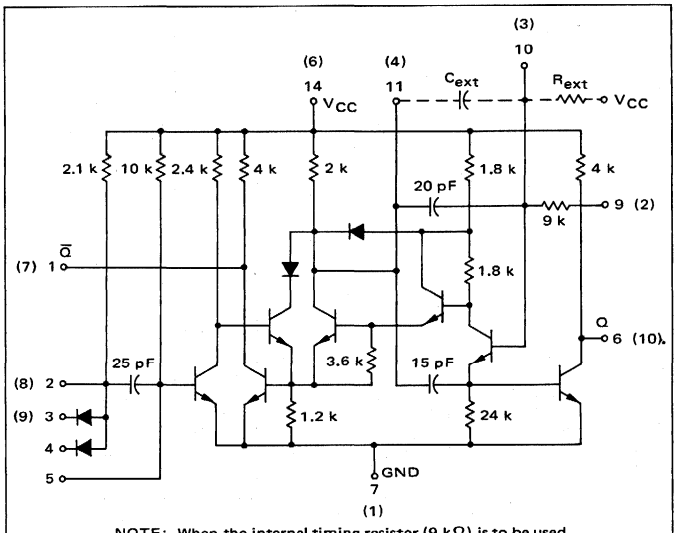


	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC950	−55°C	11.4	-1.50	0	4.00	-	-	4.50	5.50	-
MC950	+25°C	12.0	-1.50	0	4.00	4.50	5.00	4.50	5.50	8.00
MC950	+125°C	10.8	-1.50	0	4.00	-	-	4.50	5.50	-
MC850	0°C	14.0	-1.50	0.45	4.00	-	-	5.00	5.00	-
MC850	+25°C	14.0	-1.50	0.45	4.00	5.00	5.00	5.00	5.00	8.00
MC850	+75°C	13.3	-1.50	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC950 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC850 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	-	-	-	-	14	-	-	1,7
		11	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		11	-	-	-	-	-		-	-	7,13
	V_{OH}	3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	-	-	-	-		-	-	7,13*
		11	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	11	-	-	-	-		-	-	1*,7
Short-Circuit Current	I_{SC}	3	-11.5	-	-14.0	-	-13.0	-	mAdc	-12.6	-	-13.7	-	-12.6	-	mAdc	-	-	-	-	-	-	-	14	-	3,7,13
		11	-11.5	-	-14.0	-	-13.0	-	mAdc	-12.6	-	-13.7	-	-12.6	-	mAdc	-	-	-	-	-	-	-	14	-	1,7,11
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	1	-	-	-	14	-	7
		13	-	2.0	-	2.0	-	5.0		-	5.0	-	5.0	-	10		-	-	-	13	-	-	-		-	7
	I_{RCP}	5	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	5	-	-	-		-	4,7,10
		6	-	20	-	20	-	30		-	30	-	30	-	40		-	-	-	6	-	-	-		-	4,7,10
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	3,14	-	-	-	-	7,13*
		11	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	11,14	-	-	-	-	1*,7
Forward Current	$1.5\ I_F$	1	-	-2.40	-	-2.40	-	-2.25	mAdc	-	-2.20	-	-2.20	-	-2.10	mAdc	-	-	1	13	-	-	-	14	-	7
		4	-		-		-			-		-		-			-	-	4	10	-	-	-		-	
		10	-		-		-			-		-		-			-	-	10	4	-	-	-		-	
		13	-		-		-			-		-		-			-	-	13	1	-	-	-		-	
	I_2	2	-	-	-4.60	-6.90	-	-		-	-	-3.85	-7.15	-	-		-	-	-	-	-	-	-		-	2,7
	I_{12}	12	-	-	-4.60	-6.90	-	-		-	-	-3.85	-7.15	-	-		-	-	-	-	-	-	-		-	7,12
Power Drain Current	I_{PDH}	14	-	-	-	9.0	-	-	mAdc	-	-	-	10	-	-	mAdc	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	14	-	-	mAdc	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	14	1,7,13
Switching Times																	Pulse In	Pulse Out								
	t_{pd}^+	5,6,3	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	5,6	3	-	-	-	14	-	-	-	7
	t_{pd}^-	5,6,3	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	5,6	3	-	-	-	14	-	-	-	7

Pins not listed are left open.
*Momentarily ground this terminal before taking measurement.

MC951F, G • MC851F, P, G



NOTE: When the internal timing resistor (9 kΩ) is to be used, connect Pin 9 to Pin 14 (flat and dual in-line packages) or pins 2 and 6 (can). DO NOT MAKE THIS CONNECTION IF USING THE EXTERNAL CAPACITOR AND RESISTOR.

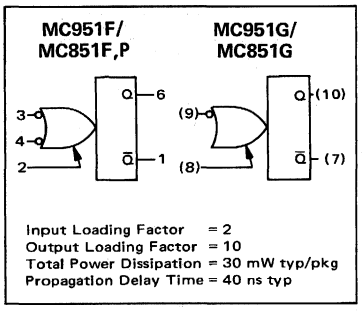
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

Maximum permissible current into Pin 9 (2) = 10 mAdc.

The MC951/MC851 is a monolithic monostable multivibrator circuit which gives complementary output pulses upon the dynamic zero transition of the input waveform. The output pulse width is determined by an R-C timing circuit and, due to differentiation of the input, is essentially independent of the input pulse width. With internal components, nominal pulse width is 100 ns.

Provisions are available to increase the pulse width by adding external capacitance and to increase pulse width stability by utilizing a precision external resistor in place of the internal charging resistor.

Typical applications include analog comparators, elimination of transients on pulse waveforms, and provision for delays to insure the proper sequence of digital operations in computer applications.



Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 30 mW typ/pkg
Propagation Delay Time = 40 ns typ

APPLICATIONS INFORMATION

OUTPUT PULSE WIDTH

EXTERNAL COMPONENTS USED	INTERNAL RESISTOR CONNECTION	PULSE WIDTH ns (APPROX)
None	Pin 9 to VCC	100
Cext (between Pins 10 & 11)	Pin 9 to VCC	4.5 (Cext + 20)
Rext (between Pin 10 & VCC) (9 kΩ min, 15 kΩ max)	Pin 9 open	0.5 Rext (Cext + 20)

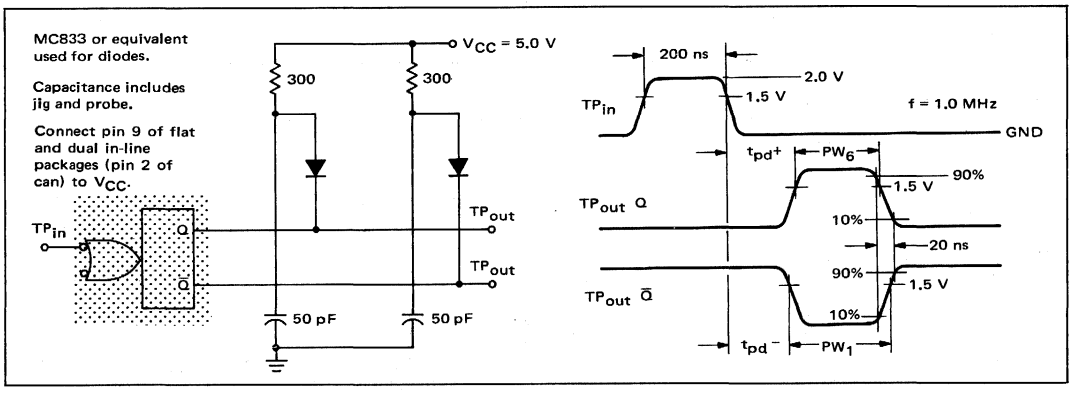
Capacitance values in pF, Resistance values in kΩ
Pin numbers shown for devices in flat and dual in-line packages.

MAXIMUM INPUT FALL TIME TO TRIGGER

t_f ns	VOLTAGE SWING VOLTS
25	1.0
50	2.0
100	4.0

Output duty cycle ≤ 40%. Higher duty cycles obtainable at a possible decrease of performance.

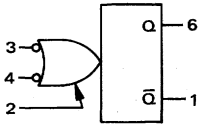
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	1	2	3	4	5	6	7	–	9	10	11	–	–	14
Metal Can	7	8	9	–	–	10	1	–	2	3	4	–	–	6



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC951	−55°C	15.0	-0.18	0	4.00	-	4.50	5.50	-
	+25°C	15.0	-0.18	0	4.00	5.00	4.50	5.50	8.00
	+125°C	14.0	-0.18	0	4.00	-	4.50	5.50	-
MC851	0°C	15.0	-0.18	0.45	4.00	-	5.00	5.00	-
	+25°C	15.0	-0.18	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	14.0	-0.18	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC951 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC851 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	1	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	1	-	-	-	-	14	-	-	7,10
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	1	-	-	-	-	14	-	-	5,7
		6	-		-		-			-		-		-			6	-	-	-	-	9,14	-	-	7
	V_{OH}	1	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	1	-	-	-	9,14	-	-	7
		6	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	6	-	-	-	14	-	-	7,10
Reverse Current	I_R	3	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	3	-	-	14	-	2,7
		4	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	4	-	-	14	-	2,7
Forward Current	$0.5\,I_F$	2	-0.80	-	-0.80	-	-0.75	-	mAdc	-0.70	-	-0.70	-	-0.67	-	mAdc	-	-	2	-	-	-	14	-	7
		11	-0.80	-	-0.80	-	-0.75	-		-0.70	-	-0.70	-	-0.67	-		-	-	10	-	-	-	↓	-	↓
	$0.5I_F/2I_F$	3	-0.80	-3.20	-0.80	-3.20	-0.75	-3.00		-0.70	-2.80	-0.70	-2.80	-0.67	-2.67		-	-	3	4	-	-		-	
		4	-0.80	-3.20	-0.80	-3.20	-0.75	-3.00		-0.70	-2.80	-0.70	-2.80	-0.67	-2.67		-	-	4	3	-	-	↓	-	↓
	I_9	9	-	-	0.50	0.75	-	-	↓	-	-	0.40	0.80	-	-	↓	-	-	-	-	-	-	9,14	-	7,10
Power Drain Current	I_{PDL}	9,14†	-	-	-	9.0	-	-	mAdc	-	-	-	12	-	-	mAdc	-	-	-	-	9,14	-	-	-	3,4,7
	I_{max}	14	-	-	-	22	-	-	mAdc	-	-	-	25	-	-	mAdc	-	-	-	-	-	-	-	14	3,4,7
Switching Times																	Pulse In	Pulse Out							
	t_{pd+}	3,6	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	3	6	-	-	9,14	-	-	-	7
	t_{pd-}	3,1	-	-	-	50	-	-	↓	-	-	-	50	-	-	↓	↓	1	-	-	↓	-	-	-	↓
	PW_1	3,1	-	-	90	220	-	-		-	-	90	220	-	-			1	-	-		-	-	-	
	PW_6	3,6	-	-	70	160	-	-	↓	-	-	70	160	-	-	↓	↓	6	-	-	↓	-	-	-	↓

Pins not listed are left open.
†I_{PDL} is measured at pins 9 and 14 simultaneously.

MC938F · MC838F, P

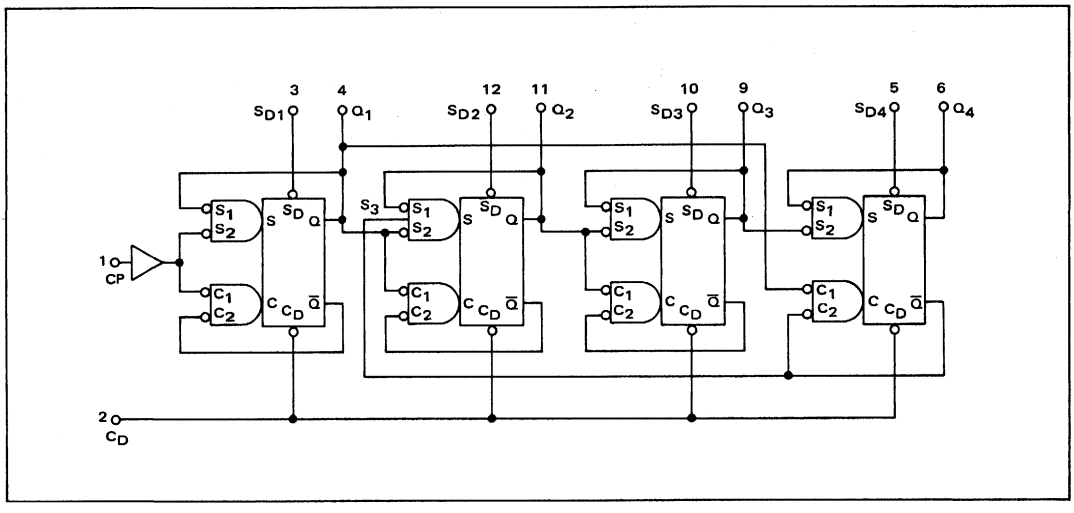
This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 BCD with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin is 1.0 volt.

Input Loading Factor
- S_D = 1.5
- C_D = 5
- CP = 1

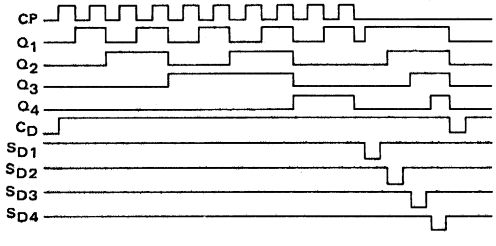
Output Loading Factor = 8

Total Power Dissipation = 150 mW typ/pkg

Maximum Counting Frequency = 30 MHz typ



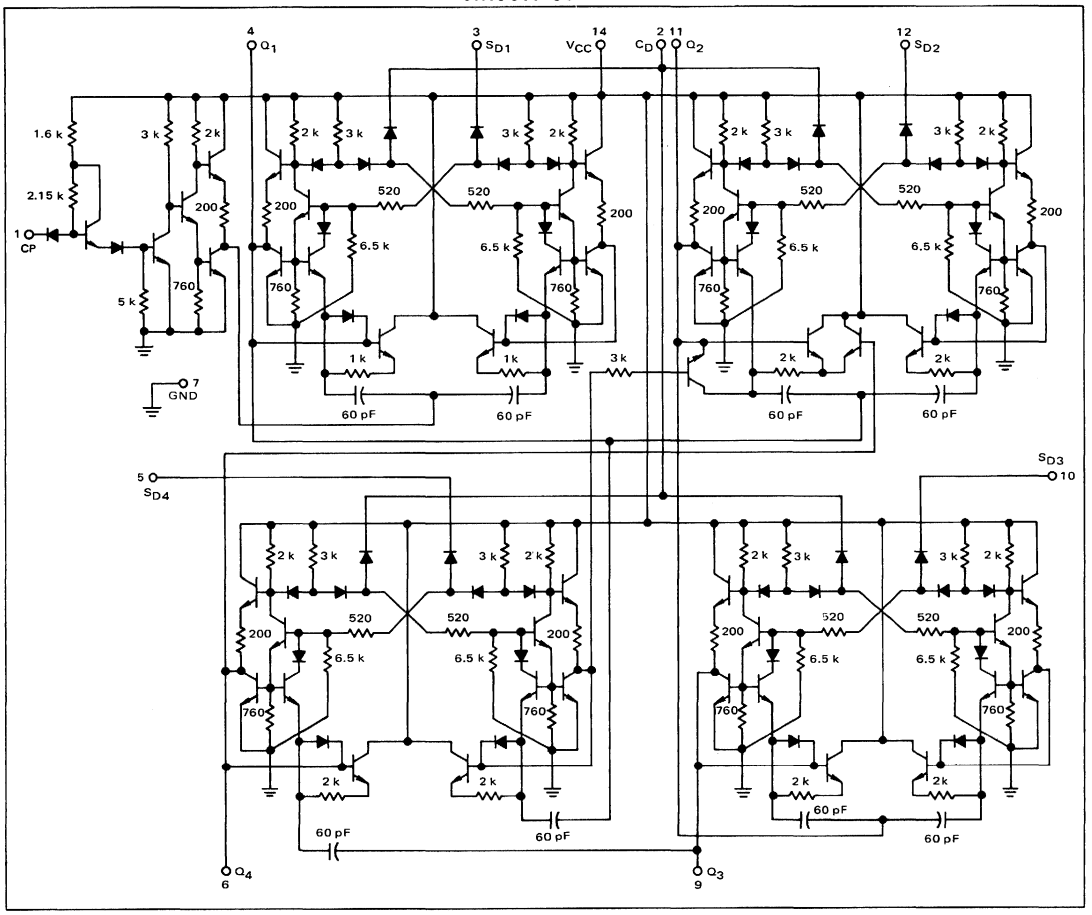
COUNTER SEQUENCE



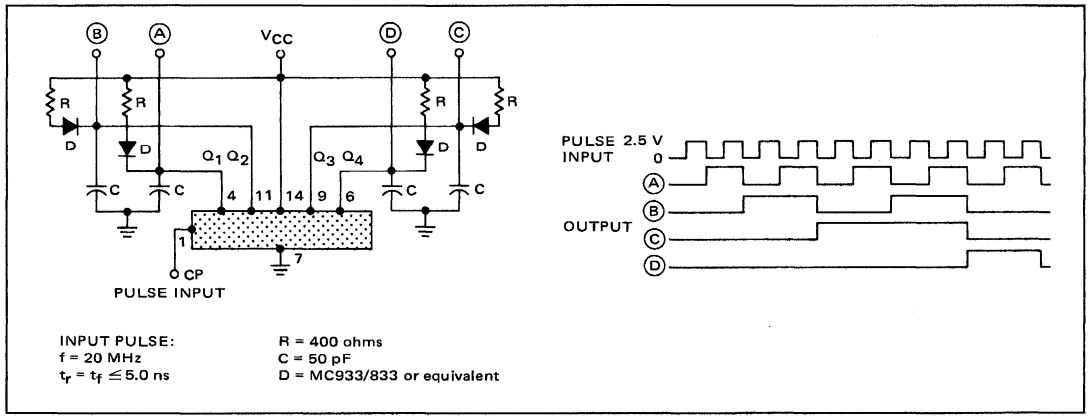
DECODING LOGIC

0	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
1	Q_1	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
2	$\overline{Q}_1$	Q_2	$\overline{Q}_3$	
3	Q_1	Q_2	$\overline{Q}_3$	
4	$\overline{Q}_1$	$\overline{Q}_2$	Q_3	
5	Q_1	$\overline{Q}_2$	Q_3	
6	$\overline{Q}_1$	Q_2	Q_3	
7	Q_1	Q_2	Q_3	
8	$\overline{Q}_1$	Q_4		
9	Q_1	Q_4		

CIRCUIT SCHEMATIC



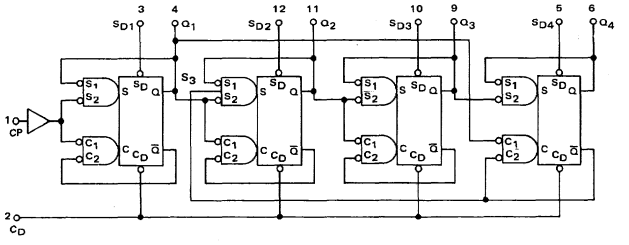
COUNTING FREQUENCY TEST CIRCUIT AND WAVEFORMS



INPUT PULSE:
f = 20 MHz
$t_r = t_f \leq 5.0$ ns

R = 400 ohms
C = 50 pF
D = MC933/833 or equivalent

ELECTRICAL CHARACTERISTICS



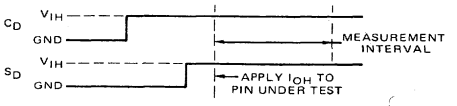
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC938	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
MC938	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
MC938	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC838	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
MC838	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
MC838	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC938 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC838 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	4	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	4	-	3,5,10,12	-	-	-	14	-	-	1,2,7
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	↓	-	-	-	↓	-	-	↓
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	9	-	↓	-	-	-	↓	-	-	↓
		11	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	11	-	↓	-	-	-	↓	-	-	↓
	V_{OH}	4	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	4*	2*,3*,5, 10,12	-	-	-	↓	-	-	1,7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	6*	2*,3,5*, 10,12	-	-	-	↓	-	-	↓
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	9*	2*,3,5, 10*,12	-	-	-	↓	-	-	↓
		11	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	11*	2*,3,5, 10,12*	-	-	-	↓	-	-	↓
Short-Circuit Current	I_{SC}	4	-9.0	-	-12.0	-	-10.0	-	mAdc	-9.0	-	-10.0	-	-9.0	-	mAdc	-	-	2,5,10,12	-	-	-	-	14	-	1,3,4,7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,10,12	-	-	-	-	↓	-	1,5,6,7
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,5,12	-	-	-	-	↓	-	1,7,9,10
		11	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,5,10	-	-	-	-	↓	-	1,7,11,12

Pins not listed are left open.

† Momentarily ground this terminal before applying test condition.

* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



ELECTRICAL CHARACTERISTICS (continued)

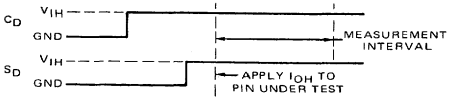
@ Test Temperature		TEST CURRENT/VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC938	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC838	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC938 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC838 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	1	-	-	14	-	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	3†	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5†	-	-		-	
		10	-		-		-			-		-		-			-	-	-	-	10†	-	-		-	
		12	-		-		-			-		-		-			-	-	-	-	12†	-	-		-	
	$4\ I_R$	2	-	8.0	-	8.0	-	20	↓	-	20	-	20	-	40	↓	-	-	-	-	2†	-	-	↓	-	↓
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	1	-	-	-	14	-	7
	$1.5\ I_F$	3	-	-2.40	-	-2.40	-	-2.25	↓	-	-2.10	-	-2.10	-	-2.00	↓	-	-	-	3	-	-	-	↓	-	↓
		5	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	5	-	-	-		-	
		10	-		-		-			-		-		-			-	-	-	10	-	-	-		-	
		12	-		-		-			-		-		-			-	-	-	12	-	-	-		-	
	$5\ I_F$	2	-	-8.00	-	-8.00	-	-7.50	↓	-	-7.00	-	-7.00	-	-6.65	↓	-	-	-	2	-	-	-	↓	-	↓
Power Drain Current	I_{PDH}	14	-	-	-	40	-	-	mAdc	-	-	-	43.5	-	-	mAdc	-	-	10*	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	28	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	-	-	-	-	-	14	2,3,5,7, 10,12
																	Pulse In	Pulse Out								
Counting Frequency	f_C	1,4,6, 9,11	-	-	-	20	-	-	MHz	-	-	-	20	-	-	MHz	1	4,6,9,11	-	-	-	14	-	-	-	7

Pins not listed are left open.

† Momentarily ground this terminal before applying test condition.

* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



MC939F · MC839F, P

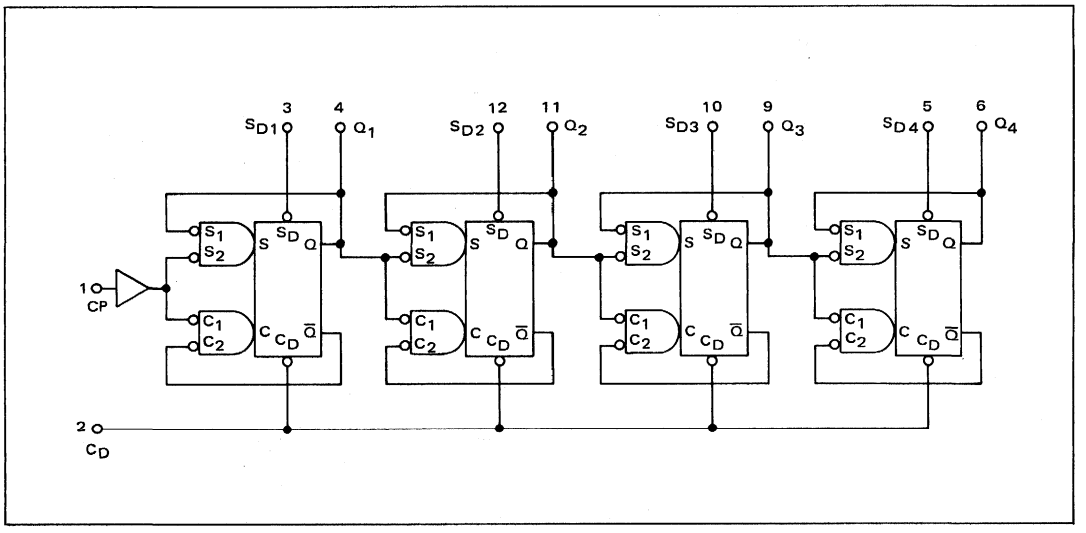
This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 binary code with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin in 1.0 volt.

Input Loading Factor:
$S_D = 1.5$
$C_D = 5$
$CP = 1$

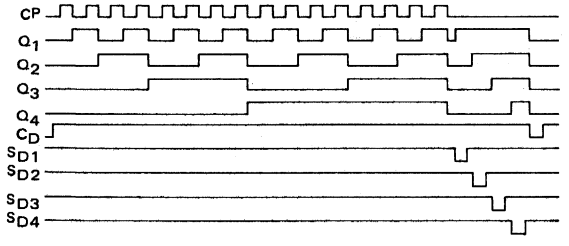
Output Loading Factor = 8

Total Power Dissipation = 150 mW typ/pkg

Maximum Counting Frequency = 30 MHz typ



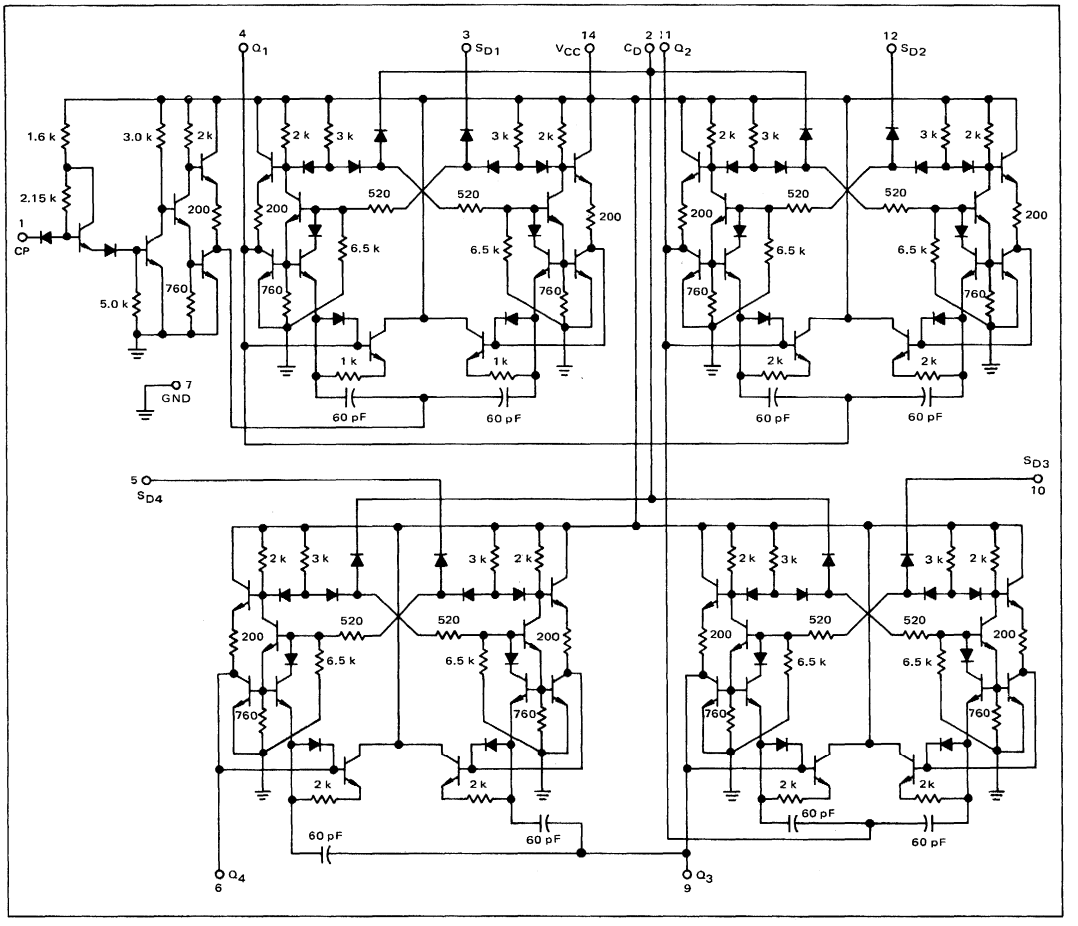
COUNTER SEQUENCE



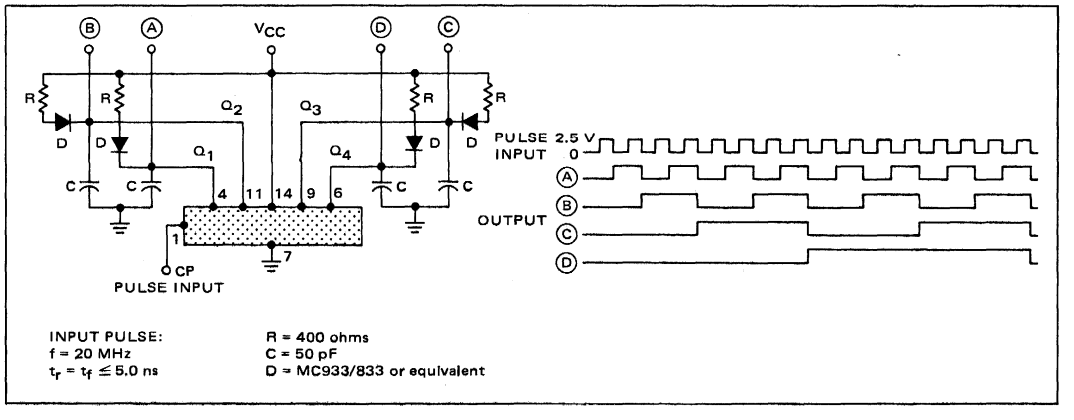
DECODING LOGIC

0	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
1	Q_1	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
2	$\overline{Q}_1$	Q_2	$\overline{Q}_3$	$\overline{Q}_4$
3	Q_1	Q_2	$\overline{Q}_3$	$\overline{Q}_4$
4	$\overline{Q}_1$	$\overline{Q}_2$	Q_3	$\overline{Q}_4$
5	Q_1	$\overline{Q}_2$	Q_3	$\overline{Q}_4$
6	$\overline{Q}_1$	Q_2	Q_3	$\overline{Q}_4$
7	$\overline{Q}_1$	Q_2	Q_3	$\overline{Q}_4$
8	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	Q_4
9	Q_1	$\overline{Q}_2$	$\overline{Q}_3$	Q_4
10	$\overline{Q}_1$	Q_2	$\overline{Q}_3$	Q_4
11	Q_1	Q_2	$\overline{Q}_3$	Q_4
12	$\overline{Q}_1$	$\overline{Q}_2$	Q_3	Q_4
13	Q_1	$\overline{Q}_2$	Q_3	Q_4
14	$\overline{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

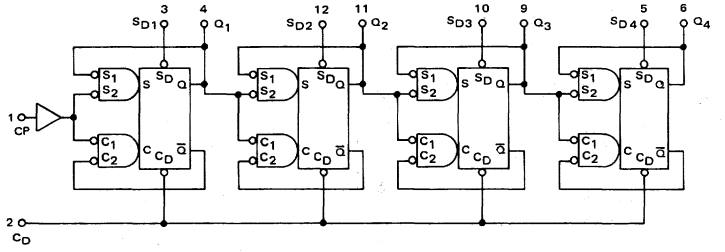
CIRCUIT SCHEMATIC



COUNTING FREQUENCY TEST CIRCUIT AND WAVEFORMS



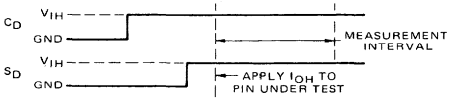
ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC939	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC839	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC939 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC839 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	4	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	4	-	3,5,10,12	-	-	-	14	-	-	1,2,7
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	↓	-	-	-	↓	-	-	↓
		9	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	9	-	↓	-	-	-	↓	-	-	↓
		11	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	11	-	↓	-	-	-	↓	-	-	↓
	V_{OH}	4	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	4*	2*,3*, 5,10,12	-	-	-	↓	-	-	1,7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	6*	2*,3,5*, 10,12	-	-	-	↓	-	-	↓
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	9*	2*,3,5, 10*,12	-	-	-	↓	-	-	↓
		11	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	11*	2*,3,5, 10,12*	-	-	-	↓	-	-	↓
Short-Circuit Current	I_{SC}	4	-9.0	-	-12.0	-	-10.0	-	mAdc	-9.0	-	-10.0	-	-9.0	-	mAdc	-	-	2,5,10,12	-	-	-	-	14	-	1,3,4,7
		6	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,10,12	-	-	-	-	↓	-	1,5,6,7
		9	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,5,12	-	-	-	-	↓	-	1,7,9,10
		11	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	2,3,5,10	-	-	-	-	↓	-	1,7,11,12

Pins not listed are left open.
† Momentarily ground this terminal before applying test condition.
* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:

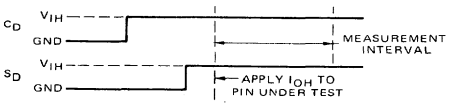


ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature		TEST CURRENT / VOLTAGE VALUES mA I_{OL}	mA I_{OH}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_{max}
MC939	−55°C	11.4	-0.12	2.10	0	4.00	-	4.50	5.50	-
	+25°C	12.0	-0.12	2.00	0	4.00	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	2.00	0	4.00	-	4.50	5.50	-
MC839	0°C	12.0	-0.12	2.00	0.45	4.00	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.90	0.45	4.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	1.80	0.50	4.00	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC939 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC839 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	µAdc	-	5.0	-	5.0	-	10	µAdc	-	-	-	-	1	-	-	14	-	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	3†	-	-	↓	-	↓
		5	-		-		-			-		-		-			-	-	-	-	5†	-	-		-	
		10	-		-		-			-		-		-			-	-	-	-	10†	-	-		-	
		12	-		-		-			-		-		-			-	-	-	-	12†	-	-		-	
	4 I_R	2	-	8.0	-	8.0	-	20		-	20	-	20	-	40		-	-	-	-	2†	-	-		-	
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	1	-	-	-	14	-	7
	1.5 I_F	3	-	-2.40	-	-2.40	-	-2.25		-	-2.10	-	-2.10	-	-2.00		-	-	-	3	-	-	-		-	
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5	-	-	-	↓	-	↓
		10	-		-		-			-		-		-			-	-	-	10	-	-	-		-	
		12	-		-		-			-		-		-			-	-	-	12	-	-	-		-	
	5 I_F	2	-	-8.00	-	-8.00	-	-7.50		-	-7.00	-	-7.00	-	-6.65		-	-	-	2	-	-	-		-	
Power Drain Current	I_{PDH}	14	-	-	-	40	-	-	mAdc	-	-	-	43.5	-	-	mAdc	-	-	2†	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	28	-	-	mAdc	-	-	-	32	-	-	mAdc	-	-	-	-	-	-	-	-	14	2,3,5,7, 10,12
																	Pulse In	Pulse Out								
Counting Frequency	f_C	1, 4, 6, 9,11	-	-	-	20	-	-	MHz	-	-	-	20	-	-	MHz	1	4,6,9,11	-	-	-	14	-	-	-	7

Pins not listed are left open.
† Momentarily ground this terminal before applying test condition.
* Inputs to C_D (pin 2) and appropriate S_D (pins 3, 5, 10, or 12) as shown:



DUAL 4-INPUT EXPANDERS

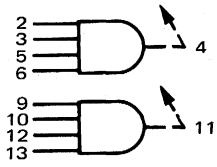
MC933F • MC833F, P

DUAL 4-3 INPUT EXPANDERS

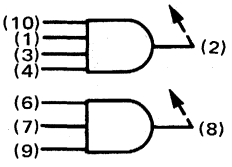
MC933G • MC833G

This dual expander consists of two independent diode networks with characteristics matched to the input diodes of the gate and buffer elements in this logic family. Its use increases the fan-in capability of other MDTL devices to a maximum of 20 while only slightly affecting performance.

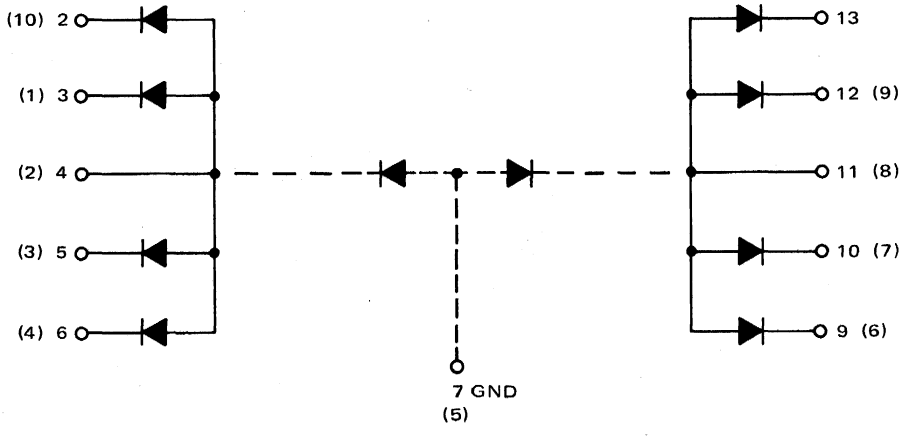
MC933F/MC833F, P



MC933G/MC833G



Input Loading Factor = 1



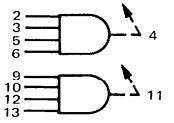
Number at end of terminal represents pin number for flat and dual in-line packages. Number in parenthesis indicates pin number for metal can.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.

NOTE: Although the test conditions and test limits are the same for devices in ALL available packages, the table shows pin connections for testing only the flat and dual in-line packaged devices. To test devices in the metal can, substitute pin numbers shown in the conversion table below.

PACKAGE	PIN NUMBER												
Flat/Dual In-Line	–	2	3	4	5	6	7	–	9	10	11	12	13	–
Metal Can	–	10	1	2	3	4	5	–	6	7	8	9	–	–



Characteristic	Symbol	Pin Under Test	MC933 Test Limits −55°C Min	MC933 Test Limits −55°C Max	MC933 Test Limits +25°C Min	MC933 Test Limits +25°C Max	MC933 Test Limits +125°C Min	MC933 Test Limits +125°C Max	MC933 Unit	MC833 Test Limits 0°C Min	MC833 Test Limits 0°C Max	MC833 Test Limits +25°C Min	MC833 Test Limits +25°C Max	MC833 Test Limits +75°C Min	MC833 Test Limits +75°C Max	MC833 Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{FD}	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: V_R	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: Gnd
																	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{FD} 2.00	TEST CURRENT / VOLTAGE VALUES (All Temperatures) Volts V_R 4.00	
Forward Voltage	V_{FD}	4	–	0.98	–	0.82	–	0.65	Vdc	–	0.90	–	0.82	–	0.75	Vdc	4	–	2,7
			–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	↓	–	3,7
			–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	↓	–	5,7
			–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	↓	–	6,7
		↓	0.85	–	0.70	–	0.50	–	↓	0.75	–	0.68	–	0.60	–	↓	↓	–	2,3,5,6,7
Reverse Current	I_R	2	–	2.0	–	2.0	–	5.0	μAdc	–	5.0	–	5.0	–	10	μAdc	–	2	3,5,6,7
		3	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	3	2,5,6,7
		5	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	5	2,3,6,7
		6	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓	–	6	2,3,5,7
	$5\ I_R$	4	–	10	–	10	–	25	↓	–	–	–	–	–	–	↓	–	4	7
	$2\ I_R$	4	–	–	–	–	–	–	↓	–	–	–	10	–	–	↓	–	4	7

Pins not listed are left open.

DTL

INTEGRATED CIRCUITS

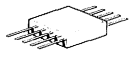
MC200/250 SERIES

MC200 series (−55 to +125°C)
MC250 series (0 to 75°C)

The DTL family of integrated logic circuits is characterized by moderate speed and low power dissipation.



CASE 71A



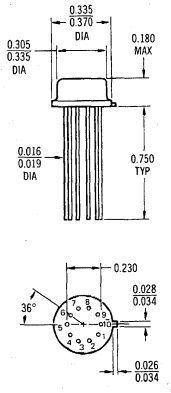
CASE 72
(TO-91)

FUNCTIONS AND CHARACTERISTICS ($V+ = 4$ V, $V- = -2$ V, $T_A = 25°C$)

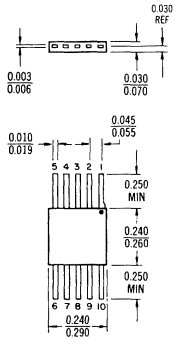
FUNCTION	TYPE①		FAN-OUT		Propagation Delay	Power Dissipation	CASE
	−55 to +125°C	0 to +75°C	MC200 SERIES	MC250 SERIES	t_{pd} ns typ	mW typ	
4-Input Gate NAND/NOR	MC201	MC251	5	4	30	6	71A, 72
3-Input Gate NAND/NOR	MC202	MC252	5	4	30	6	71A, 72
3-Input Power Gate NAND/NOR	MC204	MC254	20	12	40	30	71A, 72
Line Driver	MC205	MC255	20	12	55	50	71A, 72
Dual 2-Input Gate NAND/NOR	MC206	MC256	5	4	30	12	71A, 72
Dual 3-2 Input Gate NAND/NOR	MC207	MC257	5	4	30	12	71A, 72
Dual 3-2 Input Gate NAND/NOR	MC208	MC258	4	3	30	30	71A, 72
Clocked R-S Flip-Flop	MC209	MC259	8	6	60	16	71A, 72
Clocked R-S Flip-Flop (Pulse Triggered Binary)	MC210	MC260	8	6	60	16	71A, 72
Dual 3-Input Gate NAND/NOR	MC212	MC262	5	4	30	12	71A, 72
Dual 3-Input Gate NAND/NOR	MC213	MC263	4	3	30	30	71A, 72
			V_R (Volts)		t_{rr} (ns)		
6-Input Gate AND (Expander)	MC203	MC253	8	8	4	—	71A, 72
Dual 3-Input Gate AND (Expander)	MC215	MC265	8	8	4	—	71A, 72
Dual 3-Input Diode Array	MC217	MC267	8	8	4	—	71A, 72

① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC201G = Metal Can, MC201F = Flat Package.)

OUTLINE DIMENSIONS



CASE 71A



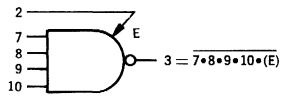
CASE 72
(TO-91)

Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

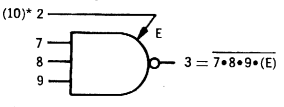
Numbers at ends of terminals represent pin numbers.
Inputs have a fan-in of 1 unless otherwise noted. For fan-out capability, see Functions and Characteristics table.
(V^+ = pin 6, V^- = pin 5 unless otherwise noted. Gnd = 1.)

GATES

MC201, MC251
4-Input Gate NAND/NOR

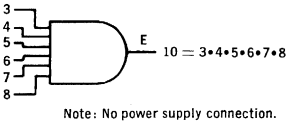


MC202, MC252
MC204, MC254
3-Input Gate NAND/NOR



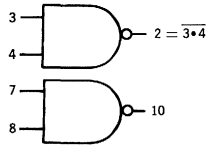
*MC204, MC254
Fan-in = 2 for MC204, MC254

MC203, MC253
6-Input Gate AND
(Expander)

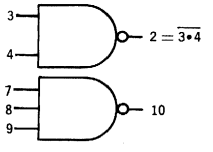


Note: No power supply connection.

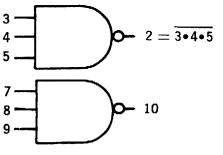
MC206, MC256
Dual 2-Input Gate NAND/NOR



MC207, MC257
MC208, MC258
Dual 3-2 Input Gate NAND/NOR

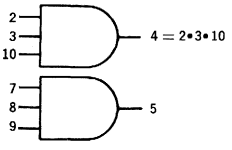


MC212, MC262
MC213, MC263
Dual 3-Input Gate NAND/NOR



Note: No V- connection.

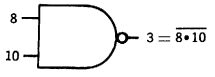
MC215, MC265
Dual 3-Input Gate AND
(Expander)



Note: No power supply connection.

DRIVERS

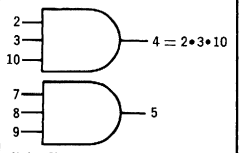
MC205, MC255
Line Driver



Fan-in = 2

DIODE ARRAYS

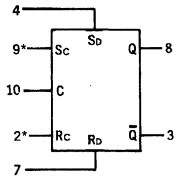
MC217, MC267
Dual Diode Array



Note: No power supply connection.

FLIP-FLOPS

MC209, MC259
Clocked R-S Flip-Flop



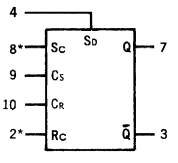
CLOCKED SET-RESET		
S_C	R_C	Q
0	0	?
0	1	1
1	0	0
1	1	No Change

DIRECT SET-RESET		
S_D	R_D	Q
0	0	‡
0	1	1
1	0	0
1	1	No Change

*Fan-in = 0.75 for MC209, 1 for MC259

‡Both Q and $\bar{Q}$ in 1 state until either S_D or C_D rises.

MC210, MC260 Clocked R-S Flip-Flop (Pulse Triggered Binary)



*Fan-in = 0.7

S_C	C_S	C_R	R_C	Q	$\bar{Q}$
1	X	1	X	NC	NC
X	1	X	1	NC	NC
1	X	X	1	NC	NC
0	0	X	1	1	0
0	0	1	X	1	0
1	X	0	0	0	1
X	1	0	0	0	1
0	0	0	0	U	U

Low level on S_D overrides other inputs and results in high level on Q.
0 on pins C_S or C_R means transition to low level.
X = don't care.
NC = no change.
U = indeterminate state.

MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS
MC900/MC800 SERIES

MEDIUM-POWER
MRTL
INTEGRATED CIRCUITS

INDEX

Medium-power MRTL logic circuits are specified over two different temperature ranges. Typical gate speed is 12 ns, with power dissipation averages of 19 mW (input high) and 5.0 mW (inputs low) per logic node.

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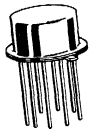
NUMERICAL INDEX

(Functions and Characteristics)

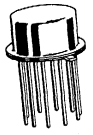
V_{CC} = 3.0 V ± 10%, T_A = 25°C

Function	Type ①		Case	Output Loading Factor each output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Page No.
	-55 to +125°C	0 to +100°C					
Buffer	MC900	MC800	72, 96	25	20	16/45 ②	6-31
Counter Adapter	MC901	MC801	96	5	22	55	6-76
R-S Flip-Flop	MC902	MC803	96	4	14	22	6-38
3-Input NOR Gate	MC903	MC803	72, 96	5	12	19/5.0 ②	6-12
Half Adder	MC904	MC804	72, 96	5	14	45	6-66
Half-Shift Register	MC905	MC805	72, 96	4	22	53	6-57
Half-Shift Register (w/o Inverter)	MC906	MC806	72, 96	4	22	36	6-60
4-Input NOR Gate	MC907	MC807	72, 96	5	12	19/5.0 ②	6-15
Dual 2-Input NOR Gate	MC914	MC814	72, 96	5	12	38/10 ②	6-19
Dual 3-Input NOR Gate	MC915	MC815	72, 96A	5	12	38/10 ②	6-21
J-K Flip-Flop	MC916	MC816	72, 96	3	35	62/54 ③	6-40
Quad 2-Input NOR Gate	MC924	MC824	83	5	12	76/20 ②	6-27
Dual 4-Input NOR Gate	MC925	MC825	83	5	12	38/10 ②	6-23
J-K Flip-Flop	MC926	MC826	72, 96A	5	35	130/65 ③	6-44
Quad Inverter	MC927	MC827	72, 96A	5	12	76/20 ②	6-78
5-Input NOR Gate	MC929	MC829	72, 96	5	12	19/5.0 ②	6-17
Quad Exclusive OR Gate	MC971	MC871	83	5	12	72	6-29
J-K Flip-Flop	MC974	MC874	96	5	35	130/65 ③	6-47
Dual Half Adder	MC975	MC875	83	5	20	90	6-68
Dual Half-Shift Register	MC983	MC883	83	4	22	110	6-62
Dual Half-Shift Register w/Inverter	MC984	MC884	83	4	22	75	6-64
Quad 2-Input Expander	MC985	MC885	83	–	12	17/– ②	6-84
Dual 4-Input Expander	MC986	MC886	83	–	12	17/– ②	6-82
Dual 3-Input Buffer, non inverting	MC988	MC888	83	25	24	128/42 ②	6-36
Hex Inverter	MC989	MC889	83	5	12	76/20 ②	6-80
Dual J-K Flip-Flop	MC990	MC890	83	3	35	124/108 ③	6-50
Dual J-K Flip-Flop	MC991	MC891	83	5	40	155/130 ③	6-54
Triple 3-Input NOR Gate	MC992	MC892	83	5	12	57/15 ②	6-25
Dual Full Adder	MC996	MC896	83	4	60	70	6-70
Dual Full Subtractor	MC997	MC897	83	4	60	70	6-73
Dual Buffer	MC999	MC899	72, 96A	25	20	32/90 ②	6-34
Hex Expander	MC9919	MC9819	83	–	12	13/– ②	6-86

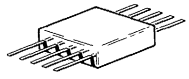
① G Suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC900G = Metal Can, MC900F = Flat Package.
② Inputs High/Inputs Low
③ Only Clock Input High/Inputs Low



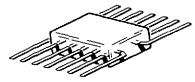
TO-99



TO-100



TO-91



TO-86

MAXIMUM RATINGS
($T_A = 25°C$)

Characteristic	Symbol	Rating	Unit
Input Voltage	—	±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 s)	—	+12	Vdc
Operating Temperature Range MC900 Series MC800 Series	T_A	-55 to +125 0 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CONDITION TOLERANCES

$V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

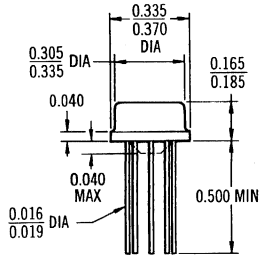
DEFINITIONS

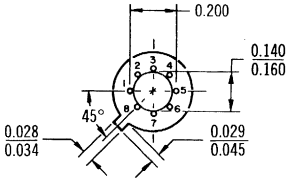
I_{A3}, I_{A4}, I_{A5}	Minimum available output current from a device with an output loading of 3, 4, or 5. Output voltage not to fall below the value of V_{in}.
I_{AB}	Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.
I_{CEX}	Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.
I_{in}	Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.
2 I_{in}, 3 I_{in}	Maximum input current drawn by one input of a device with 2 or 3 bases internally tied together.
V_{BOT}	A high-value voltage applied to an input of a device to insure saturation of the driven transistor.
V_{CC}	Supply voltage.
$V_{CE(sat)}$	Maximum saturation voltage with V_{BOT} applied to the input.
V_{in}	Minimum high-level voltage applied to the input of a device.
V_{off}	The maximum voltage which may be applied to an input terminal without turning the transistor on.
V_{on}	The minimum voltage which may be applied to an input terminal that will turn the transistor on.
V_{out}	The maximum output voltage with V_{on} applied to the input.
V_R	Value of external resistor connected to V_{CC} for test purposes. V_{RH} = highest node resistor value V_{RL} = lowest node resistor value
Release Time	The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.
Set-up Time	The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load, if only one gate is connected to V_{CC}.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by 2 loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused inputs should be returned to ground.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled where the input loading factor is increased by 2.33.

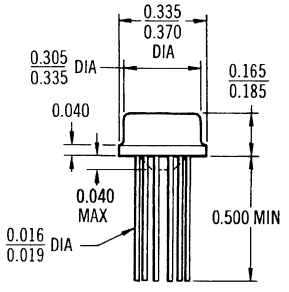
OUTLINE DIMENSIONS

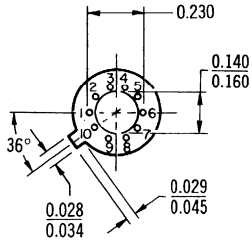




Pin 4 connected to case.

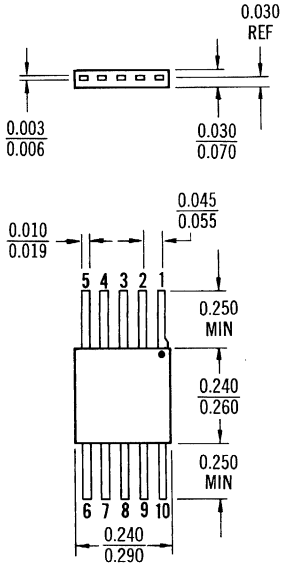
TO-99





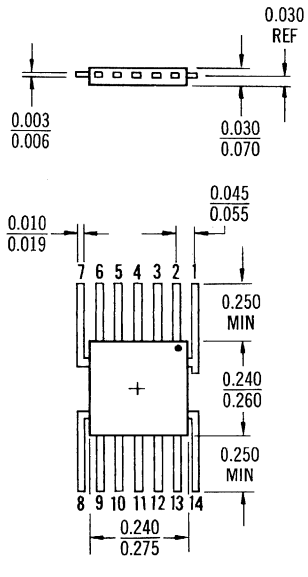
Pin 5 connected to case.

TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TO-86

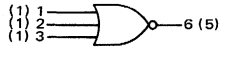
MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC900/MC800 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

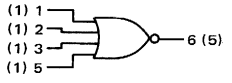
MC903G • MC803G
3-Input Gate



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

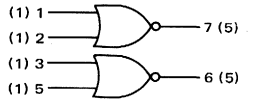
MC907G • MC807G
4-Input Gate



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

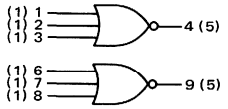
MC914G • MC814G
Dual 2-Input Gate



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

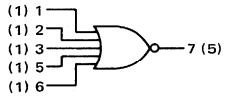
MC915G • MC815G
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

MC929G • MC829G
5-Input Gate

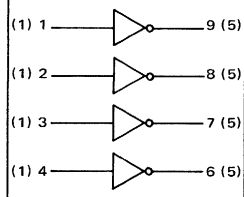


$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

INVERTERS

MC927G • MC827G
Quad Inverter

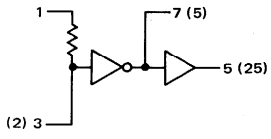


$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

BUFFERS

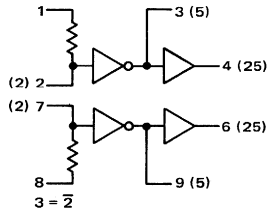
MC900G • MC800G
Buffer



$7 = \overline{3}$
$5 = \overline{3}$

t_{pd} = 20 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999G • MC899G
Dual Buffer

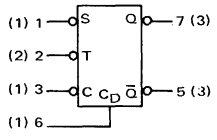


$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

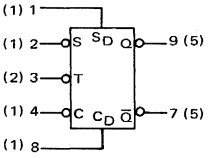
FLIP-FLOPS

MC916G • MC816G
J-K Flip-Flop



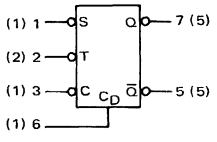
t_{pd} = 30 ns
P_D = 62 mW (Only Clock Input High)
54 mW (Inputs Low)

MC926G • MC826G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

MC974G • MC874G
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Input High)
65 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC926 and MC826 only

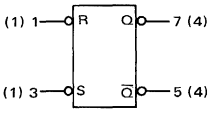
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC902G • MC802G
R-S Flip-Flop

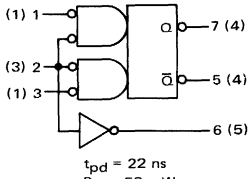


t_{pd} = 14 ns
P_D = 22 mW

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	0

HALF-SHIFT REGISTERS

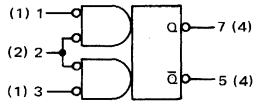
MC905G • MC805G
Half-Shift Register



t_{pd} = 22 ns
P_D = 53 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$
$6 = \overline{2}$

MC906G • MC806G
Half-Shift Register
(Without Inverter)

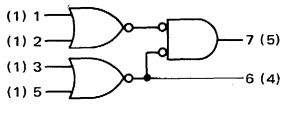


t_{pd} = 22 ns
P_D = 36 mW

$7 = \overline{5}\,(1 + 2)$
$5 = \overline{7}\,(2 + 3)$

HALF ADDERS

MC904G • MC804G
Half Adder

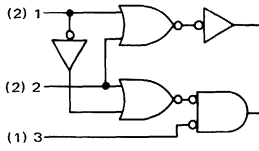


$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$
t_{pd} = 14
P_D = 45

IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

COUNTER ADAPTERS

MC901G • MC801G
Counter Adapter



t_{pd} = 22 ns
P_D = 55 mW

$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$

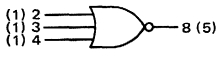
MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these four pages describe the MC900/MC800 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of –55 to +125°C for the MC900 Series, and 0 to +100°C for the MC800 Series, with V_{CC} = 3.0 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

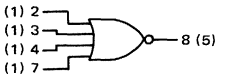
MC903F • MC803F
3-Input Gate



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

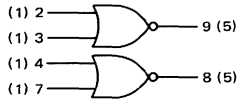
MC907F • MC807F
4-Input Gate



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

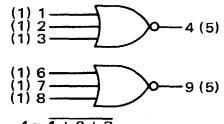
MC914F • MC814F
Dual 2-Input Gate



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

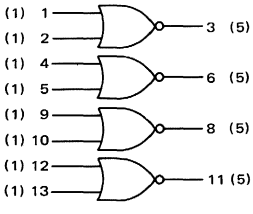
MC915F • MC815F
Dual 3-Input Gate



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

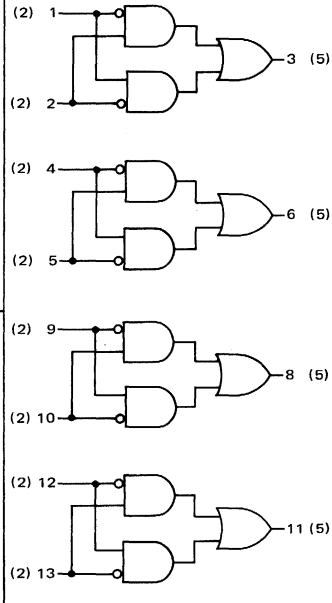
MC924F • MC824F
Quad 2-Input Gate



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

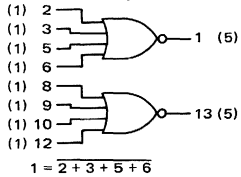
MC971F • MC871F
Quad Exclusive "OR" Gate



$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 72 mW

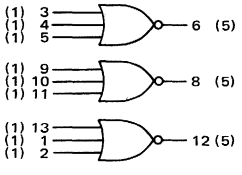
MC925F • MC825F
Dual 4-Input Gate



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 38 mW (Input High)
10 mW (Inputs Low)

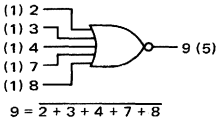
MC992F • MC892F
Triple 3-Input Gate



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 57 mW (Input High)
15 mW (Inputs Low)

MC929F • MC829F
5-Input Gate

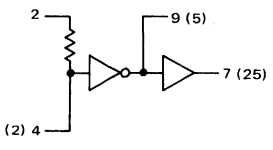


$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 19 mW (Input High)
5 mW (Inputs Low)

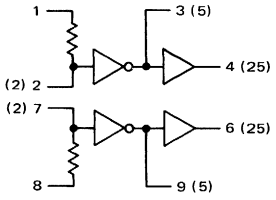
BUFFERS

MC900F • MC800F
Buffer



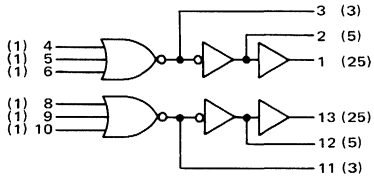
$9 = \overline{4}$
$7 = \overline{4}$
t_{pd} = 15 ns
P_D = 16 mW (Input High)
45 mW (Inputs Low)

MC999F • MC899F
Dual Buffer



$3 = \overline{2}$
$4 = \overline{2}$
t_{pd} = 15 ns
P_D = 32 mW (Input High)
90 mW (Inputs Low)

MC988F • MC888F
Dual 3-Input Buffer
(Non-Inverting)



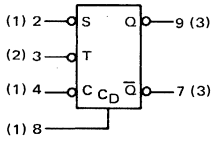
t_{pd} = 24 ns
P_D = 128 mW (Input High)
42 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

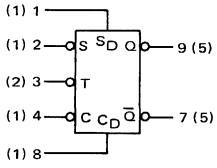
FLIP-FLOPS

MC916F • MC816F
J-K Flip-Flop



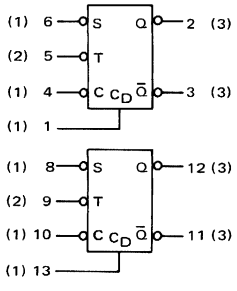
t_{pd} = 35 ns
P_D = 62 mW (Only Clock Inputs High)
54 mW (Inputs Low)

MC926F • MC826F
J-K Flip-Flop



t_{pd} = 35 ns
P_D = 130 mW (Only Clock Inputs High)
65 mW (inputs Low)

MC990F • MC890F
Dual J-K Flip-Flop



t_{pd} = 35 ns
P_D = 124 mW (Only Clock Inputs High)
108 Mw (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

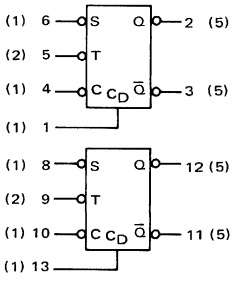
CLOCKED INPUT OPERATION ③
all types

t_n ④		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

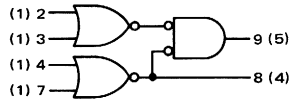
MC991F • MC891F
Dual J-K Flip-Flop



t_{pd} = 40 ns
P_D = 155 mW (Only Clock Input High)
130 mW (Inputs Low)

HALF ADDERS

MC904F • MC804F
Half Adder



$9 = (2 + 3)\ (4 + 7)$

$8 = \overline{4 + 7}$

t_{pd} = 14 ns

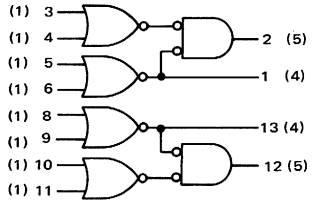
P_D = 45 mW

IF: $4 = \overline{2}$, & $7 = \overline{3}$

THEN: $8 = 2 \cdot 3$

$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

MC975F • MC875F
Dual Half Adder



t_{pd} = 20 ns

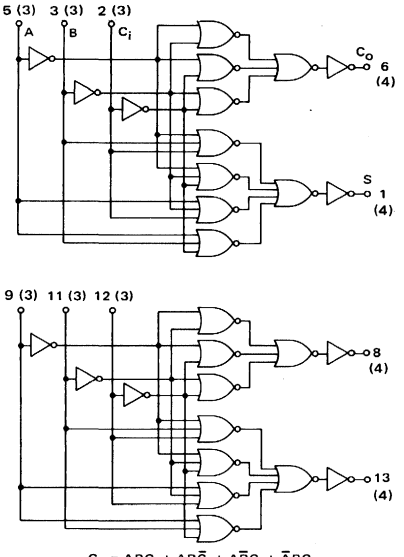
P_D = 120 mW

$2 = (3 + 4)\ (5 + 6)$

$1 = \overline{5 + 6}$

FULL ADDER

MC996F • MC896F
Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i + \overline{A}B\overline{C_i}$

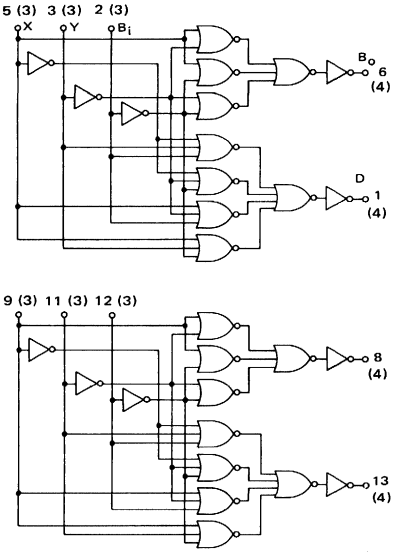
t_{pd} = 60 ns

P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC997F • MC897F
Dual Full Subtractor



$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + \overline{Y}X\overline{B_i} + Y\overline{X}\overline{B_i} + YXB_i$

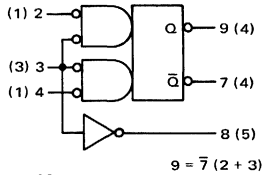
t_{pd} = 60 ns

P_D = 84 mW

TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

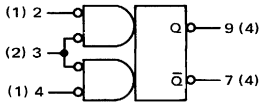
MC905F • MC805F
Half-Shift Register



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 53 mW

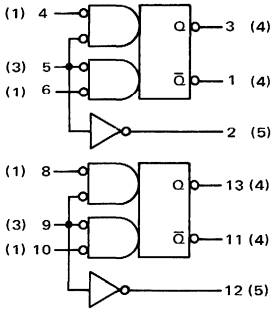
MC906F • MC806F
Half-Shift Register
(Without Inverter)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 36 mW

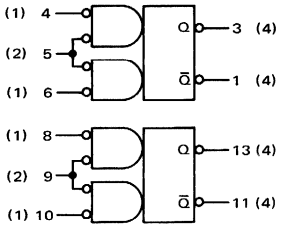
MC983F • MC883F
Dual Half-Shift Register



$1 = \overline{3}\ (6 + 5)$
$3 = \overline{1}\ (5 + 4)$
$2 = \overline{5}$

t_{pd} = 22 ns
P_D = 140 mW

MC984F • MC884F
Dual Half-Shift Register
(Without Inverter)

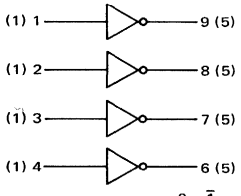


$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 120 mW

INVERTERS

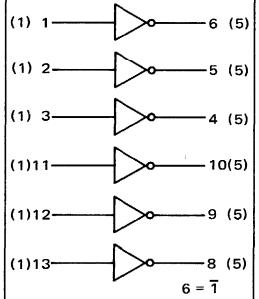
MC927F • MC827F
Quad Inverter



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

MC989F • MC889F
Hex Inverter

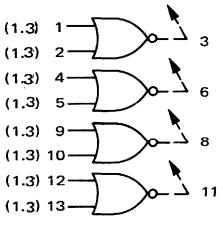


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 76 mW (Input High)
20 mW (Inputs Low)

EXPANDERS

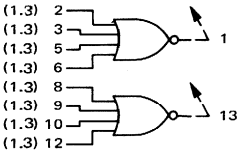
MC985F • MC885F
Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 17 mW (Input High)
Negligible (Inputs Low)

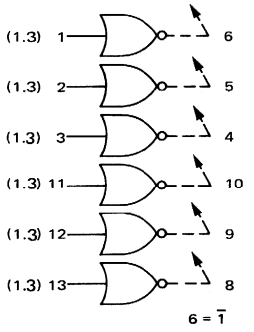
MC986F • MC886F
Dual 4-Input Expander



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 17 mW (Input High)
Negligible (Inputs Low)

MC9919F • MC9819F
Hex Expander



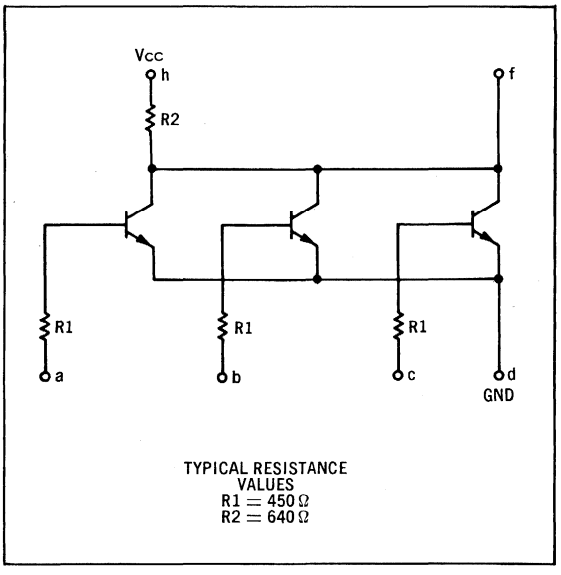
$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

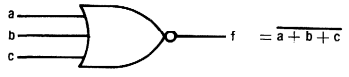
MC903 • MC803

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules)



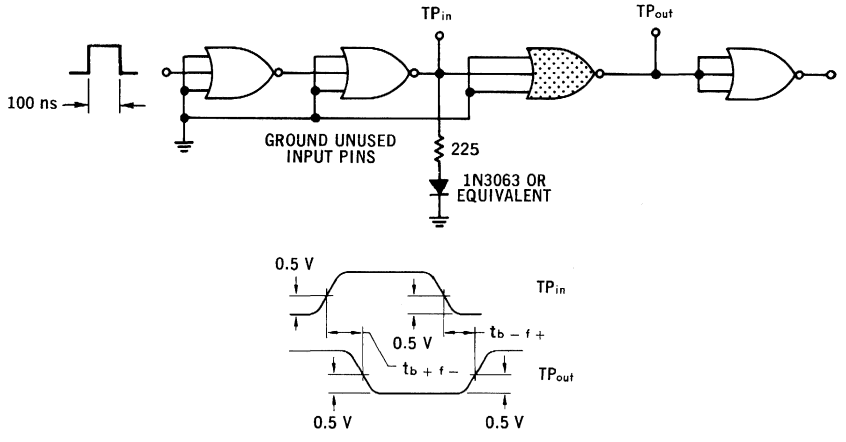
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω



PIN CONNECTIONS

SCHEMATIC	a	b	c	d	—	f	—	h
G PACKAGE (TO-99)	1	2	3	4	—	6	—	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

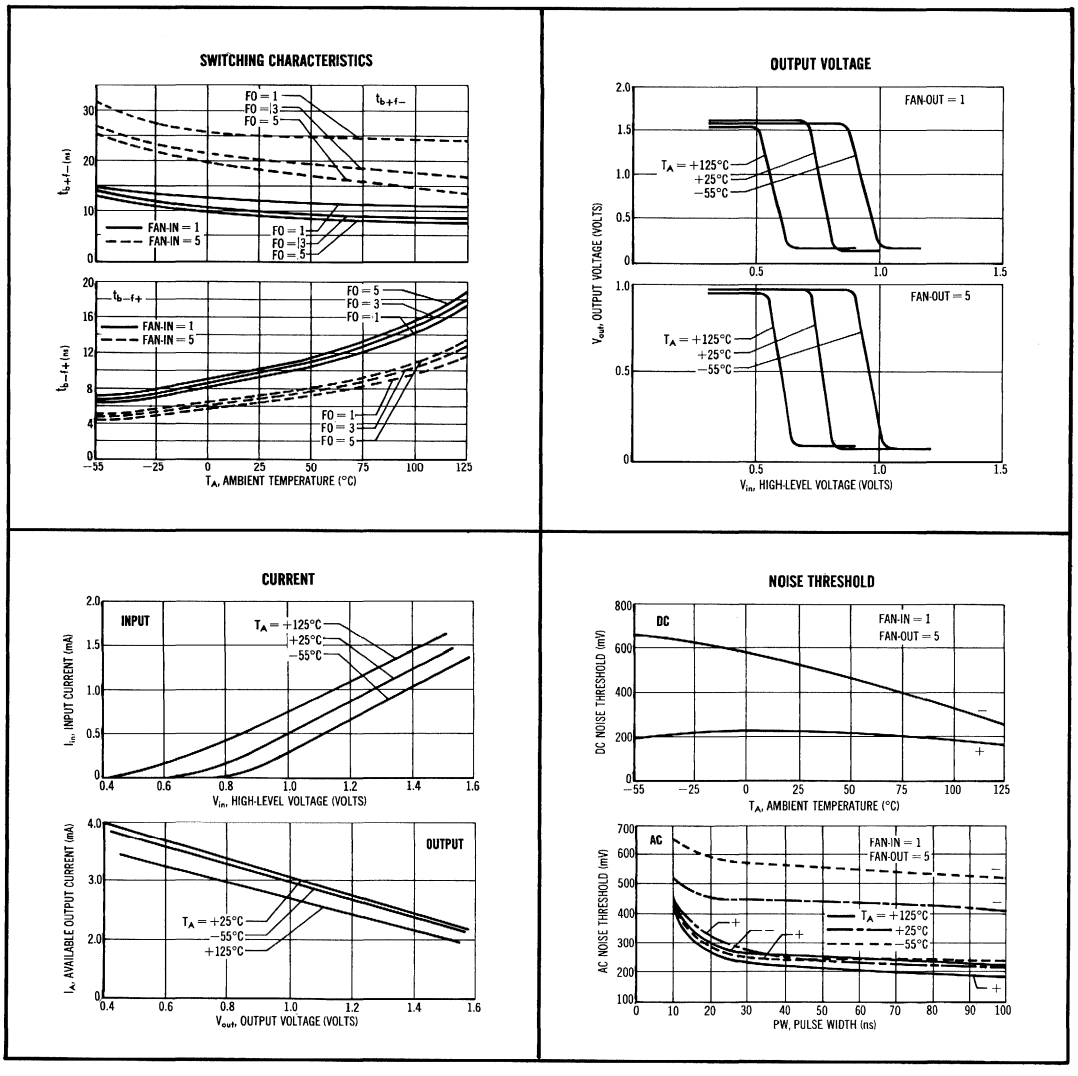
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC903	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC803	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC903 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC803 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b, c	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b	-		
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	f	-	-	a, b, c	-	d
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
																	Pulse In	Pulse Out				
Switching Time	t	b+f-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	b	f	-	-	h	d
		b-f+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	b	f	-	-	h	d

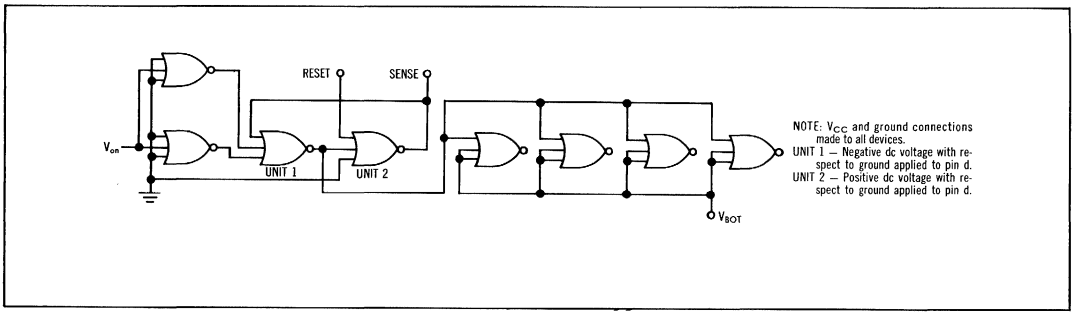
Pins not listed are left open

Pins e and g omitted

TYPICAL CURVES



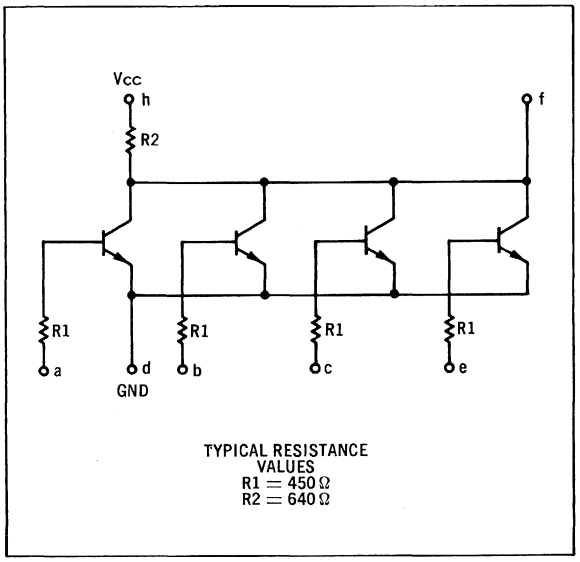
TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS



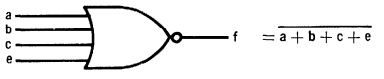
MC907 • MC807

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



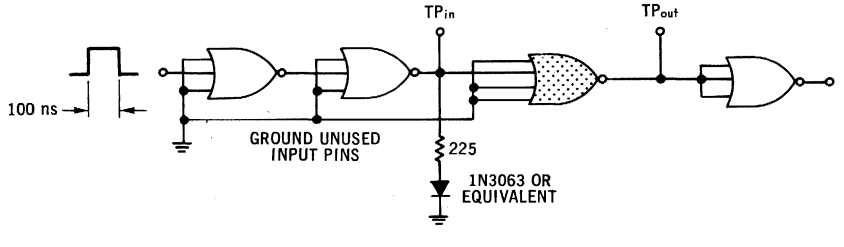
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

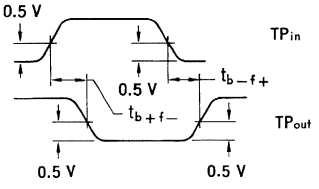


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	—	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC907	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC807	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

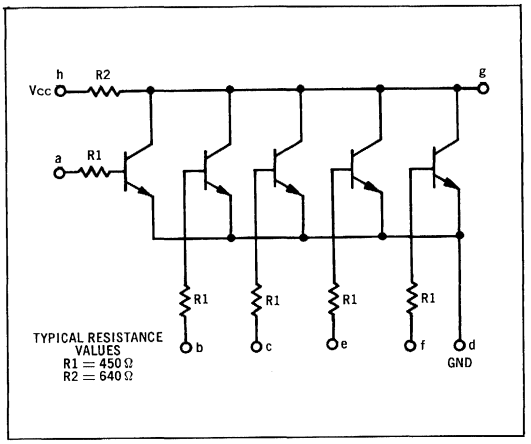
Characteristic	Symbol	Pin Under Test	MC907 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC807 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b, c, e	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e	-		
		e	-		-		-			-		-		-			e	-	a, b, c	-		
Output Current	I_{A5}	f	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	f	-	a, b, c, e	h	d
Output Leakage Current	I_{CEX}	f	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	f	-	-	a, b, c, e	-	d
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
			-		-		-			-		-		-			-	c	-	-		
			-		-		-			-		-		-			-	e	-	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	↓
			-		-		-			-		-		-			-	-	c	-		
			-		-		-			-		-		-			-	-	e	-		
																	Pulse In	Pulse Out				
Switching Time	t	b+f-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	b	f	-	-	h	d
		b-f+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	b	f	-	-	h	d

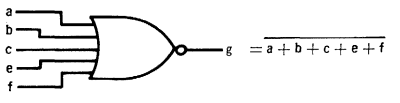
Pins not listed are left open.

MC929 • MC829

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Provides positive logic NOR function. Individual gates may be paralleled with other logic elements for increasing the number of inputs (subject to loading rules).

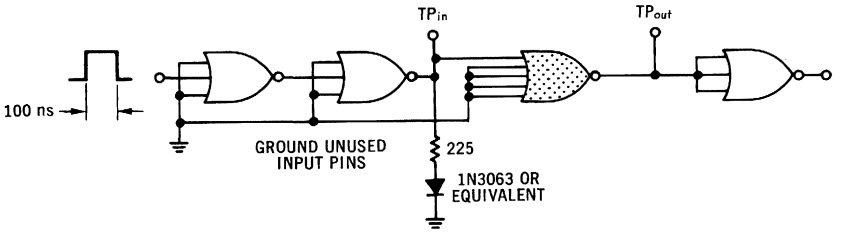


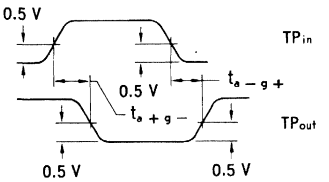


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC929	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC829	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

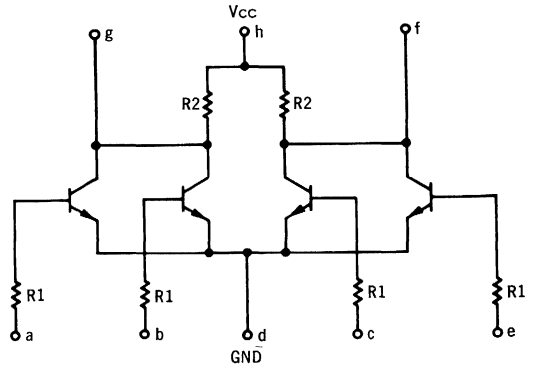
Characteristic	Symbol	Pin Under Test	MC929 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC829 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b, c, e, f	-	h	d
		b	-		-		-			-		-		-			b	-	a, c, e, f	-		
		c	-		-		-			-		-		-			c	-	a, b, e, f	-		
		e	-		-		-			-		-		-			e	-	a, b, c, f	-		
		f	-		-		-			-		-		-			f	-	a, b, c, e	-		
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a,b,c,e,f	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	g	-	-	a,b,c,e,f	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
			-		-		-			-		-		-			-	b	-	-		
			-		-		-			-		-		-			-	c	-	-		
			-		-		-			-		-		-			-	e	-	-		
			-		-		-			-		-		-			-	f	-	-		
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
			-		-		-			-		-		-			-	-	b	-		
			-		-		-			-		-		-			-	-	c	-		
			-		-		-			-		-		-			-	-	e	-		
			-		-		-			-		-		-			-	-	f	-		
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	Pulse In: a	Pulse Out: g	-	-	h	b,c,d,e,f
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	b,c,d,e,f

Pins not listed are left open.

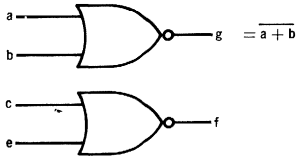
MC914 • MC814

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



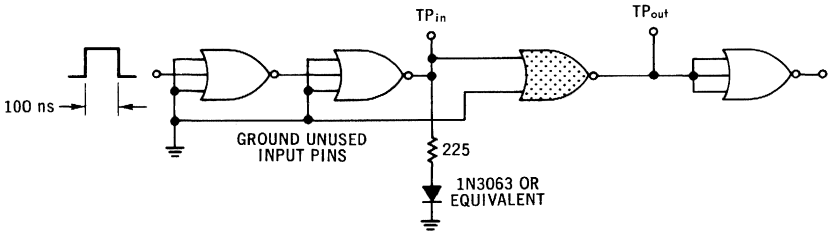
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

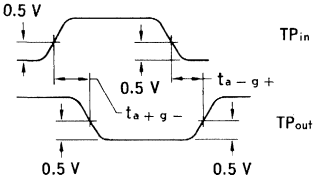


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC914	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC814	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

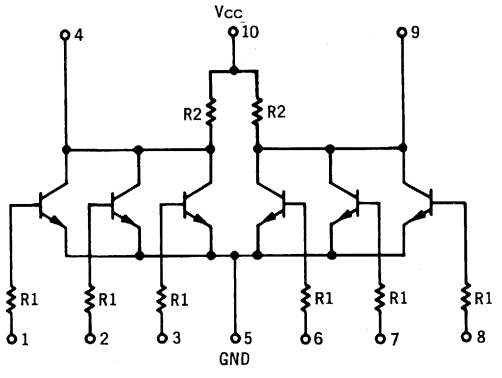
Characteristic	Symbol	Pin Under Test	MC914 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC814 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
		b	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	b	-	a	-	h	d
Output Current	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	a, b	h	d
Output Leakage Current	I_{CEX}	g	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	g	-	-	a, b	-	d
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	a	-	-	h	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	b	-	-	h	d
Saturation Voltage	$V_{CE(sat)}$	g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a	-	h	d
		g	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	b	-	h	d
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	a	g	-	-	h	d
		a-g+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	a	g	-	-	h	d

Ground inputs of gate not under test. Other pins not listed are left open.

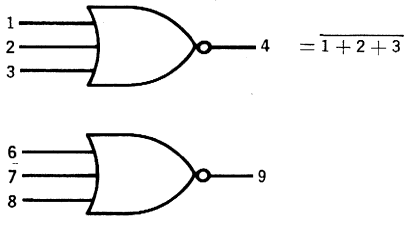
MC915 • MC815

Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Two 3-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

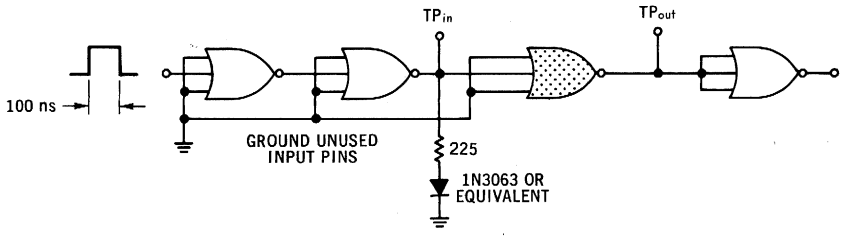


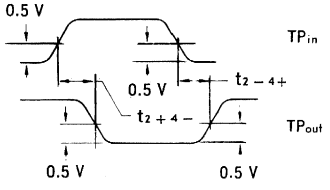
TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω



"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC915 −55°C	1.014	1.014	1.50	0.710	3.00
MC915 +25°C	0.844	0.815	1.50	0.565	3.00
MC915 +125°C	0.674	0.674	1.50	0.320	3.00
MC815 0°C	0.909	0.909	1.50	0.574	3.00
MC815 +25°C	0.844	0.844	1.50	0.554	3.00
MC815 +100°C	0.710	0.710	1.50	0.370	3.00

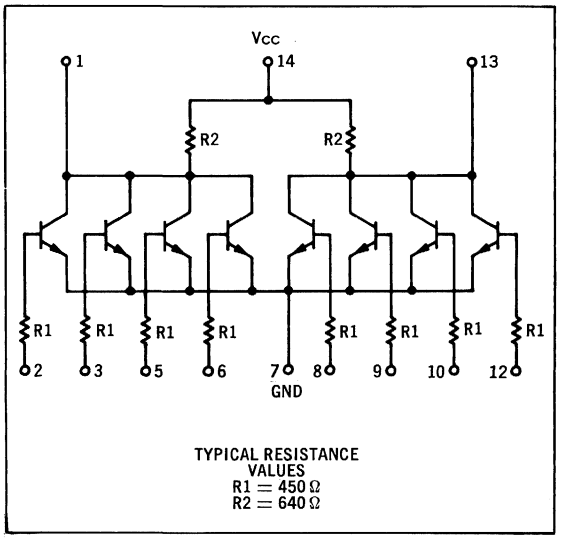
Characteristic	Symbol	Pin Under Test	MC915 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC815 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	2,3	-	10	5
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,3	-	↓	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	1,2	-	↓	↓
Output Current	I_{A5}	4	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	4	-	1,2,3	10	5
Output Leakage Current	I_{CEX}	4	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	4	-	-	1,2,3	-	5
Output Voltage	V_{out}	4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	4	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	10	5
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	↓
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓
																	Pulse In	Pulse Out				
Switching Time	t	2+4-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	2	4	-	-	10	5
		2-4+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	2	4	-	-	10	5

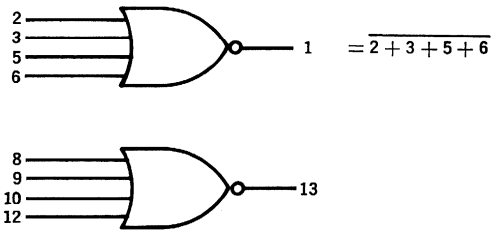
Ground inputs of gate not under test. Other pins not listed are left open.

MC925 • MC825

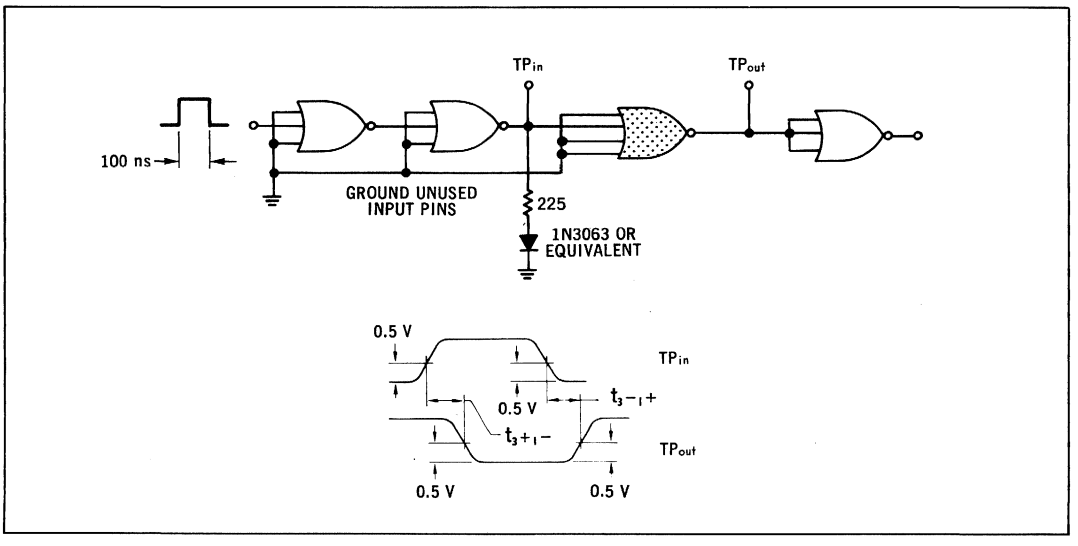
Available in TO-86 Flat Package, Add "F" Suffix.

Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC925	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC825	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

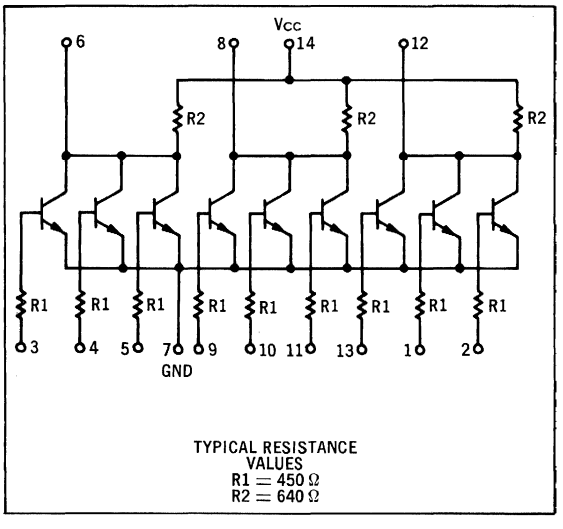
Characteristic	Symbol	Pin Under Test	MC925 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC825 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	3,5,6	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,5,6	-	↓	↓
		5	-		-		-			-		-		-			5	-	2,3,6	-		
		6	-		-		-			-		-		-			6	-	2,3,5	-		
Output Current	I_{A5}	1	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1	-	2,3,5,6	14	7
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	1	-	-	2,3,5,6	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2,5,6,7
			-		-		-			-		-		-			-	5	-	-		2,3,6,7
			-		-		-			-		-		-			-	6	-	-		2,3,5,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3,5,6,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	2,5,6,7
			-		-		-			-		-		-			-	-	5	-		2,3,6,7
			-		-		-			-		-		-			-	-	6	-		2,3,5,7
																	Pulse In	Pulse Out				
Switching Time	t	3+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	3	1	-	-	14	2,5,6,7
		3-1+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	3	1	-	-	14	2,5,6,7

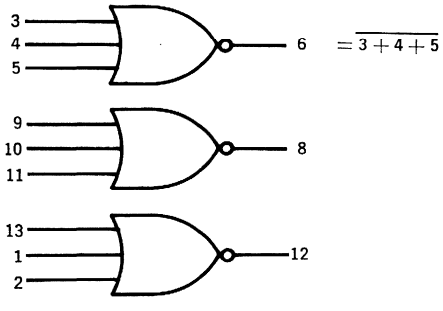
Ground inputs of gate not under test. Other pins not listed are left open.

MC992 • MC892

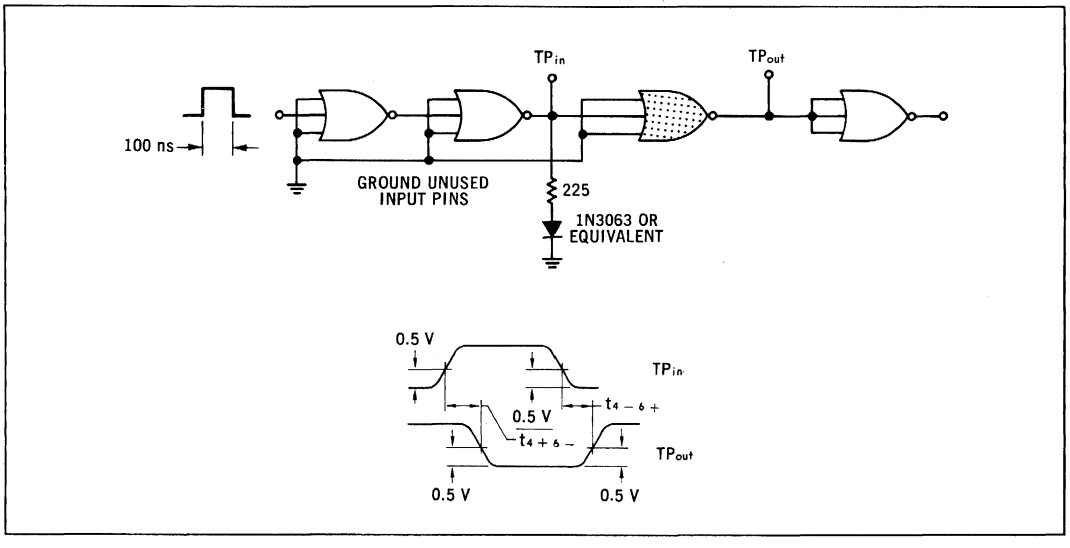
Available in TO-86 Flat Package, Add "F" Suffix.

Three 3-input positive logic NOR gates in a single package may be used independently, paralleled for increased number of inputs (subject to loading rules), or cross coupled to form bistable elements.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC992	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC892	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

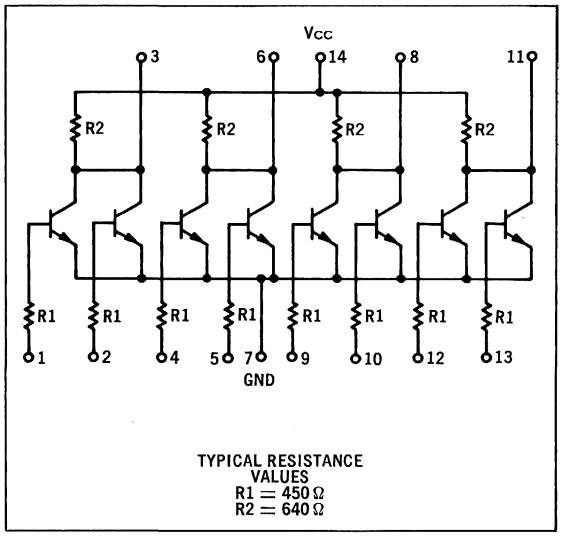
Characteristic	Symbol	Pin Under Test	MC992 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC892 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	3	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	3	-	4,5	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3,5	-	↓	↓
		5	-		-		-			-		-		-			5	-	3,4	-		
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	3,4,5	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	3,4,5	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	3,5,7
			-		-		-			-		-		-			-	5	-	-		3,4,7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	4,5,7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	3,5,7
			-		-		-			-		-		-			-	-	5	-		3,4,7
																	Pulse In	Pulse Out				
Switching Time	t	4+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	4	6	-	-	14	3,5,7
		4-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	4	6	-	-	14	3,5,7

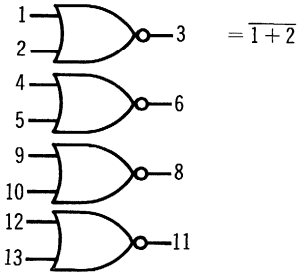
Ground inputs of gates not under test. Other pins not listed are left open.

MC924 • MC824

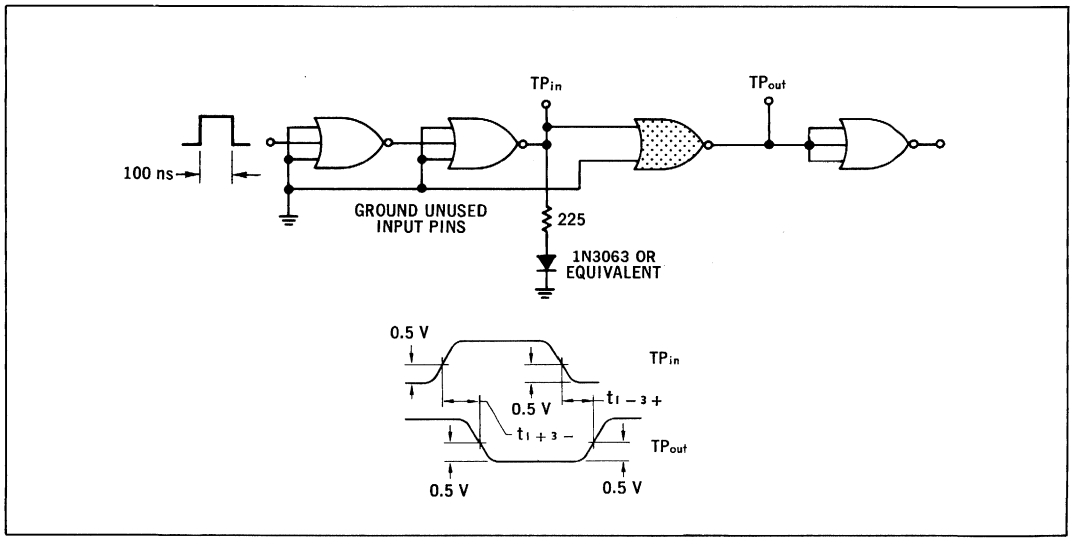
Available in TO-86 Flat Package, Add "F" Suffix.

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. The gate circuits may be used independently, or connected together to form flip-flops or non-inverting gates.





SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
Other gates are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC924	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC824	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

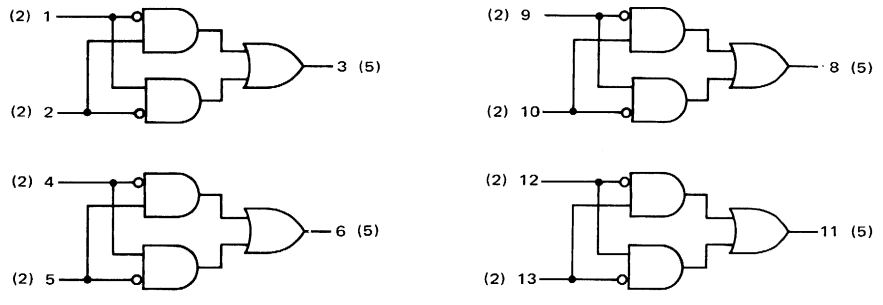
Characteristic	Symbol	Pin Under Test	MC924 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC824 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	2	-	14	7
		2	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	2	-	1	-	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	3	-	-	1,2	14	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	-	3	-	1,2	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1,7
																	Pulse In	Pulse Out				
Switching Time	t	1+3-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	3	-	-	14	2,7
		1-3+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	3	-	-	14	2,7

Ground inputs of gates not under test. Other pins not listed are left open.

MC971 • MC871

Available in TO-86 flat package, add "F" suffix

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



POSITIVE LOGIC
$3 = 1\cdot\overline{2} + \overline{1}\cdot 2$

t_{pd} = 12 ns typ
P_D = 72 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

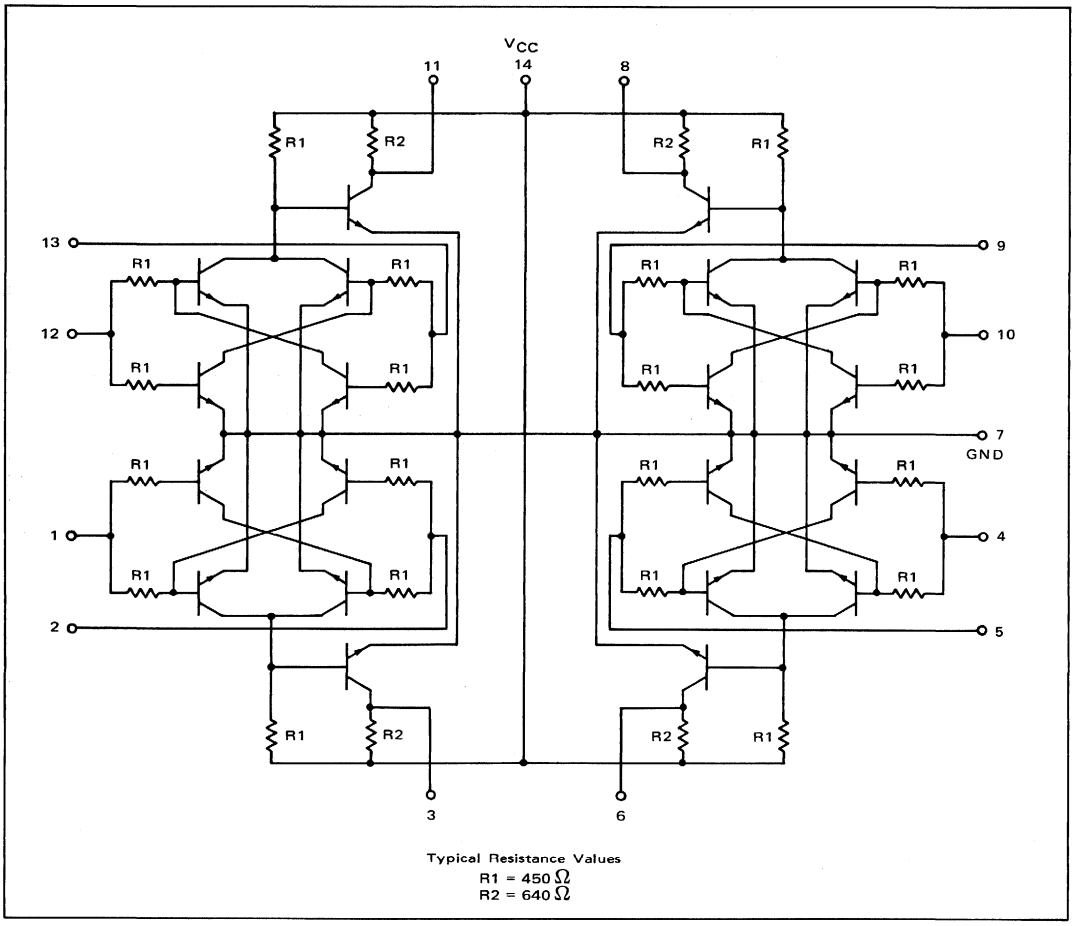
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

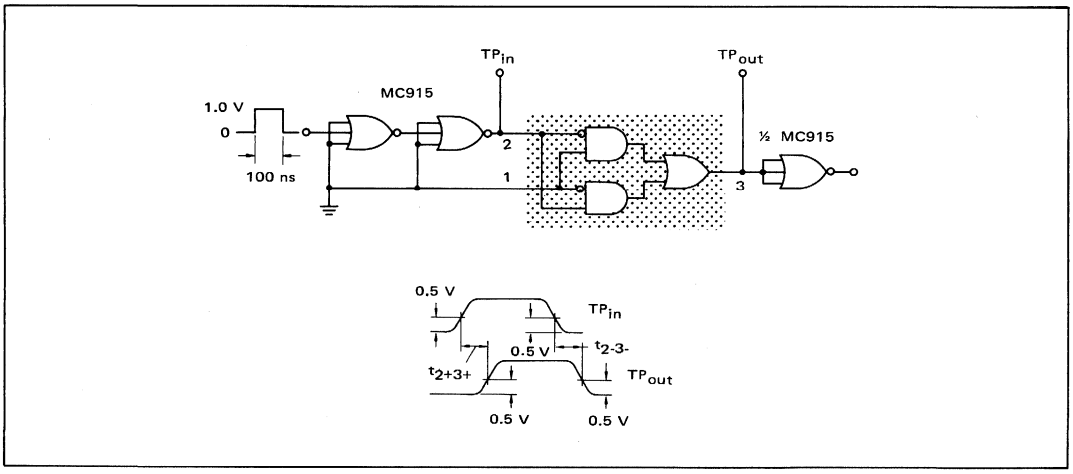
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC971	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC871	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC971 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC871 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	990	-	870	-	940	µAdc	-	1008	-	900	-	900	µAdc	1	-	-	2	14	7
		2	-	990	-	870	-	940	µAdc	-	1008	-	900	-	900	µAdc	2	-	-	1	14	7
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1,3	-	2	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	2,3	-	1	14	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	1,2	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1,2	-	-	14	7
Switching Time	t	1+3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In: 1	2	Pulse Out: 3	-	14	7
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2+3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓
		2-3-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	2	-	↓	1	↓	↓

Ground inputs of gates not under test. Other pins not listed are left open.



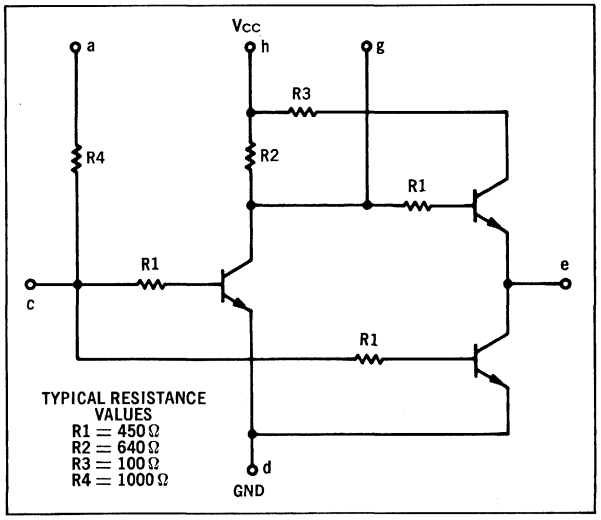
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

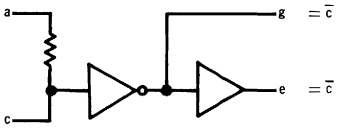


MC900 • MC800

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

The buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms, and various multivibrator applications.



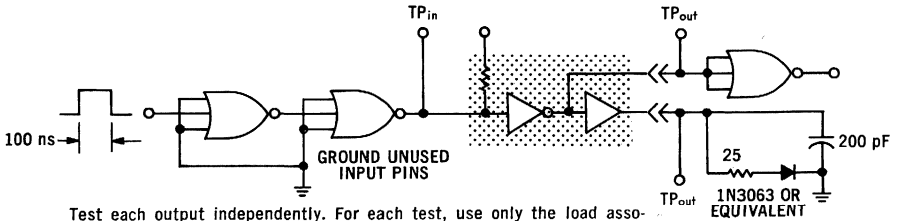


Outputs e and g may not be used simultaneously

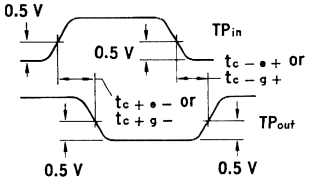
PIN CONNECTIONS

SCHEMATIC	a	—	c	d	e	—	g	h
G PACKAGE (TO-99)	1	—	3	4	5	—	7	8
F PACKAGE (TO-91)	.2	3	4	5	7	8	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

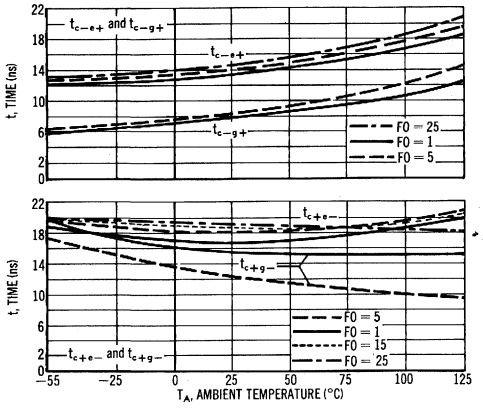
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC900	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC800	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC900 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC800 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\,I_{in}$	c	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	c	-	-	-	h	-	d
Output Current	I_{AB}	e	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	e	-	c	h	-	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	g	-	c	h	-	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	e	d
		g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	e	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c	-	h	-	↓
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	a,h	-	↓
Switching Time	t	c+e-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In: c	Pulse Out: e	-	-	h	-	d
		c-e+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	↓	e	-	-	↓	-	↓
		c+g-	-	-	-	28	-	-		-	-	-	28	-	-			g	-	-		-	
		c-g+	-	-	-	32	-	-		-	-	-	32	-	-			g	-	-		-	

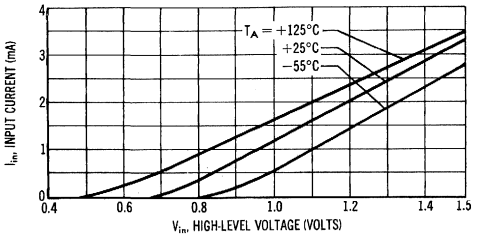
Pins not listed are left open.

* Resistor Value to V_{CC}

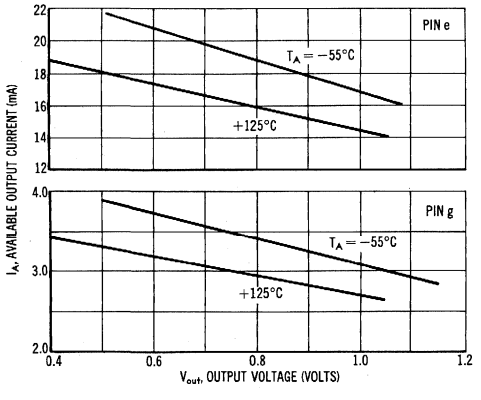
SWITCHING CHARACTERISTICS



INPUT CURRENT

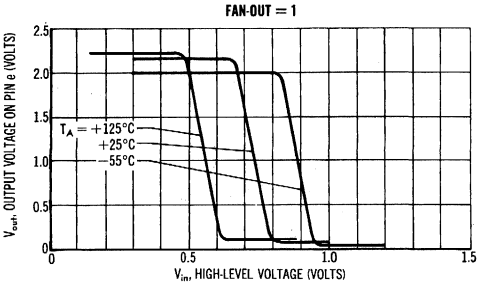


AVAILABLE OUTPUT CURRENT

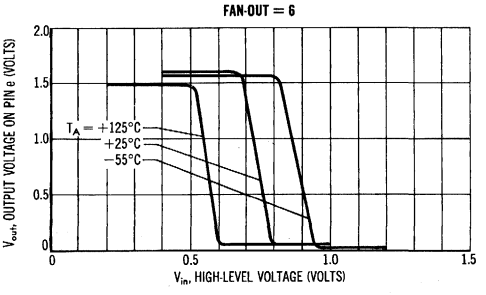


OUTPUT VOLTAGE

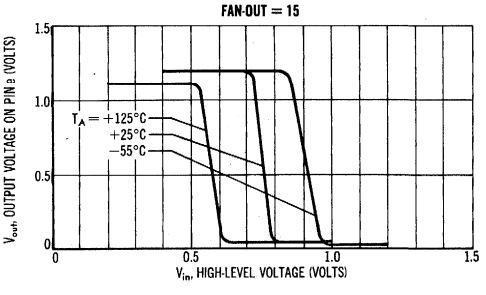
FAN-OUT = 1



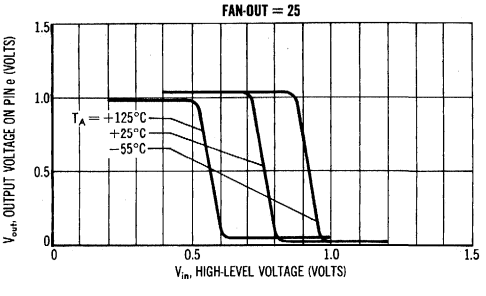
FAN-OUT = 6



FAN-OUT = 15



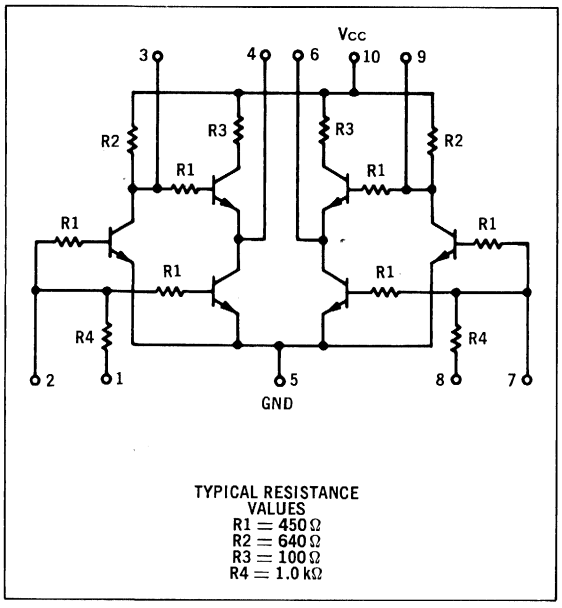
FAN-OUT = 25



MC999 • MC899

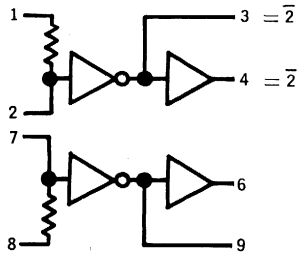
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



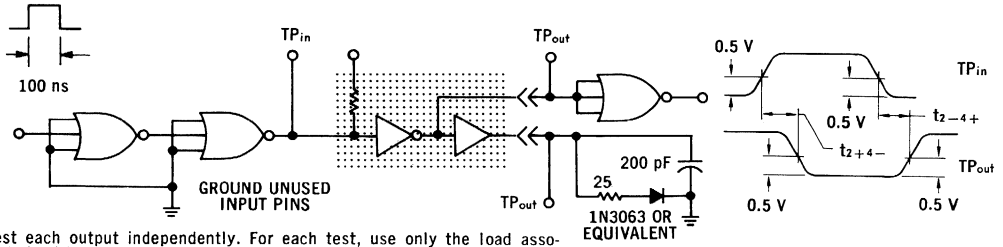
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω
R4 = 1.0 kΩ

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME



Outputs 3 and 4 may not be used simultaneously
Outputs 9 and 6 may not be used simultaneously

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC999	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC899	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

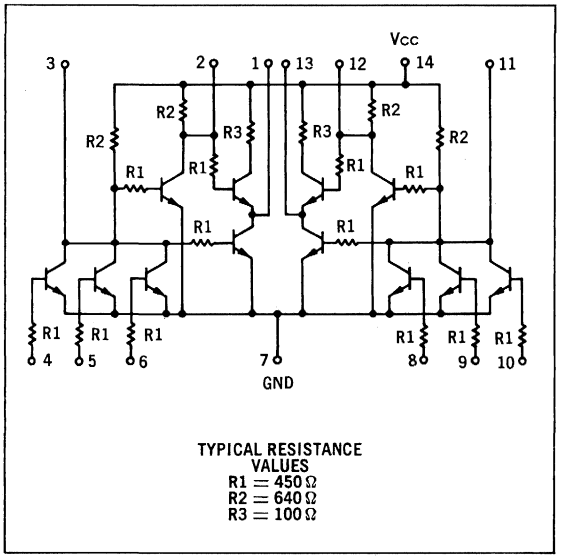
Characteristic	Symbol	Pin Under Test	MC999 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC899 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Grd
Input Current	$2\,I_{in}$	2	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	2	-	-	-	10	-	5
Output Current	I_{A5}	3	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	3	-	2	10	-	5
	I_{AB}	4	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	4	-	2	10	-	5
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	-	5
		4	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	10	4	5
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	10	-	5
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	-	1, 10	-	↓
		4	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	2	-	10	4	↓
Switching Time	t	2+3-	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	Pulse In: 2	Pulse Out: 3	-	-	10	-	5
		2-3+	-	-	-	32	-	-		-	-	-	32	-	-		↓	3	-	-	↓	-	↓
		2+4-	-	-	-	30	-	-		-	-	-	30	-	-			4	-	-		-	
		2-4+	-	-	-	45	-	-		-	-	-	45	-	-		↓	4	-	-	↓	-	↓

Ground inputs of buffer not under test. Other pins not listed are left open.

* Resistor value to V_{CC}

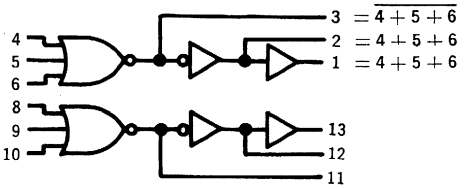
MC988 • MC888

Available in TO-86 Flat Package, Add "F" Suffix.



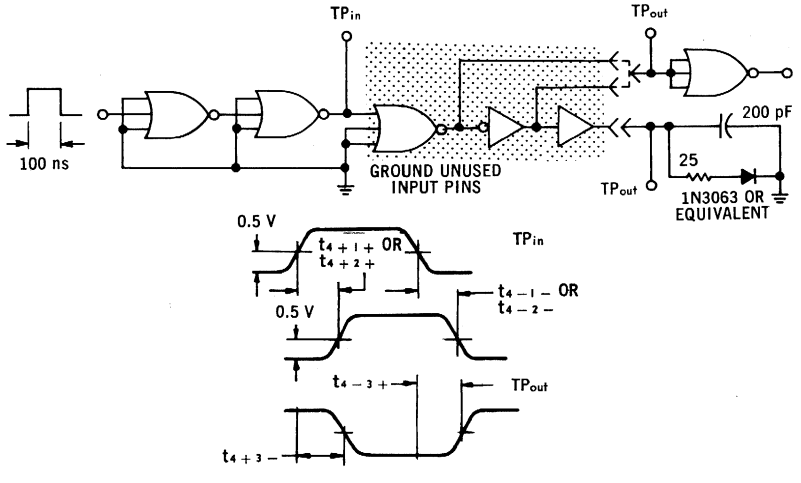
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and a non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, however, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.



Outputs 1, 2, or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



Test each output independently. For each test, use only the load associated with the output under test (pin 2 test uses the same load as pin 3 test). Outputs not under test should be left open.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC988	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC888	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

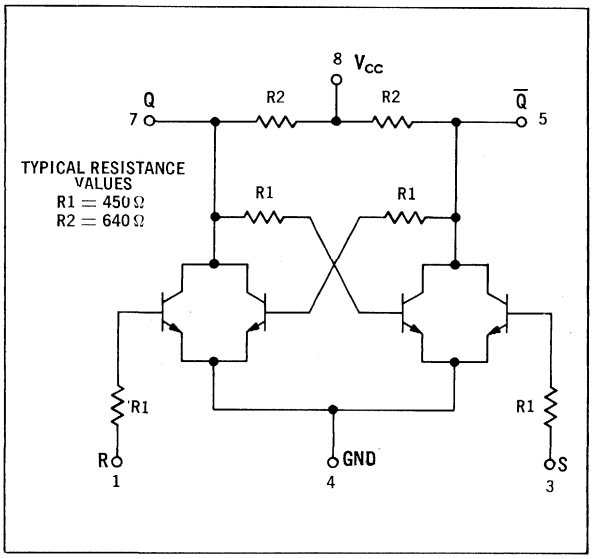
Characteristic	Symbol	Pin Under Test	MC988 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC888 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5,6	-	14	-	7
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	4,6	-	↓	-	↓
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	4,5	-	↓	-	↓
Output Current	I_{AB}	1	12.4	-	12.7	-	11.8	-	mAdc	12.6	-	11.9	-	11.25	-	mAdc	-	1	-	3	14	-	7,11
	I_{A5}	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2	-	3	↓	-	7,11
	I_{A3}	3	1.48	-	1.52	-	1.41	-	↓	1.51	-	1.43	-	1.35	-	↓	-	3	-	4,5,6	↓	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	-	-	14	1	4,5,6,7,11
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	4,5,6,7,11
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	-	4,5,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	4	-	-	↓	-	5,6,7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	3	-	14	1	4,5,6,7,11
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	-	4,5,6,7,11
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	-	4,5,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	5	-	↓	-	4,6,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4	-	↓	-	5,6,7
																	Pulse In	Pulse Out					
Switching Time	t	4+1+	-	-	-	65	-	-	ns	-	-	-	65	-	-	ns	4	1	-	-	14	-	5,6,7
		4-1-	-	-	-	58	-	-	↓	-	-	-	58	-	-	↓	4	1	-	-	↓	-	↓
		4+2+	-	-	-	42.5	-	-	↓	-	-	-	42.5	-	-	↓	4	2	-	-	↓	-	↓
		4-2-	-	-	-	42.5	-	-	↓	-	-	-	42.5	-	-	↓	4	2	-	-	↓	-	↓
		4+3-	-	-	-	20	-	-	↓	-	-	-	20	-	-	↓	4	3	-	-	↓	-	↓
		4-3+	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	4	3	-	-	↓	-	↓

Ground inputs of buffer not under test. Other pins not listed are left open.

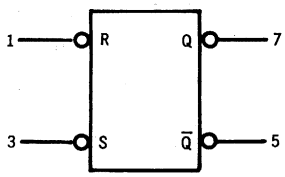
* Resistor Value to V_{CC}.

MC902 • MC802

Available in TO-99 Metal Can, Add "G" Suffix

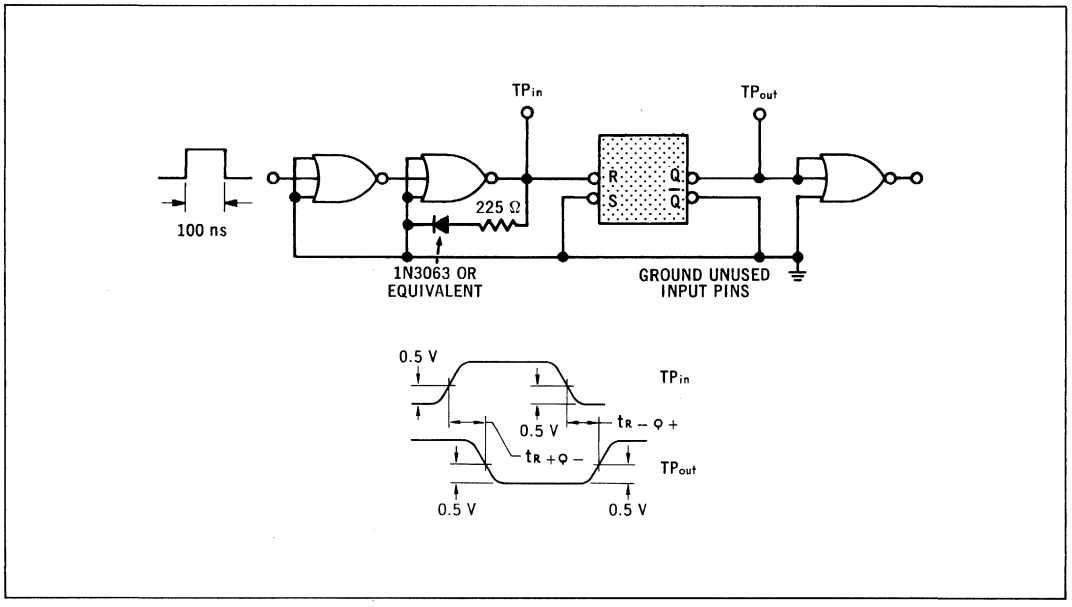


This flip-flop is formed by internally cross-coupling two basic RTL NOR gates.



R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	0

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



ELECTRICAL CHARACTERISTICS

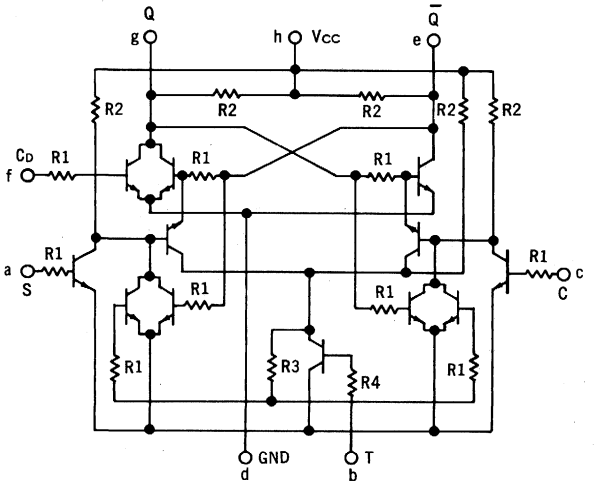
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC902	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC802	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC902 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC802 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	5	-	8	4
		3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	7	-	8	4
Output Current	I_{A4}	5	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	5	1	3	8	4
	I_{A4}	7	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	7	3	1	8	4
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	1	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	7	-	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	3	-	↓	↓
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1,3	-	8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	4,5 †
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1,3	-	↓	4
		7	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	3	↓	4,7 †
																	Pulse In	Pulse Out				
Switching Time	t	1+7-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	7	-	-	8	4
		1-7+	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	7	-	-	8	4

Pins 2 and 6 omitted. Other pins not listed are left open. † Silicon Diode to Ground

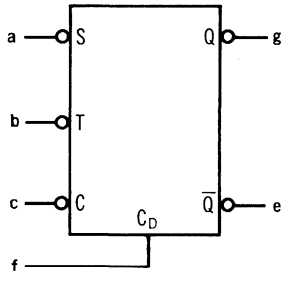
MC916 • MC816

Available in TO-99 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

J-K flip-flop with a direct clear input in addition to the clocked input.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transistion is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.

PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC916	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC816	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC916 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC816 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	e	-	h	d
	$2\ I_{in}$	b	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	b	-	a, c, g	-	↓	↓
	I_{in}	c	-	495	-	435	-	470		-	504	-	450	-	450		c	-	g	-		
		f	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	f	-	e	-	↓	↓
Output Current	I_{A3}	e	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	e	a, f	-	h	d
		e	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	e, f	a	-	↓	d
		g		-		-		-			-		-		-		-	g	c	f		d, e †
Output Voltage	V_{out}	g	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	f	-	-	h	
		g‡#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	a, c	-	-	↓	
		g‡	-		-		-			-		-		-			-	c	-	a		d, e
		g‡§	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	-	a, c		d, f
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	-	f	h	d, e †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	f	-	↓	d, e
		g	-		-		-			-		-		-			-	-	-	-		d, g †
Turn-On Voltage	V_{on}	g‡§	1014	-	815	-	674	-	mVdc	909	-	844	-	710	-	mVdc	-	a, c	-	-	h	d, f
		g‡	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	a	-	c	↓	
		g‡#*		-		-		-			-		-		-		-	-	-	a, c		

† Silicon Diode to Ground

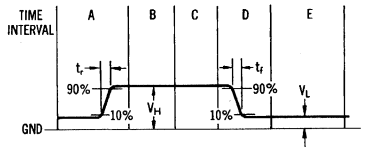
* MC916 pin g loaded by: 1.52 mAdc (+25°C), 1.48 mAdc (−55°C), 1.41 mAdc (+125°C); MC816 pin g loaded by: 1.42 mAdc (+25°C), 1.51 mAdc (0°C), 1.35 mAdc (+100°C)

Pins not listed are left open.

‡ Pin b = Clock pulse to pin b (see Figure 1).

§ Pin e = LOW, # Pin g = LOW } Set by a momentary ground prior to the application of the negative-going Clock Pulse.

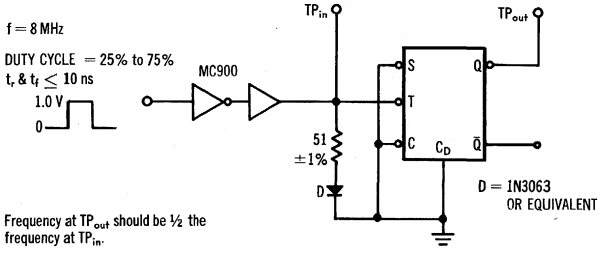
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

MC816		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC916		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

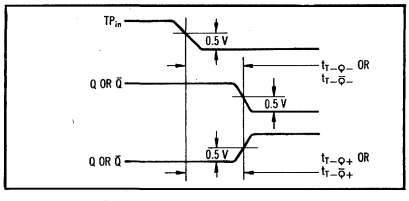


FIGURE 3B — SET-UP AND RELEASE TIME

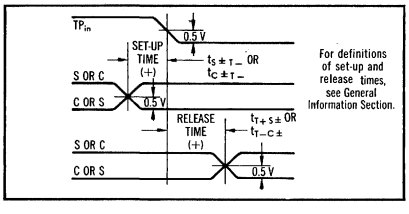
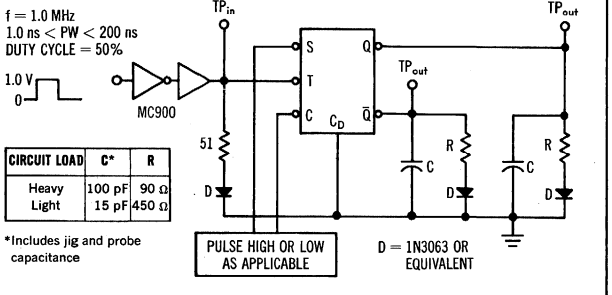


FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

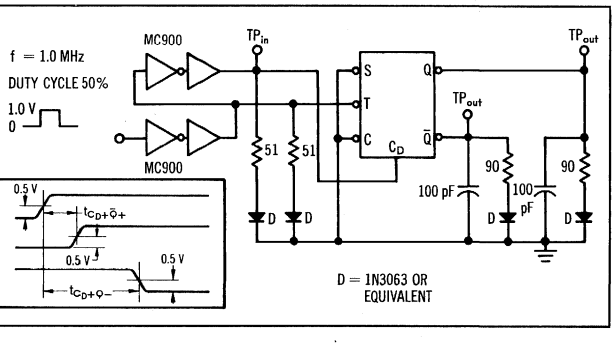
*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	60
$t_{T-\bar{Q}-}$	3A, 3C	60
t_{T-Q+}	3A, 3C	100
$t_{T-\bar{Q}+}$	3A, 3C	100
$t_{S\pm T-}$	3B, 3C	50
$t_{C\pm T-}$	3B, 3C	50
$t_{T-S\pm}$	3B, 3C	50
$t_{T-C\pm}$	3B, 3C	50
t_{CD+Q-}	4	50
$t_{CD+\bar{Q}+}$	4	90

1. Change of state occurs on trailing edge of clock pulse.
2. With a high level on C_D, and with the proper SET and CLEAR inputs for a low level at $\bar{Q}$, $\bar{Q}$ will be high except for a short period after the negative-going edge of a clock pulse. $\bar{Q}$ will go low for up to 50 ns, and then return to a high level within 100 ns after a negative clock transition.

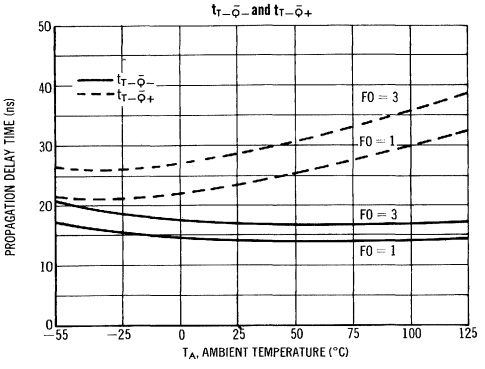
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



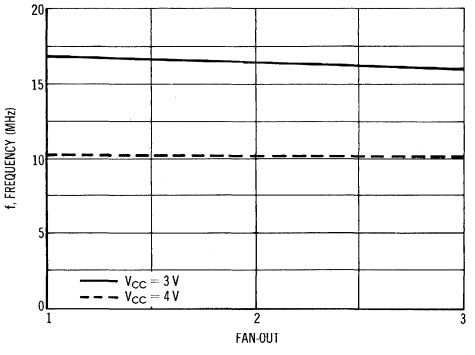
TYPICAL CURVES

TYPICAL PROPAGATION DELAY TIME

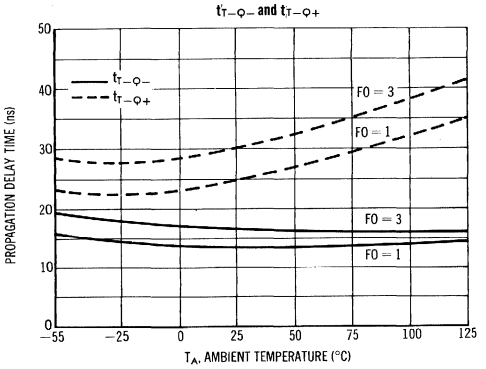
$t_{T-\bar{Q}-}$ and $t_{T-\bar{Q}+}$



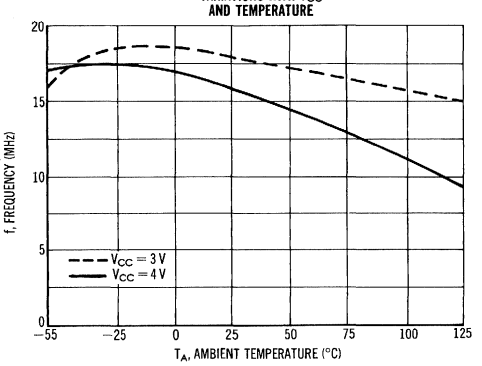
TOGGLE FREQUENCY VARIATIONS WITH FAN-OUT AND V_{CC}



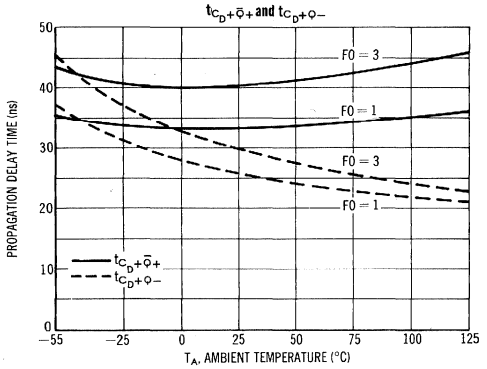
t_{T-Q-} and t_{T-Q+}



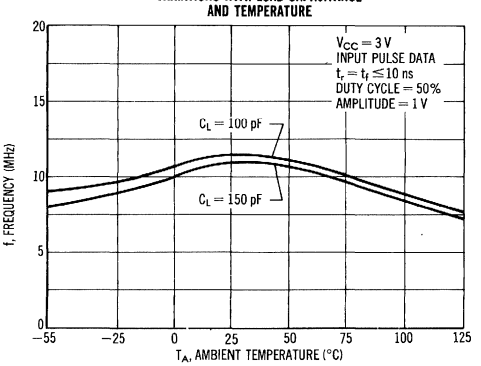
VARIATIONS WITH V_{CC} AND TEMPERATURE



$t_{C_D+\bar{Q}+}$ and t_{C_D+Q-}



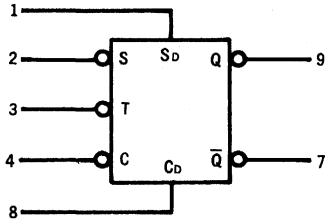
VARIATIONS WITH LOAD CAPACITANCE AND TEMPERATURE



MC926 • MC826

Available in TO-100 Metal Can, Add "G" Suffix
Available in TO-91 Flat Package, Add "F" Suffix

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



t_{pd} = 35 ns typ
P_D = 130 mW typ (Only Clock Input High)
65 mW typ (Inputs Low)

DIRECT INPUT OPERATION①

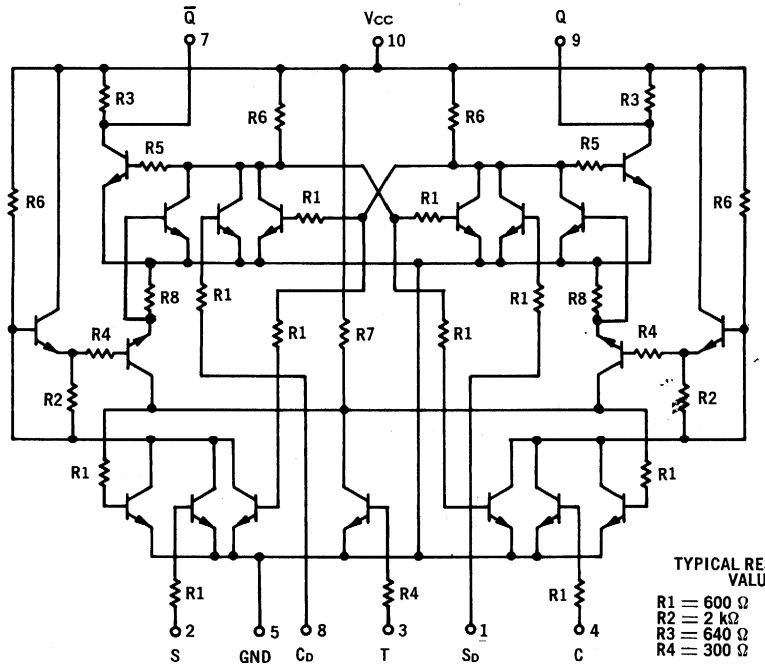
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④		t_{n+1}④	
S	C	Q	$\overline{Q}$
1	1	Q_n⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

① Clock (T) to remain unchanged.
② The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
③ Direct inputs (C_D and S_D) must be low.
④ The time period prior to the negative transistor of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
⑤ Q_n is the state of the Q output in the time period t_n.

"F" PACKAGE AND "G" PACKAGE
PIN-OUTS ARE THE SAME.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 kΩ	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 kΩ

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC926	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC826	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

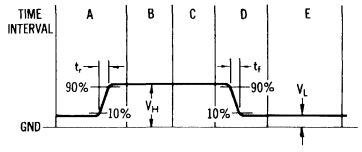
Characteristic	Symbol	Pin Under Test	MC926 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC826 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	10	5
	I_{in}	2	-	495	-	435	-	470		-	504	-	450	-	450		2	-	8	-		
	$2\ I_{in}$	3	-	990	-	870	-	940		-	1010	-	900	-	900		3	-	2,4	-		
	I_{in}	4	-	495	-	435	-	470		-	504	-	450	-	450		4	-	1	-		
	I_{in}	8	-	495	-	435	-	470		-	504	-	450	-	450		8	-	-	-		
Output Current	I_{A5}	7	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7,8	1	-	10	5
		9	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	1,9	8	-	10	5
Saturation Voltage	$V_{CE(sat)}$	7	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	8	10	5
		7#‡	-		-		-			-		-		-			-	2	-	4		
		7#‡	-		-		-			-		-		-			-	-	-	2,4		
		7§‡	-		-		-			-		-		-			-	2,4	-	-		
		9	-		-		-			-		-		-			-	8	-	1		
		9§‡	-		-		-			-		-		-			-	4	-	2		
		9#‡	-		-		-			-		-		-			-	2,4	-	-		
		9§‡	-		-		-			-		-		-			-	-	-	2,4		

§ Pin 1 = High, # Pin 8 = High — Set by momentary application of V_{BOT} prior to the application of the negative going clock pulse.

‡ Pin 3 = ⌐‾|_

Pins not listed are left open.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.

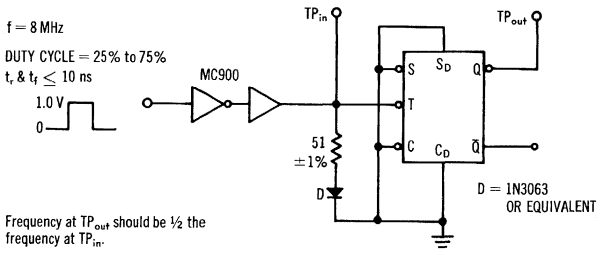
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC826		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC926		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

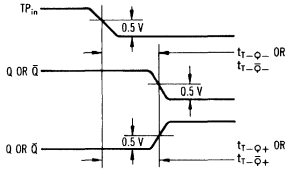
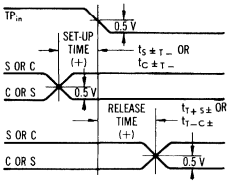
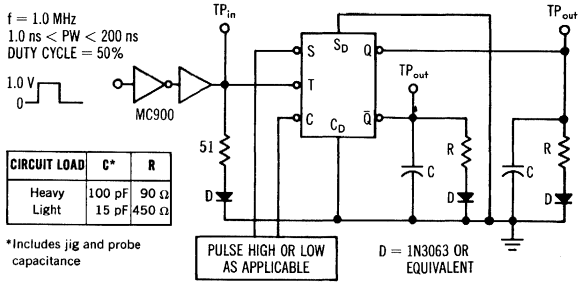


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

*Includes jig and probe capacitance

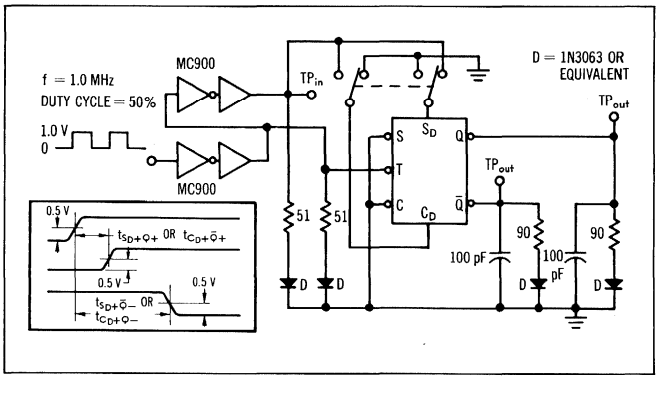
SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
$t_{C_D^+}$ or $t_{S_D^+}$ to output −	4	—	90
$t_{C_D^+}$ or $t_{S_D^+}$ to output +	4	—	70

Lightly loaded

* Negative switching time means the inputs can momentarily change before the clock pulse transition.

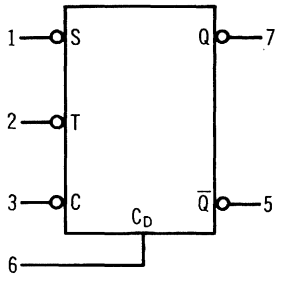
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC974 • MC874

Available in TO-99 metal can, add "G" suffix.

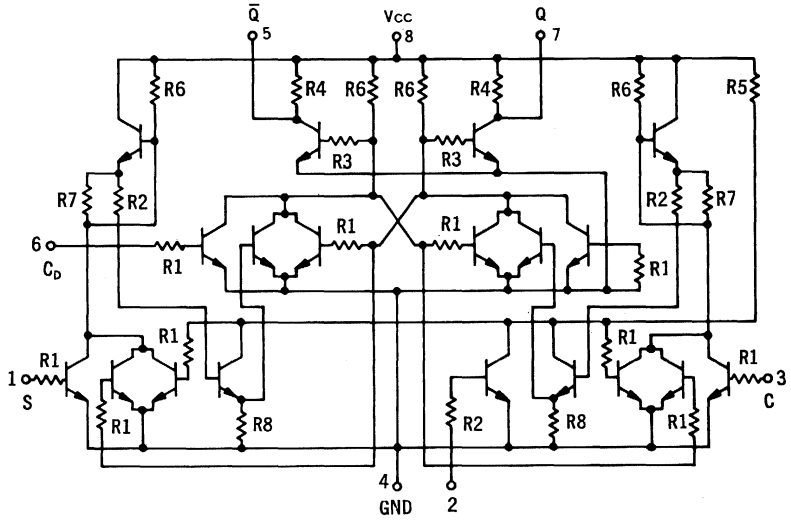
J-K flip-flop with a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

① Direct input (C_D) must be low.
② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 700 Ω
R2 = 300 Ω	R6 = 900 Ω
R3 = 550 Ω	R7 = 2k Ω
R4 = 640 Ω	R8 = 3k Ω

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC974	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC874	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC974 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC874 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	6	-	8	4
	$2\ I_{in}$*	2	-	990	-	870	-	940		-	1008	-	900	-	900		2	-	1,3	-		
	I_{in}	3 Δ	-	495	-	435	-	470		-	504	-	450	-	450		3	-	-	-		
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	-	-		
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5,6	-	-	8	4
		7 Δ	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	7	-	-	8	4
Saturation Voltage	$V_{CE(sat)}$	5‡§	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	3	8	4
		5‡§	-		-		-			-		-		-			-	-	-	1,3		
		5Δ§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ	-		-		-			-		-		-			-	6	-	-		
		7‡§	-		-		-			-		-		-			-	1,3	-	-		
		7Δ§	-		-		-			-		-		-			-	3	-	1		
		7Δ§	-		-		-			-		-		-			-	-	-	1,3		

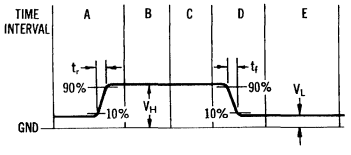
Pins not listed are left open.

Δ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 6 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 6, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note §) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 1 and 3, and proceed with the test.

‡ Momentarily apply V_{BOT} to pin 6 prior to the arrival of the negative-going clock pulse to effect a change of state.

§ Clock Pulse to pin 2:

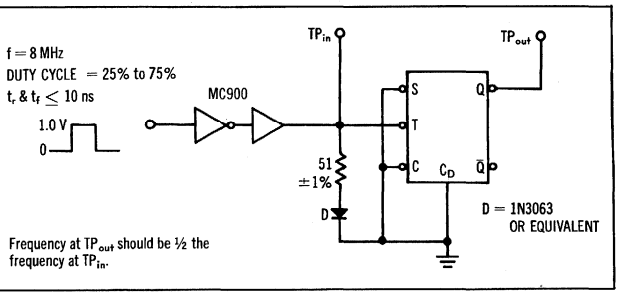
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC874		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC974		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.724 V

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

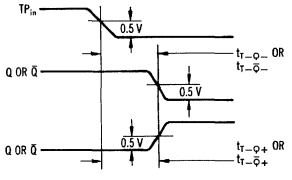
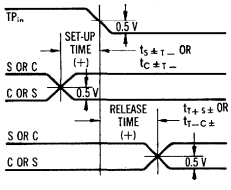
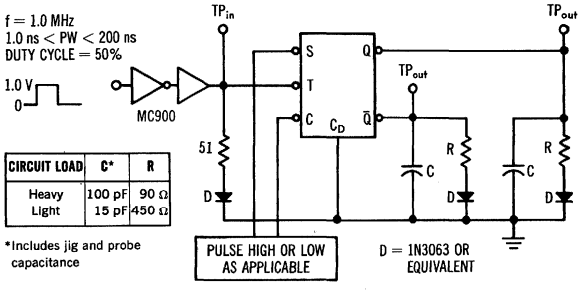


FIGURE 3B — SET-UP AND RELEASE TIME



For definitions of set-up and release times, see General Information Section.

FIGURE 3C — TEST CIRCUIT



CIRCUIT LOAD	C*	R
Heavy	100 pF	90 Ω
Light	15 pF	450 Ω

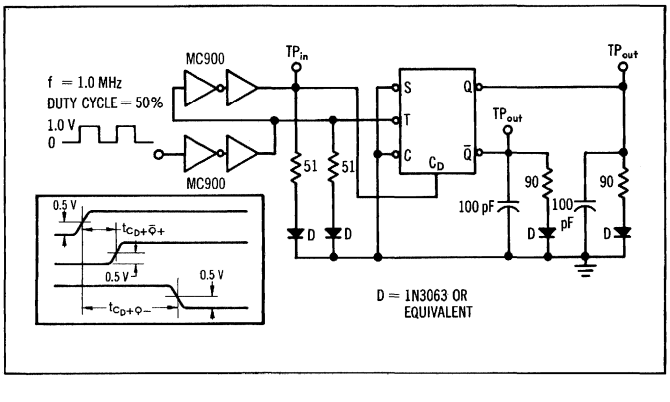
*Includes jig and probe capacitance

SWITCHING TIMES

Test	Figure No.	Minimum Over Full Temperature Range (ns)	Maximum Over Full Temperature Range (ns)
t_{T-Q-}	3A, 3C	25#	90
$t_{T-\bar{Q}-}$	3A, 3C	25#	90
t_{T-Q+}	3A, 3C	25#	90
$t_{T-\bar{Q}+}$	3A, 3C	25#	90
t_{S+T-}	3B, 3C	—	50
t_{S-T-}	3B, 3C	—	30
t_{C+T-}	3B, 3C	—	50
t_{C-T-}	3B, 3C	—	30
t_{T-S+}	3B, 3C	—	0*
t_{T-S-}	3B, 3C	—	+5*
t_{T-C+}	3B, 3C	—	0*
t_{T-C-}	3B, 3C	—	+5*
t_{C_D+Q-}	4	—	90
$t_{C_D+\bar{Q}+}$	4	—	70

Lightly loaded * Negative switching time means the inputs can momentarily change before the clock pulse transition.

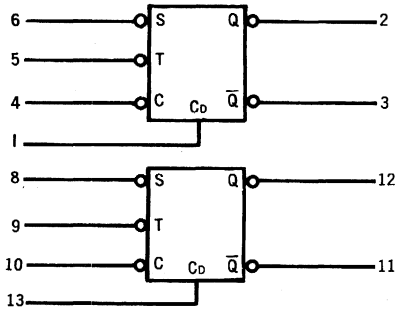
FIGURE 4 — DIRECT CLEAR PROPAGATION DELAY TIME



MC990 • MC890

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



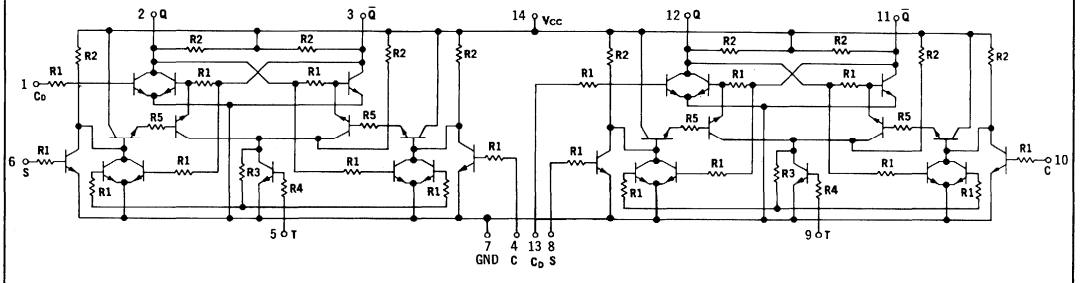
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC990	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC890	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC990 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC890 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	3	-	14	4,5,6,7
	I_{in}	4	-	495	-	435	-	470		-	504	-	450	-	450		4	-	2	-		1,5,6,7
	$2\ I_{in}$	5	-	990	-	870	-	940		-	1010	-	900	-	900		5	-	4,6	-		1,7
	I_{in}	6	-	495	-	435	-	470		-	504	-	450	-	450		6	-	3	-		1,4,5,7
Output Current	I_{A3}	2#	1.48	-	1.52	-	1.41	-	mAdc	1.51	-	1.43	-	1.35	-	mAdc	-	2	4	1	14	5,6,7
		3		-		-		-			-		-		-		-	3	1,6	-		4,5,7
		3		-		-		-			-		-		-		-	1,3	6	-		4,5,7
Output Voltage	V_{out}	2	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3,4,5,6,7
		2Δ§	-		-		-			-		-		-			-	4,6	-	-		1,7
		2#§	-		-		-			-		-		-			-	4	-	6		1,7
		2#§	-		-		-			-		-		-			-	-	-	4,6		1,7
		2†	-	-	-	-	-	-		-	-	-	-	-	-		-	-	-	-		1,6,7
		2*	-	-	-	-	-	-		-	-	-	-	-	-		-	-	-	-		1,6,7
		3#§	-	710	-	-	-	320		-	574	-	-	-	370		-	4,6	-	-		1,7
		3Δ§	-		-	-	-			-		-	-	-			-	6	-	4		
		3Δ§	-		-		-			-		-		-			-	-	-	4,6		
Saturation Voltage	$V_{CE(sat)}$	2	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3,4,5,6,7
		2Δ	-		-		-			-		-		-			-	-	-	-		1,4,5,6,7
		3#	-		-		-			-		-		-			-	-	-	1		4,5,6,7
Turn On Voltage	V_{on}	2‡	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1,4,7
		2**	-	-	0.815	-	-	-	Vdc	-	-	0.844	-	-	-	Vdc	-	-	-	-	14	1,4,7

Ground inputs of flip-flop not under test. Pins not listed are left open.

Pin 3 = LOW, Δ Pin 2 = LOW } Set by a momentary ground prior to the application of the negative-going clock pulse.

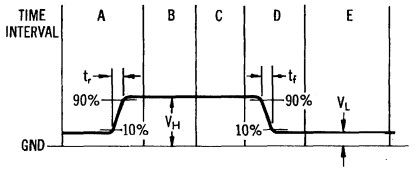
§ Clock Pulse to Pin 5 (See Figure 1)

† Clock Pulse on Pin 5, data pulse on Pin 4 (See Figure 2)
‡ Clock Pulse on Pin 5, data pulse on Pin 6 (See Figure 2)

* Clock Pulse on Pin 5, data pulse on Pin 4, momentary ground on Pin 2 (See Figure 3)
** Clock Pulse on Pin 5, data pulse on Pin 6, momentary ground on Pin 3 (See Figure 3)

CLOCK PULSE DEFINITIONS

FIGURE 1



SEQUENCE OF EVENTS:

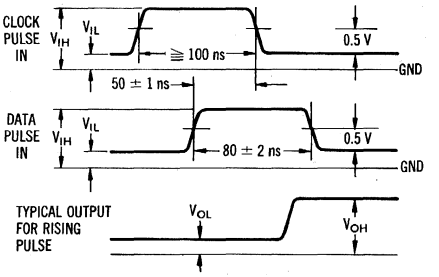
A. Voltage applied to Clock pin is raised to V_{IH}. t_r is not critical, however should be less than 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC890		
T_A	V_L	V_H
25°C	0.554 V	0.894 V
0°C	0.574 V	0.959 V
100°C	0.370 V	0.760 V

All voltages ±10 mV

MC990		
T_A	V_L	V_H
25°C	0.565 V	0.865 V
−55°C	0.710 V	1.064 V
125°C	0.320 V	0.674 V

FIGURE 2

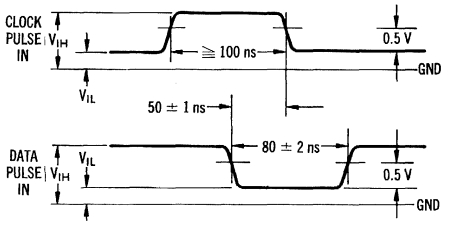


INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
$t_r \leqq$ 10 ns
$t_f \leqq$ 10 ns
f = 1.0 MHz typ

NOTE:
Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

FIGURE 3



INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
$t_r \leqq$ 10 ns
$t_f \leqq$ 10 ns
f = 1.0 MHz typ

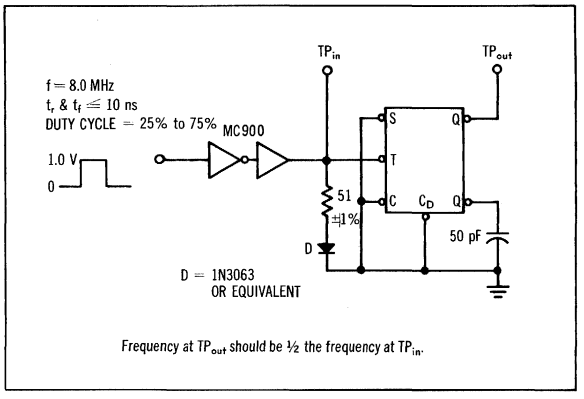
SEQUENCE OF EVENTS:

A. Apply all dc biases required.
B. Apply momentary ground to pin indicated. This sets the flip-flop. Momentary ground must occur before the pulses shown above every time, or the flip-flop will toggle to the wrong condition every alternate pulse.
C. After momentary ground has been released, apply pulses marked above.
D. Measure voltage of designated output after the pulse. Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

SWITCHING TIMES

Test	Figure No.	Maximum (ns) @ 25°C Only	Maximum (ns) Over Full Temperature Range
t_{T-Q-}	5	40	60
t_{T-Q+}	5	80	100
$t_{T-\bar{Q}-}$	5	40	60
$t_{T-\bar{Q}+}$	5	80	100
t_{C_D+Q-}	6	—	50
$t_{C_D+\bar{Q}+}$	6	—	90

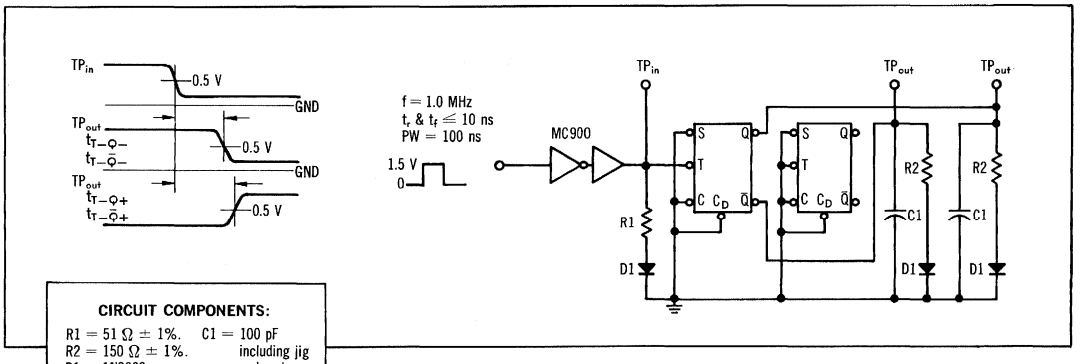
FIGURE 4 — TOGGLE MODE TEST CIRCUIT



Frequency at TP_{out} should be ½ the frequency at TP_{in}.

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 5

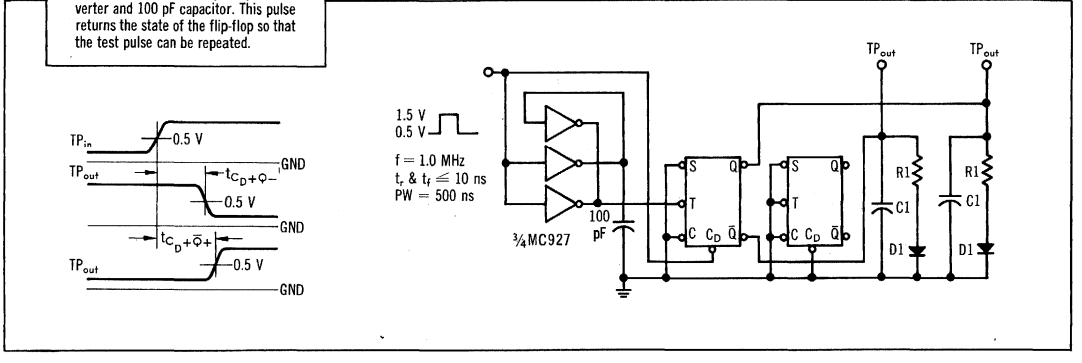


CIRCUIT COMPONENTS:

R1 = 51 Ω ± 1%. C1 = 100 pF including jig and probe.
R2 = 150 Ω ± 1%.
D1 = 1N3063 or equivalent.

NOTE:
The TOG pulse is developed by the inverter and 100 pF capacitor. This pulse returns the state of the flip-flop so that the test pulse can be repeated.

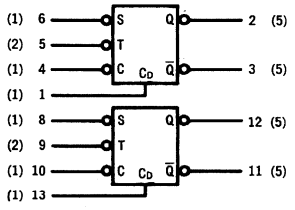
FIGURE 6



MC991 • MC891

Available in TO-86 flat package, add "F" suffix.

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



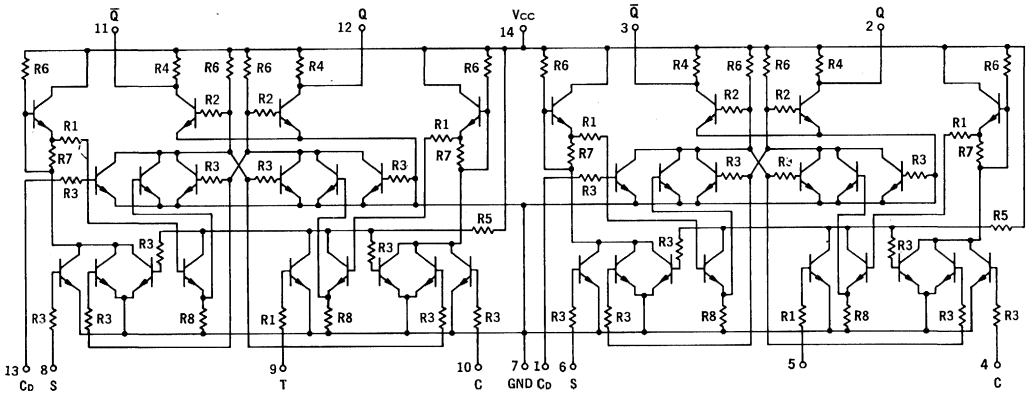
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

t_{pd} = 40 ns typ
f_{TOG} = 4.0 MHz max
P_D = 155 mW typ (Only Clock Input High)
130 mW typ (Inputs Low)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES

R1 = 300 Ω R4 = 640 Ω R7 = 2.0 k
R2 = 550 Ω R5 = 700 Ω R8 = 3.0 k
R3 = 600 Ω R6 = 900 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC991	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC891	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC991 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC891 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4 §	-	495	-	435	-	470	μAdc	-	600	-	600	-	570	μAdc	4	-	-	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940		-	1200	-	1200	-	1140		5	-	4, 6	-		
	I_{in}	6	-	495	-	435	-	470		-	600	-	600	-	570		6	-	1	-		
	I_{in}	1	-	495	-	435	-	470		-	600	-	600	-	570		1	-	-	-		
Output Current	I_{A5}	2 §	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	2	-	-	14	7
		3	2.47	-	2.54	-	2.35	-	mAdc	3.0	-	3.0	-	2.85	-	mAdc	-	1, 3	-	-	14	7
Output Voltage	V_{out}	2†⑤	-	710	-	300	-	320	mVdc	-	500	-	400	-	400	mVdc	-	4	-	-	14	1, 7
		2‡④	-		-		-			-		-		-			-	-	-	6		
		2†⑥	-		-		-			-		-		-			-	4	-	-		
		2‡⑦	-		-		-			-		-		-			-	-	-	6		
		3†④	-		-		-			-		-		-			-	-	-	4		
		3‡⑤	-		-		-			-		-		-			-	6	-	-		
		3†⑦	-		-		-			-		-		-			-	-	-	4		
		3‡⑥	-		-		-			-		-		-			-	6	-	-		
Saturation Voltage	$V_{CE(sat)}$	2§	-	200	-	210	-	280	mVdc	-	400	-	300	-	350	mVdc	-	1	-	-	14	7
		2* #	-		-		-			-		-		-			-	4, 6	-	-		
		2*§	-		-		-			-		-		-			-	4	-	6		
		2*§	-		-		-			-		-		-			-	-	-	4, 6		
		3* #	-		-		-			-		-		-			-	6	-	4		
		3* #	-		-		-			-		-		-			-	-	-	4, 6		
		3*§	-		-		-			-		-		-			-	4, 6	-	-		

Ground input pins of flip-flop not under test. Other pins not listed are left open.

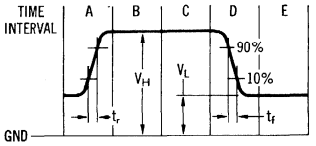
§ Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 1 to preclear the flip-flop.
(2) After V_{BOT} is removed from pin 1, ground pins 4 and 6.
(3) Apply a negative-going clock pulse to pin 5 (see note *) while pins 4 and 6 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove the grounds from pins 4 and 6 and proceed with the test.

* Clock pulse to pin 5, see Figure 1.
\# Pin 1 = HIGH, set by a momentary application of V_{BOT} prior to the application of the negative-going clock.

† Clock pulse to pin 5, data pulse to pin 6.
‡ Clock pulse to pin 5, data pulse to pin 4.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

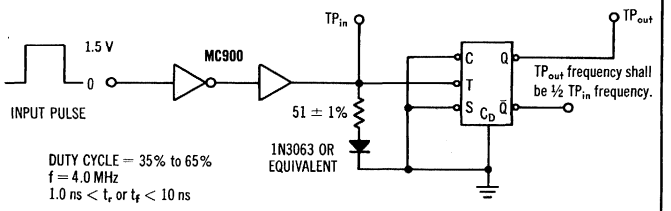
FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be < 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC991

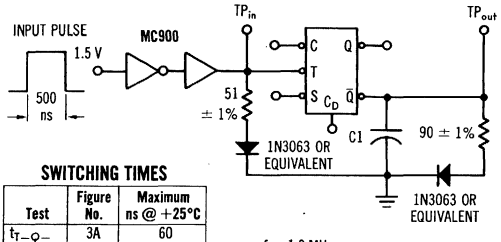
T_A	V_L	V_H
+25°C	+0.565 V ± 10 mV	+0.844 V ± 10 mV
−55°C	+0.710 V ± 10 mV	+1.014 V ± 10 mV
+125°C	+0.320 V ± 10 mV	+0.674 V ± 10 mV

MC891

T_A	V_L	V_H
+25°C	+0.554 V ± 10 mV	+1.430 V ± 10 mV
0°C	+0.574 V ± 10 mV	+1.310 V ± 10 mV
+100°C	+0.370 V ± 10 mV	+1.190 V ± 10 mV

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT



SWITCHING TIMES

Test	Figure No.	Maximum ns @ +25°C
t_{T-Q-}	3A	60
t_{T-Q+}	3A	60
$t_{T-\bar{Q}-}$	3A	60
$t_{T-\bar{Q}+}$	3A	60
t_{CD+Q-}	3B	90
$t_{CD+\bar{Q}+}$	3B	70

f = 1.0 MHz
1.0 ns < t_r or t_f < 10 ns

C1 = 100 pF INCLUDING PROBE & JIG CAPACITANCE

FIGURE 3A — CLOCK-TO-OUTPUT PROPAGATION DELAY TIME

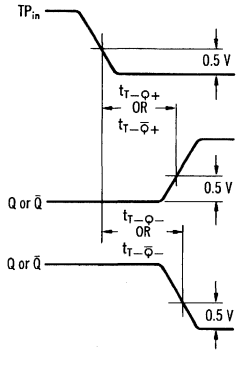
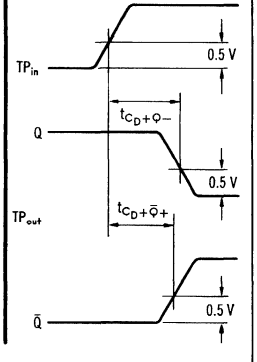
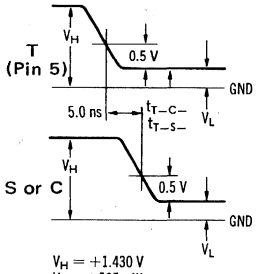


FIGURE 3B — DIRECT CLEAR PROPAGATION DELAY TIME



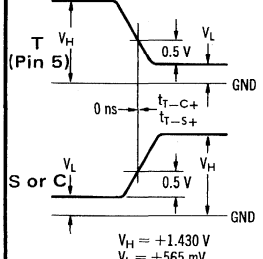
TEST WAVEFORMS FOR V_{out} TESTS

FIGURE 4



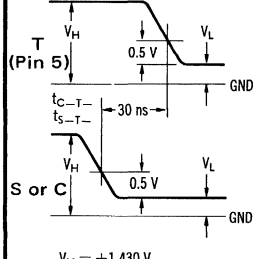
V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 5



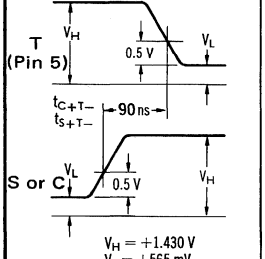
V_H = +1.430 V
V_L = +565 mV
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

FIGURE 6



V_H = +1.430 V
V_L = +565 mW
1.0 ns < t_f < 10 ns

FIGURE 7

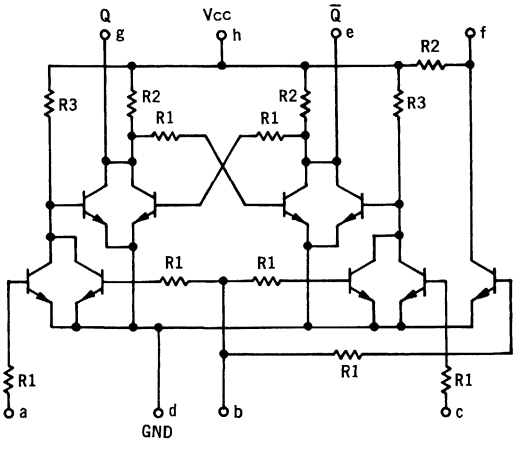


V_H = +1.430 V
V_L = +565 mV
1.0 ns < t_f < 10 ns
1.0 ns < t_r < 10 ns

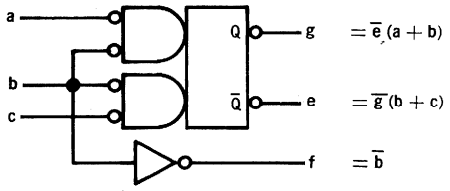
MC905 • MC805

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

This half-shift register is a bistable storage element with a built-in inverter for the gating signal. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



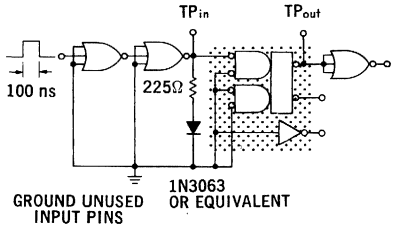
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

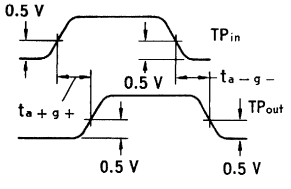


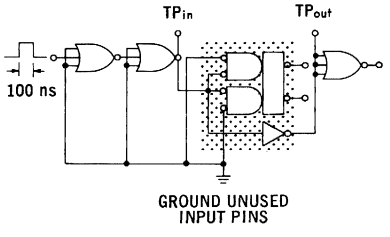
PIN CONNECTIONS

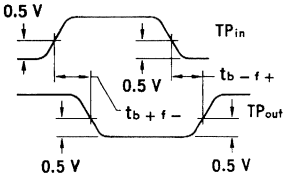
SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS









ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC905	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC805	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

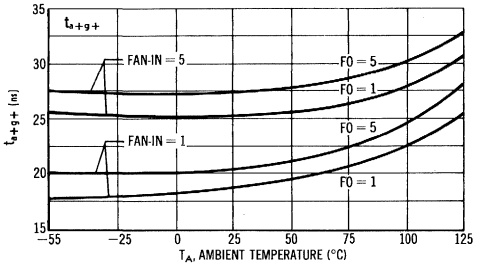
Characteristic	Symbol	Pin Under Test	MC905 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC805 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b	-	h	d
	$3\ I_{in}$	b	-	1480	-	1300	-	1410	↓	-	1510	-	1350	-	1350	↓	b	-	a, c	-	↓	↓
	I_{in}	c	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	c	-	b	-	↓	↓
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
	I_{A4}	e	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	c, e	-	-	↓	d
	I_{A5}	f	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	f	-	b	↓	d
	I_{A4}	g	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	b, g	-	-	↓	d, e †
	I_{A4}	g	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	a, g	-	-	↓	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	↓
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	a, b	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	b, c	↓	d, g
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	b	-	↓	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	a, b, c	-	↓	d, g †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	a, b	↓	d, e
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e
		a-g-	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	a	g	-	-	↓	d, e
		b+f-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	b	f	-	-	↓	d
		b-f+	-	-	-	24	-	-	↓	-	-	-	24	-	-	↓	b	f	-	-	↓	d

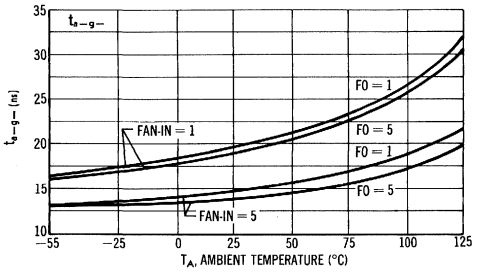
† Silicon Diode to Ground

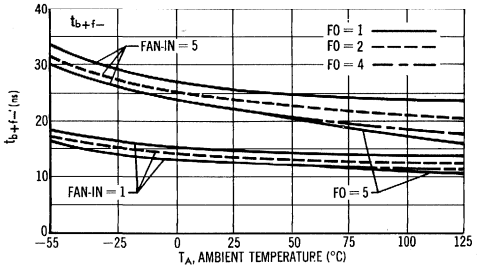
Pins not listed are left open.

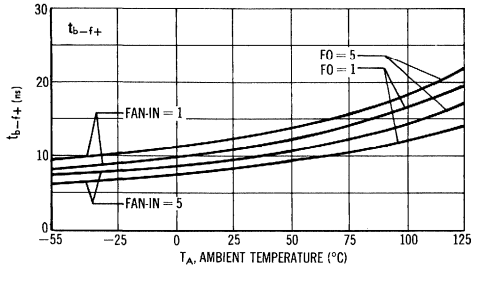
TYPICAL CURVES

SWITCHING CHARACTERISTICS

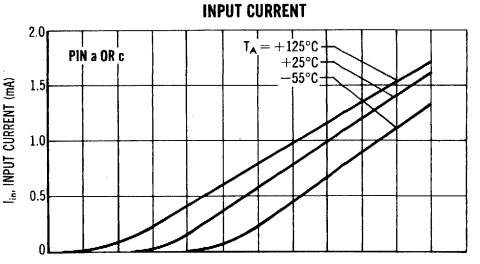


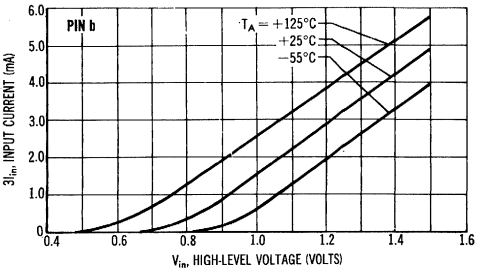




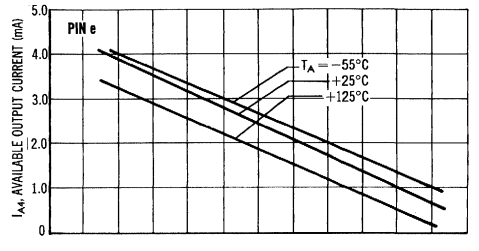


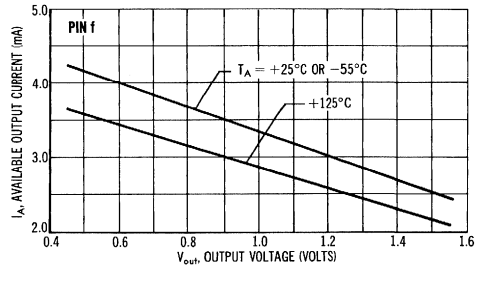
INPUT CURRENT





AVAILABLE OUTPUT CURRENT

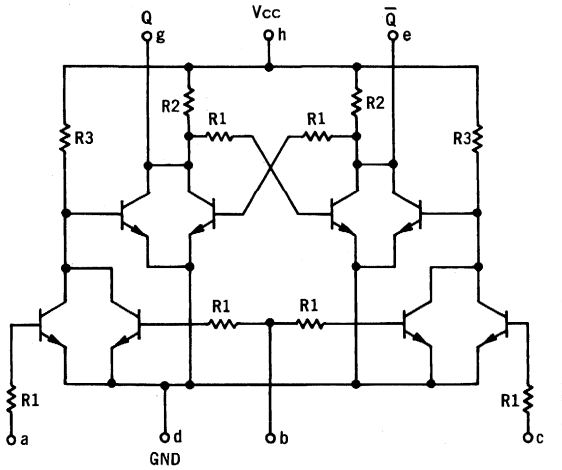




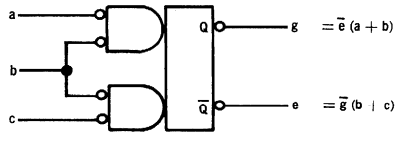
MC906 • MC806

Available in TO-99 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

This half-shift register is a bistable storage element. Information coming in on pins a and c will be transferred to pins g and e when the gating signal, pin b, goes low. If all three inputs, a, b, and c, are low, the outputs, g and e, will both be low.



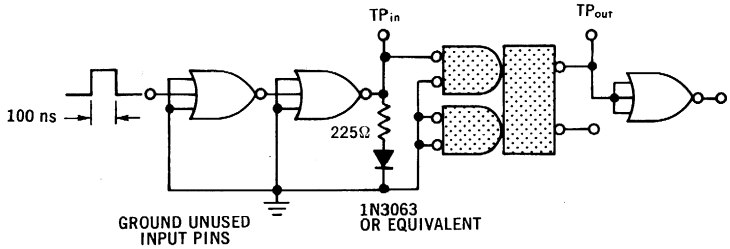
TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

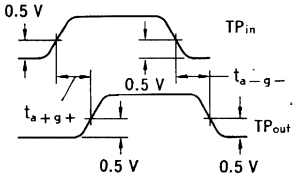


PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	—	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC906	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC806	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC906 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC806 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	a	-	b	-	h	d
	$2\,I_{in}$	b	-	990	-	870	-	940	↓	-	1010	-	900	-	900	↓	b	-	a, c	-	↓	↓
	I_{in}	c	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	c	-	b	-	↓	↓
Output Current	I_{A4}	e	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	b, e	-	-	h	d, g †
		e	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	c, e	-	-	↓	d
		g	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	b, g	-	-	↓	d, e †
		g	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	a, g	-	-	↓	d
Output Voltage	V_{out}	e	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	g	b, c	-	h	d
		g		710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	e	a, b	-	h	d
Saturation Voltage	$V_{CE(sat)}$	e	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	a, b, c	-	h	d, e †
		e	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	b, c	↓	d, g
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	a, b, c	-	↓	d, g †
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	a, b	↓	d, e
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e
		a−g−	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d, e

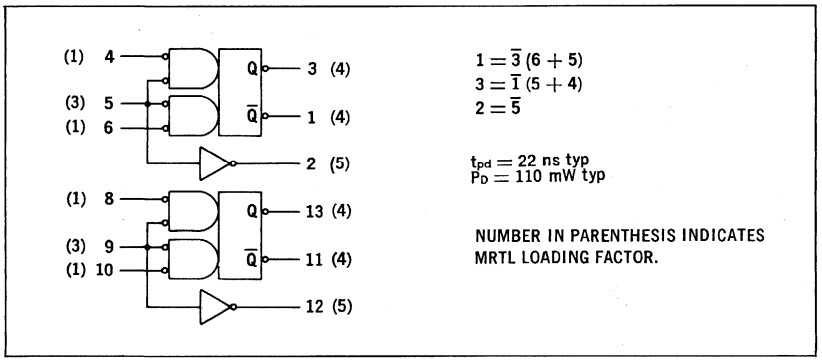
† Silicon Diode to Ground

Pins not listed are left open.

MC983 • MC883

Available in TO-86 flat package, add "F" suffix.

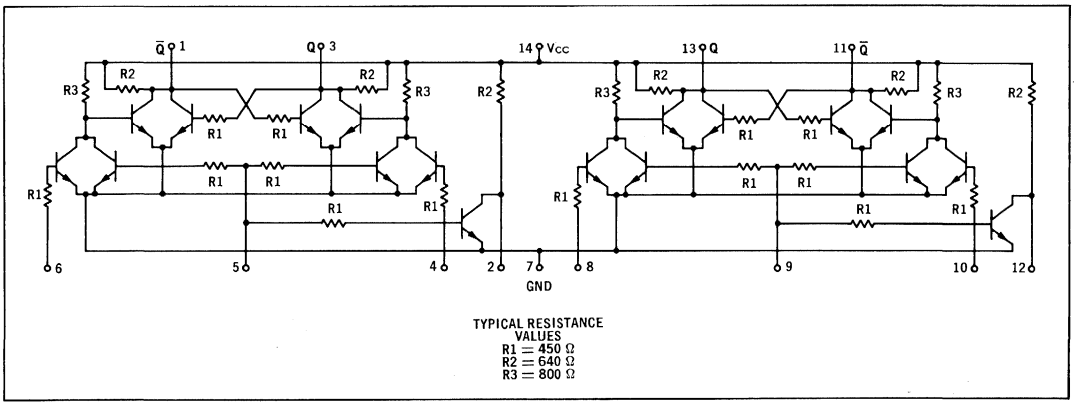
Two half-shift registers in a single package, each having a built-in inverter for the gating signal. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 1 and 3, will both be low.



$1 = \overline{3}\,(6 + 5)$
$3 = \overline{1}\,(5 + 4)$
$2 = \overline{5}$

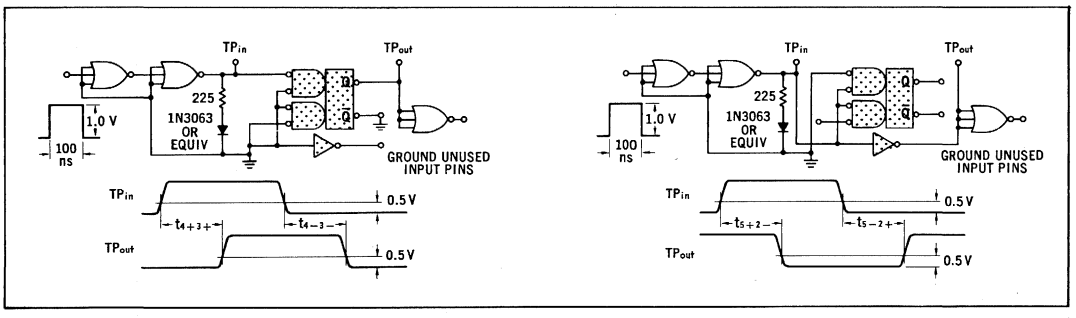
t_{pd} = 22 ns typ
P_D = 110 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC983	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC883	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

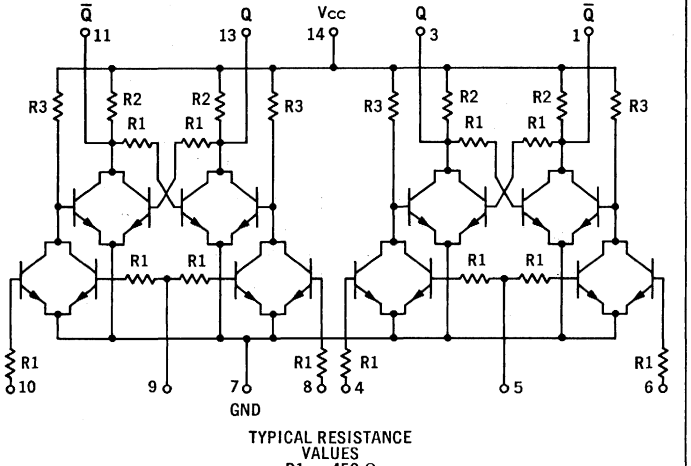
Characteristic	Symbol	Pin Under Test	MC983 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC883 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$3I_{in}$	5	-	1485	-	1305	-	1410	↓	-	1512	-	1350	-	1350	↓	5	-	4,6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	6	-	5	-	↓	↓
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,5	-	-	14	3*,7
	I_{A4}	1	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	1,6	-	-	↓	7
	I_{A5}	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2	-	5	↓	7
	I_{A4}	3	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	3,5	-	-	↓	1*,7
	I_{A4}	3	1.98	-	2.19	-	1.88	-	↓	2.02	-	2.05	-	1.80	-	↓	-	3,4	-	-	↓	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5,6	-	14	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	4,5	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4,5,6	-	14	1*,7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5,6	↓	2,7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	5	-	↓	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	4,5,6	-	↓	3*,7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5,6	↓	1,7
																	Pulse In	Pulse Out				
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1,7
		4-3-	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	4	3	-	-	↓	1,7
		5+2-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	5	2	-	-	↓	7
		5-2+	-	-	-	24	-	-	↓	-	-	-	24	-	-	↓	5	2	-	-	↓	7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

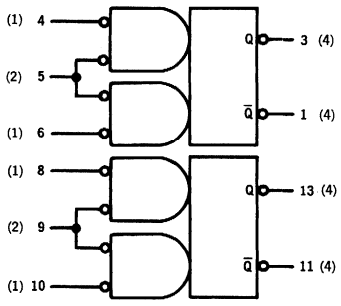
MC984 • MC884

Available in TO-86 flat package, add "F" suffix.

This bistable storage element consists of two half-shift registers in a single package. For example, information coming in on pins 4 and 6 will be transferred to pins 3 and 1 when the gating signal, pin 5, goes low. If all three inputs, 4, 5, and 6, are low, the outputs, 3 and 1, will both be low.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

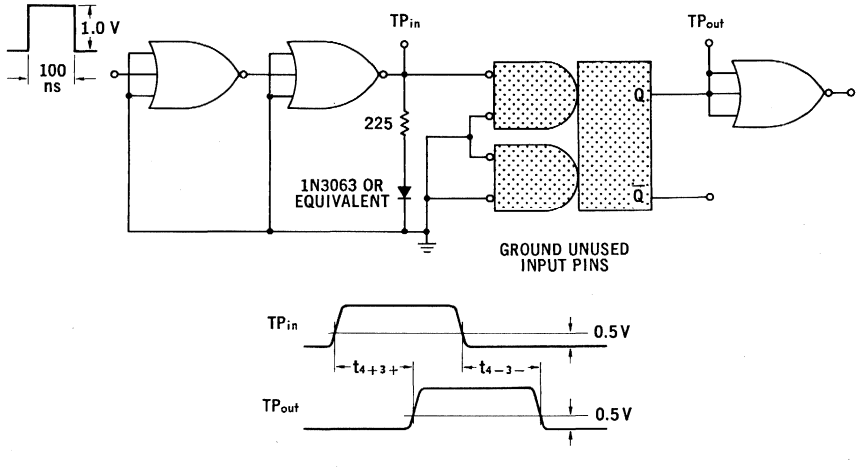


$3 = \overline{1}\,(4 + 5)$
$1 = \overline{3}\,(6 + 5)$

t_{pd} = 22 ns typ
P_D = 75 mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures shown are for one half-shift register only.
The other half-shift register is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC984	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC884	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

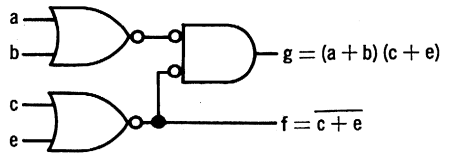
Characteristic	Symbol	Pin Under Test	MC984 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC884 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	4	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	4	-	5	-	14	7
	$2I_{in}$	5	-	990	-	870	-	940	↓	-	1008	-	900	-	900	↓	5	-	4, 6	-	↓	↓
	I_{in}	6	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	6	-	5	-	↓	↓
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1, 5	-	-	14	3*, 7
		1	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1, 6	-	-	↓	7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 5	-	-	↓	1*, 7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3, 4	-	-	↓	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	5, 6	-	14	7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	4, 5	-	14	7
Saturation Voltage	V_{CE}	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	4, 5, 6	-	14	1*, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	5, 6	↓	3, 7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 5, 6	↓	3*, 7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 5	↓	1, 7
																	Pulse In	Pulse Out				
Switching Time	t	4+3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1, 7
		4-3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	4	3	-	-	14	1, 7

Ground input pins of half-shift register not under test. Other pins not listed are left open. *Momentary ground.

MC904 • MC804

Available in TO-99 metal can, add "G" suffix.
Available in TO-91 flat package, add "F" suffix.

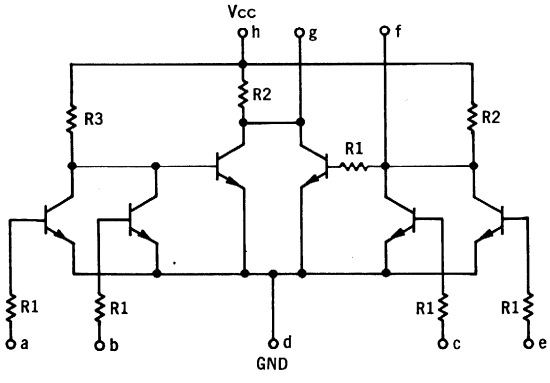
This half-adder device can be used to supply the SUM and CARRY operations on two input signals. If the inputs are applied to pins a and b, and their complements to pins c and e, the SUM of the inputs appears on pin g while the CARRY appears on pin f.



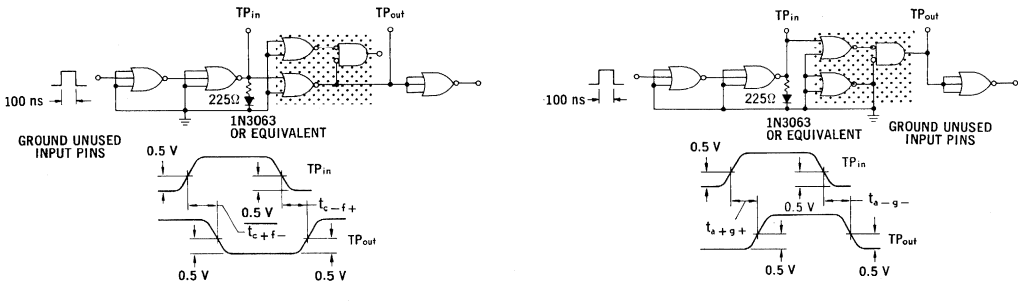
PIN CONNECTIONS

SCHEMATIC	a	b	c	d	e	f	g	h
G PACKAGE (TO-99)	1	2	3	4	5	6	7	8
F PACKAGE (TO-91)	2	3	4	5	7	8	9	10

TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC904	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC804	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

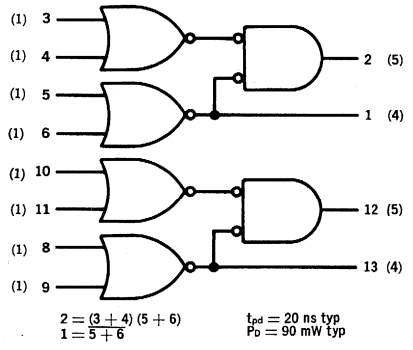
Characteristic	Symbol	Pin Under Test	MC904 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC804 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	a	-	b	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a	-	↓	↓
		c	-		--		-			-		-		-			c	-	e	-		
		e	-		-		-			-		-		-			e	-	c	-		
Output Current	I_{A4}	f	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	f	-	c, e	h	d
	I_{A5}	g	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	a, c, g	-	-	↓	↓
	I_{A5}	g	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	b, e, g	-	-		
Output Voltage	V_{out}	f	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	c	-	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	e	-	-	↓	↓
		g	-		-		-			-		-		-			-	f	a, b	-		
Saturation Voltage	$V_{CE(sat)}$	f	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	c	-	h	d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	-	↓	↓
		g	-		-		-			-		-		-			-	-	a, b	c, e		
		g	-		-		-			-		-		-			-	-	c, e	a, b		
																	Pulse In	Pulse Out				
Switching Time	t	a+g+	-	-	-	36	-	-	ns	-	-	-	36	-	-	ns	a	g	-	-	h	d
		a-g-	-	-	-	36	-	-	↓	-	-	-	36	-	-	↓	a	g	-	-	↓	↓
		c+f-	-	-	-	20	-	-		-	-	-	20	-	-		c	f	-	-		
		c-f+	-	-	-	30	-	-		-	-	-	30	-	-		c	f	-	-		

Pins not listed are left open.

MC975 • MC875

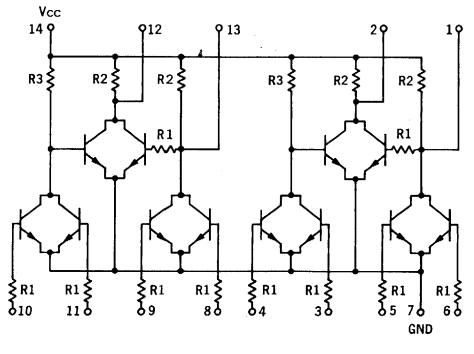
Available in TO-86 flat package, add "F" suffix.

A dual half-adder device contained in a single package. Each can be used to supply the SUM and CARRY operations on two input signals. For example, if the inputs are applied to pins 3 and 4, and their complements to pins 5 and 6, the SUM of the inputs appears on pin 2 while the CARRY appears on pin 1.



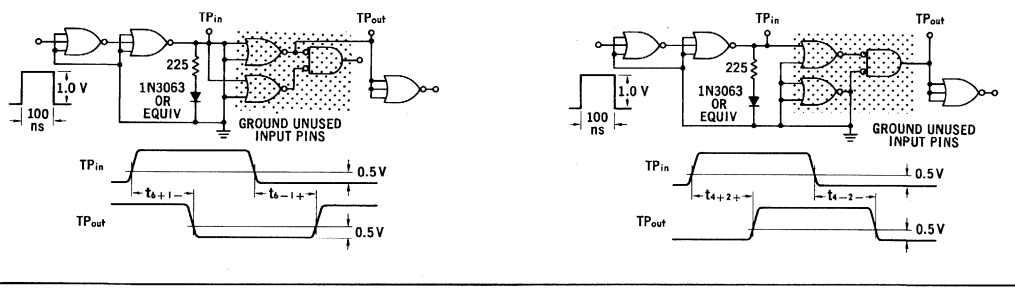
$2 = \overline{(3+4)(5+6)}$ $t_{pd} = 20$ ns typ
$1 = \overline{5+6}$ $P_D = 90$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC975	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC875	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

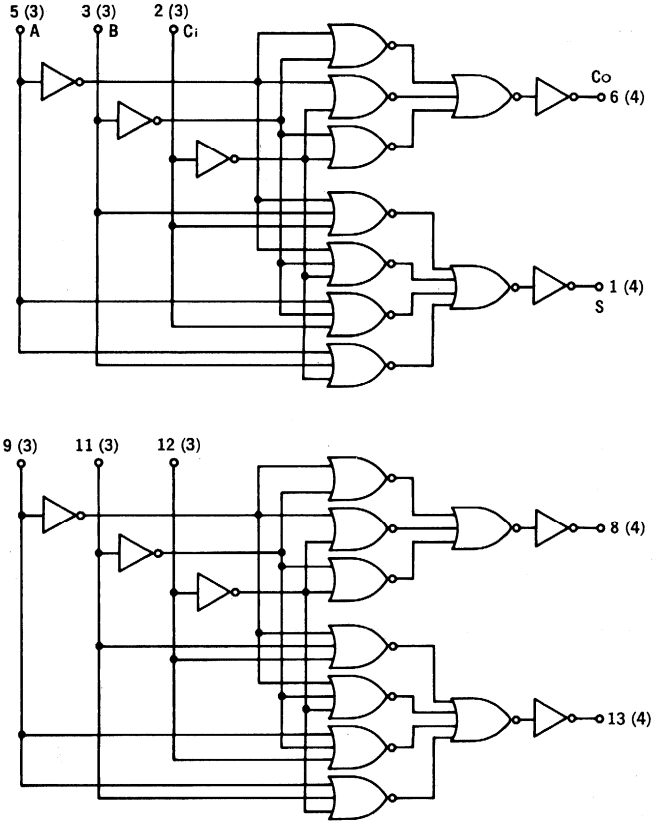
Characteristic	Symbol	Pin Under Test	MC975 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC875 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	3	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	3	-	4	-	14	7
		4	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	4	-	3	-	↓	↓
		5	-		-		-			-		-		-			5	-	6	-		
		6	-		-		-			-		-		-			6	-	5	-		
Output Current	IA4	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1	-	5, 6	14	7
	IA5	2	2.47	-	2.54	-	2.35	-	↓	2.52	-	2.38	-	2.25	-	↓	-	2, 3, 5	-	-	↓	↓
	IA5	2	2.47	-	2.54	-	2.35	-		2.52	-	2.38	-	2.25	-		-	2, 4, 6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	5	-	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	↓
		2	-		-		-			-		-		-			-	1	3, 4	-		
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	5	-	14	7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	↓
		2	-		-		-			-		-		-			-	-	3, 4	5, 6		
		2	-		-		-			-		-		-			-	-	5, 6	3, 4		
																	Pulse In	Pulse Out				
Switching Time	t	6+1-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	6	1	-	-	14	7
		6-1+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	6	1	-	-	↓	7
		4+2+	-	-	-	36	-	-		-	-	-	36	-	-		4	2	-	-		1, 7
		4-2-	-	-	-	36	-	-		-	-	-	36	-	-		4	2	-	-		1, 7

Ground input pins of half-adder not under test. Other pins not listed are left open.

MC996 • MC896

Available in TO-86 flat package, add "F" suffix.

Provides the SUM and CARRY functions while requiring only AUGEND (A) and ADDEND (B) inputs with CARRY IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

POSITIVE LOGIC

$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}\overline{B}C_i$

$t_{pd} = 60$ ns typ

$P_D = 70$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

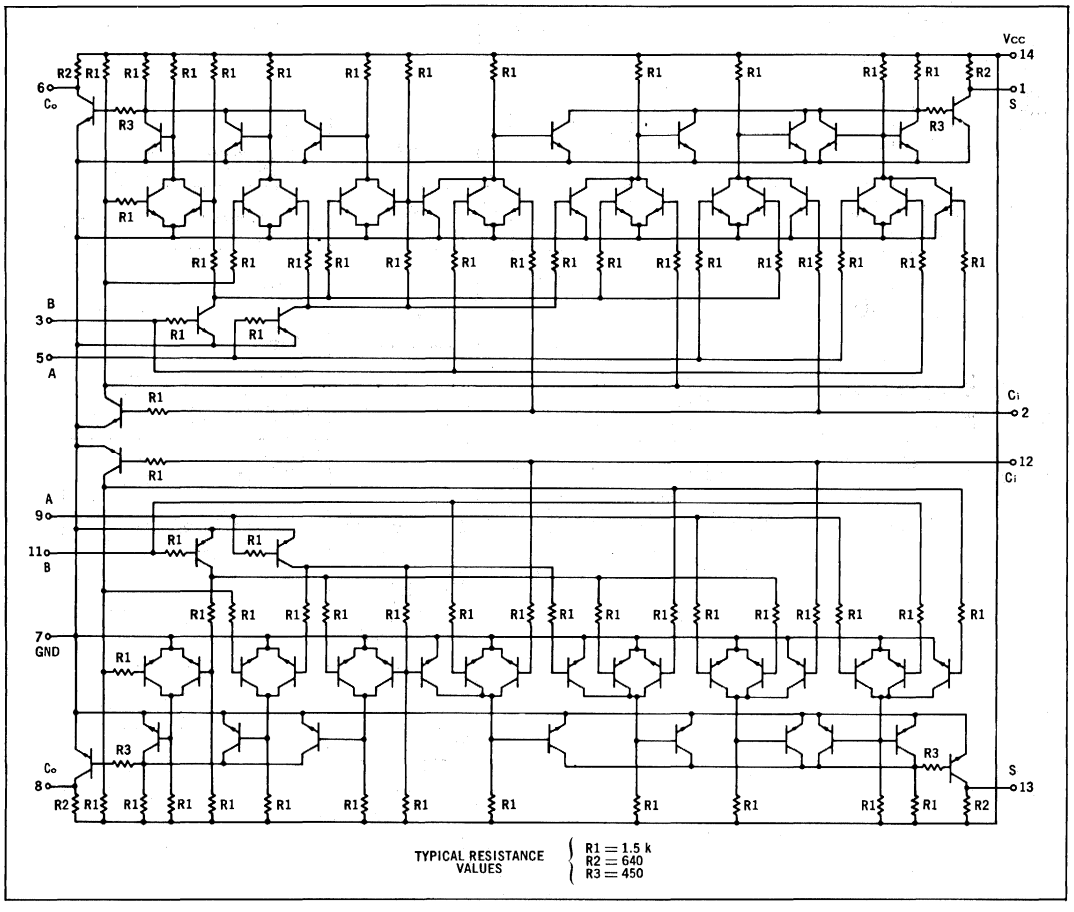
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one adder.
The other adder is tested in the same manner.

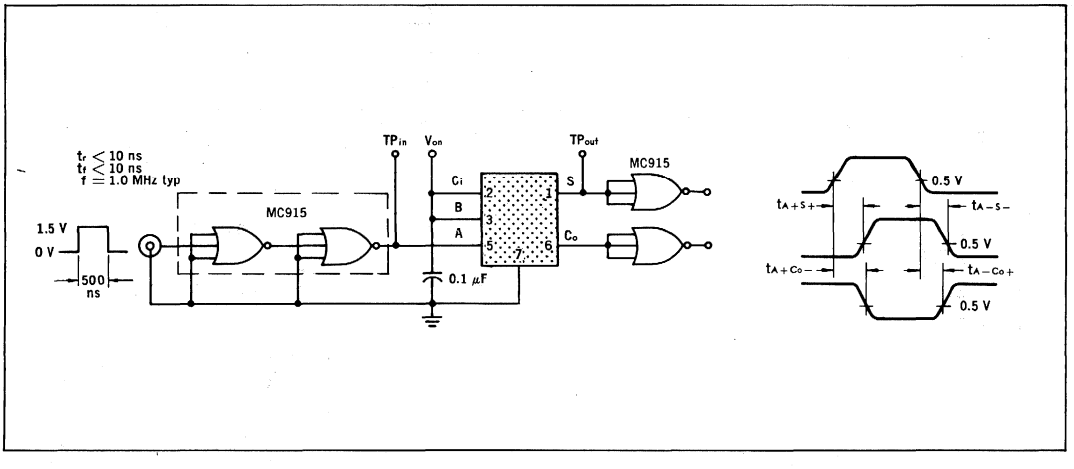
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC996	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC896	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC996 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC896 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	-	-	↓	↓
		5	-		-		-			-		-		-			5	-	-	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,2	-	3,5	14	7
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	1,3	-	2,5	↓	↓
				-		-		-			-		-		-		-	1,5	-	2,3		
				-		-		-			-		-		-		-	1,2,3,5	-	-		
		6		-		-		-			-		-		-		-	2,3,6	-	5		
		↓		-		-		-			-		-		-		-	2,5,6	-	3		
				-		-		-			-		-		-		-	3,5,6	-	2		
				-		-		-			-		-		-		-	2,3,5,6	-	-		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2,3,5	14	7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,3	-	5	↓	↓
			-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	2,5	-	3		
		6	-		-		-			-		-		-			-	-	-	2,3,5		
		↓	-		-		-			-		-		-			-	2	-	3,5		
			-		-		-			-		-		-			-	3	-	2,5		
			-		-		-			-		-		-			-	5	-	2,3		
																	Pulse In		Pulse Out			
Switching Time	t	5+1+	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	5	2,3	1	-	14	7
		5-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	2,3	1	-	↓	↓
		5+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	3		
		5-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	3		
		3+1+	-	-	-	75	-	-		-	-	-	75	-	-		3	-	1	2,5		
		3-1-	-	-	-	75	-	-		-	-	-	75	-	-		↓	-	1	2,5		
		3+6+	-	-	-	85	-	-		-	-	-	85	-	-			2	6	5		
		3-6-	-	-	-	65	-	-		-	-	-	65	-	-			2	6	↓		
		2+1-	-	-	-	70	-	-		-	-	-	70	-	-		2	3	1			
		2-1+	-	-	-	80	-	-		-	-	-	80	-	-		↓	↓	1			
		2+6+	-	-	-	70	-	-		-	-	-	70	-	-				6			
		2-6-	-	-	-	80	-	-	↓	-	-	-	80	-	-	↓			6	↓		

Ground input pins of adder not under test.
Other pins not listed are left open.



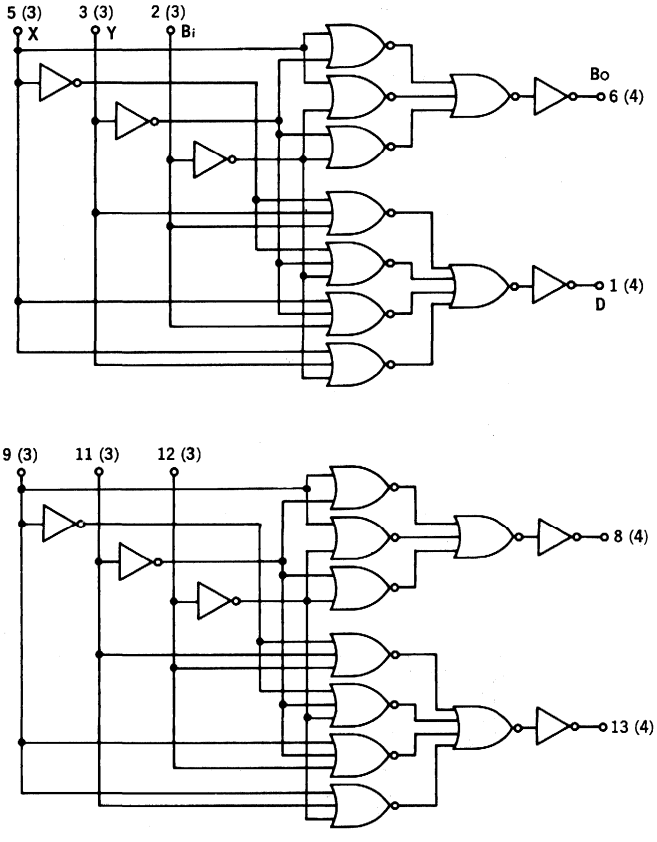
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC997 • MC897

Available in TO-86 flat package, add "F" suffix.

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN.



TRUTH TABLE

INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

POSITIVE LOGIC

$D = YX\overline{B}_i + Y\overline{X}\overline{B}_i + \overline{Y}X\overline{B}_i + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B}_i + \overline{Y}XB_i + YXB_i$

$t_{pd} = 60$ ns typ

$P_D = 70$ mW typ

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR

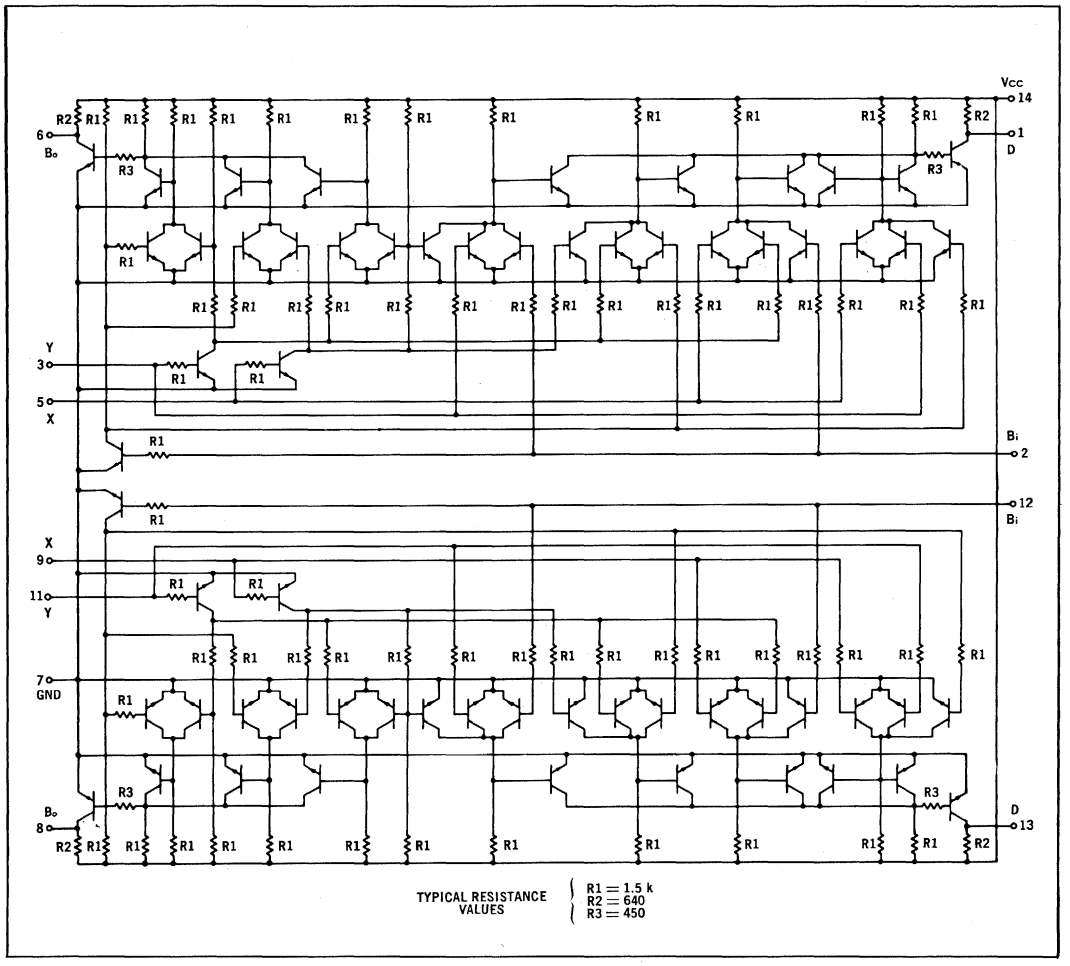
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one subtractor.
The other subtractor is tested in the same manner.

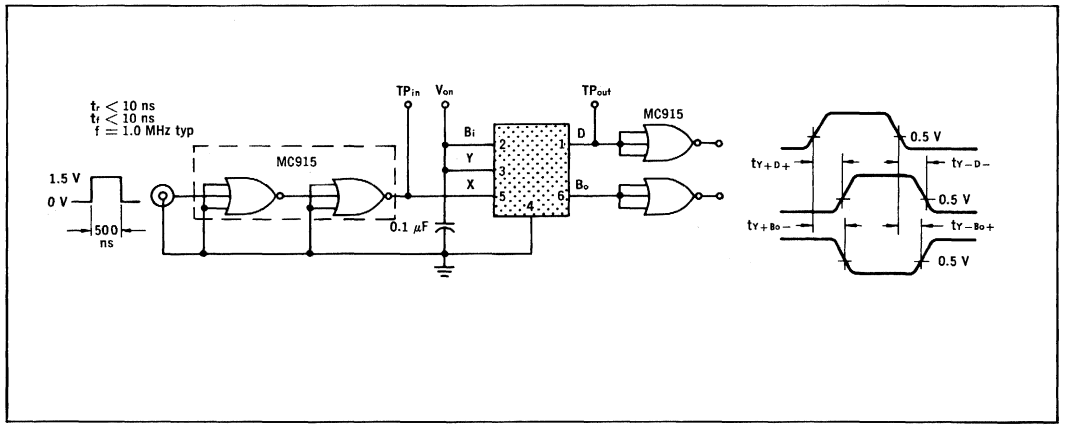
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC997	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC897	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC997 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC897 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1485	-	1305	-	1410	μAdc	-	1512	-	1350	-	1350	μAdc	2	-	-	-	14	7
		3	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	3	-	-	-	↓	↓
		5	-		-		-			-		-		-			5	-	-	-		
Output Current	I_{A4}	1	1.98	-	2.19	-	1.88	-	mAdc	2.02	-	2.05	-	1.80	-	mAdc	-	1,2	-	3,5	14	7
		↓		-		-		-	↓		-		-		-	↓	-	1,3	-	2,5	↓	↓
				-		-		-			-		-		-		-	1,5	-	2,3		
				-		-		-			-		-		-		-	1,2,3,5	-	-		
		6		-		-		-			-		-		-		-	2,3,5,6	-	-		
		↓		-		-		-			-		-		-		-	2,6	-	3,5		
				-		-		-			-		-		-		-	3,6	-	2,5		
				-		-		-			-		-		-		-	2,3,6	-	5		
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	-	-	2,3,5	7	14
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,3	-	5	↓	↓
			-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	2,5	-	3		
		6	-		-		-			-		-		-			-	2,5	-	3		
		↓	-		-		-			-		-		-			-	3,5	-	2		
			-		-		-			-		-		-			-	-	-	2,3,5		
			-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	5	-	2,3	↓	↓
Switching Time																	Pulse In		Pulse Out			
	t	5+1+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	5	2,3	1	-	14	7
		5-1-	-	-	-	60	-	-	↓	-	-	-	60	-	-	↓	↓	↓	1	-	↓	↓
		5+6+	-	-	-	65	-	-		-	-	-	65	-	-				6	-		
		5-6-	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	6	-		
		3+1+	-	-	-	↓	-	-		-	-	-	↓	-	-		3	-	1	2,5		
		3-1-	-	-	-		-	-		-	-	-		-	-			-	1	2,5		
		3+6-	-	-	-	65	-	-		-	-	-	65	-	-		↓	2	6	5		
		3-6+	-	-	-	60	-	-		-	-	-	60	-	-			2	6	↓		
		2+1-	-	-	-	↓	-	-		-	-	-	↓	-	-		2	3	1			
		2-1+	-	-	-		-	-		-	-	-		-	-		↓	3	1	↓		
		2+6+	-	-	-		-	-		-	-	-		-	-			3,5	6	-		
		2-6-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	3,5	6	-	↓	↓

Ground input pins of subtractor not under test.
Other pins not listed are left open.



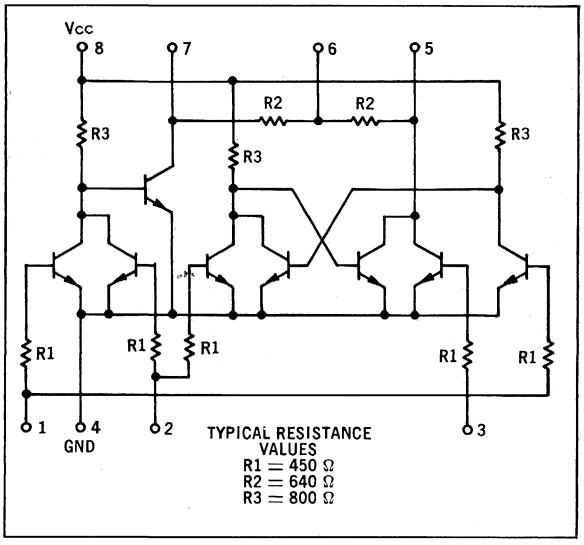
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

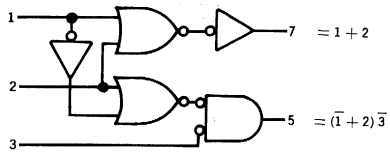


MC901 • MC801

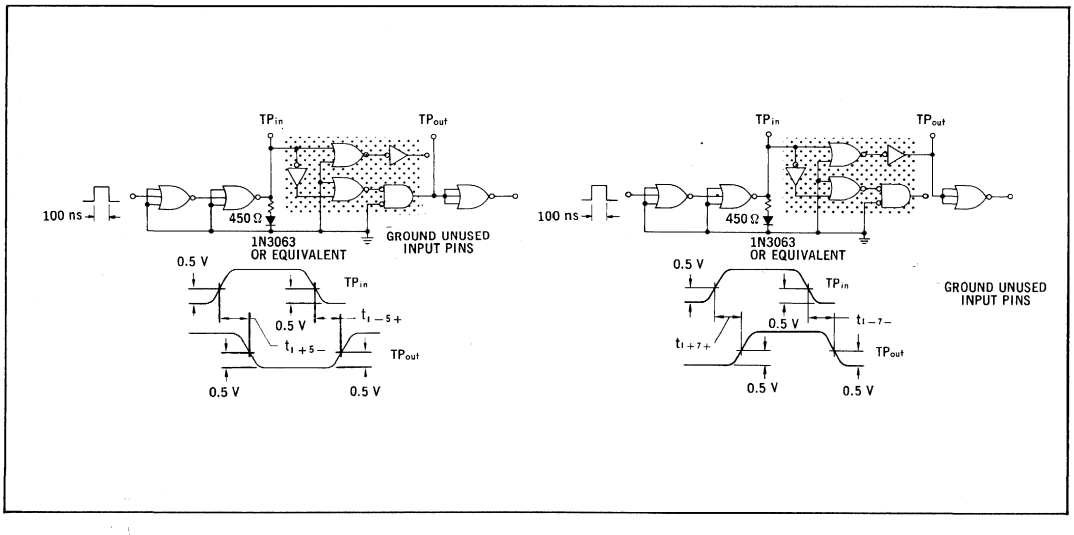
Available in TO-99 metal can, add "G" suffix.

This device provides the true output at pin 7 and the complement output at pin 5 for an input applied to pin 1. A positive gating signal may be applied to pin 2 to inhibit both outputs. A positive signal applied to pin 3 will hold output pin 5 at near-ground potential. The output nodes are returned separately to the power supply so that the outputs might be paralleled with other circuits.





SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC901	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC801	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

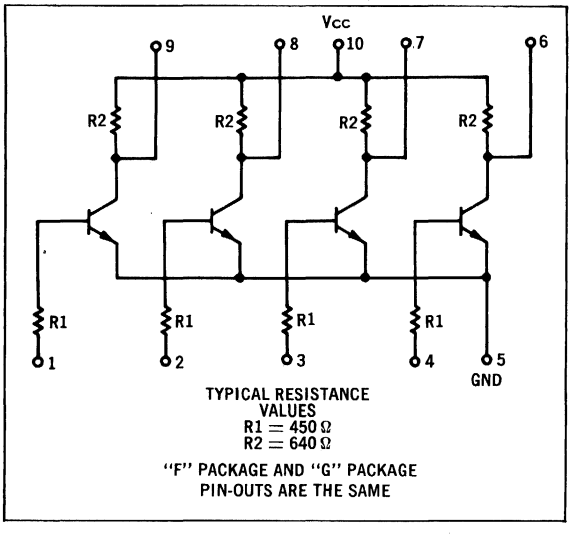
Characteristic	Symbol	Pin Under Test	MC901 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC801 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2\ I_{in}$	1	-	990	-	870	-	940	μAdc	-	1010	-	900	-	900	μAdc	1	-	2	-	6,8	4
	$2\ I_{in}$	2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	2	-	1	-	↓	↓
	$2\ I_{in}$	2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	2	-	-	-	↓	↓
	I_{in}	3	-	495	-	435	-	470	↓	-	504	-	450	-	450	↓	3	-	1	-	↓	↓
Output Current	I_{A5}	5	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	5	-	1,3	6,8	4
		5	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,5	1	3	↓	↓
		7		-		-		-			-		-		-		-	1,7	-	-		
		7		-		-		-			-		-		-		-	2,7	-	-		
Output Voltage	V_{out}	5	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	3	2	-	6,8	4
Saturation Voltage	$V_{CE(sat)}$	5	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	1	-	2	6,8	4
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2,3	-	↓	↓
		7	-		-		-			-		-		-			-	-	-	1,2		
																	Pulse In	Pulse Out				
Switching Time	t	1+5-	-	-	-	42	-	-	ns	-	-	-	42	-	-	ns	1	5	-	-	6,8	4
		1-5+	-	-	-	42	-	-	↓	-	-	-	42	-	-	↓	↓	5	-	-	↓	↓
		1+7+	-	-	-	38	-	-		-	-	-	38	-	-			7	-	-		
		1-7-	-	-	-	36	-	-		-	-	-	36	-	-			7	-	-		

Pins not listed are left open.

MC927 • MC827

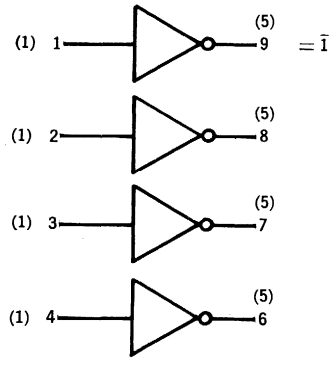
Available in TO-100 Metal Can, Add "G" Suffix.
Available in TO-91 Flat Package, Add "F" Suffix.

Four individual circuits each perform the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

"F" PACKAGE AND "G" PACKAGE PIN-OUTS ARE THE SAME

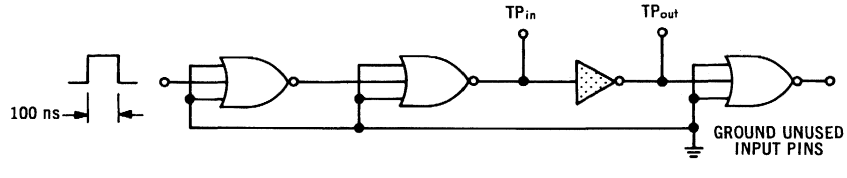


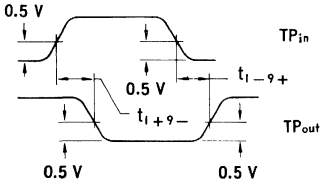
Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC927	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC827	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC927 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC827 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1*	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	*	-	10	5
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	4	10	5
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	4	-	5
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	4	1, 2, 3	-	10	5
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1, 2, 3, 4	-	10	5
																	Pulse In	Pulse Out				
Switching Time	t	1+9-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	9	-	-	10	5
		1-9+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	9	-	-	10	5

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

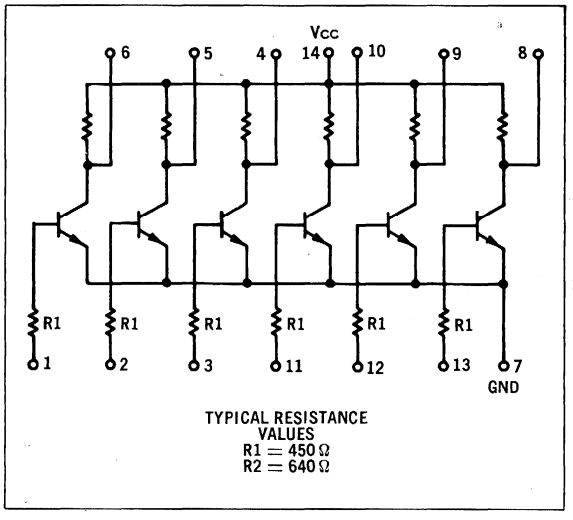
Ground inputs of inverters not used in test.

Other pins not listed are left open.

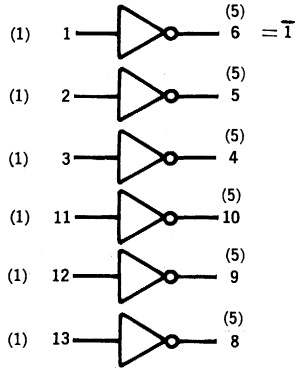
MC989 • MC889

Available in TO-86 flat package, add "F" suffix.

Six individual circuits are contained in a package. Each provides the simple inversion function.



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

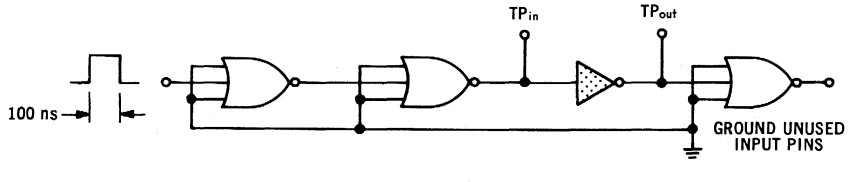


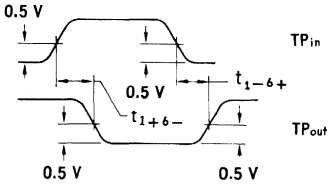
Number in parenthesis indicates MRTL loading factor.

t_{pd} = 12 ns typ

P_D = 76 mW typ (Input High)
20 mW typ (Inputs Low)

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC989	−55°C	1.014	1.014	1.50	0.710	3.00
	+25°C	0.844	0.815	1.50	0.565	3.00
	+125°C	0.674	0.674	1.50	0.320	3.00
MC889	0°C	0.909	0.909	1.50	0.574	3.00
	+25°C	0.844	0.844	1.50	0.554	3.00
	+100°C	0.710	0.710	1.50	0.370	3.00

Characteristic	Symbol	Pin Under Test	MC989 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC889 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1*	-	495	-	435	-	470	µAdc	-	504	-	450	-	450	µAdc	1	-	-	-	14	7
Output Current	I_{A5}	6	2.47	-	2.54	-	2.35	-	mAdc	2.52	-	2.38	-	2.25	-	mAdc	-	6	-	1	14	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	µAdc	-	100	-	225	-	225	µAdc	6	-	-	1	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	7
																	Pulse In	Pulse Out				
Switching Time	t	1+6-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	1	6	-	-	14	7
		1-6+	-	-	-	28	-	-	ns	-	-	-	28	-	-	ns	1	6	-	-	14	7

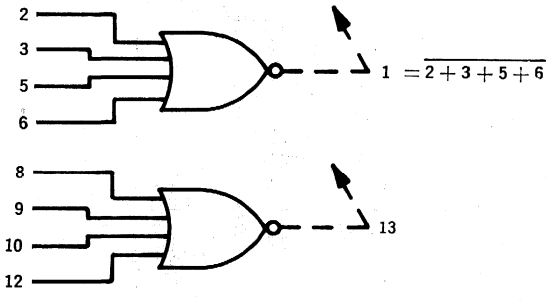
Ground inputs of inverters not used in test. Other pins not listed are left open.

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

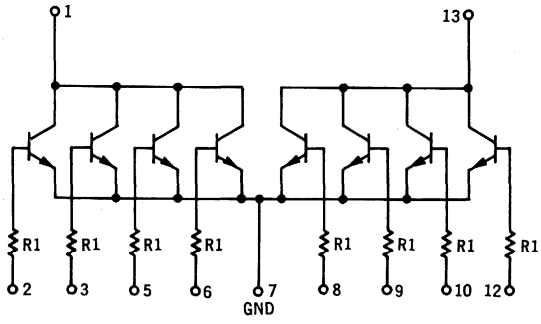
MC986 • MC886

Available in TO-86 flat package, add "F" suffix.

Two 4-input gate expanders housed in a single package may be used independently or combined. Each of these expanders increases the input capability of a standard MRTL gate by four.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC986	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC886	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC986 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC886 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	3, 5, 6	-	14	1	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2, 5, 6	-	↓	↓	↓
		5	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	5	-	2, 3, 6	-	↓	↓	↓
		6	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	6	-	2, 3, 5	-	↓	↓	↓
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	2, 3, 5, 6	14	-	7
Output Voltage	V_{out}	1	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	1	3, 5, 6, 7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓	2, 5, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	5	-	-	↓	↓	2, 3, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	6	-	-	↓	↓	2, 3, 5, 7
Saturation Voltage	$V_{CE(sat)}$	1	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	1	3, 5, 6, 7
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓	2, 5, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	5	-	↓	↓	2, 3, 6, 7
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	6	-	↓	↓	2, 3, 5, 7

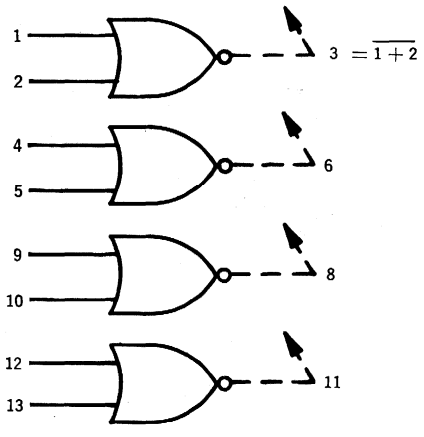
Ground inputs of expander not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

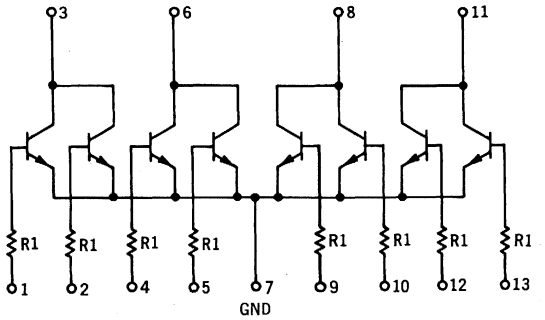
MC985 • MC885

Available in TO-86 flat package, add "F" suffix.

Four 2-input expanders housed in a single package increase the input capability of MRTL gates.



When an expander is added to a gate, subtract 0.4 load unit from the output of the gate for each expander circuit added.



V_{CC} connection to pin 14 not shown.

TYPICAL RESISTANCE VALUE
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
Other expanders are tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC985	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC885	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC985 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC885 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	2	-	14	3	7
		2	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	2	-	1	-	14	3	7
Output Leakage Current	I_{CEX}	3	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	3	-	-	1,2	14	-	7
Output Voltage	V_{out}	3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	3	2,7
		3	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	2	-	-	14	3	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	3	2,7
		3	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	2	-	14	3	1,7

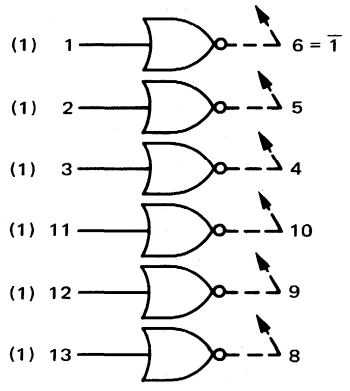
Ground inputs of expanders not under test. Other pins not listed are left open.

* Resistor Value to V_{CC}.

MC9919 • MC9819

Available in TO-86 flat package, add "F" suffix.

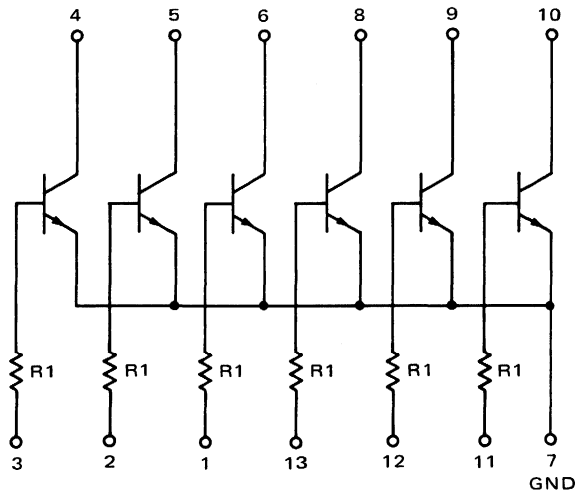
Six individual expanders are contained in a single package providing increased input capability for MRTL gates.



t_{pd} = 12 ns
P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MRTL LOADING FACTOR.

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added. The input loading factor of the expanded gate is 1.3. Pin 14 of the expander must be connected to V_{CC}.



V_{CC} connection to pin 14 not shown.

Typical Resistance Values
R1 = 450Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9919	−55°C	1.014	1.014	1.50	0.710	3.00	680
	+25°C	0.844	0.815	1.50	0.565	3.00	680
	+125°C	0.674	0.674	1.50	0.320	3.00	680
MC9819	0°C	0.909	0.909	1.50	0.574	3.00	680
	+25°C	0.844	0.844	1.50	0.554	3.00	680
	+100°C	0.710	0.710	1.50	0.370	3.00	680

Characteristic	Symbol	Pin Under Test	MC9919 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC9819 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+100°C Min	+100°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	495	-	435	-	470	μAdc	-	504	-	450	-	450	μAdc	1	-	-	-	14	6	7
Output Leakage Current	I_{CEX}	6	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	6	-	-	1	14	-	7
Output Voltage	V_{out}	6	-	710	-	300	-	320	mVdc	-	574	-	400	-	370	mVdc	-	1	-	-	14	6	7
Saturation Voltage	$V_{CE(sat)}$	6	-	200	-	210	-	280	mVdc	-	290	-	260	-	340	mVdc	-	-	1	-	14	6	7

Ground inputs of expanders not used in test. Other pins not listed are left open.

* Resistor value to V_{CC}.

LOW-POWER
mW MRTL
INTEGRATED CIRCUITS
MC908/MC808 SERIES

LOW POWER

mW MRTL

INTEGRATED CIRCUITS

Low-power mW MRTL circuits are designed for use where minimal system power consumption is desired. Typical gate speed is 27 ns, with typical power dissipation of 6.5 mW (input high), and 0.5 mW (inputs low) per logic node.

INDEX

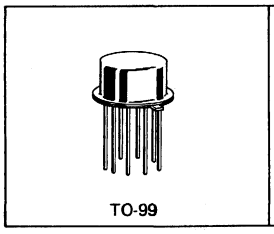
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MC918, MC818	Dual 3-Input Gates	6-107
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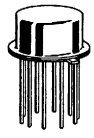
NUMERICAL INDEX
(Functions and Characteristics)

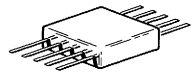
V_{CC} = 3.0 V ±10% for MC908 Series, 3.6 V ±10% for MC808 Series; T_A = 25°C

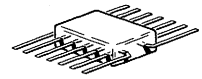
Function	Type ①		Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation ② mW typ/pkg		Page No.
	0 to +75°C	−55 to +125°C				MC808 Series	MC908 Series	
Half Adder	MC808	MC908	72,96	4	60	19/12.5	14/8.5	6-141
2-Input Buffer	MC809	MC909	72,96	30	57	7.0/23	5.5/16	6-115
Dual 2-Input NOR Gate	MC810	MC910	72,96	4	27	10/2.5	8.0/1.0	6-104
Dual 4-Input OR/NOR Gate	MC811	MC911	72,96	4	60	8.0/5.5	6.0/3.5	6-100
Half Adder	MC812	MC912	72,96	4	66	15.5/10.5	11.5/5.5	6-143
Type D Flip-Flop	MC813	MC913	72,96	3	75	24/17.5 ③	17.5/13 ③	6-122
Quad 2-Input NOR Gate	MC817	MC917	83	4	27	20/5.0	16/2.5	6-113
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J-K Flip-Flop	MC820	MC920	72,96	2	50	20.5/14.5 ④	15.5/10 ④	6-126
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5-Input NOR Gate	MC828	MC928	72,96	4	27	7.5/1.0	6.5/0.5	6-102
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J-K Flip-Flop	MC882	MC982	96	2	80	23/21 ④	15/13 ④	6-132
Triple 3-Input NOR Gate	MC893	MC993	83	4	27	18/3.5	14/2.0	6-111
Dual 2-Input Buffer	MC898	MC998	83	30	57	14/46	11/32	6-120
Quad 2-Input Expander	MC9821	MC9921	83	–	27	20/ –	20/ –	6-148

① G suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC818G = Metal Can, MC818F = Flat Package.
② Input High/Inputs Low unless otherwise noted.
③ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low
④ Only Clock Input High/All Inputs Low


TO-99


TO-100


TO-91


TO-86

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	–	+4.0	Vdc
Power Supply Voltage (Pulsed ≤ 1.0 s)	–	+12	Vdc
Operating Temperature Range MC908 Series MC808 Series	T_A	−55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TEST CONDITION TOLERANCES

V_{BOT} = ±10 mV V_{CC} = ±10 mV V_{in} = ±2 mV V_{on} = ±2 mV V_{off} = ±2 mV

DEFINITIONS

I_{A2}, I_{A3}, I_{A4} — Minimum available output current from a device with an output loading of 2, 3, or 4.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} — The maximum available current from the output of a Dual Gate.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

$0.8\ I_{in}$ — The current drawn from the V_{in} supply by an inverter transistor for a fan-in of 1.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

$1.8\ I_{in}$ — Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

$2\ I_{in}$ — Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L — Isolation leakage current.

V_{BOT} — A high-value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied into the input.

V_{in} — Minimum high-level voltage applied to the input of a device.

V_{LL} — A supply voltage low enough to allow flow of leakage currents only.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

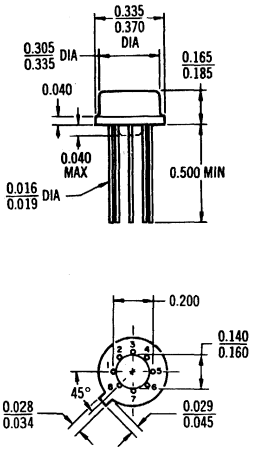
Release Time — The time that the J or K input data must be held after the negative-going clock input transition in order to propagate correct data.

Set-Up Time — The time that the J or K input data must be present prior to the negative-going clock input transition in order to propagate correct data.

GENERAL RULES

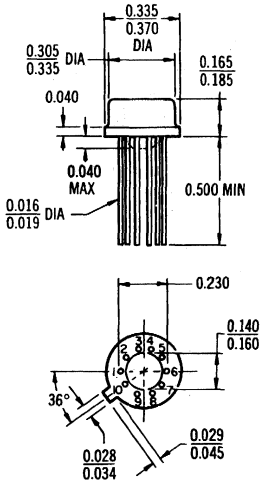
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- A gate output connected in parallel with another output reduces the drive capability by ½ load. (Paralleling gate circuits requires a V_{CC} connection to only one of the gates.)
- Any number of gates may be paralleled if the input loading is increased by ¼ load.
- All unused inputs should be returned to ground.

OUTLINE DIMENSIONS



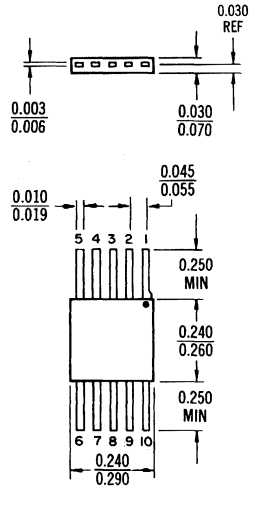
Pin 4 connected to case.

TO-99



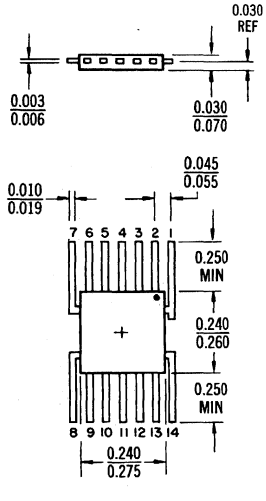
Pin 5 connected to case.

TO-100



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

TO-91



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TO-86

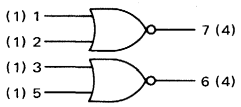
mW MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these two pages describe the MC908 /MC808 MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability — fan-out — (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of −55 to +125°C with V_{CC} = 3.0 V ±10% for the MC908 Series, and 0 to +75°C with V_{CC} = 3.6 V ±10% for the MC808 Series. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

MC910G • MC810G
Dual 2-Input Gate

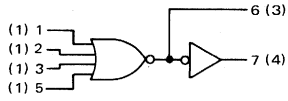


$7 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC910G	MC810G
Input High	8.0	10
Inputs Low	1.0	2.5

MC911G • MC811G
4-Input Gate



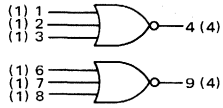
$6 = \overline{1 + 2 + 3 + 5}$

$7 = 1 + 2 + 3 + 5$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC911G	MC811G
Input High	6.0	8.0
Inputs Low	3.5	5.5

MC918G • MC818G
Dual 3-Input Gate

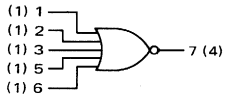


$4 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC918G	MC818G
Input High	9.5	12
Inputs Low	1.0	2.5

MC928G • MC828G
5-Input Gate



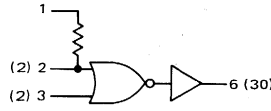
$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC928G	MC828G
Input High	6.5	7.5
Inputs Low	0.5	1.0

BUFFERS

MC909G • MC809G
Buffer

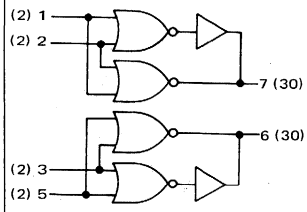


$6 = \overline{2 + 3}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC909G	MC809G
Input High	5.5	7.0
Inputs Low	16	23

MC981G • MC881G
Dual Buffer



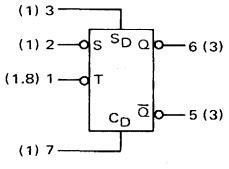
$7 = \overline{1 + 2}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC981G	MC881G
Input High	11	14
Inputs Low	32	46

FLIP-FLOPS

MC913G • MC813G
Type D Flip-Flop



t_{pd} = 75 ns typical

Total Power Dissipation mW typ		
	MC913G	MC813G
Direct Set and Direct Clear Inputs Low, All other Inputs High	17.5	24
Inputs Low	13	17.5

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

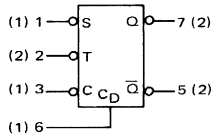
CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

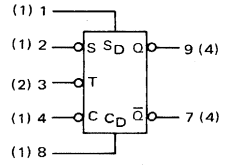
MC920G • MC820G
J-K Flip Flop



t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC920G	MC820G
Only Clock Input High	15.5	20.5
Inputs Low	10	14.5

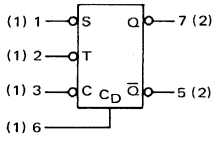
MC922G • MC822G
J-K Flip-Flop



t_{pd} = 70 ns typical

Total Power Dissipation mW typ		
	MC922G	MC822G
Only Clock Input High	17.5	24
Inputs Low	13	20

MC982G • MC882G
J-K Flip-Flop



t_{pd} = 80 ns typical

Total Power Dissipation mW typ		
	MC982G	MC882G
Only Clock Input High	15	23
Inputs Low	13	21

DIRECT INPUT OPERATION ① MC922 and MC822 only

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

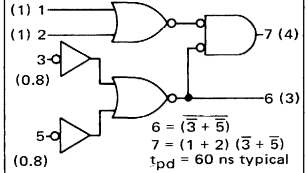
t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

HALF ADDERS

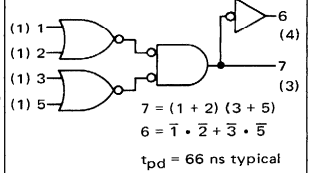
MC908G • MC808G
Half Adder



$6 = (\overline{3} + \overline{5})$
$7 = (1 + 2)(\overline{3} + \overline{5})$
t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC908G	MC808G
Input High	14	19
Inputs Low	8.5	12.5

MC912G • MC812G
Half Adder

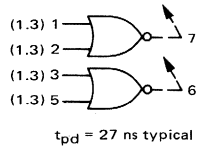


$7 = (1 + 2)(3 + 5)$
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$
t_{pd} = 66 ns typical

Total Power Dissipation mW typ		
	MC912G	MC812G
Input High	11.5	15.5
Inputs Low	5.5	10.5

EXPANDER

MC921G • MC821G
Dual 2-Input Expander



t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC921G	MC821G
Input High	3.0	3.0
Inputs Low	--	--

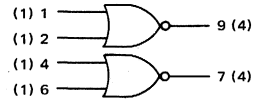
mW MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams on these three pages describe the MC908/MC808 MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal).

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. Loading data are valid over the temperature range of −55 to +125°C with V_{CC} = 3.0 V ±10% for the MC908 Series, and 0 to +75°C with V_{CC} = 3.6 V ±10% for the MC808 Series. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

MC910F • MC810F
Dual 2-Input Gate

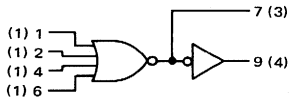


$9 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC910F	MC810F
Input High	8.0	10
Inputs Low	1.0	2.5

MC911F • MC811F
4-Input Gate



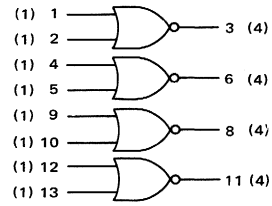
$7 = \overline{1 + 2 + 4 + 6}$

$9 = 1 + 2 + 4 + 6$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC911F	MC811F
Input High	6.0	8.0
Inputs Low	3.5	5.5

MC917F • MC817F
Quad 2-Input Gate

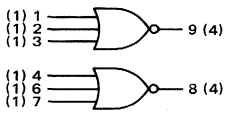


$3 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC917F	MC817F
Input High	16	20
Inputs Low	2.5	5.0

MC918F • MC818F
Dual 3-Input Gate

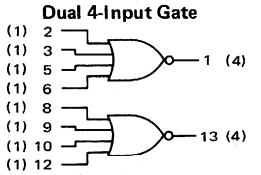


$9 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC918F	MC818F
Input High	9.5	12
Inputs Low	1.0	2.5

MC919F • MC819F
Dual 4-Input Gate

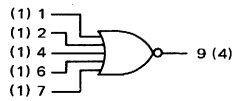


$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC919F	MC819F
Input High	11	1.3
Inputs Low	1.0	2.5

MC928F • MC828F
5-Input Gate

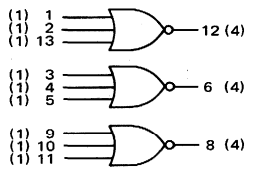


$9 = \overline{1 + 2 + 4 + 6 + 7}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC928F	MC828F
Input High	6.5	7.5
Inputs Low	0.5	1.0

MC993F • MC893F
Triple 3-Input Gate



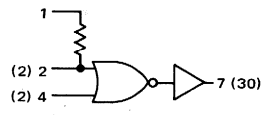
$12 = \overline{1 + 2 + 13}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC993F	MC893F
Input High	14	18
Inputs Low	2.0	3.5

BUFFERS

MC909F • MC809F
Buffer

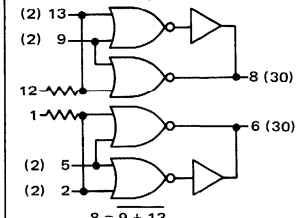


$7 = \overline{2 + 4}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC909F	MC809F
Input High	5.5	7.0
Inputs Low	16	23

MC998F • MC898F
Dual 2-Input Buffer



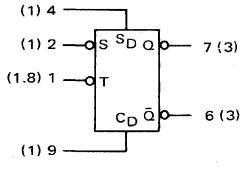
$8 = \overline{9 + 13}$

t_{pd} = 57 ns typical

Total Power Dissipation mW typ		
	MC998F	MC898F
Input High	11	14
Inputs Low	32	46

FLIP-FLOPS

MC913F • MC813F
Type D Flip-Flop



t_{pd} = 75 ns typical

Total Power Dissipation mW typ		
	MC913F	MC813F
Direct Set and Direct Clear Inputs Low, All other Inputs High	17.5	24
Inputs Low	13	17.5

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

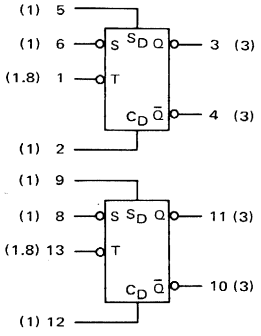
t_n		t_{n+1}	
S	Q		$\bar{Q}$
1	1		0
0	0		1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state.
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse

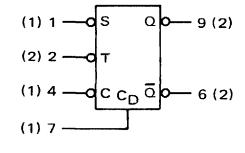
Total Power Dissipation mW typ		
	MC978F	MC878F
Direct Set and Direct Clear Inputs Low, All other Inputs High	35	48
Inputs Low	26	35

MC978F • MC878F
Dual Type D Flip-Flop



t_{pd} = 60 ns typical

MC920F • MC820F
J-K Flip-Flop



t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC920F	MC820F
Only Clock Input High	15.5	20.5
Inputs Low	10	14.5

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC920 and MC820 only

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

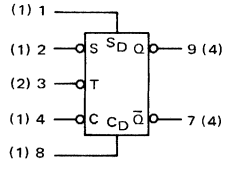
CLOCKED INPUT OPERATION ③ all types

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

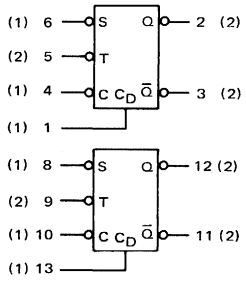
MC922F • MC822F
J-K Flip-Flop



t_{pd} = 70 ns typical

Total Power Dissipation mW typ		
	MC922F	MC822F
Only Clock Input High	17.5	24
Inputs Low	13	20

MC976F • MC876F
Dual J-K Flip-Flop

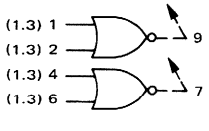


t_{pd} = 50 ns typical

Total Power Dissipation mW typ		
	MC976F	MC876F
Only Clock Input High	31	41
Inputs Low	20	29

EXPANDERS

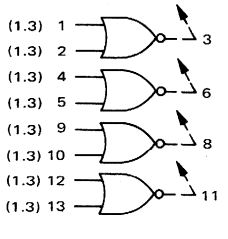
MC921F • MC821F
Dual 2-Input Expander



t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC921F	MC821F
Input High	3.0	3.0
Inputs Low	--	--

MC9921F • MC9821F
Quad 2-Input Expander



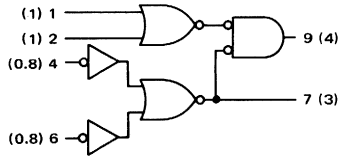
$3 = \overline{1 + 2}$

t_{pd} = 27 ns typical

Total Power Dissipation mW typ		
	MC9921F	MC9821F
Input High	20	20
Inputs Low	–	–

HALF ADDERS

MC908F • MC808F
Half Adder



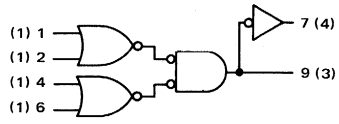
$9 = (1 + 2)(\overline{4} + \overline{6})$

$7 = (\overline{\overline{4} + \overline{6}})$

t_{pd} = 60 ns typical

Total Power Dissipation mW typ		
	MC908F	MC808F
Input High	14	19
Inputs Low	8.5	12.5

MC912F • MC812F
Half Adder



$7 = \overline{1} \cdot \overline{2} + \overline{4} \cdot \overline{6}$

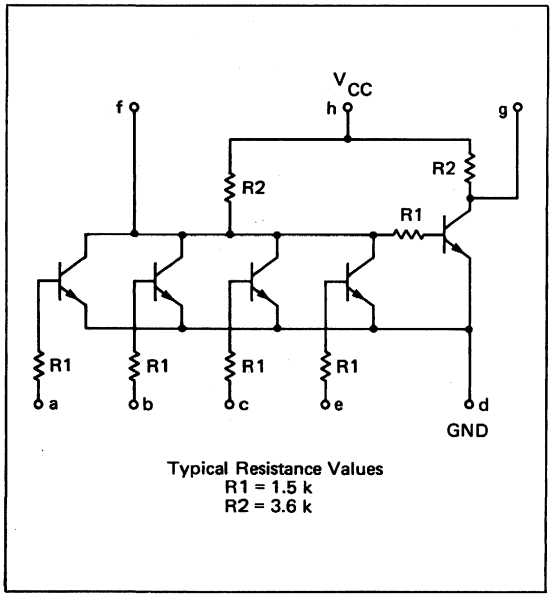
$9 = (1 + 2)(4 + 6)$

t_{pd} = 66 ns typical

Total Power Dissipation mW typ		
	MC912F	MC812F
Input High	11.5	15.5
Inputs Low	5.5	10.5

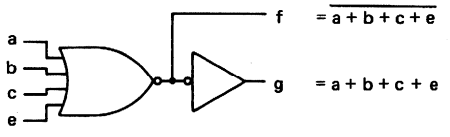
MC911 • MC811

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



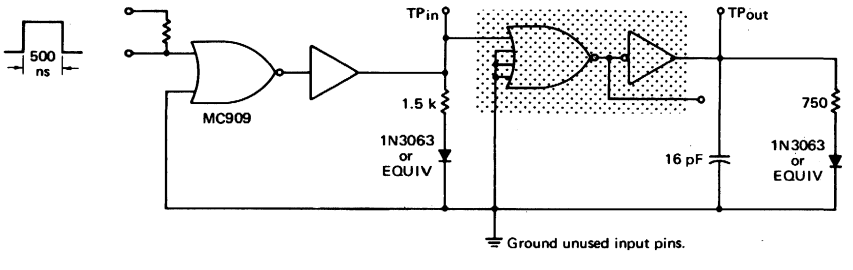
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

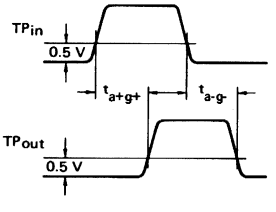
Provides the positive logic NOR function and its complement through an inverter. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC911	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC811	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

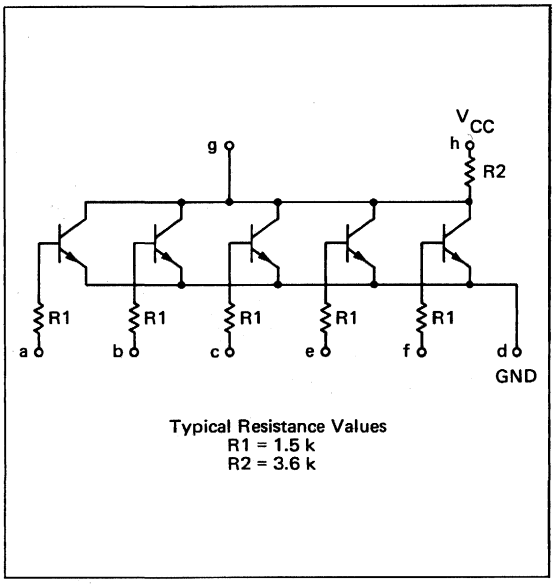
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC911 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC811 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c, e	-	h	-	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e	-	↓	-	↓
		c	-		-		-			-		-		-			c	-	a, b, e	-		-	
		e	-		-		-			-		-		-			e	-	a, b, c	-		-	
Output Current	I_{A3}	f	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	f	-	-	a, b, c, e	h	-	d
	I_{A4}	g	475	-	494	-	418	-		570	-	570	-	535	-	μAdc	g	-	-	f	↓	-	a, b, c, d, e
	I_{AM}	g	-	730	-	815	-	830	↓	-	-	-	-	-	-	-	g	-	-	f		-	a, b, c, d, e
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	-	b, c, d, e
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	-	a, c, d, e
		f	-		-		-			-		-		-			-	c	-	-		-	a, b, d, e
		f	-		-		-			-		-		-			-	e	-	-		-	a, b, c, d
		g	-		-		-			-		-		-			-	f	-	-		-	a, b, c, d, e
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	-	b, c, d, e
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	-	a, c, d, e
		f	-		-		-			-		-		-			c	-	-	-		-	a, b, d, e
		f	-		-		-			-		-		-			e	-	-	-		-	a, b, c, d
		g	-		-		-			-		-		-			f	-	-	-		-	a, b, c, d, e
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, e
																	Pulse In	Pulse Out					
Switching Time	t	a+g+	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	a	g	-	-	h	-	b, c, d, e
		a-g-	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	a	g	-	-	h	-	b, c, d, e

Pins not listed are left open.

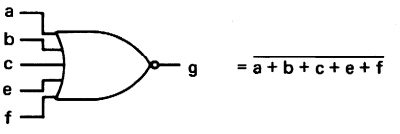
MC928 • MC828

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



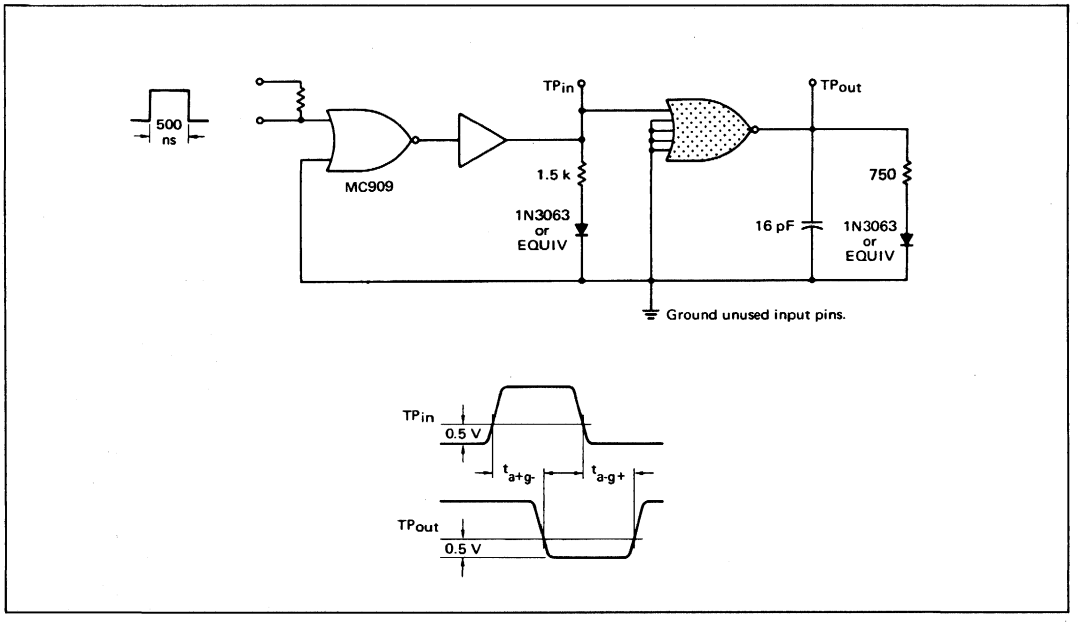
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

Provides the positive logic NOR function. Individual gate elements may be paralleled or used with other logic elements for increasing the number of inputs (subject to loading rules).



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC928	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC828	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

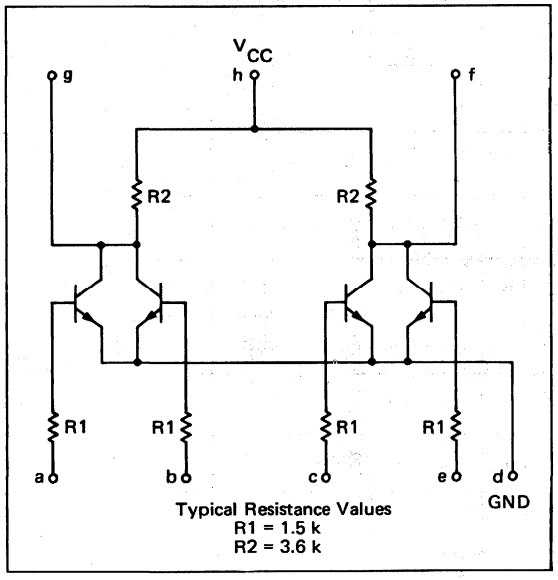
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC928 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC828 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c, e, f	-	h	d
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c, e, f	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b, e, f	-		
		e	-		-		-			-		-		-			e	-	a, b, c, f	-		
		f	-		-		-			-		-		-			f	-	a, b, c, e	-		
Output Current	I_{A4}	g	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	g	-	-	a,b,c,e,f	h	d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	b,c,d,e,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	a,c,d,e,f
		g	-		-		-			-		-		-			-	c	-	-		a,b,d,e,f
		g	-		-		-			-		-		-			-	e	-	-		a,b,c,d,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	f	-	-	↓	a,b,c,d,e
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	b,c,d,e,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	a,c,d,e,f
		g	-		-		-			-		-		-			c	-	-	-		a,b,d,e,f
		g	-		-		-			-		-		-			e	-	-	-		a,b,c,d,f
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	f	-	-	-	↓	a,b,c,d,e
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	h	a,b,c,d,e,f
																	Pulse In	Pulse Out				
Switching time	t	a+g-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	a	g	-	-	h	b,c,d,e,f
		a-g+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	a	g	-	-	h	b,c,d,e,f

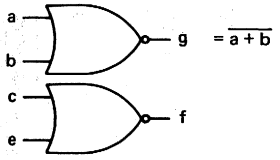
Pins not listed are left open.

MC910 • MC810

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

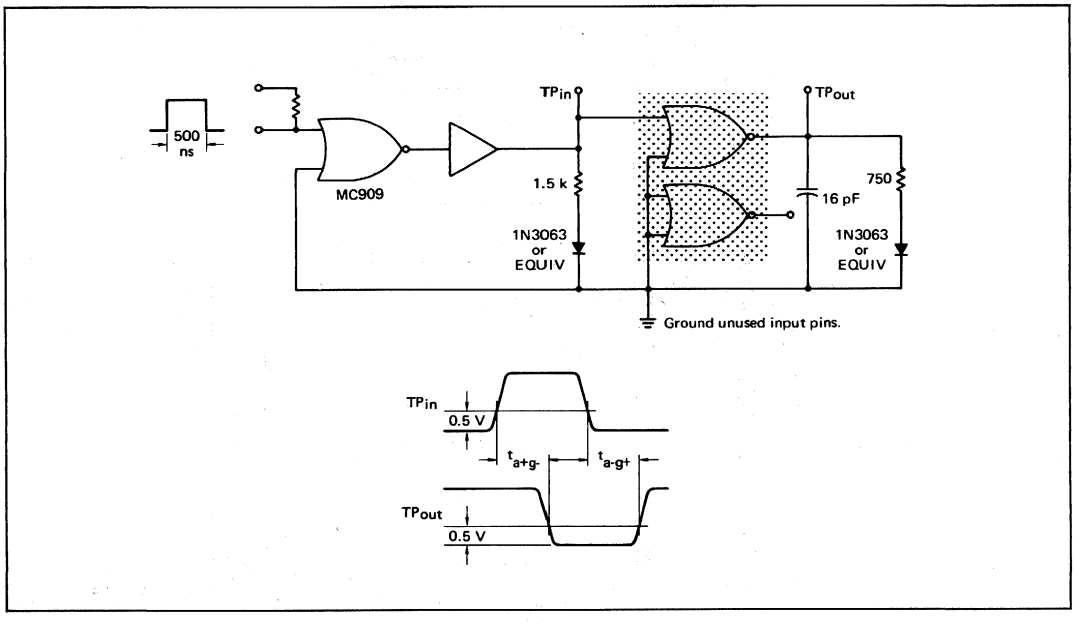


Two 2-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

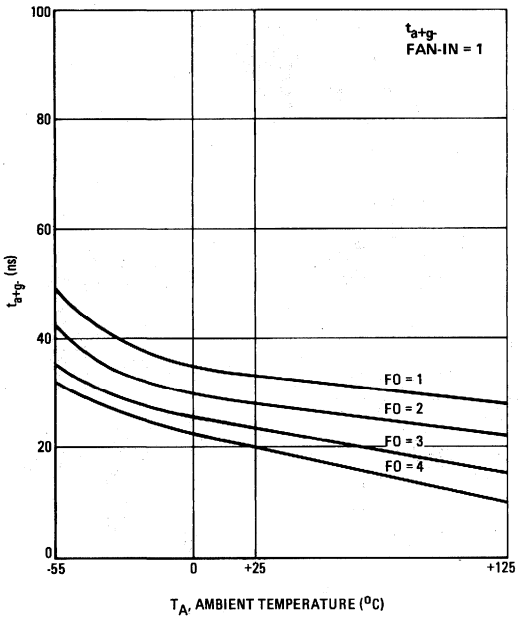
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

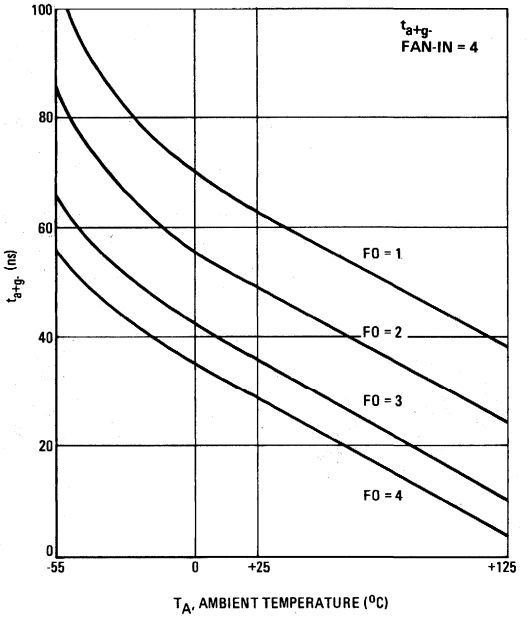
	@Test Temperature	V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
		TEST VOLTAGE VALUES (Volts)				
MC910	−55°C	0.970	0.935	1.80	0.650	3.00
MC910	+25°C	0.805	0.750	1.80	0.450	3.00
MC910	+125°C	0.590	0.555	1.80	0.260	3.00
MC810	0°C	0.880	0.850	1.80	0.500	3.60
MC810	+25°C	0.830	0.800	1.80	0.460	3.60
MC810	+75°C	0.740	0.710	1.80	0.400	3.60

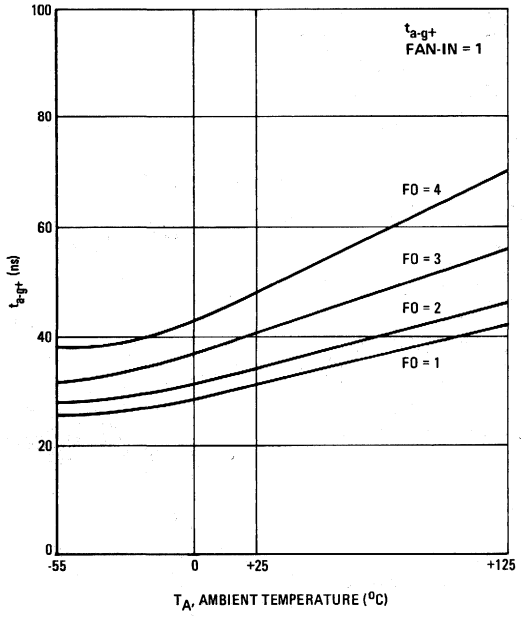
Characteristic	Symbol	Pin Under Test	MC910 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC810 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	µAdc	-	150	-	140	-	140	µAdc	a	-	b	-	h	d
		b	-	125	-	130	-	110	µAdc	-	150	-	140	-	140	µAdc	b	-	a	-	h	d
Output Current	I_{A4}	g	475	-	494	-	418	-	µAdc	570	-	570	-	535	-	µAdc	g	-	c	a, b	h	d
	I_{AM}	g	-	730	-	815	-	830	µAdc	-	-	-	-	-	-	-	g	-	c	a, b	h	d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	b, d
		g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	a, d
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	b, d
		g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	a, d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	µAdc	-	100	-	100	-	100	µAdc	-	-	-	-	h	a, b, d
																	Pulse In	Pulse Out				
Switching Time	t	a+g-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	a	g	-	-	h	d
		a-g+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	a	g	-	-	h	d

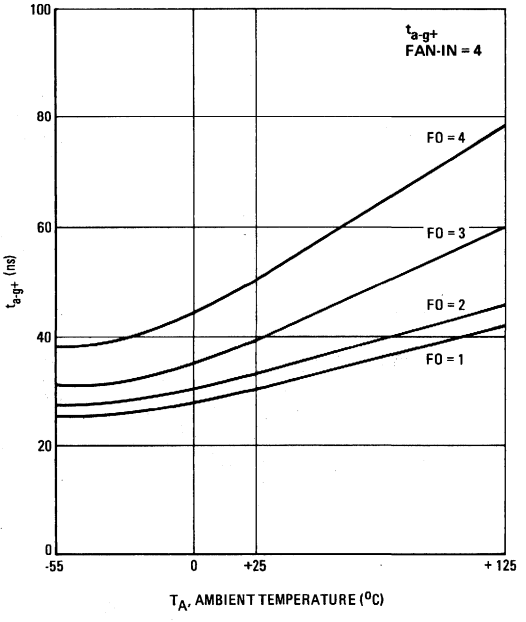
Ground input pins of gate not under test. Other pins not listed are left open.

SWITCHING CHARACTERISTICS



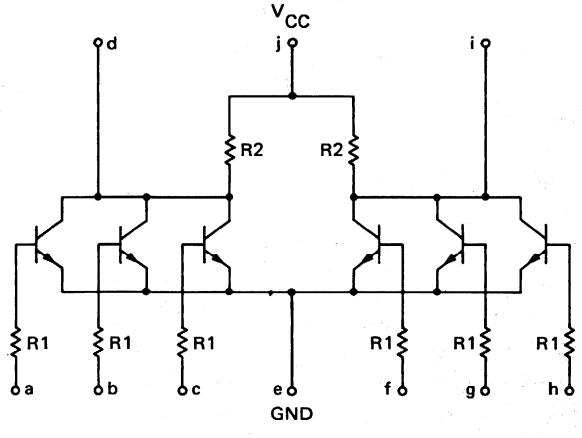






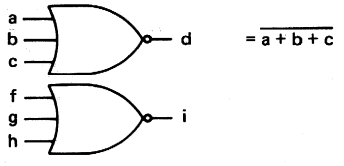
MC918 • MC818

Available in TO-100 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



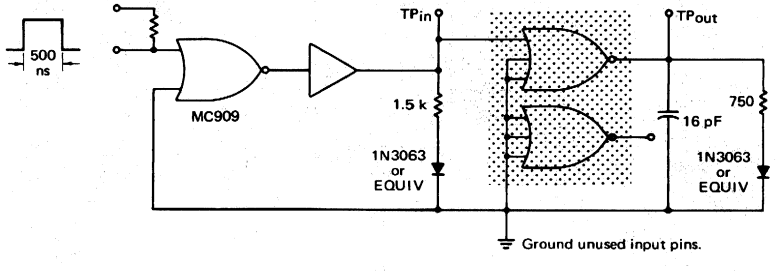
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

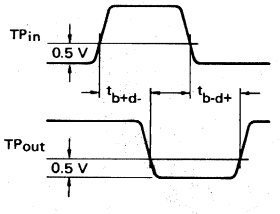
Two 3-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



PIN CONNECTIONS										
Schematic	a	b	c	d	e	f	g	h	i	j
G Package (TO-100)	1	2	3	4	5	6	7	8	9	10
F Package (TO-91)	1	2	3	9	5	4	6	7	8	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

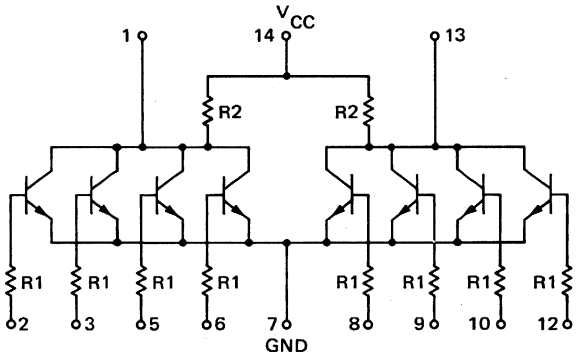
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC918	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC818	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC918 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC818 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b, c	-	j	e
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a, c	-	↓	↓
		c	-		-		-			-		-		-			c	-	a, b	-		
Output Current	I_{A4}	d	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	d	-	g	a, b, c	j	e
	I_{AM}	d	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	d	-	g	a, b, c	j	e
Output Voltage	V_{out}	d	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	j	b, c, e
		d	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	b	-	-	↓	a, c, e
		d	-		-		-			-		-		-			-	c	-	-		a, b, e
Saturation Voltage	$V_{CE(sat)}$	d	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	j	b, c, e
		d	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	-	-	↓	a, c, e
		d	-		-		-			-		-		-			c	-	-	-		a, b, e
Isolation Leakage Current	I_L	j	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	j	a, b, c, e
																	Pulse In	Pulse Out				
Switching Time	t	b+d-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	b	d	-	-	j	a, c, e
		b-d+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	b	d	-	-	j	a, c, e

Ground input pins of gates not under test. Other pins not listed are left open.

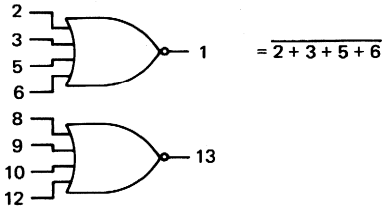
MC919 • MC819

Available in TO-86 Flat Package, Add F Suffix.

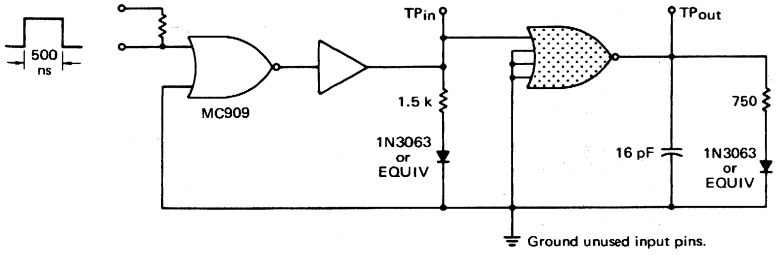


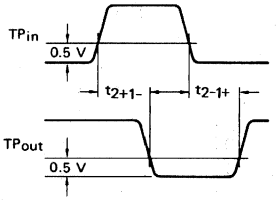
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

Two 4-input positive logic NOR gates in a single package may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

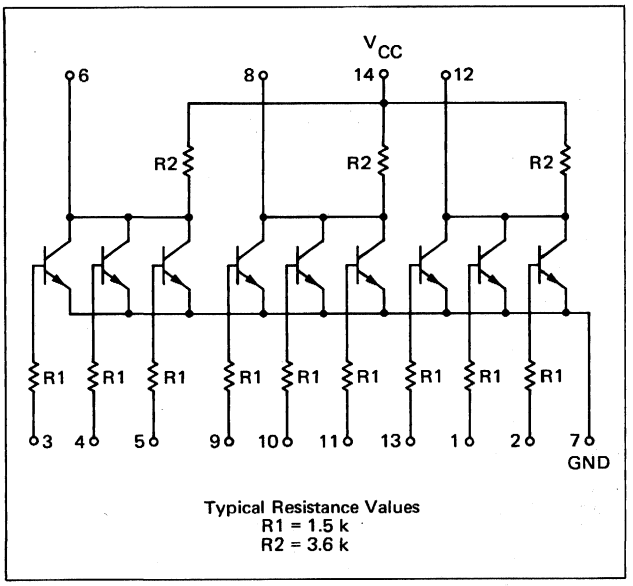
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC919	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC819	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.880	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC919 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC819 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	3, 5, 6	-	14	7
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2, 5, 6	-	↓	↓
		5	-		-		-			-		-		-			5	-	2, 3, 6	-		
		6	-		-		-			-		-		-			6	-	2, 3, 5	-		
Output Current	I_{A4}	1	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	1	-	8	2, 3, 5, 6	14	7
	I_{AM}	1	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	1	-	8	2, 3, 5, 6	14	7
Output Voltage	V_{out}	1	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	3, 5, 6, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	2, 5, 6, 7
		1	-		-		-			-		-		-			-	5	-	-		2, 3, 6, 7
		1	-		-		-			-		-		-			-	6	-	-		2, 3, 5, 7
Saturation Voltage	$V_{CE(sat)}$	1	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	3, 5, 6, 7
		1	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	-	-	↓	2, 5, 6, 7
		1	-		-		-			-		-		-			5	-	-	-		2, 3, 6, 7
		1	-		-		-			-		-		-			6	-	-	-		2, 3, 5, 7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	2,3,5,6,7
																	Pulse In	Pulse Out				
Switching Time	t	2+1-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	2	1	-	-	14	5, 6, 7
		2-1+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	2	1	-	-	14	5, 6, 7

Ground input pins of gates not under test. Other pins not listed are left open.

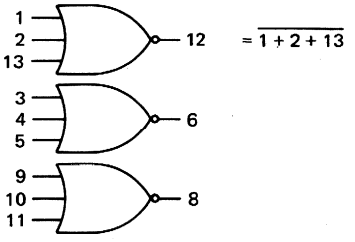
MC993 • MC893

Available in TO-86 Flat Package, Add F Suffix.

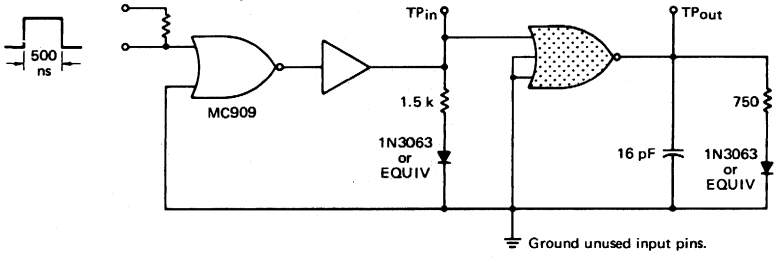


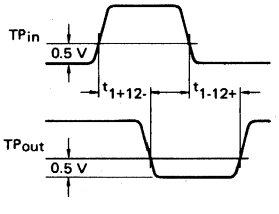
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

Three 3-input positive logic NOR gates in a single package may be used independently, paralleled for increased number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

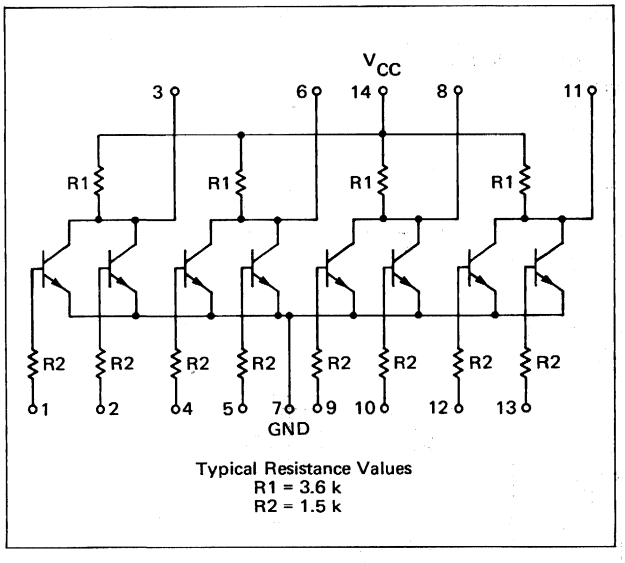
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC993	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC893	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC993 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC893 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2, 13	-	14	7
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 13	-	↓	↓
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	1, 2	-	↓	↓
Output Current	I_{A4}	12	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	12	-	3, 9	1, 2, 13	14	7
	I_{AM}	12	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	12	-	3, 9	1, 2, 13	14	7
Output Voltage	V_{out}	12	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	13	-	-	14	1, 2, 7
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2, 7, 13
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	1, 7, 13
Saturation Voltage	$V_{CE(sat)}$	12	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	13	-	-	-	14	1, 2, 7
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	1	-	-	-	↓	2, 7, 13
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	-	-	↓	1, 7, 13
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	1,2,7,13
																	Pulse In	Pulse Out				
Switching Time	t	1+12-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	1	12	-	-	14	2, 7, 13
		1-12+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	12	-	-	14	2, 7, 13

Ground input pins of gates not under test. Other pins not listed are left open.

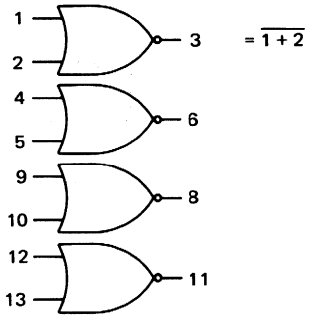
MC917 • MC817

Available in TO-86 Flat Package, Add F Suffix.

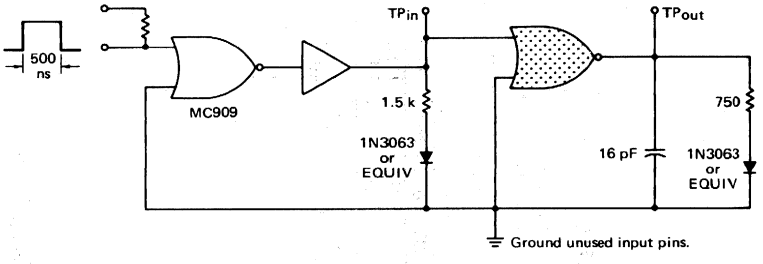


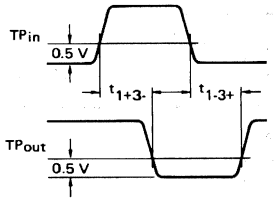
Typical Resistance Values
R1 = 3.6 k
R2 = 1.5 k

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. Each may be used independently or connected together to form non-inverting gates or flip-flops.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only.
Other gates are tested in the same manner.

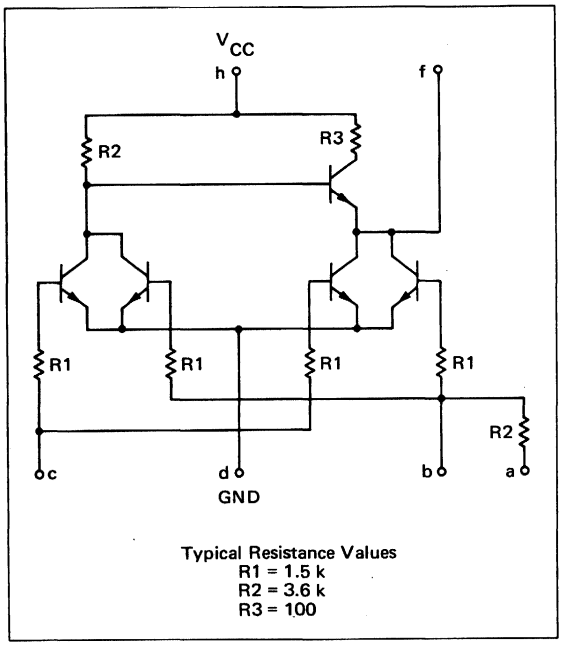
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC917	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC817	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

Characteristic	Symbol	Pin Under Test	MC917 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC817 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2	-	14	7
		2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	1	-	14	7
Output Current	I_{A4}	3	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	3	-	4, 9, 12	1, 2	14	7
	I_{AM}	3	-	730	-	815	-	830	μAdc	-	-	-	-	-	-	-	3	-	4, 9, 12	1, 2	14	7
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	2, 7
		3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc		2	-	-	14	1, 7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	14	2, 7
		3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	1, 7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	14	1, 2, 7
																	Pulse In	Pulse Out				
Switching Time	t	1+3-	-	-	-	50	-	-	ns	-	-	-	50	-	-	ns	1	3	-	-	14	2, 7
		1-3+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	3	-	-	14	2, 7

Ground input pins of gates not under test. Other pins not listed are left open.

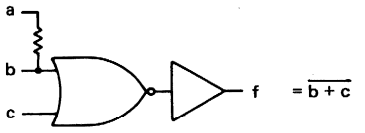
MC909 • MC809

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



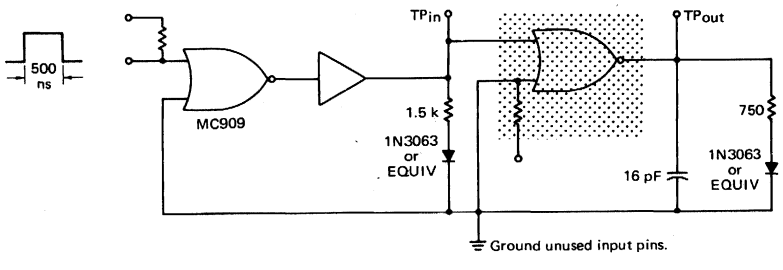
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

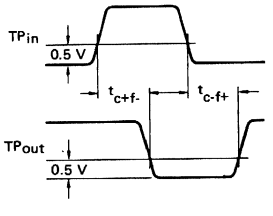
This buffer is designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	—	6	—	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





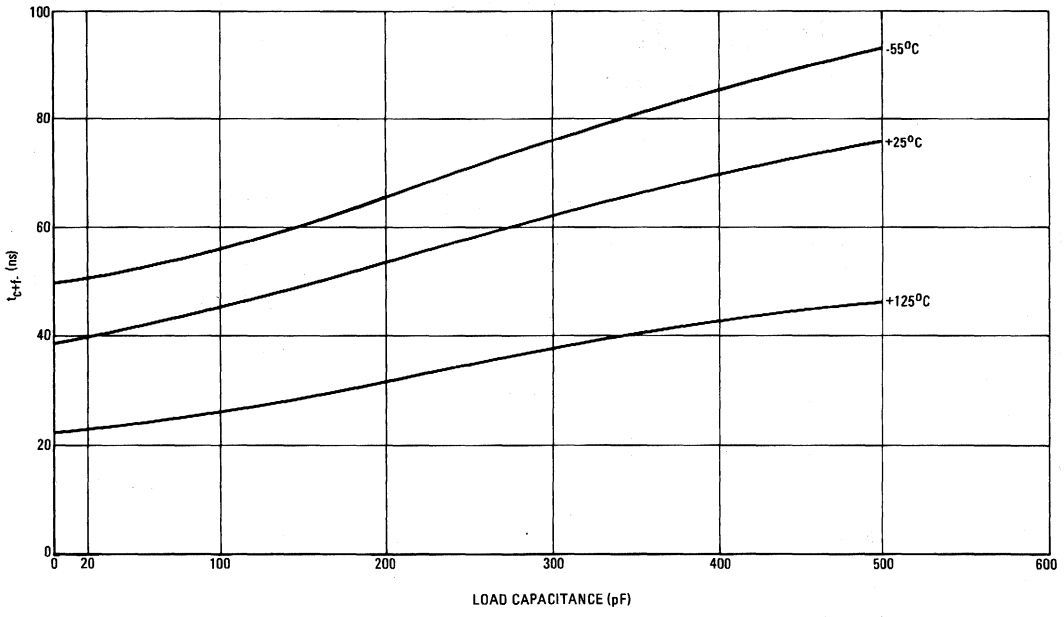
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ)
MC909	−55°C	0.970	0.935	1.80	0.650	3.00	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0
MC809	0°C	0.880	0.850	1.80	0.500	3.60	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7

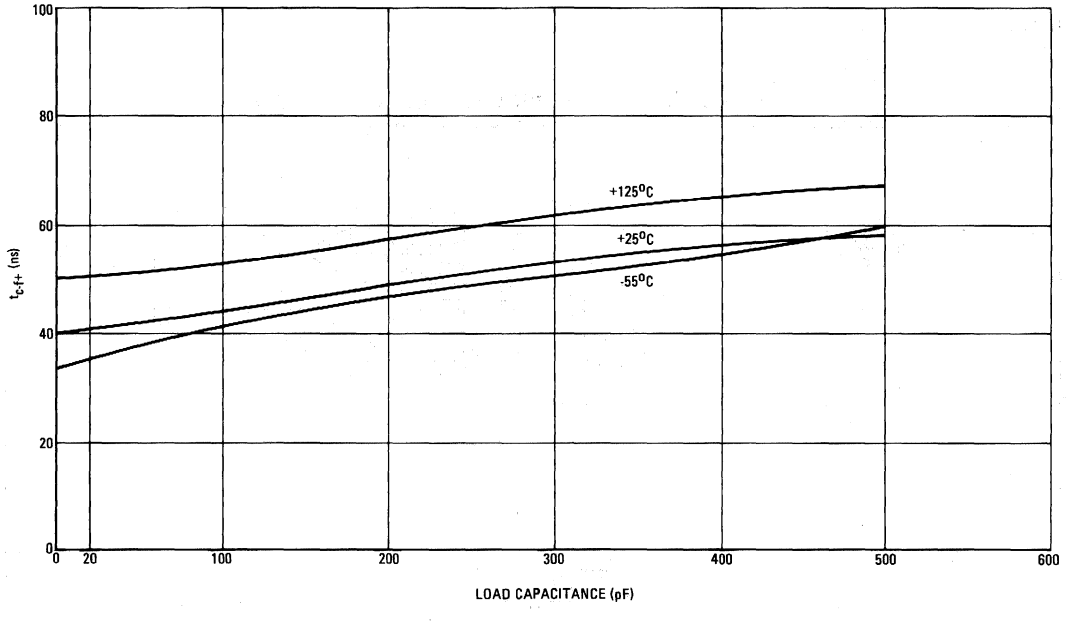
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC909 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC809 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	Gnd
Input Current	$2I_{in}$	b	-	250	-	260	-	220	µAdc	-	300	-	280	-	280	µAdc	b	-	c	-	h	-	d
		c	-	250	-	260	-	220	µAdc	-	300	-	280	-	280	µAdc	c	-	b	-	h	-	d
Output Current	I_{AB}	f	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	f	-	-	b, c	h	-	d
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	f	c, d
		f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	c	-	-	h	f	b, d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	f	c, d
		f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	c	-	-	-	h	f	b, d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	µAdc	-	100	-	100	-	100	µAdc	-	-	-	-	h	-	b, c, d
																	Pulse In	Pulse Out					
Switching Time	t	c+f-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	c	f	-	-	h	-	b, d
		c-f+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	c	f	-	-	h	-	b, d

Pins not listed are left open. *Resistor value to V_{CC}

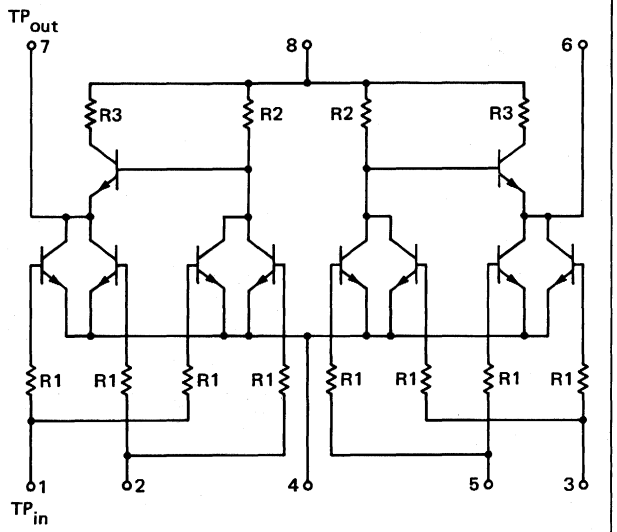
PROPAGATION DELAY versus TEMPERATURE





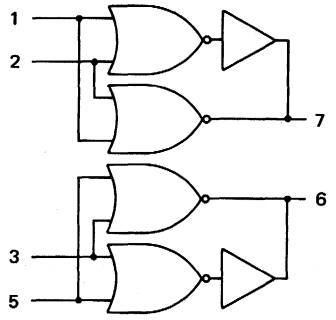
MC981 • MC881

Available in TO-99 Metal Can, Add G Suffix.



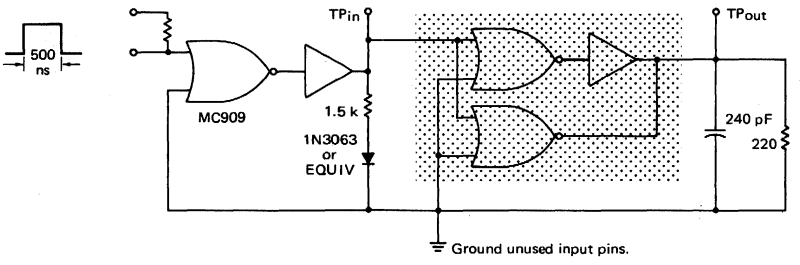
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

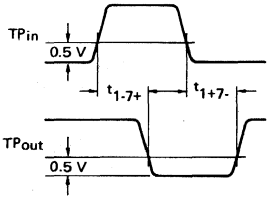
These Buffers are designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit.



$7 = \overline{1+2}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one buffer only.
The other buffer is tested in the same manner.

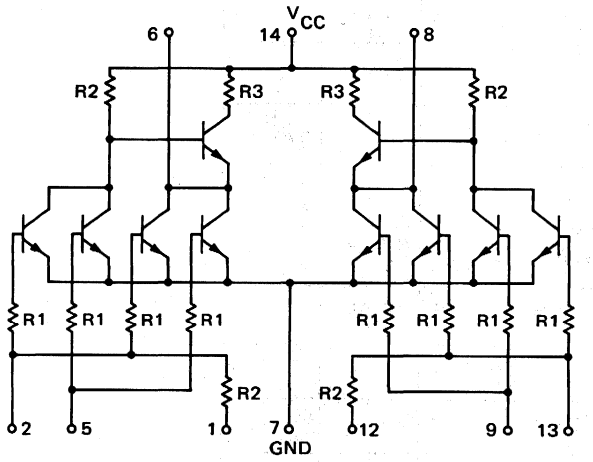
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	($k\Omega$)
MC981	−55°C	0.970	0.935	1.80	0.650	3.00	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0
MC881	0°C	0.880	0.850	1.80	0.500	3.60	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7

Characteristic	Symbol	Pin Under Test	MC981 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC881 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	Gnd
Input Current	$2I_{in}$	1	-	250	-	260	-	220	µAdc	-	300	-	280	-	280	µAdc	1	-	2	-	8	-	4
		2	-	250	-	260	-	220	µAdc	-	300	-	280	-	280	µAdc	2	-	1	-	8	-	4
Output Current	I_{AB}	7	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	7	-	-	1,2	8	-	4
Output Voltage	V_{out}	7	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	8	7	2,4
		7	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	8	7	1,4
Saturation Voltage	$V_{CE(sat)}$	7	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	8	7	2,4
		7	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	8	7	1,4
Isolation Leakage Current	I_L	8	-	100	-	100	-	100	µAdc	-	100	-	100	-	100	µAdc	-	-	-	-	8	-	1,2,3,4,5
																	Pulse In	Pulse Out					
Switching Time	t	1+7-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	1	7	-	-	8	-	2,4
		1-7+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	1	7	-	-	8	-	2,4

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

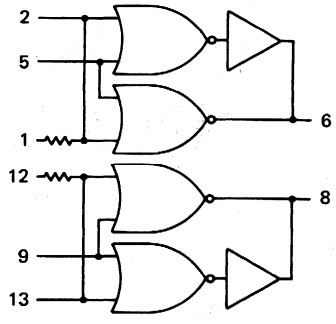
MC998 • MC898

Available in TO-86 Flat Package, Add F Suffix.



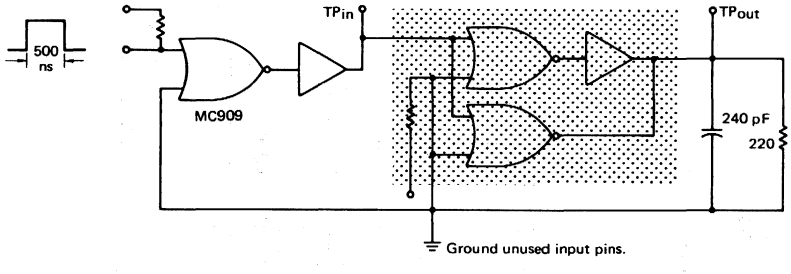
Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 100

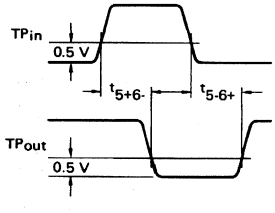
These Buffers are designed to drive a greater number of loads than the basic Resistor Transistor Logic Circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



$6 = \overline{2 + 5} = \overline{2} \cdot \overline{5}$

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures shown are for one buffer only.
The other buffer is tested in the same manner.

@Test Temperature		V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	(kΩ)
		TEST VOLTAGE VALUES (Volts)						
MC998	−55°C	0.970	0.935	1.80	0.650	3.00	0.500	4.27
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400	4.3
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300	5.0
MC898	0°C	0.880	0.850	1.80	0.500	3.60	0.450	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350	4.7

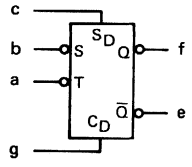
Characteristic	Symbol	Pin Under Test	MC998 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC898 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	V_{RH}*	Gnd
Input Current	$2I_{in}$	2	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	2	-	5	-	14	-	-	7
		5	-	250	-	260	-	220	μAdc	-	300	-	280	-	280	μAdc	5	-	2	-	14	-	-	7
Output Current	I_{AB}	6	3.75	-	4.0	-	3.3	-	mAdc	4.5	-	4.5	-	4.5	-	mAdc	6	-	-	2,5	14	-	-	7
Output Voltage	V_{out}	6	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	-	6	5,7
		6	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	5	-	-	14	-	6	2,7
Saturation Voltage	$V_{CE(sat)}$	6	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	2	-	14	-	6	5,7
		6	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	5	-	14	-	6	2,7
Isolation Leakage Current	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	-	2,5,7
																	Pulse In	Pulse Out						
Switching Time	t	5+6-	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	5	6	-	-	14	-	-	2,7
		5-6+	-	-	-	70	-	-	ns	-	-	-	70	-	-	ns	5	6	-	-	14	-	-	2,7

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC913 • MC813

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

The MC913/MC813 RTL Type D Flip-Flop is a storage element that stores the state of pin b during negative transitions of pin a. The flip-flop is not affected by changes of pin b during either the low or high state of the clock. Using pins c and g as inputs produces a standard R-S flip-flop.



DIRECT INPUT OPERATION ①

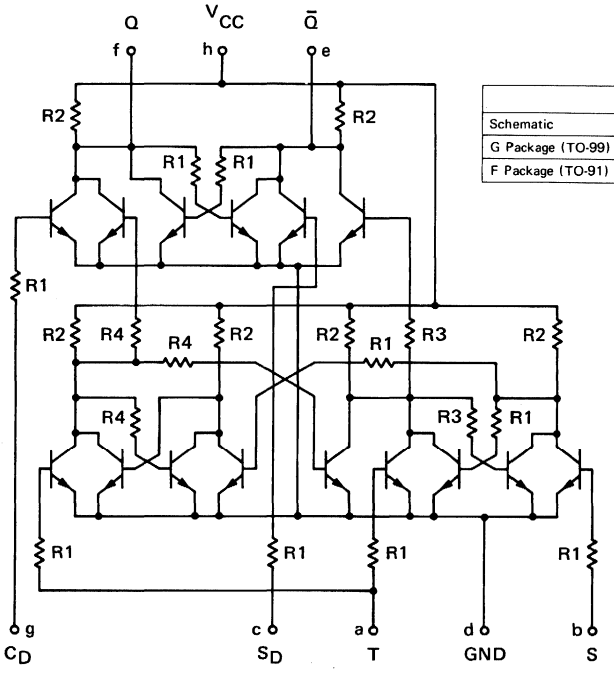
S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	$t_n + 1$	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
$t_n + 1$ = time period subsequent to negative transition of clock pulse



PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 180
R4 = 480

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC913	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC813	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC913 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC813 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	$1.8\ I_{in}$	a	-	225	-	234	-	198	μAdc	-	270	-	252	-	252	μAdc	a	-	-	-	h	-	b, c, d, g
	$1.8\ I_{in}$	a	-	225	-	234	-	198		-	270	-	252	-	252		a	-	b	-		-	c, d, g
	I_{in}	b*	-	125	-	130	-	110		-	150	-	140	-	140		b	-	-	a		-	c, d, g
		c*	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		c	-	b	↓		-	d, g
		g*	-		-		-			-		-		-			g	-	-			-	b, c, d
Output Current	I_{A3}	e	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	e	a	b, g	c	h	-	d
		e*	↓	-	↓	-	↓	-		↓	-	↓	-	↓	-		e	-	g	a, c		-	b, d
		f		-		-		-			-		-		-		-	g	a, c	-		-	b, d
		f*		-		-		-			-		-		-		f	b	c	a, g	↓	-	d
Output Voltage	V_{out}	e	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	c	a, g	-	h	-	b, d
		e	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	f	a	-		-	b, c, d, g
		f	-		-		-			-		-		-			-	g	a, c	-		-	b, d
		f	-		-		-			-		-		-			-	e	a	-	↓	-	b, c, d, g
Saturation Voltage	$V_{CE\,(sat)}$	e	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	c	-	a, g	-	h	-	b, d
		e	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		f	-	a	-		-	b, c, d, g
		e*	-		-		-			-		-		-			-	b	g	a		-	c, d
		f	-		-		-			-		-		-			g	-	a, c	-		-	b, d
		f	-		-		-			-		-		-			e	-	a	-		-	b, c, d, g
		f*	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓		-	-	c	a, b	↓	-	d, g
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, g

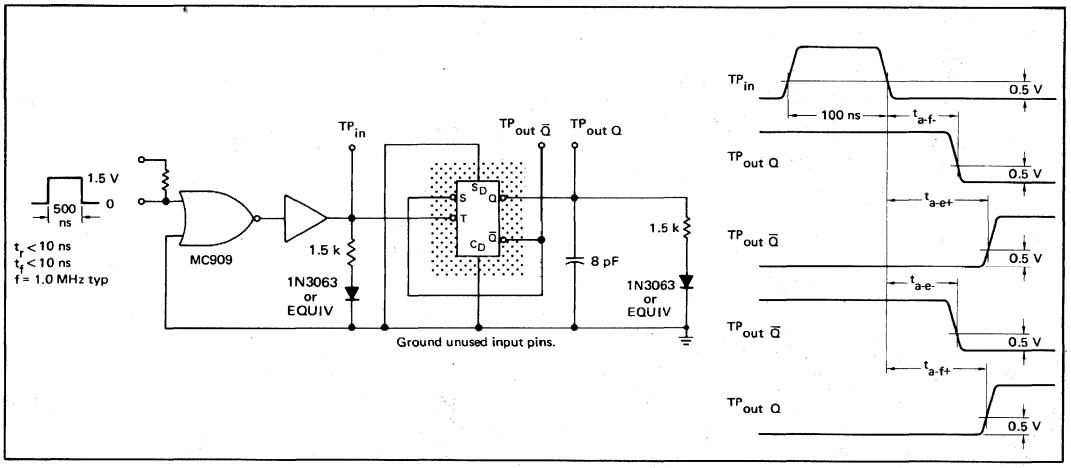
Pins not listed are left open.

*The voltage applied to pin a must change from V_{RL} to V_{off} prior to making measurements.

V_{RL} = Resistance value to V_{CC}; V_{RL} = 2.8 k ohms @ -55°C, @ 0°C; V_{RL} = 2.7 k ohms @ +25°C, V_{RL} = 3.0 k ohms @ +125°C @ +75°C

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 1



SET-UP AND RELEASE TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 2A

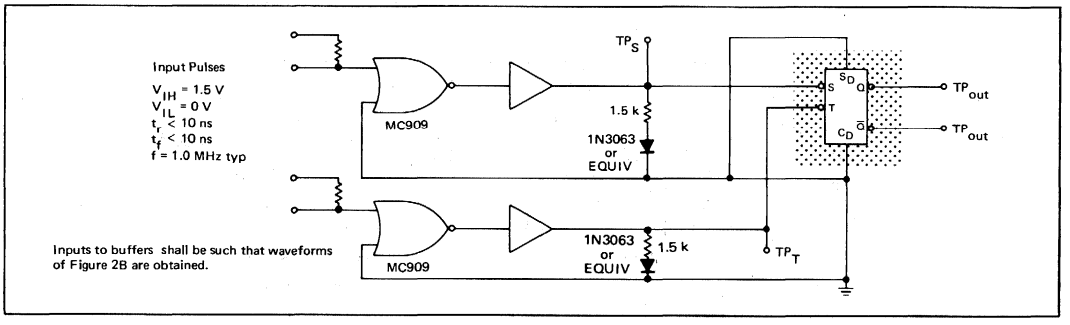
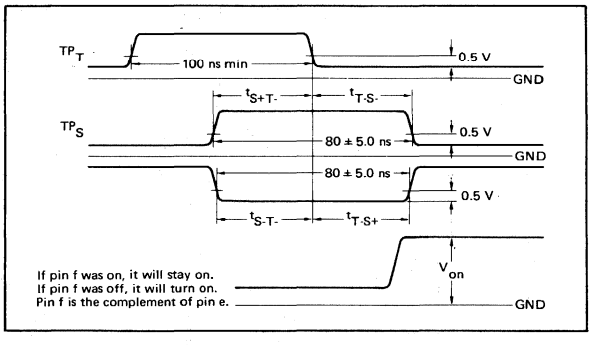


FIGURE 2B

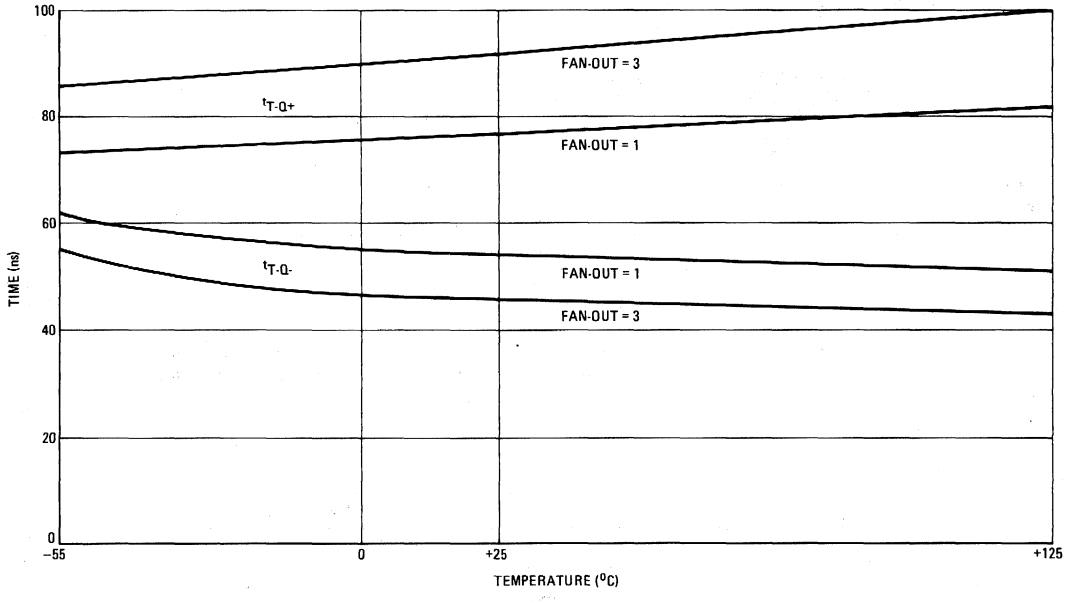


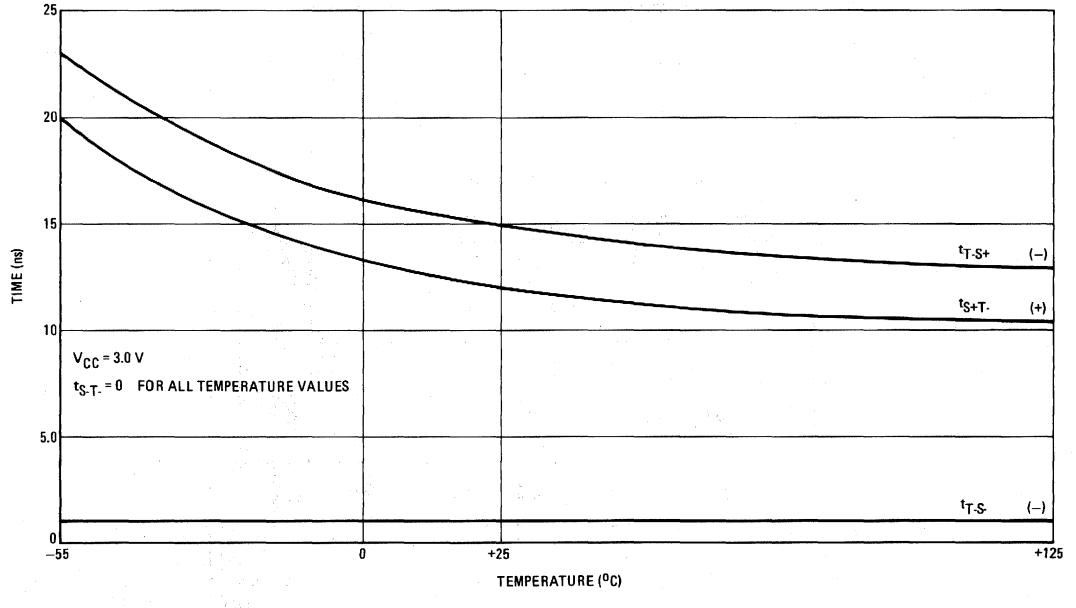
SWITCHING TIMES

Test	Fig. No.	ns @ 25°C	
		min	max
$t_{T-\bar{Q}-}$*	1	--	80
$t_{T-\bar{Q}+}$*	1	--	120
t_{T-Q-}*	1	--	80
t_{T-Q+}*	1	--	120
t_{S+T-}	2	60	--
t_{T-S-}	2	30	--
t_{S-T-}	2	60	--
t_{T-S+}	2	30	--

*Tie pin b to pin e

SWITCHING TIMES versus TEMPERATURE

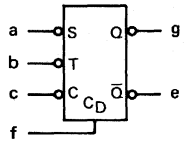




MC920 • MC820

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

J-K Flip-Flop with a direct clear input in addition to the clocked inputs.

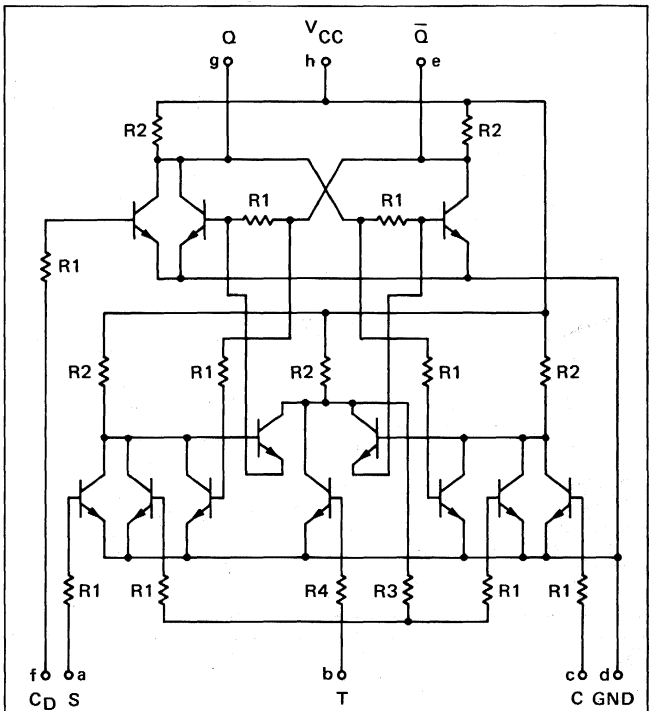


Direct Input (C_D) must be low.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse.
Q_n = state of Q output in time period t_n.

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 3.0 k
R4 = 750

ELECTRICAL CHARACTERISTICS

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_{LL}
MC920	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC820	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC920 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC820 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	e	-	h	-	d
	$2I_{in}$	b	-	250	-	260	-	220		-	300	-	280	-	280		b	-	a, c	-		-	
	I_{in}	c	-	125	-	130	-	110		-	150	-	140	-	140		c	-	g	-		-	
	I_{in}	f	-	125	-	130	-	110		-	150	-	140	-	140		f	-	e	-		-	
Output Current	I_{A2}	e	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	e	a, f	-	h	-	d
		e		-		-		-			-		-		-		-	e, f	a	-		-	
		g#		-		-		-			-		-		-		-	g	c	f		-	
Output Voltage	V_{out}	e#	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	g	-	-	h	-	d
		e*#	-		-		-			-		-		-			-	a, c	-	-		-	d, f
		e*§	-		-		-			-		-		-			-	a	-	c		-	
		e*§	-		-		-			-		-		-			-	-	-	a, c		-	
		g	-		-		-			-		-		-			-	f	-	-		-	d, e
		g§	-		-		-			-		-		-			-	e	-	-		-	d
		g*§	-		-		-			-		-		-			-	a, c	-	-		-	d, f
		g*#	-		-		-			-		-		-			-	c	-	a		-	
		g*#	-		-		-			-		-		-			-	-	-	a, c		-	
Saturation Voltage	$V_{CE(sat)}$	e#	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	-	f	h	-	d
		g	-		-		-			-		-		-			-	-	f	-		-	d, e
		g§	-		-		-			-		-		-			-	-	-	-		-	d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	d

Pins not listed are left open.

Pin e = LOW
§ Pin g = LOW
} Set by a momentary ground prior to the application of the negative-going clock pulse.

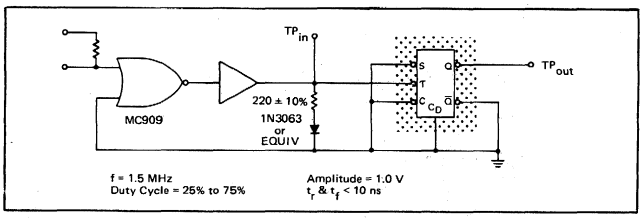
* = Clock Pulse to Pin b. (see Fig. 4)

SWITCHING TIMES

Test	Fig. No.	Over-All Temperature Range		Unit
		min	max	
T-$\bar{Q}$-	2	20	80	ns
T-Q+	2	--	120	ns
C_D+Q-	3	--	60	ns
C_D+$\bar{Q}$+	3	--	120	ns

NOTE: Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

FIGURE 1 - TOGGLE MODE TEST CIRCUIT



SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 2

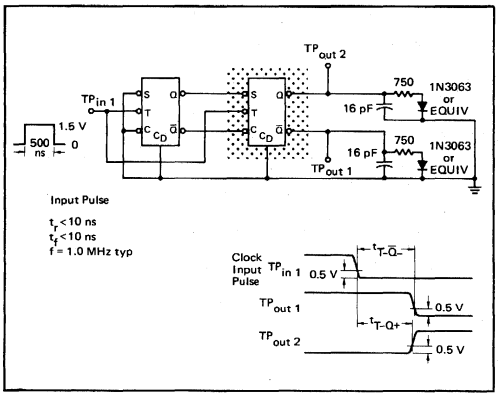


FIGURE 3

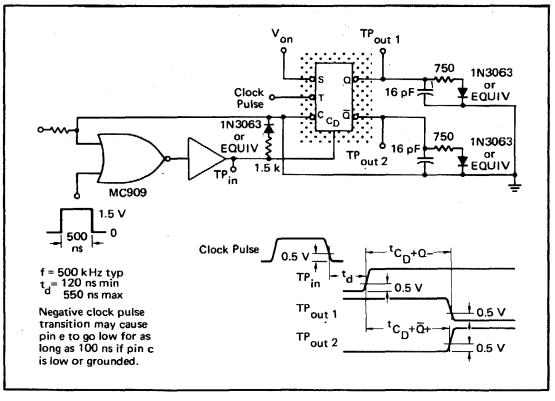
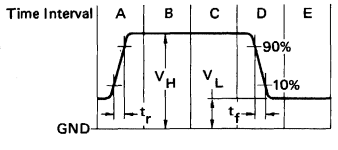


FIGURE 4



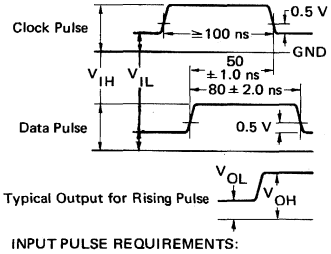
SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $<1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC820

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

FIGURE 5



INPUT PULSE REQUIREMENTS:

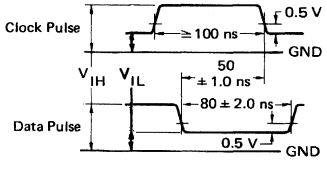
V_{IL} = 0.200 V max
V_{IH} = 0.894 V min. 1.500 V max
t≤10 ns
t≤10 ns
f = 1.0 MHz typ

NOTE:
Measurements for output voltages should be taken at least 100 ns after pulses have occurred.

MC920

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

FIGURE 6



INPUT PULSE REQUIREMENTS:

V_{IL} = 0.200 V max
V_{IH} = 0.894 V min, 1.500 V max
t≤10 ns
t≤10 ns
f = 1.0 MHz typ

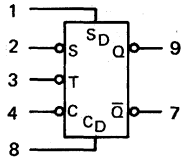
SEQUENCE OF EVENTS:

A. Apply all dc biases required.
B. Apply momentary ground to pin indicated. This sets the flip-flop. Momentary ground must occur before the pulses shown above every time, or the flip-flop will toggle to the wrong condition every alternate pulse.
C. After momentary ground has been released, apply pulses marked above.
D. Measure voltage of designated output after the pulse measurements for output voltages should be taken at least 100 ns after pulses have occurred.

MC922 • MC822

Available in TO-100 Metal Can, Add G Suffix
Available in TO-91 Flat Package, Add F Suffix

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



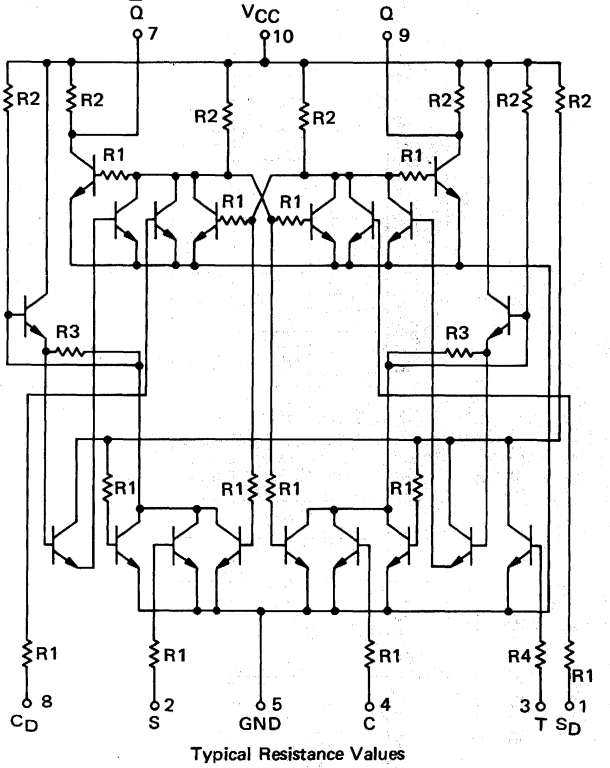
CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	③	③
1	0	1	0
0	1	0	1
1	1	0	0

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n, and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values

R1 = 1.5 k R3 = 2.0 k
R2 = 3.6 k R4 = 750

F Package And G Package Pin-Outs Are The Same

ELECTRICAL CHARACTERISTICS

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC922	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC822	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

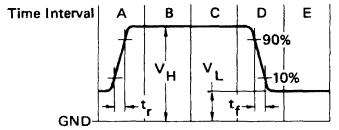
Characteristic	Symbol	Pin Under Test	MC922 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC822 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	-	-	10	5
	I_{in}	2	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	2	-	8	-	↓	↓
	$2\ I_{in}$	3	-	250	-	260	-	220		-	300	-	280	-	280		3	-	2, 4	-		
	I_{in}	4	-	125	-	130	-	110		-	150	-	140	-	140		4	-	1	-		
	I_{in}	8	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	8	-	-	-	↓	↓
Output Current	I_{A4}	7	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	-	7, 1	8	-	10	5
		9	475	-	494	-	418	-	μAdc	570	-	570	-	535	-	μAdc	-	8, 9	1	-	10	5
Saturation Voltage	$V_{CE(sat)}$	7	-	220	-	222	-	220	mVdc	-	250	-	250	-	250	mVdc	-	1	-	8	10	5
	↓	7*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	4	↓	↓
		7*#	-		-		-			-		-		-			-	-	-	2, 4		
		7§*	-		-		-			-		-		-			-	2, 4	-	-		
		9	-		-		-			-		-		-			-	8	-	1		
		9§*	-		-		-			-		-		-			-	4	-	2		
		9*#	-		-		-			-		-		-			-	2, 4	-	-		
		9§*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2, 4	↓	↓

§ Pin 1 = High
# Pin 8 = High
Set by momentary application of V_{BOT} prior to the negative going clock pulse.

* Pin 3 = Clock pulse to pin 3 (see Figure 1).

Pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $<1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

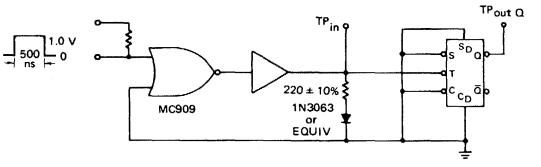
MC822

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+850 ± 2.0 mVdc
0°C	+500 ± 2.0 mVdc	+900 ± 2.0 mVdc
+75°C	+400 ± 2.0 mVdc	+760 ± 2.0 mVdc

MC922

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+800 ± 2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+985 ± 2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+605 ± 2.0 mVdc

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz
Duty Cycle = 25% to 75%
t_r & t_f < 10 ns

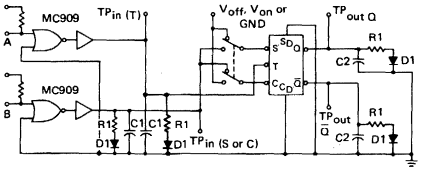
NOTE:
Waveform at the output test point should be ½ the frequency of the waveform at the input test point.

SWITCHING TIMES

Test	Figure No. 3	Maximum (ns)
t_{T-Q-}	3B	150
$t_{T-\bar{Q}-}$	3B	150
t_{T-Q+}	3B	100
$t_{T-\bar{Q}+}$	3B	100
t_{S+T-}	3C	50
t_{S-T-}	3C	30
t_{C+T-}	3C	50
t_{C-T-}	3C	30
t_{T-S+}	3C	0
t_{T-S-}	3C	+5
t_{T-C+}	3C	0
t_{T-C-}	3C	+5
$t_{C_D+\bar{Q}-}$	4	140
t_{C_D+Q+}	4	70
$t_{S_D+\bar{Q}+}$	4	140
t_{S_D+Q-}	4	70

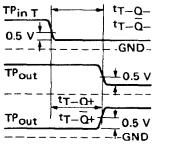
SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

FIGURE 3A - SET-UP, RELEASE AND SWITCHING TIMES TEST CIRCUIT



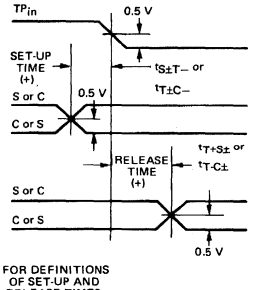
C1 = 20 pF Including Jig and Probe
C2 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or Equivalent

FIGURE 3B - SWITCHING TIME WAVEFORMS



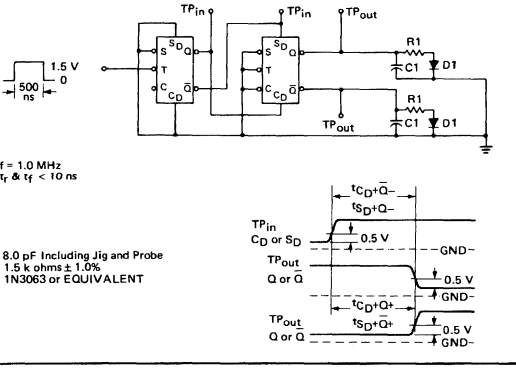
NOTE: Whichever input pin (S or C) is tied to MC909 Buffer on input pin B is at virtual ground when the input is tied to V_{BOT}.

FIGURE 3C - SET-UP AND RELEASE TIME



FOR DEFINITIONS OF SET-UP AND RELEASE TIMES, SEE GENERAL INFORMATION SECTION.

FIGURE 4 - DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY TIME



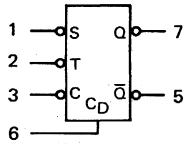
f = 1.0 MHz
t_r & t_f < 10 ns

C1 = 8.0 pF Including Jig and Probe
R1 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or EQUIVALENT

MC982 • MC882

Available in TO-99 Metal Can, Add G Suffix.

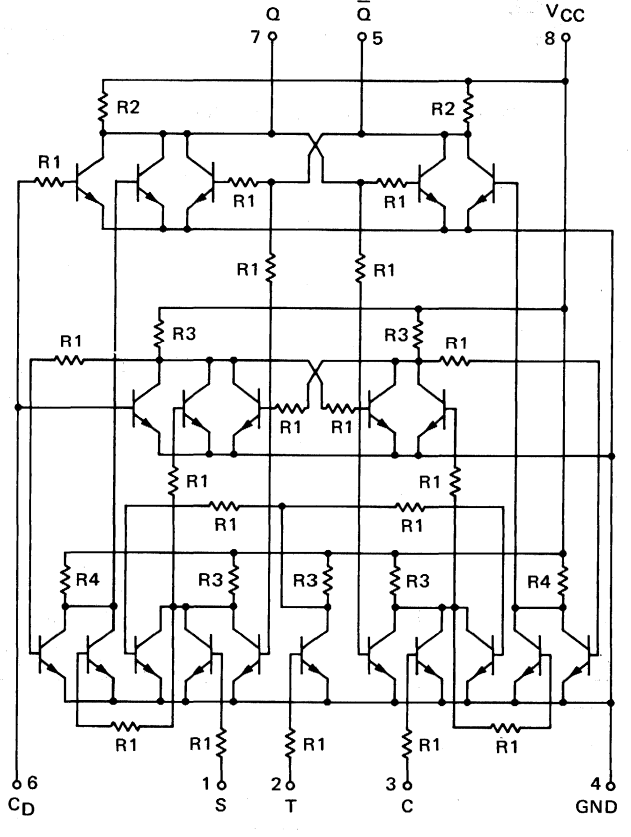
J-K Flip-Flop with a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION ①

t_n ③		t_{n+1} ②	
S	C	Q	$\overline{Q}$
1	1	Q_n ③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ④

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 4.5 k
R4 = 7.2 k

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC982	−55°C	0.970	0.935	1.80	0.650	3.00
	+25°C	0.805	0.750	1.80	0.450	3.00
	+125°C	0.590	0.555	1.80	0.260	3.00
MC882	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC982 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC882 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Grd
Input Current	I_{in}	1#*	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	-	-	3	-	8	4,6
		2	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	2	-	3	-	↓	1,3,4,6
		3*§	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	-	1	-	↓	4,6
	$2\ I_{in}$	6	-	250	-	260	-	220	↓	-	300	-	280	-	280	↓	6	-	2,3,5	-	↓	4
Output Current	I_{A2}	5*†	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	-	3	-	8	1,4,6
		7*‡	238	-	247	-	209	-	μAdc	270	-	290	-	255	-	μAdc	-	-	1	-	8	3,4,6
Saturation Voltage	$V_{CE(sat)}$	5**Δ	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	1	-	3	8	4,6
		5**Δ	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	-	-	1,3	↓	4,6
		7	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	6	1,2	-	↓	3,4,5
		7**◇	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	1,3	-	-	↓	4
		7**ΔΔ	-	↓	-	↓	-	↓		-	↓	-	↓	-	↓	↓	-	3	-	1	↓	4,6
		7**ΔΔ	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1,3	↓	4,6

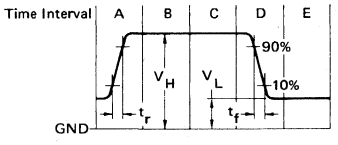
Pins not listed are left open.

* = Pin 2 Clock Pulse a
** = Pin 2 Clock Pulse c
\# = Pin 1 Clock Pulse b
§ = Pin 3 Clock Pulse b
† = Pin 5 Clock Pulse b
‡ = Pin 7 Clock Pulse b (See Figure 4.)

Δ Pin 5 = } Momentary ground prior to negative transition of Clock Pulse c.
ΔΔ Pin 7 = }

◇ Pin 6 = Momentary V_{BOT} prior to negative transition of Clock Pulse c.

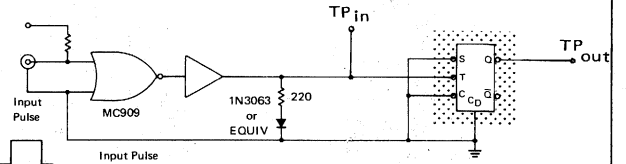
FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be <1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



MC882

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850 ±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900 ±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760 ±2.0mVdc

MC982

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800 ±2.0mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0mVdc
+125°C	+260 ± 2.0 mVdc	+0.605 ±2.0mVdc

SWITCHING TIME TEST CIRCUITS AND WAVE FORMS

FIGURE 3A

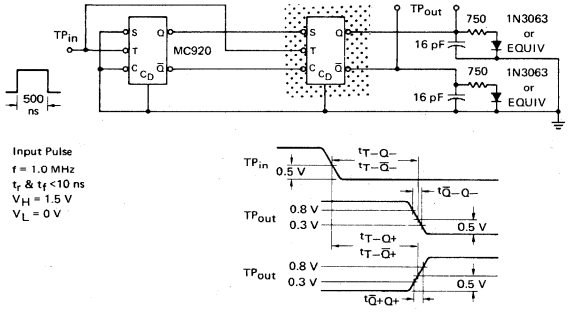
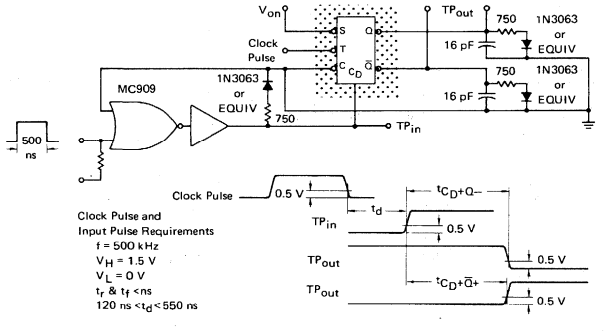


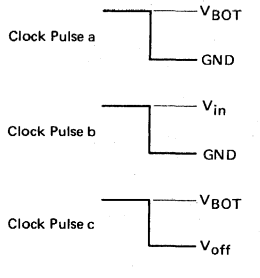
FIGURE 3B



SWITCHING TIMES

Test	Fig. No.	ns @ +25°C min	ns @ +25°C max
t_{T-Q-}	3A	40	140
t_{T-Q+}	3A	70	195
$t_{T-\overline{Q}-}$	3A	40	140
$t_{T-\overline{Q}+}$	3A	70	195
$t_{\overline{Q}+Q+}$	3A	30	100
$t_{\overline{Q}-Q-}$	3A	5	40
t_{C_D+Q-}	3B	55	--
$t_{C_D+\overline{Q}+}$	3B	5	--

FIGURE 4 - CORRELATION OF CLOCK PULSE a, b, & c

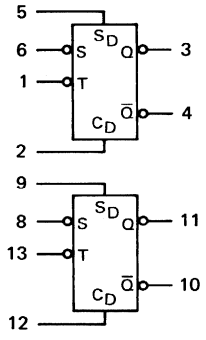


The negative transition of Clock Pulse a must precede the negative transition of Clock Pulse b.

MC978 • MC878

Available in TO-86 Flat Package, Add F Suffix.

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



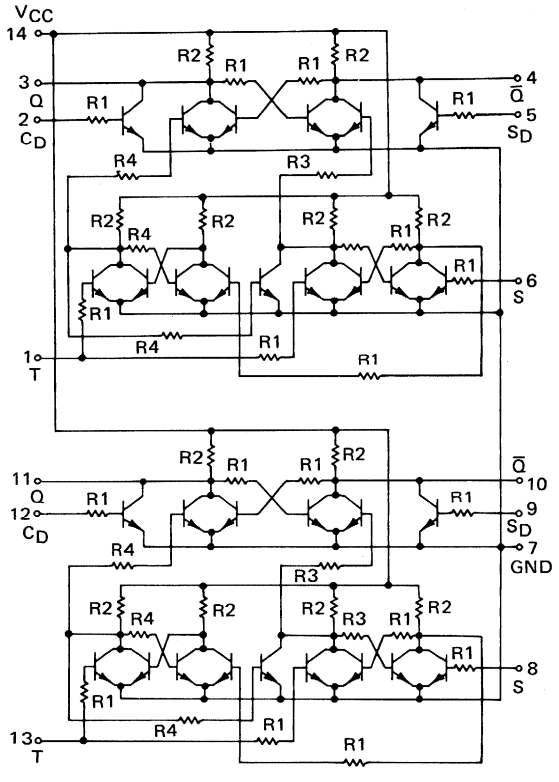
DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	④	④
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ④

t_n ①	t_{n+1} ①	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_C = C_C = 0$. The output state cannot be predetermined in the case when the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k
R3 = 180
R4 = 480

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

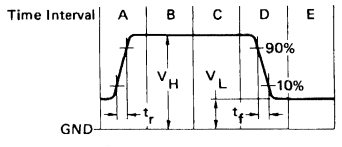
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC978	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC878	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC978 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC878 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Grd
Input Current	$1.8\ I_{in}$	1	-	225	-	234	-	198	μAdc	-	270	-	252	-	252	μAdc	1	-	6	-	14	-	2, 5, 7
	$1.8\ I_{in}$	1	-	225	-	234	-	198		-	270	-	252	-	252		1	-	-	-		-	2, 5, 6, 7
	I_{in}	2#	-	125	-	130	-	110		-	150	-	140	-	140		2	-	-	-		-	5, 6, 7
		5#	-		-		-			-		-		-			5	-	6	-		-	2, 7
		6#	-		-		-			-		-		-			6	-	-	-		-	2, 5, 7
Output Current	I_{A3}	3	350	-	364		308	-	μAdc	420	-	430	-	395	-	μAdc	3	1	5	2	14	-	6, 7
		3#		-		-		-					-		-		3	6	5	2		-	7
		4		-		-		-			-		-		-		4	1	2, 6	5		-	
		4#		-		-		-			-		-		-		4	-	2	5, 6		-	
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	1, 5	-	14	-	6, 7
		3	-		-		-			-		-		-			-	4	1	-		-	2, 5, 6, 7
		4	-		-		-			-		-		-			-	5	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			-	3	1	-		-	2, 5, 6, 7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	450	-	400	-	350	mVdc	2	-	1, 5	-	14	-	6, 7
		3	-		-		-			-		-		-			4	-	1	-		-	2, 5, 6, 7
		3*	-		-		-			-		-		-			-	-	1	5		-	6, 7
		3§†	-		-		-			-		-		-			-	-	-	6		-	2, 7
		3#‡	-		-		-			-		-		-			-		5	-		-	2, 7
		4	-		-		-			-		-		-			5	-	1, 2	-		-	6, 7
		4	-		-		-			-		-		-			3	-	1	-		-	2, 5, 6, 7
		4†	-		-		-			-		-		-			-	-	1	2		-	6, 7
		4§*	-		-		-			-		-		-			-	6	-	-		-	5, 7
		4#**	-		-		-			-		-		-			-	-	2	-		-	5, 7
Current Leakage	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	1, 2, 5, 6, 7

\# = Pin 1 Clock Pulse a
§ = Pin 1 Clock Pulse b
* = Pin 2 Data Pulse a
** = Pin 6 Data Pulse a
† = Pin 5 Data Pulse a
‡ = Pin 6 Data Pulse b
See Figure 4

Ground inputs of flip-flop not under test. Other pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\,\mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

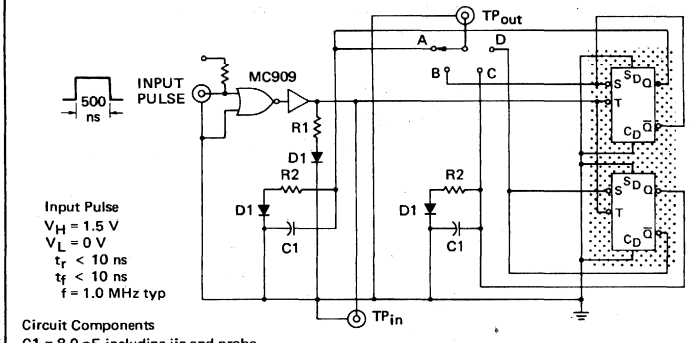
MC878

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760±2.0mVdc

MC978

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800 ±2.0 mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0 mVdc
+125°C	+260 ± 2.0 mVdc	+0.605 ±2.0 mVdc

FIGURE 2 - SWITCHING TIMES TEST AND WAVEFORMS



Input Pulse
V_H = 1.5 V
V_L = 0 V
t_r < 10 ns
t_f < 10 ns
f = 1.0 MHz typ

Circuit Components
C1 = 8.0 pF including jig and probe
R1 = 220 ohms ± 1.0%
R2 = 1.5 k ohms ± 1.0%
D1 = 1N3063 or equivalent

SWITCHING TIMES

TEST	SWITCH	MAXIMUM (ns @ 25°C)
t_{T-Q+}	A	120
t_{T-Q-}	A	80
$t_{T-\bar{Q}+}$	B	120
$t_{T-\bar{Q}-}$	B	80
$t_{T-\bar{Q}+}$	D	120
$t_{T-\bar{Q}-}$	D	80
t_{T-Q+}	C	120
t_{T-Q-}	C	80

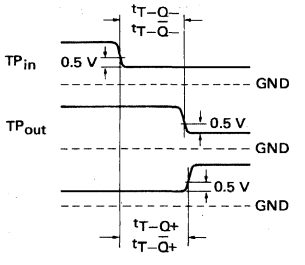
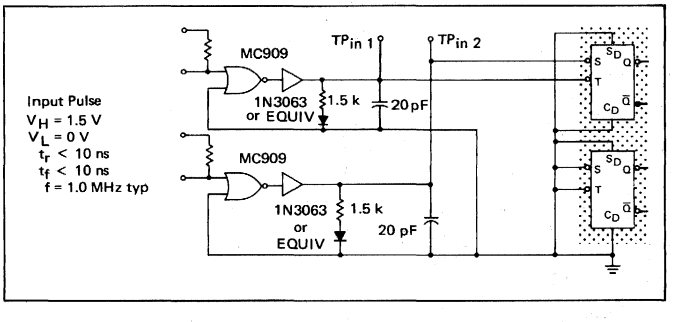


FIGURE 3A - SET UP AND RELEASE TIMES TEST CIRCUIT



Input Pulse
V_H = 1.5 V
V_L = 0 V
t_r < 10 ns
t_f < 10 ns
f = 1.0 MHz typ

FIGURE 3B - INPUT PULSE WIDTHS FOR SET UP AND RELEASE TIMES

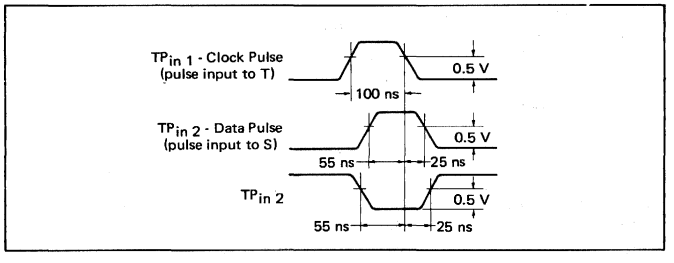
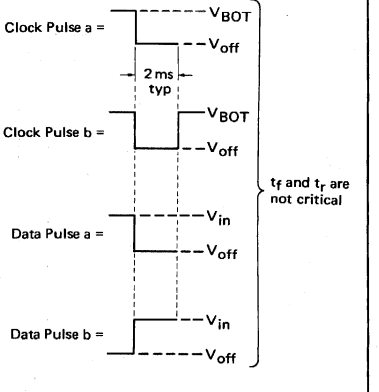


FIGURE 4 - CORRELATION OF CLOCK PULSE a & b AND DATA PULSE a & b

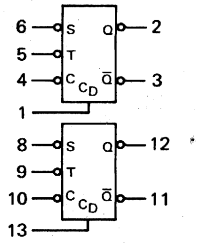


When applicable, the negative transition of Clock Pulse a must precede the transition of Data Pulse a and Data Pulse b. The negative and positive transitions of Clock Pulse b must follow the negative transition of Data Pulse a.

MC976 • MC876

Available in TO-86 Flat Package, Add F Suffix.

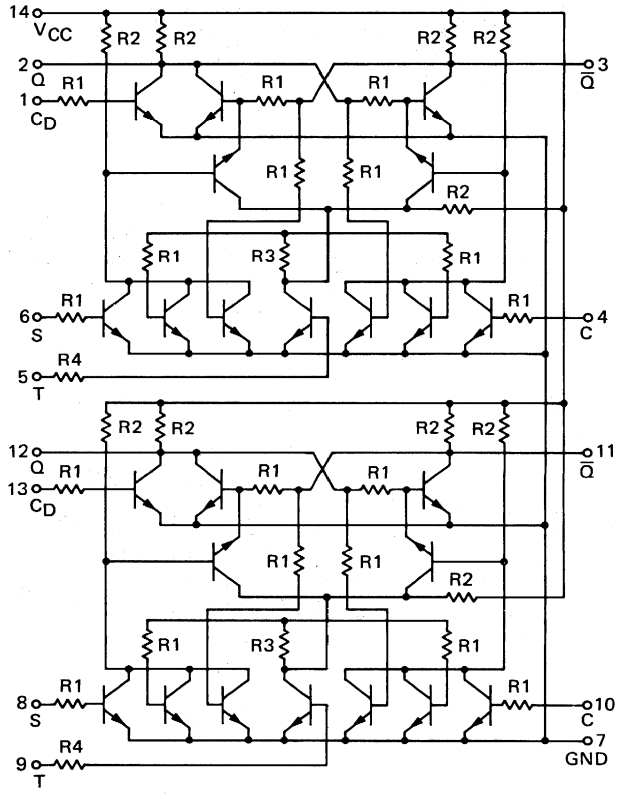
Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



CLOCKED INPUT OPERATION①

t_n ③		t_{n+1} ③	
S	C	Q	$\bar{Q}$
1	1	Q_n ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ⑥

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.



Typical Resistance Values

R1 = 1.5 k R3 = 3.0 k

R2 = 3.6 k R4 = 750

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one flip-flop only.
The other flip-flop is tested in the same manner.

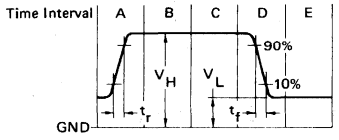
	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC976	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC876	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

Characteristic	Symbol	Pin Under Test	MC976 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC876 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	3	-	14	-	7
	I_{in}	4	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	4	-	2	-	↓	-	↓
	$2\ I_{in}$	5	-	250	-	260	-	220	↓	-	300	-	280	-	280	↓	5	-	4, 6	-	↓	-	↓
	I_{in}	6	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	6	-	3	-	↓	-	↓
Output Current	I_{A2}	2*	270	-	280	-	240	-	μAdc	320	-	320	-	300	-	μAdc	-	2	4	1	14	-	7
		3	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	1, 6	-	↓	-	↓
		3		-		-		-			-		-		-		-	1, 3	6	-		-	
Output Voltage	V_{out}	2	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	-	3, 7
		2**	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	7
		2*#	-		-		-			-		-		-			-	4, 6	-	-		-	1, 7
		2*#	-		-		-			-		-		-			-	4	-	6		-	↓
		2*#	-		-		-			-		-		-			-	-	-	4, 6		-	
		3*	-		-		-			-		-		-			-	2	-	-		-	7
		3*#	-		-		-			-		-		-			-	4, 6	-	-		-	1, 7
		3**#	-		-		-			-		-		-			-	6	-	4		-	
		3**#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	4, 6	↓	-	↓
Saturation Voltage	$V_{CE(sat)}$	2	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	1	-	14	-	3, 7
		2**	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	-	7
		3*	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1	↓	-	7
Current Leakage	I_L	14	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	14	1,4,5,6,7

= Clock Pulse to Pin 5, see Figure 1.
* = Pin 3 Low
** = Pin 2 Low
Set by a momentary ground prior to the application of the negative-going clock pulse.

Ground inputs of flip-flop not under test. Other pins not listed are left open.

FIGURE 1 - CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be < 1.0 µs
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground, when applicable.
D. Clock pulse is allowed to fall to V_L. t_f remains within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

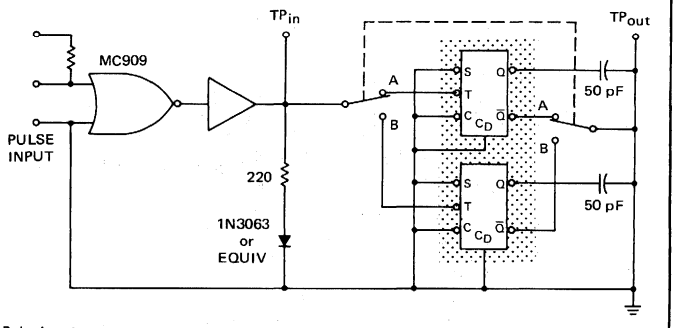
MC876

T_A	V_L	V_H
+25°C	+460 ± 2.0 mVdc	+0.850 ±2.0mVdc
0°C	+500 ± 2.0 mVdc	+0.900 ±2.0mVdc
+75°C	+400 ± 2.0 mVdc	+0.760 ±2.0mVdc

MC976

T_A	V_L	V_H
+25°C	+450 ± 2.0 mVdc	+0.800 ±2.0mVdc
−55°C	+650 ± 2.0 mVdc	+0.985 ±2.0mVdc
+125°C	+260 ± 2.0 mVdc	+0.605 ±2.0mVdc

FIGURE 2 - TOGGLE MODE TEST CIRCUIT



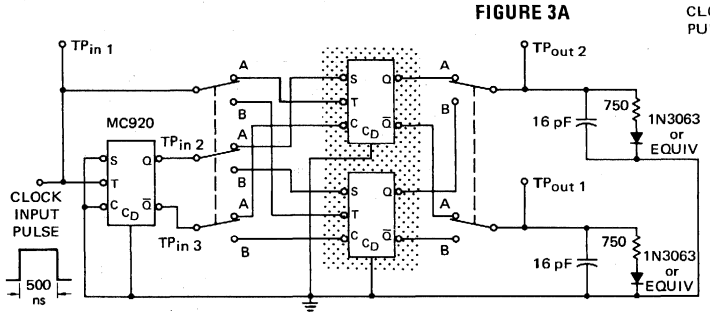
Pulse Input
f = 3.0 MHz
Duty Cycle = 35% to 65%

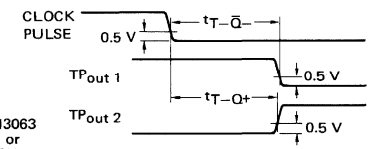
t_r & t_f < 10 ns
V_H = 1.0 V
V_L = 0 V

The circuit should toggle with an output pulse frequency of 1.5 MHz when the duty cycle varies between 35% and 65%.

SWITCHING TIMES TEST CIRCUITS AND WAVEFORMS

FIGURE 3A



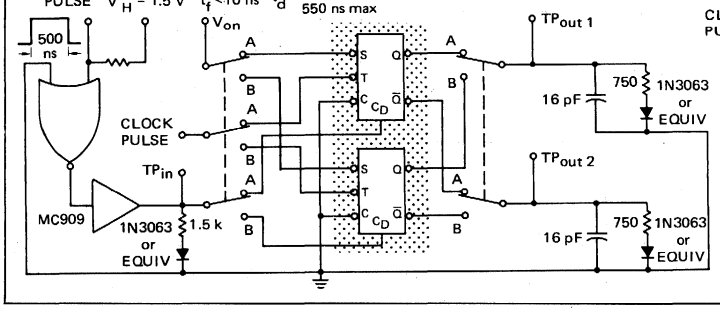


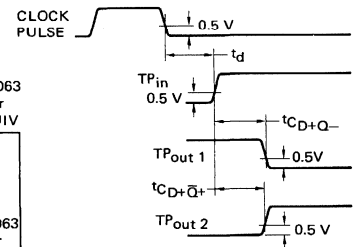
Clock Input Pulse
f = 1.0 MHz
V_H = 1.5 Vdc
V_L = 0 Vdc
t_r < 10 ns
t_f < 10 ns

SWITCHING TIMES	
TEST	MAXIMUM (ns @+25°C)
$t_{T-\overline{Q}-}$	85
t_{T-Q+}	125
t_{CD+Q-}	65
$t_{CD+\overline{Q}+}$	125

FIGURE 3B

INPUT PULSE V_L = 0 V, V_H = 1.5 V
t_r < 10 ns, t_f < 10 ns
f = 500 kHz typ
t_d = 120 ns min, 550 ns max

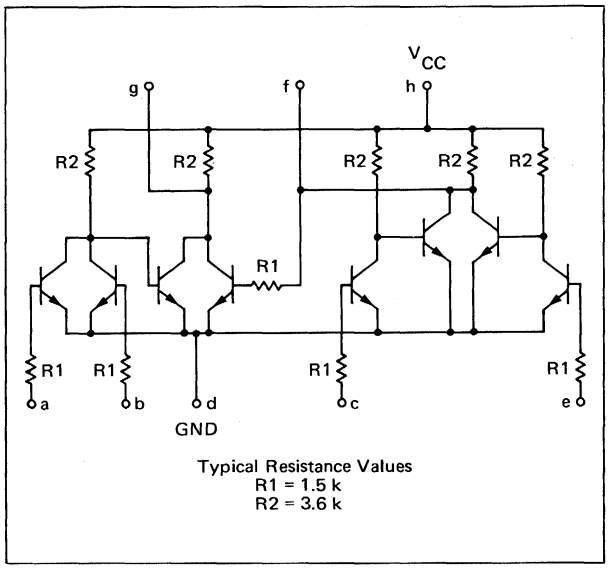




Negative clock pulse transition may cause $\overline{Q}$ to go low for as long as 100 ns.

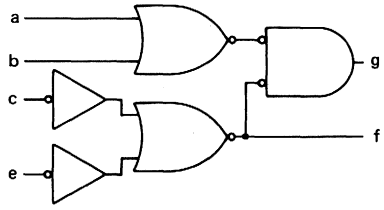
MC908 • MC808

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

The MC908/MC808 is an RTL half-adder. The binary half-adder function can be performed by connecting pin a to pin c and pin b to pin e. The "SUM" is available on pin g while the "CARRY" is available on pin f. The device is also used as a data selector by connecting pin a to pin c and using pins b and e as data inputs. A full adder can be devised by utilizing two MC908/MC808s and one MC911/MC811.

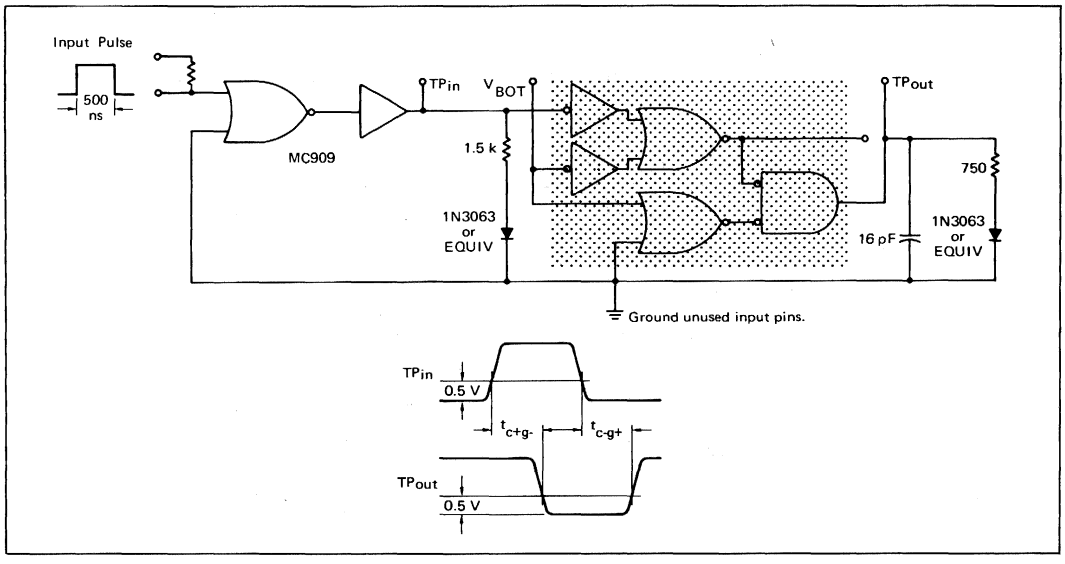


$g = (a + b)(\bar{c} + \bar{e})$

$f = \overline{\bar{c} + \bar{e}}$

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC908	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC808	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

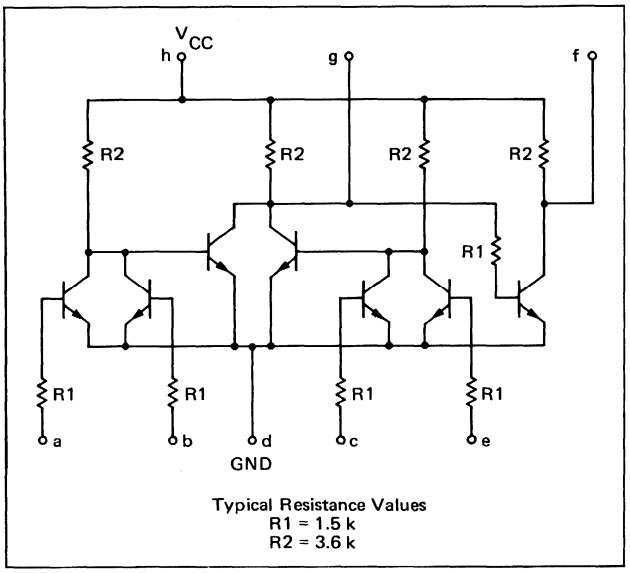
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC908 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC808 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	-	c, d, e
		b	-	125	-	130	-	110	↓	-	150	-	140	-	140	↓	b	-	a	-	↓	-	c, d, e
	0.8 I_{in}	c	-	100	-	104	-	88	↓	-	120	-	112	-	112	↓	c	-	-	-	↓	-	a, b, d, e
		e	-	100	-	104	-	88	↓	-	120	-	112	-	112	↓	e	-	-	-	↓		a, b, c, d
Output Current	I_{A3}	f	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	f	c, e	-	-	h	-	a, b, d
	I_{A4}	g	475	-	494	-	418	-	↓	570	-	570	-	535	-	↓	g	a	-	c, e	↓	-	b, d
		g	475	-	494	-	418	-	↓	570	-	570	-	535	-	↓	g	b	-	c, e	↓	-	a, d
Output Voltage	V_{out}	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	f	a, b, c, e	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	-	-	c	e	h	-	a, b, d
		f	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	e	c	↓	-	a, b, d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	a, b	↓	-	c, d, e
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	f	-	a, b, c, e	-	↓	-	d
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, e
																	Pulse In	Pulse Out					
Switching Time	t	c-g+	-	-	-	80	-	-	ns	-	-	-	80	-	-	ns	c	g	b, e	-	h	-	a, d
		c+g-	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	c	g	b, e	-	h	-	a, d

Input pins not listed are left open.

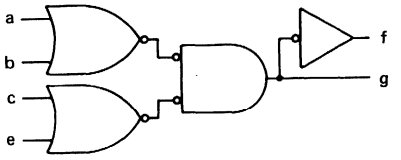
MC912 • MC812

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.



Typical Resistance Values
R1 = 1.5 k
R2 = 3.6 k

The MC912/MC812 is an RTL Half-Adder. By applying the complement of pins a and b to pins c and e, the "SUM" and "NOT SUM" functions of a binary half-adder are produced on pin g and f respectively.

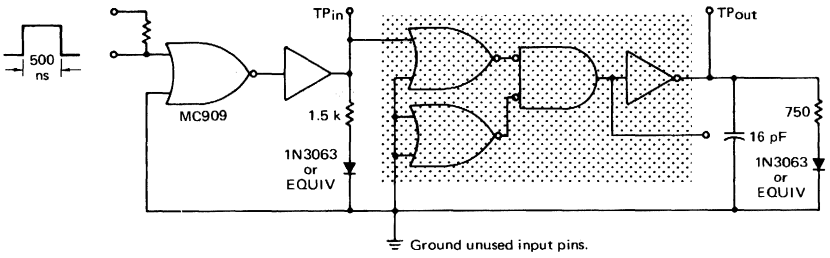


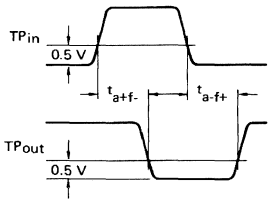
$f = \overline{a} \cdot \overline{b} + \overline{c} \cdot \overline{e}$

$g = (a + b)(c + e)$

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





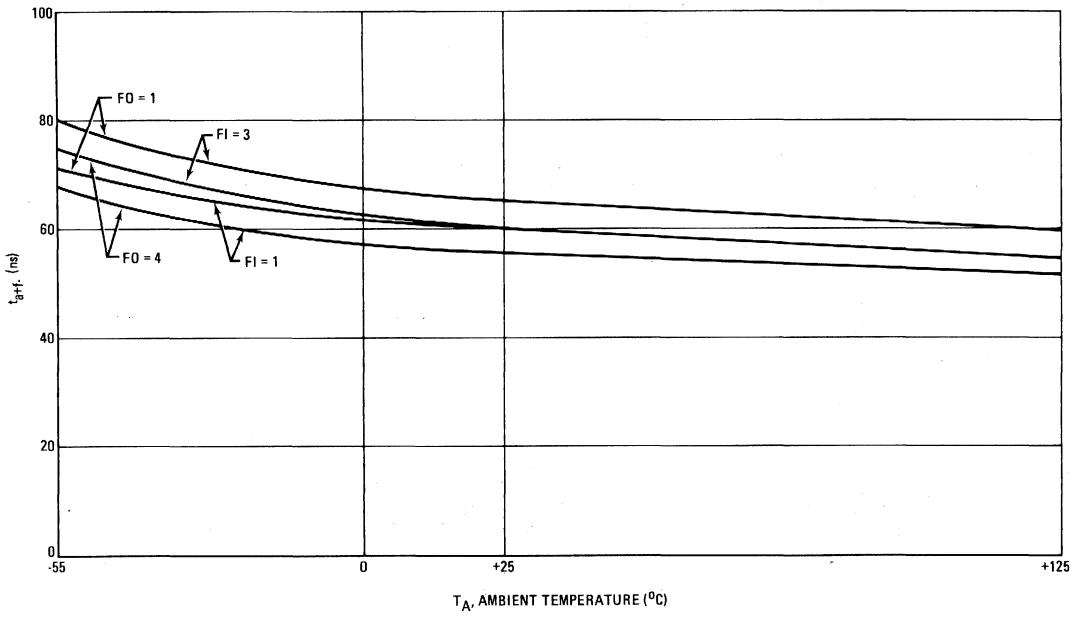
@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}
MC912	−55°C	0.970	0.935	1.80	0.650	3.00	0.500
	+25°C	0.805	0.750	1.80	0.450	3.00	0.400
	+125°C	0.590	0.555	1.80	0.260	3.00	0.300
MC812	0°C	0.880	0.850	1.80	0.500	3.60	0.450
	+25°C	0.830	0.800	1.80	0.460	3.60	0.400
	+75°C	0.740	0.710	1.80	0.400	3.60	0.350

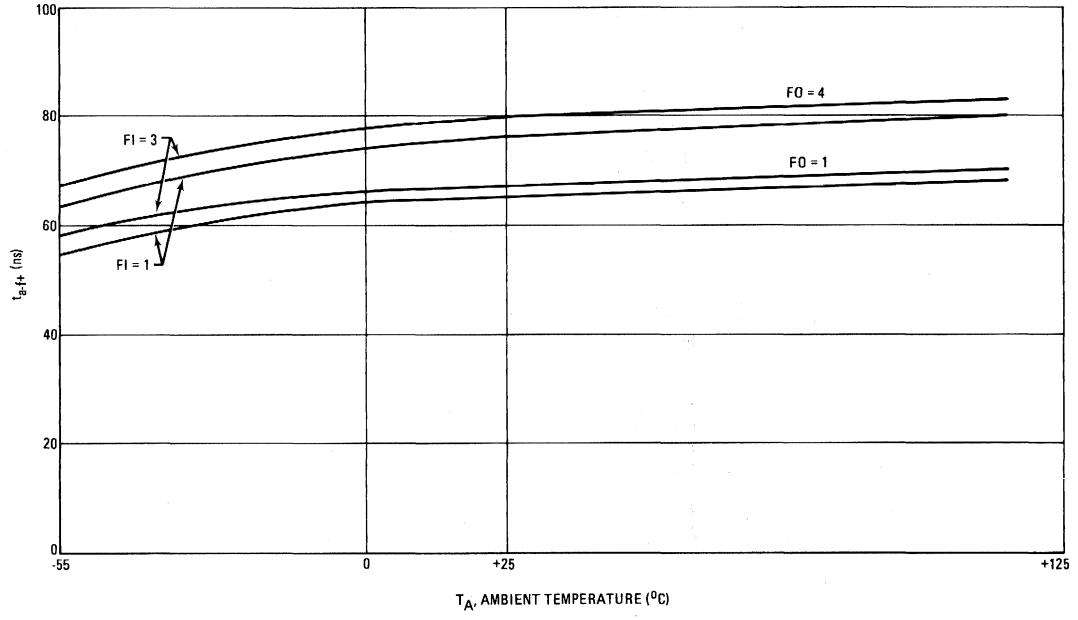
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC912 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC812 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	-	c, d, e
		b	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	b	-	a	-	↓	-	c, d, e
		c	-		-		-			-		-		-			c	-	e	-		-	a, b, d
		e	-		-		-			-		-		-			e	-	c	-		-	a, b, d
Output Current	I_{A3}	g	350	-	364	-	308	-	μAdc	420	-	430	-	395	-	μAdc	g	a, c	-	-	h	-	b, d, e
	I_{A3}	g	350	-	364	-	308	-	↓	420	-	430	-	395	-	↓	g	b, e	-	-	↓	-	a, c, d
	I_{A4}	f	475	-	494	-	418	-		570	-	570	-	535	-		f	-	-	-		-	a, b, c, d, e
Output Voltage	V_{out}	f	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	g	a, b, c, e	-	h	-	d
Saturation Voltage	$V_{CE(sat)}$	f	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	g	-	a, b, c, e	-	h	-	d
		g	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	c, e	a, b	↓	-	
		g	-		-		-			-		-		-			-	-	a, b	c, e		-	↓
Isolation Leakage Current	I_L	h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	-	h	a, b, c, d, e
																	Pulse In	Pulse Out					
Switching Time	t	a+f-	-	-	-	100	-	-	ns	-	-	-	100	-	-	ns	a	f	e	-	h	-	b, c, d
		a-f+	-	-	-	80	-	-	ns	-	-	-	80	-	-	ns	a	f	e	-	h	-	b, c, d

Input pins not listed are left open.

PROPAGATION DELAY versus TEMPERATURE

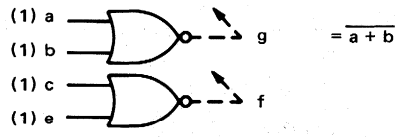




MC921 • MC821

Available in TO-99 Metal Can, Add G Suffix.
Available in TO-91 Flat Package, Add F Suffix.

This gate expander is designed to increase the fan-in capability of the gates in the mW MRTL line.



$= \overline{a + b}$

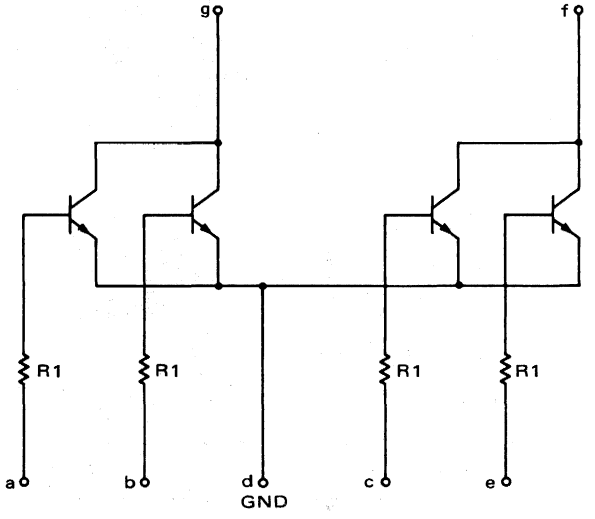
t_{pd} = 27 ns typ
P_D = 3.0 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NOTES ON USE OF THE MC921/MC821

1. The input loading factor of the expanded gate is 1.33.
2. Pin h of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.

PIN CONNECTIONS								
Schematic	a	b	c	d	e	f	g	h
G Package (TO-99)	1	2	3	4	5	6	7	8
F Package (TO-91)	1	2	4	5	6	7	9	10



Typical Resistance Value
R1 = 1.5 k

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one expander only.
Other expanders are tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k ohms) V_{RH}*	V_{RL}*
MC921	−55°C	0.970	0.935	1.80	0.650	3.00	4.27	2.8
	+25°C	0.805	0.750	1.80	0.450	3.00	4.3	2.7
	+125°C	0.590	0.555	1.80	0.260	3.00	5.0	3.0
MC821	0°C	0.880	0.850	1.80	0.500	3.60	4.3	2.7
	+25°C	0.830	0.800	1.80	0.460	3.60	4.3	2.7
	+75°C	0.740	0.710	1.80	0.400	3.60	4.7	2.8

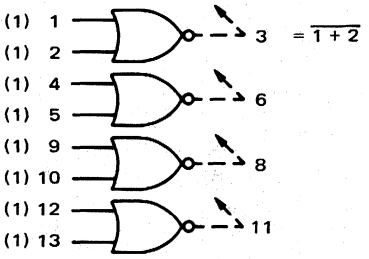
Characteristic	Symbol	Pin Under Test	MC921 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC821 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{RH}*	V_{RL}*	Gnd
Input Current	I_{in}	a	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	a	-	b	-	h	g	-	d
		b	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	b	-	a	-	h	g	-	d
Output Leakage Current	I_{CEX}	g	-	5.0	-	5.0	-	40	μAdc	-	20	-	20	-	20	μAdc	g	-	-	a, b	h	-	-	d
Output Voltage	$V_{CE(sat)}$	g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	a	-	-	h	-	g	b, d
		g	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	b	-	-	h	-	g	a, d
Saturation Voltage	$V_{CE(sat)}$	g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	a	-	-	-	h	-	g	b, d
		g	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	b	-	-	-	h	-	g	a, d
Isolation Leakage Current	I_L	g	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	g	-	-	a, b, d
		h	-	100	-	100	-	100	μAdc	-	100	-	100	-	100	μAdc	-	-	-	-	h	-	-	a, b, d

Ground input pins of expander not under test.
Other pins not listed are left open.
*Resistor value to V_{CC}.

MC9921 • MC9821

Available in TO-86 Flat Package, Add F Suffix.

This element consists of four 2-input expanders in a single package to increase the input capability of mW MRTL gates.

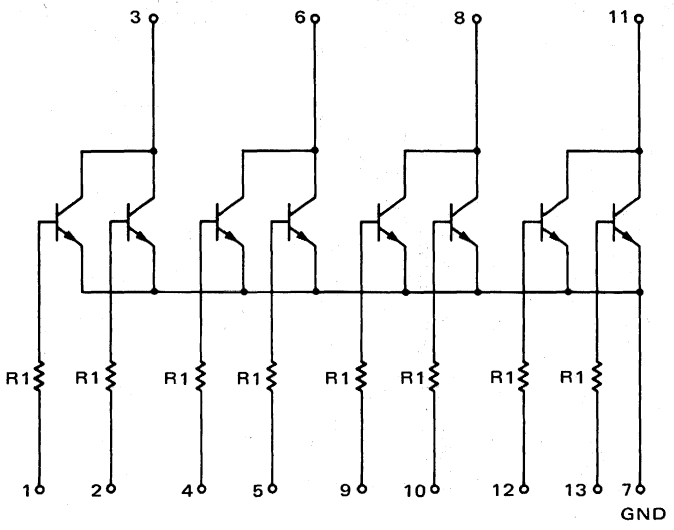


t_{pd} = 27 ns typ
P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES mW MRTL LOADING FACTOR

NOTES ON THE USE OF THE MC9921/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 14 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.



V_{CC} connection to pin 14 not shown
Typical Resistance Value
R1 = 1.5 k

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(kΩ) V_R*
MC9921	−55°C	0.970	0.935	1.80	0.650	3.00	3.6
	+25°C	0.805	0.750	1.80	0.450	3.00	3.6
	+125°C	0.590	0.555	1.80	0.260	3.00	4.0
MC9821	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	3.6

ELECTRICAL CHARACTERISTICS

Test procedures shown are for one expander only.
Other expanders are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC9921 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC9821 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	1	-	2	-	14	3	7
		2	-	125	-	130	-	110	μAdc	-	150	-	140	-	140	μAdc	2	-	1	-	14	3	7
Output Leakage Current	I_{CEX}	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	14	-	7
Output Voltage	V_{out}	3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	1	-	-	14	3	2,7
		3	-	620	-	300	-	230	mVdc	-	400	-	350	-	300	mVdc	-	2	-	-	14	3	1,7
Saturation Voltage	$V_{CE(sat)}$	3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	1	-	-	-	14	3	2,7
		3	-	220	-	220	-	220	mVdc	-	250	-	250	-	250	mVdc	2	-	-	-	14	3	1,7

Ground input pins of expanders not under test.
Other pins not listed are left open.
*Resistor value to V_{CC}.

PLASTIC
MRTL
INTEGRATED CIRCUITS
LOW-POWER
AND
MEDIUM-POWER
MC700P/MC800P SERIES

MILLIWATT AND MEDIUM-POWER
PLASTIC MRTL
INTEGRATED CIRCUITS

This series of MRTL logic circuits is packaged in the molded plastic package to provide exceptional economy. This group contains devices from both the medium-power and low-power groups; the medium-power devices have loading factors normalized for ease of mixing the two power levels in a system.

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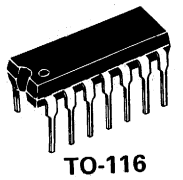
NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 3.6 V ± 10%, T_A = 25°C, Case 93

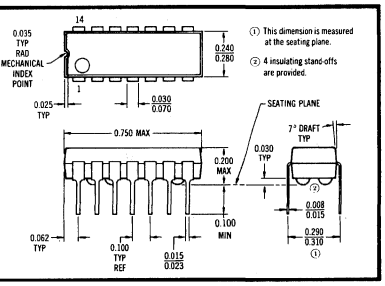
Function	Type		Output Loading Factor each output		Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg ①	Page No.
	+15 to +55°C	0 to +75°C	MC700 Series	MC800 Series			
MRTL							
Dual 3-Input NOR Gate	MC715P	MC815P	16	5	12	55/15	6-174
J-K Flip-Flop		MC816P	–	3	35	91/79 ②	6-202
J-K Flip-Flop	MC723P		10	–	35	91/79 ②	6-202
Quad 2-Input NOR Gate	MC724P	MC824P	16	5	12	100/30	6-180
Dual 4-Input NOR Gate	MC725P	MC825P	16	5	12	60/15	6-176
J-K Flip-Flop	MC726P	MC826P	16	5	35	100/86 ②	6-205
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Dual 4-Input Expander	MC786P	MC886P	–	–	12	20/–	6-213
1 J-K Flip-Flop, 1 Inverter, 2 Buffers	MC787P	MC887P	–	–	–	163/177 ③	6-224
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Dual J-K Flip-Flop	MC790P	MC890P	10	3	35	182/158 ②	6-208
Dual J-K Flip-Flop	MC791P	MC891P	16	5	40	190/160 ②	6-199
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Dual Full Adder	MC796P	MC896P	13	4	60	84	6-229
Dual Full Subtractor	MC797P	MC897P	13	4	60	84	6-232
Dual Buffer	MC799P	MC899P	80	25	20	50/100	6-186
Hex Expander	MC9719P	MC9819P	–	–	12	13/–	6-219
mW MRTL			All Series				
Quad 2-Input NOR Gate	MC717P	MC817P	4		27	20/5.0	6-172
Dual 3-Input NOR Gate	MC718P	MC818P	4		27	12/2.5	6-166
Dual 4-Input NOR Gate	MC719P	MC819P	4		27	13/2.5	6-168
J-K Flip-Flop	MC722P	MC822P	4		70	24/20 ②	6-196
Dual J-K Flip-Flop	MC776P	MC876P	2		50	41/29 ②	6-190
Dual Type D Flip-Flop	MC778P	MC878P	3		60	48/35 ④	6-193
Triple 3-Input NOR Gate	MC793P	MC893P	4		27	18/3.5	6-170
Dual 2-Input Buffer	MC798P	MC898P	30		57	14/46	6-184
Quad 2-Input Expander	MC9721P	MC9821P	–		27	20/–	6-217

① Inputs High/Inputs Low unless otherwise noted.
② Only Clock Input High/Inputs Low
③ Only Clock Input High on flip-flop, other element Inputs High/Inputs Low
④ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low

UNIBLOC* PLASTIC PACKAGE CASE 93 TO-116



TO-116



*TRADEMARK OF MOTOROLA INC.

MAXIMUM RATINGS $T_A = 25°C$

Rating	Symbol	Value	Unit
Input Voltage	—	±4.0	Vdc
Power Supply Voltage (Pulsed ≦ 1.0 s)	—	+12	Vdc
Operating Temperature Range MC700P Series MC800P Series	T_A	 +15 to +55 0 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

TEST CONDITION TOLERANCES $V_{BOT} = \pm10$ mV $V_{CC} = \pm10$ mV $V_{in} = \pm2$ mV $V_R = \pm1\%$ $V_{on} = \pm2$ mV $V_{off} = \pm2$ mV $V_{LL} = \pm2$ mV

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} — Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{in}.

I_{AB} — Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} — The maximum available current from the output of a Dual Gate.

I_{CEX} — Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} — Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

1.8 I_{in} — Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

2 I_{in} — Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L — Isolation leakage current.

I_o — Output load current.

V_{BOT} — A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} — Supply voltage.

$V_{CE(sat)}$ — Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} — Minimum high level voltage applied to the input of a device.

V_{LL} — A supply voltage low enough to allow flow of leakage currents only.

V_{off} — The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} — The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} — The maximum output voltage with V_{on} applied to the input.

V_R — Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

GENERAL RULES

- EXPANDER RULES:
  1. The MC785P/885P, MC786P/886P and MC9719P/9819P MRTL expanders can be used to expand medium-power MRTL output nodes only. The MC9721P/9821P expander can be used to expand mW MRTL output nodes only.
  2. mW MRTL and MC800 MRTL Series: When using the MC885P, MC886P, MC9819P or MC9721/9821 subtract 0.5 from the output loading factor of the expanded gate for each expander node that is connected; also increase the input loading factor of the expanded gate by a factor of 1.33.
  3. MC700 MRTL Series: When using the MC785P, MC786P or MC9719P subtract 2.0 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 3.75.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- When mixing MRTL and mWMRTL in the same system, the loading factors must be normalized in accordance with the input current of the units being driven.
- All unused inputs should be returned to ground.

LOW POWER mW MRTL DEVICES

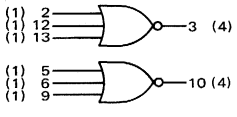
The logic diagrams shown describe the MC700P/MC800P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown on page 6-162. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

All elements in the MC700P/MC800P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

GATES

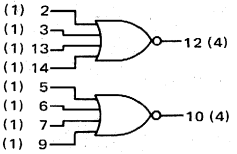
MC718P • MC818P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

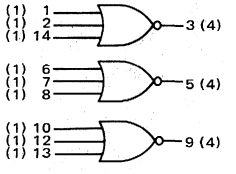
MC719P • MC819P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

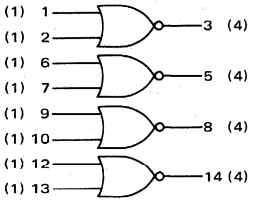
MC793P • MC893P
Triple 3-Input Gate



$3 = \overline{1 + 2 + 14}$

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

MC717P • MC817P
Quad 2-Input Gate

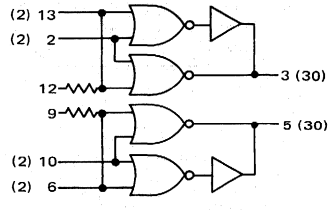


$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

BUFFERS

MC798P • MC898P
Dual 2-Input Buffer

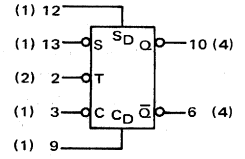


$3 = \overline{2 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

FLIP-FLOPS

MC722P • MC822P
J-K Flip-Flop



f_{Tog} = 1 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

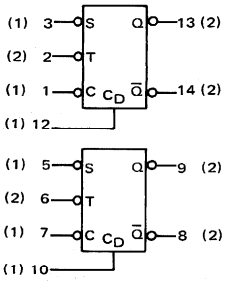
S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n ④		t_{n+1} ④	
S	C	Q	$\overline{Q}$
1	1	Q_n ⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n ⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC776P • MC876P
Dual J-K Flip-Flop



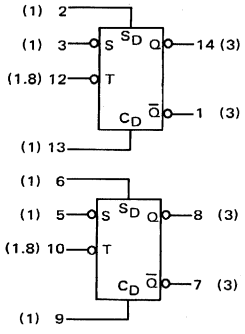
f_{Tog} = 3 MHz
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\overline{Q}$
1	1	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	-0	$\overline{Q}_n$	Q_n

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

MC778P • MC878P
Dual Type D Flip-Flop



f_{Tog} = 1 MHz
P_D = 48 mW (Direct Set (S_D) and Direct Clear (C_D) Low; all other Inputs High)
35 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

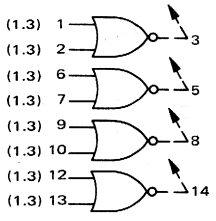
CLOCKED INPUT OPERATION ③

t_n ④	t_{n+1} ④	
S	Q	$\overline{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

EXPANDERS

MC9721P • MC9821P Quad 2-Input Expander



$3 = \overline{1 + 2}$

t_{pd} = 27 ns

P_D = 20 mW (Input High)
Negligible (Inputs Low)

MEDIUM-POWER MRTL DEVICES

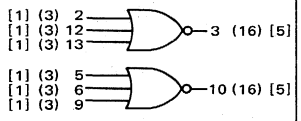
The logic diagrams shown describe the MC700P/MC800P Series of medium-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis or brackets indicates the input loading factor (if on the circuit input terminal) or load driving ability – fan-out – (if on the circuit output terminal). The bracketed number is the loading factor when working with other medium-power devices; e.g., [1] is the MRTL load factor defined as 1 times the MRTL basic gate input current (600 μAdc @ +25°C). The number in parenthesis is the loading factor when working with mW MRTL devices; e.g., (3) is the MRTL load factor defined as 3 times the mW MRTL basic gate input current (140 μAdc @ +25°C.

Using the parenthetic loading factors, these medium-power MRTL circuits are compatible with the low-power mW MRTL circuits shown on page 6-159. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C for the MC700P Series, and 0 to +75°C for the MC800P Series, with V_{CC} = 3.6 V ±10%.

All elements in the MC700P/800P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

GATES

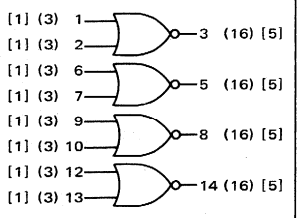
MC715P • MC815P
Dual 3-Input Gate



$3 = \overline{2 + 12 + 13}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

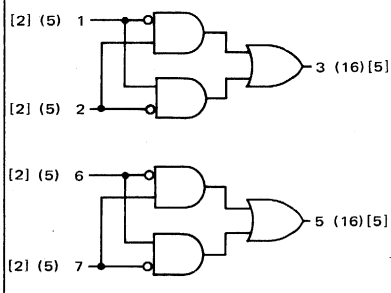
MC724P • MC824P
Quad 2-Input Gate



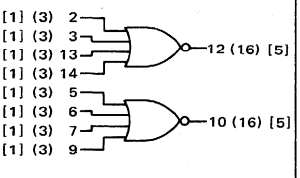
$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

MC771P • MC871P
Quad Exclusive "OR" Gate



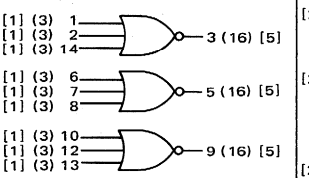
MC725P • MC825P
Dual 4-Input Gate



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

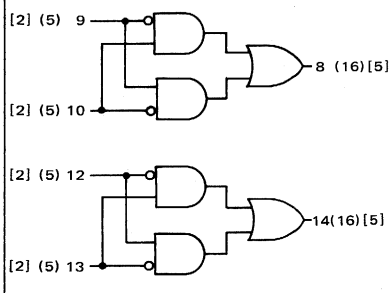
MC792P • MC892P
Triple 3-Input Gate



$3 = \overline{1 + 2 + 14}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

MC771P • MC871P
Quad Exclusive "OR" Gate

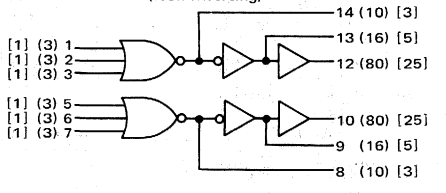


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

BUFFERS

MC788P • MC888P Dual 3-Input Buffer
(Non-Inverting)

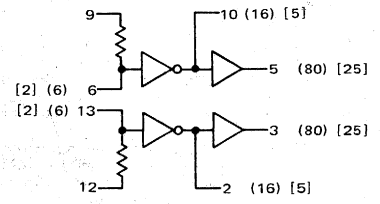


t_{pd} = 24 ns
P_D = 145 mW (Input High)
56 mW (Inputs Low)

$14 = \overline{1 + 2 + 3}$
$13 = 1 + 2 + 3$
$12 = 1 + 2 + 3$

Outputs 12, 13, or 14 may not be used simultaneously.
Outputs 8, 9, or 10 may not be used simultaneously.

MC799P • MC899P Dual Buffer



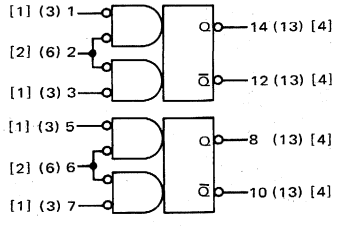
t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

$10 = \overline{6}$
$5 = \overline{6}$

Outputs 2 and 3 may not be used simultaneously.
Outputs 5 and 10 may not be used simultaneously.

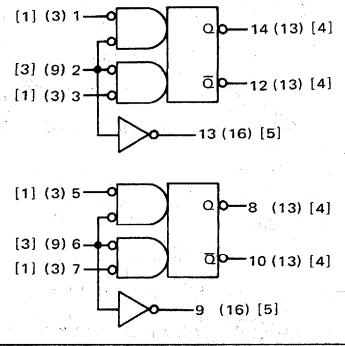
HALF-SHIFT REGISTERS

MC784P • MC884P
Dual Half-Shift Register
(Without Inverter)



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 100 mW

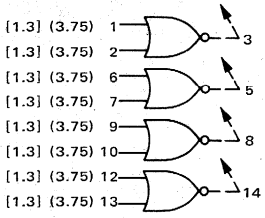
MC783P • MC883P
Half-Shift Register



$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$
t_{pd} = 22 ns
P_D = 140 mW

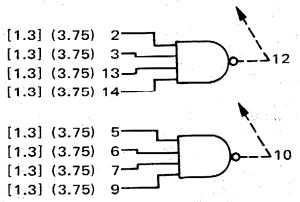
EXPANDERS

MC785P • MC885P
Quad 2-Input Expander



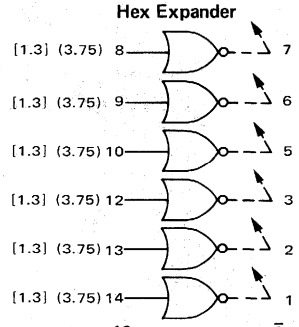
$3 = \overline{1 + 2}$
t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC786P • MC886P
Dual 4-Input Expander



$12 = \overline{2 + 3 + 13 + 14}$
t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC9719P • MC9819P
Hex Expander



t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

$7 = \overline{8}$

FLIP-FLOPS

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\overline{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

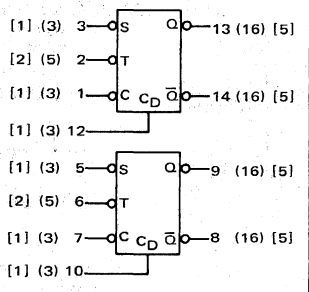
CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\overline{Q}$
1	1	Q_n⑤	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n⑤

J-K FLIP-FLOP TRUTH TABLES

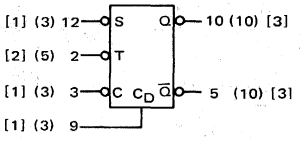
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \overline{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.
6. Clock pulse fall time must be < 100 ns.

MC791P • MC891P
Dual J-K Flip-Flop



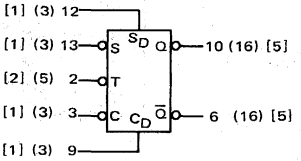
f_{Tog} = 4 MHz
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC723P • MC816P
J-K Flip-Flop



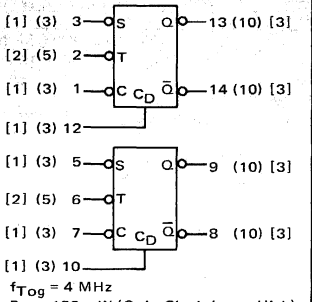
f_{Tog} = 4 MHz
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726P • MC826P
J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

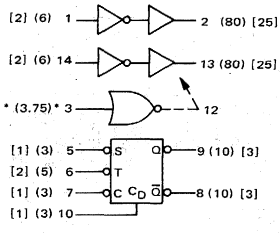
MC790P • MC890P
Dual J-K Flip-Flop



f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MULTIFUNCTION DEVICES

MC779P • MC879P
Multifunction
(1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)

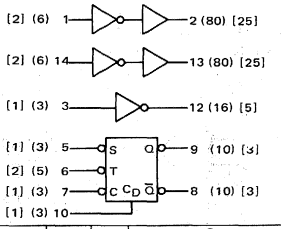


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	2.5	Negligible

‡Only Clock Input High

*Input loading factor is 3 for mW MRTL, or 1 for MRTL, if pin 12 is tied to pin 8 or 9 on the same package.

MC787P • MC887P
Multifunction
(1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)

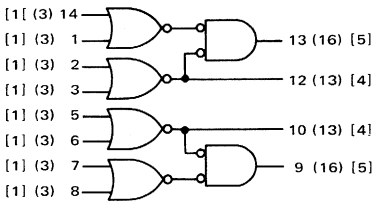


	f_{Tog} MHz	t_{pd} ns	P_D mW (Input High)	P_D mW (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

HALF ADDERS

MC775P • MC875P
Dual Half Adder



$13 = (14 + 1)(2 + 3)$

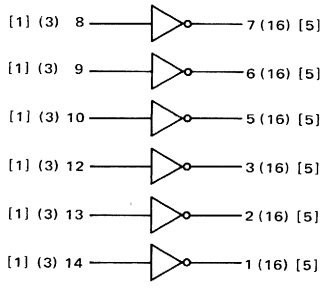
$12 = \overline{2 + 3}$

t_{pd} = 20 ns

P_D = 120 mW typ

INVERTER

MC789P • MC889P
Hex Inverter

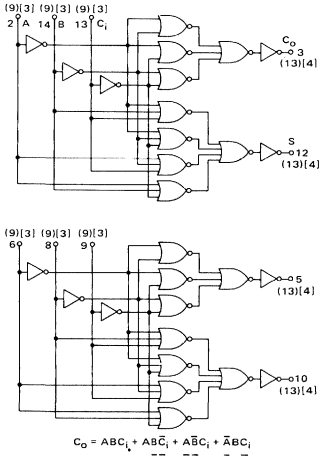


t_{pd} = 12 ns $\quad 1 = \overline{14}$

P_D = 130 mW (Input High)
15 mW (Inputs Low)

FULL ADDER

MC796P • MC896P
Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

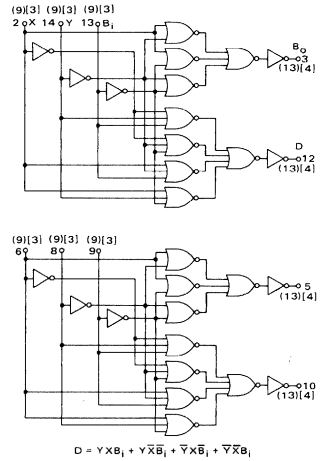
$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}\overline{B}C_i$

t_{pd} = 60 ns typical
P_D = 84 mW typical

TRUTH TABLE				
Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC797P • MC897P
Dual Full Subtractor



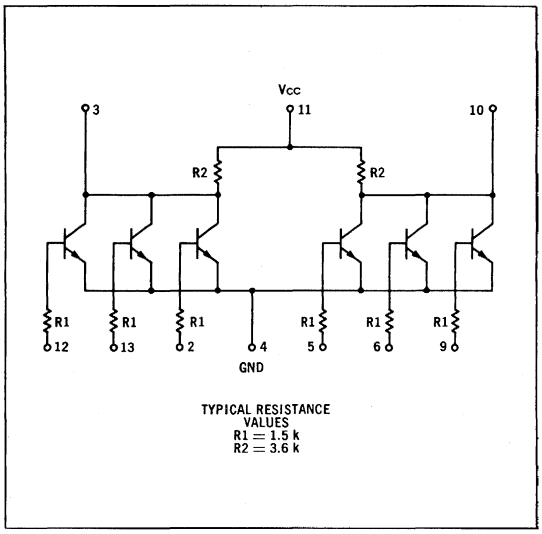
$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + YXB_i$

t_{pd} = 60 ns typical
P_D = 84 mW typical

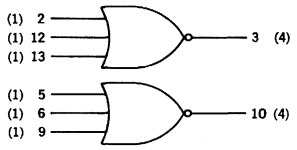
TRUTH TABLE				
Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

MC718P • MC818P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

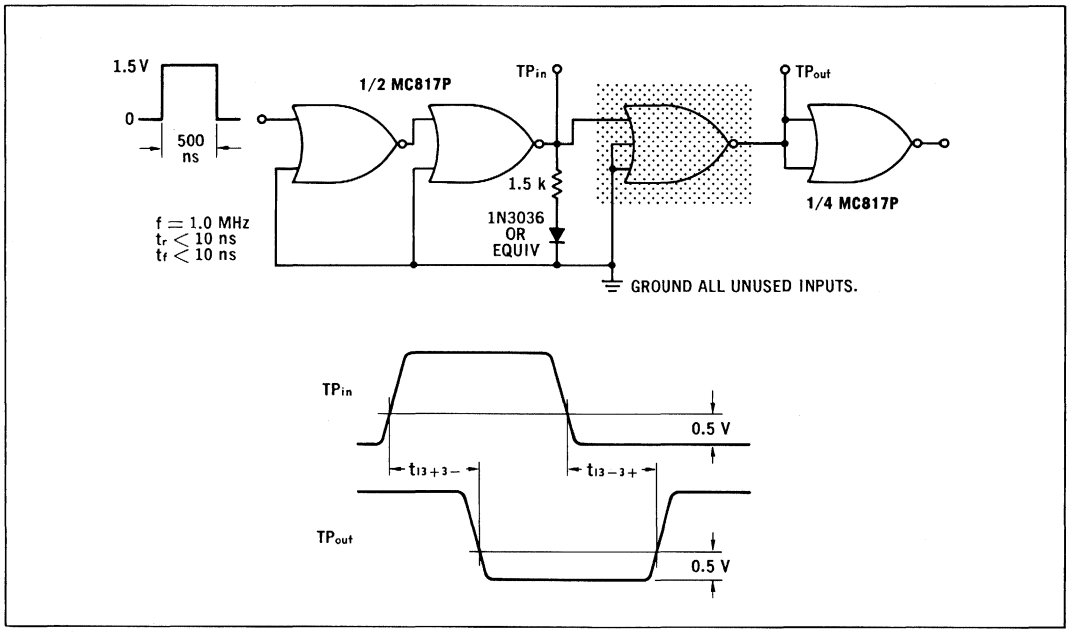


$3 = \overline{2 + 12 + 13}$

NUMBER IN PARENTHESIS INDICATES MC718P, MC818P LOADING FACTOR

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

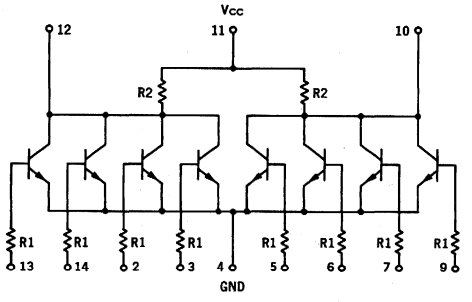
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC818P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC718P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC818P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC718P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-					13	-	2, 12	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	3	-	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,13
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3, 13	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

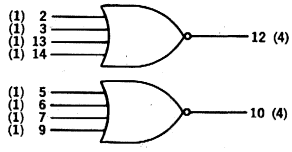
Ground unused input pins. Other pins not listed are left open.

MC719P • MC819P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.

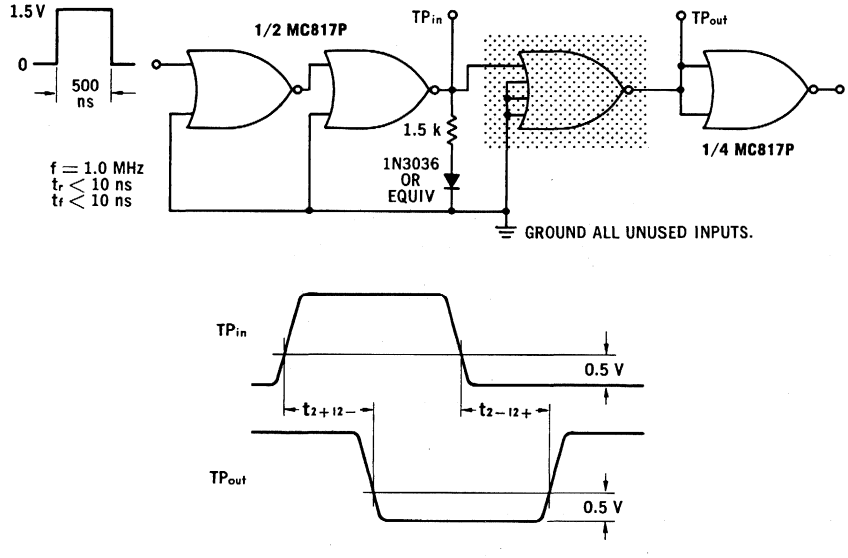


$12 = \overline{2 + 3 + 13 + 14}$

NUMBER IN PARENTHESIS INDICATES MC719P, MC819P LOADING FACTOR

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

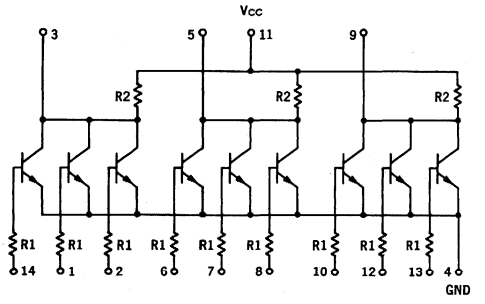
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC819P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC719P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2, 3, 14	-		
		14	-		-		-			-		-		-			14	-	2, 3, 13	-		
Output Current	I_{A4}	12	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	12	-	2,3,13, 14	11	4
Output Voltage	V_{out}	12	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-		3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	3,4,13,14

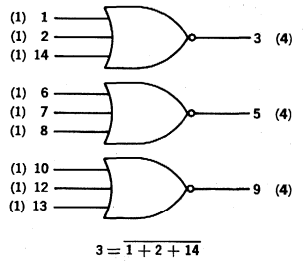
Ground inputs of gate not under test. Other pins not listed are left open.

MC793P • MC893P



TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

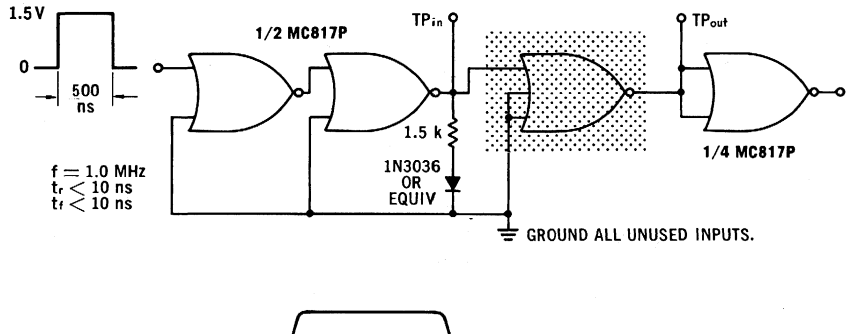


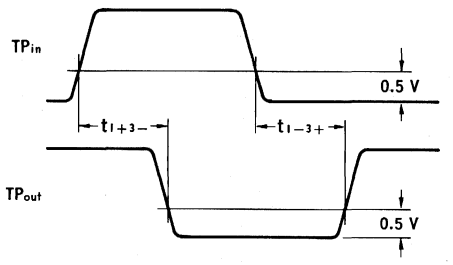
$3 = \overline{1 + 2 + 14}$

NUMBER IN PARENTHESIS INDICATES MC793P, MC893P LOADING FACTOR

t_{pd} = 27 ns
P_D = 18 mW (Input High)
3.5 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

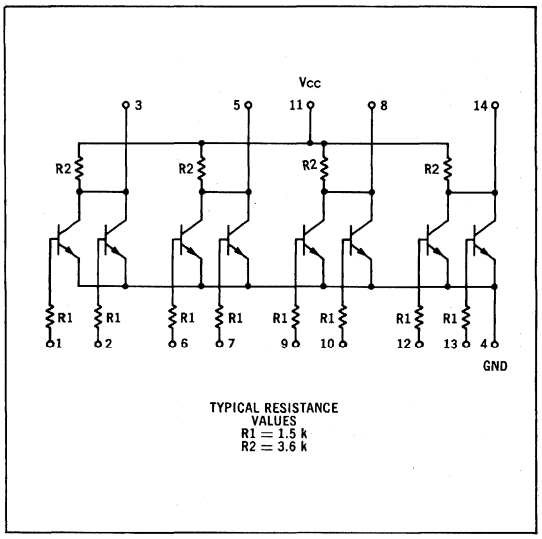
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC893P	0°C	0.880	0.850	1.80	0.500	3.60
MC893P	+25°C	0.830	0.800	1.80	0.460	3.60
MC893P	+75°C	0.740	0.710	1.80	0.400	3.60
MC793P	+15°C	0.865	0.865	1.80	0.475	3.60
MC793P	+25°C	0.850	0.850	1.80	0.460	3.60
MC793P	+55°C	0.800	0.800	1.80	0.430	3.60

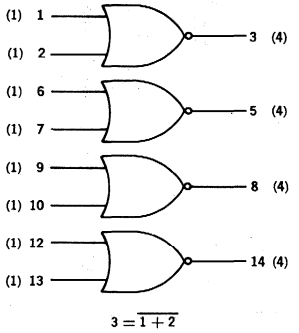
Characteristic	Symbol	Pin Under Test	MC893P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC793P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2,14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1,14	-	↓	↓
		14	-		-		-			-		-		-			14	-	1,2	-		
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2,14	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2,4,14
		3	-		-		-			-		-		-			-	2	-	-		1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-	↓	2,4,14
		3	-		-		-			-		-		-			-	-	2	-		1,4,14
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4,14

Ground input pins of gates not under test. Other pins not listed are left open.

MC717P • MC817P



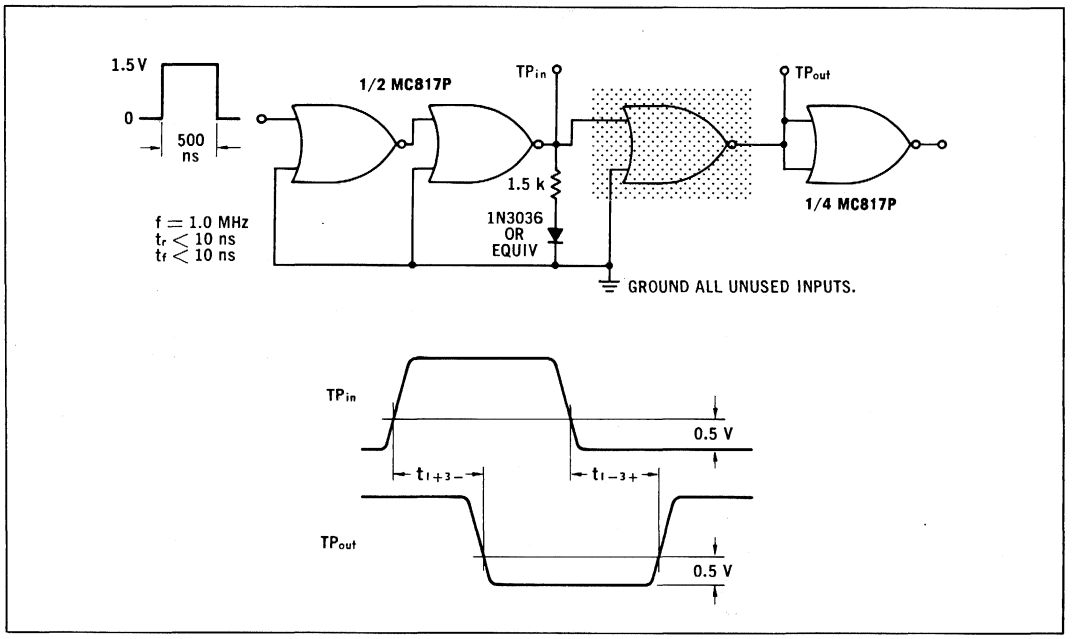
Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



NUMBER IN PARENTHESIS
INDICATES MC717P, MC817P LOADING FACTOR

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

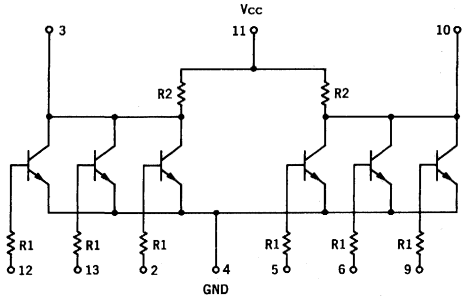
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC817P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC717P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC817P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC717P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	4
Output Current	I_{A4}	3	570	-	570	-	535	-	μAdc	570	-	570	-	570	-	μAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	90	-	-	ns	-	-	-	90	-	-	ns	Pulse In 1	Pulse Out 3	-	-	11	2,4

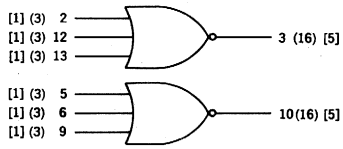
Ground input pins of gates not under test. Other pins not listed are left open.

MC715P • MC815P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



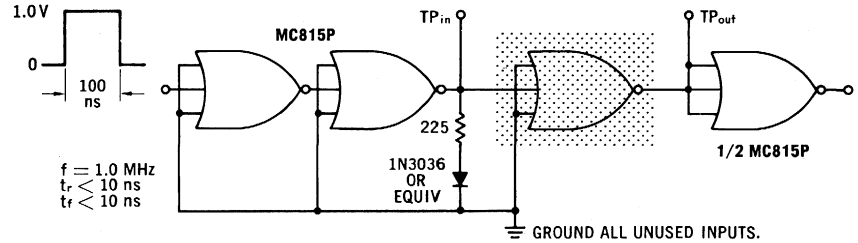
$3 = \overline{2 + 12 + 13}$

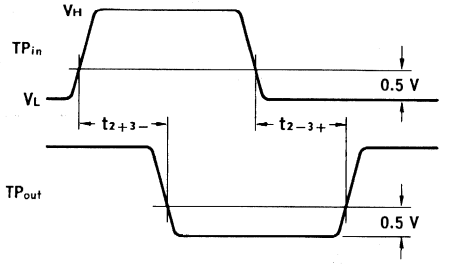
NUMBER IN PARENTHESIS INDICATES MC715P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC815P LOADING FACTOR

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

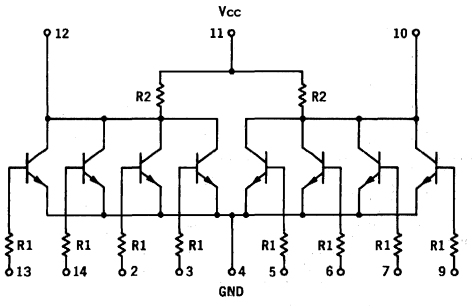
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC815P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC715P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC815P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC715P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	12, 13	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	12	-	2, 13	-	↓	↓
		13	-		-		-			-		-		-			13	-	2, 12	-		
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	2,12,13	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	2,4,12
		3	-		-		-			-		-		-			-	2	-	-		4,12,13
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	2,4,13
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	↓	2,4,12
		3	-		-		-			-		-		-			-	-	2	-		4,12,13
Switching Time	$t_{on} + t_{off}$	3,13	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	2,4,12

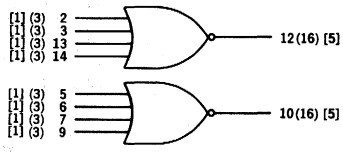
Ground input pins of gate not under test. Other pins not listed are left open. *Symbol is I_{A16} for MC715P.

MC725P • MC825P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Two 4-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



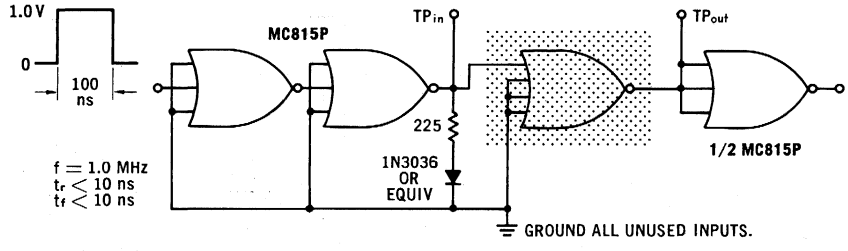
$12 = \overline{2 + 3 + 13 + 14}$

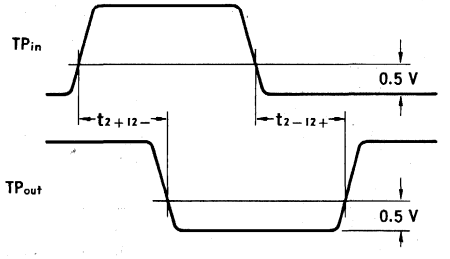
NUMBER IN PARENTHESIS INDICATES MC725P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC825P LOADING FACTOR

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

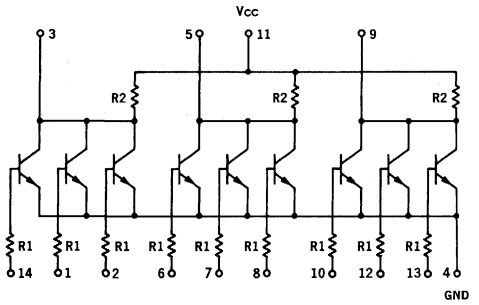
Test procedures are shown for one gate only.
The other gate is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC825P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC725P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC825P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC725P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-		
		14	-		-		-			-		-		-			14	-	2,3,13	-		
Output Current	I_{A5}*	12	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12	-	2,3,13,14	11	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-		2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-		3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-		2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-		3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-		2,4,13,14
Switching Time	$t_{on} + t_{off}$	2, 12	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 2	Pulse Out 12	-	-	11	3,4,13,14

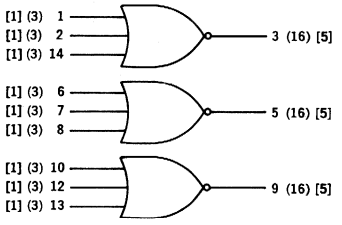
Ground input pins of gate not under test. Other pins not listed are left open. *Symbol is I_{A16} for MC725P.

MC792P • MC892P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Three 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.



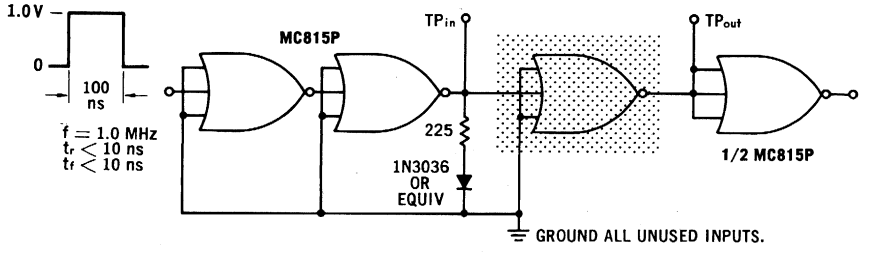
$3 = \overline{1 + 2 + 14}$

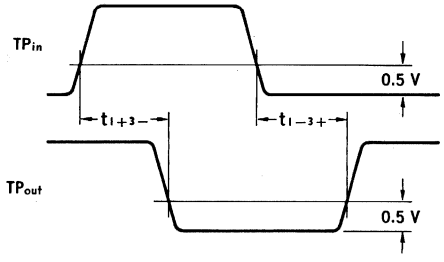
NUMBER IN PARENTHESIS INDICATES MC792P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC892P LOADING FACTOR.

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

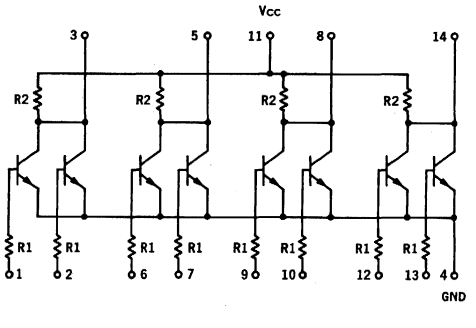
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC892P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC792P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC892P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC792P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2, 14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 14	-	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	14	-	1, 2	-	↓	↓
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1, 2, 14	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	-	↓	2,4,14
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	1,4,14
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1,2,4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1	-	↓	2,4,14
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	1,4,14
Switching Time	$t_{on} + t_{off}$	1, 3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4,14

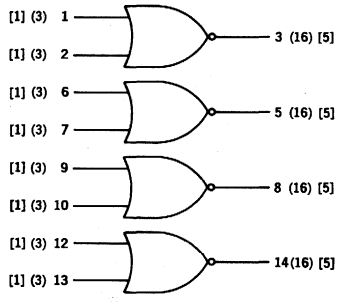
Ground input pins of gates not under test. Other pins not listed are left open. *I_{A16} is symbol for MC792P.

MC724P • MC824P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

Four 2-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-coupled to form bistable elements.

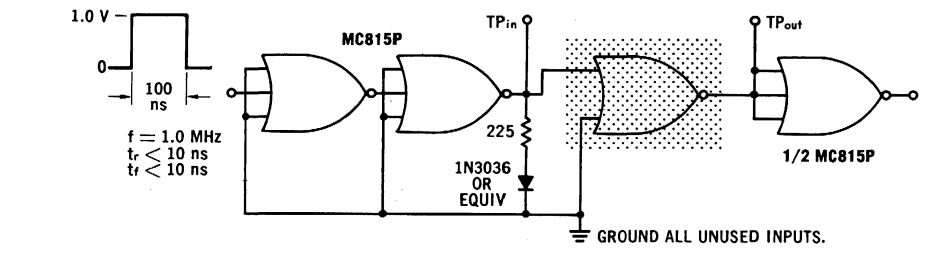


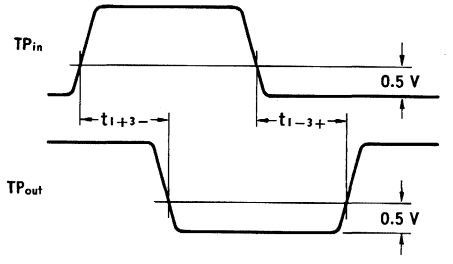
$3 = \overline{1 + 2}$

NUMBER IN PARENTHESIS INDICATES MC724P LOADING FACTOR
NUMBER IN BRACKETS INDICATES MC824P LOADING FACTOR

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only.
The other gates are tested in the same manner.

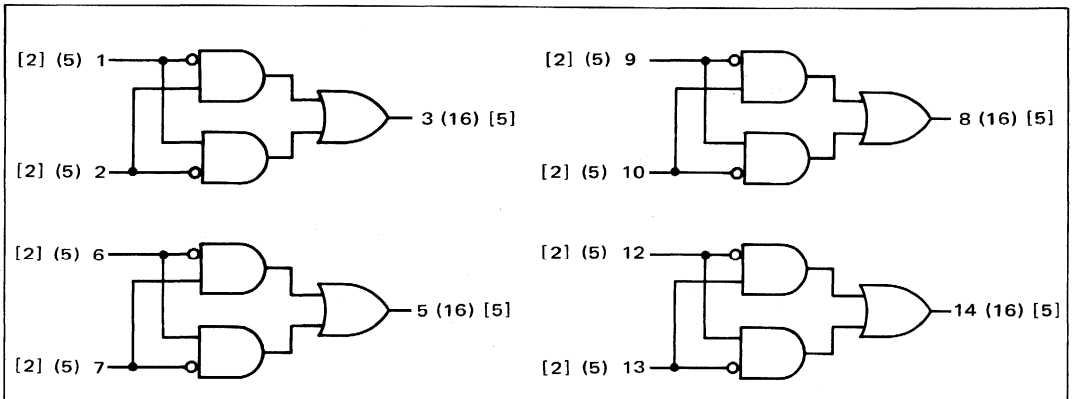
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC824P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC724P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC824P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC724P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
		2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	4
Output Current	I_{A5}*	3	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	3	-	1,2	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2,4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2,4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	1,4
Switching Time	$t_{on} + t_{off}$	1,3	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	11	2,4

Ground input pins of gates not under test. Other pins not listed are left open. *I_{A16} is symbol for MC724P.

MC771P · MC871P

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.



POSITIVE LOGIC

$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns typ

P_D = 87 mW typ

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC771P

NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC871P

ELECTRICAL CHARACTERISTICS

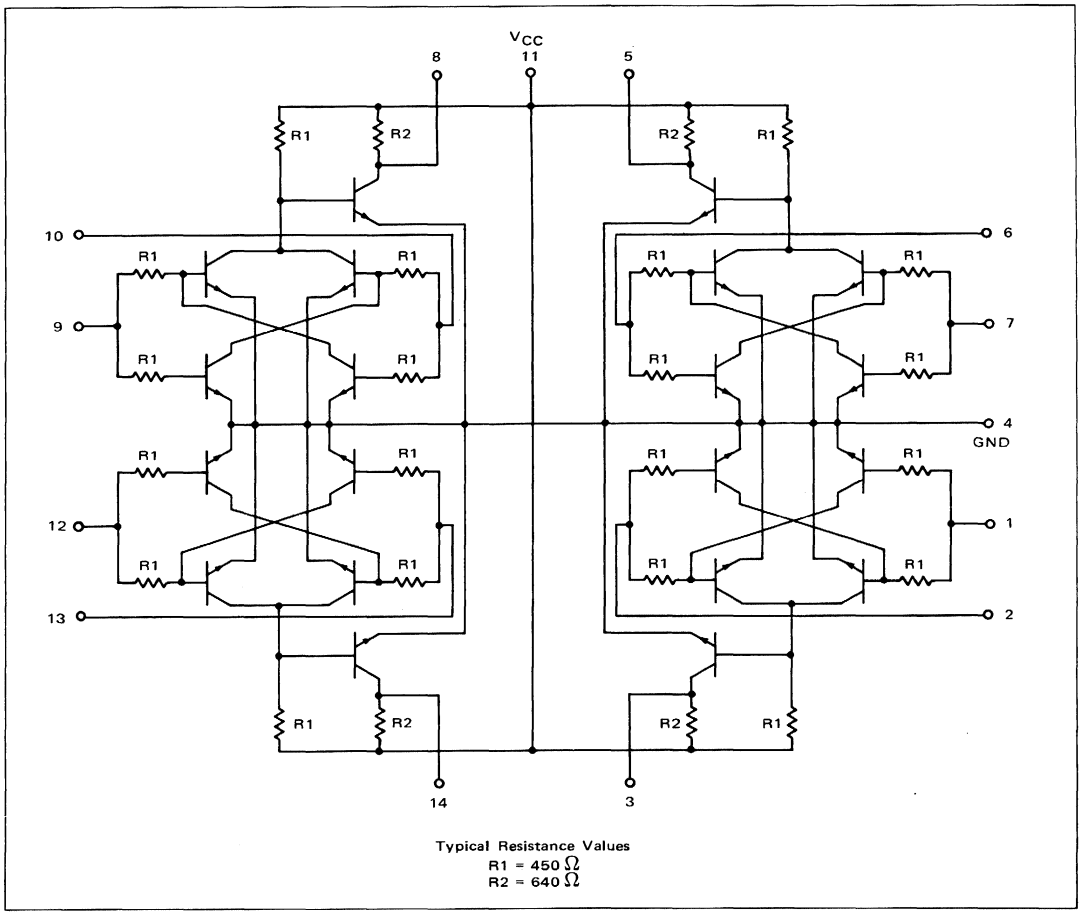
Test procedures are shown for one gate only.
The other gates are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC871P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC771P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

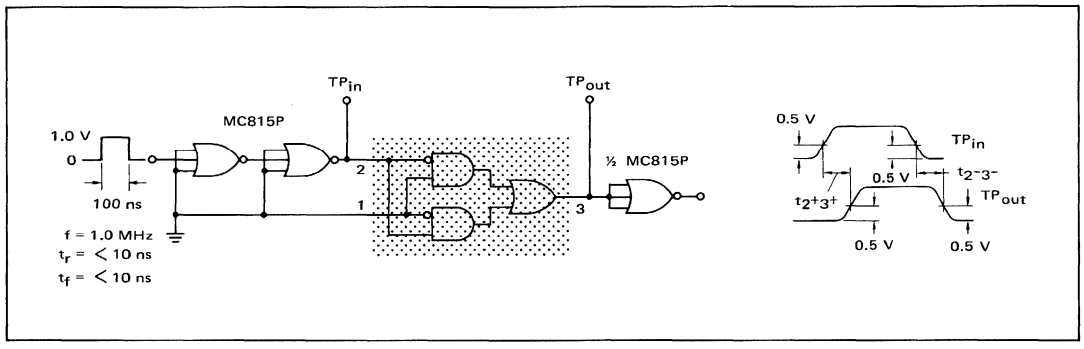
Characteristic	Symbol	Pin Under Test	MC871P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC771P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	1	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	1	-	-	2	11	4
		2	-	1.2	-	1.2	-	1.1	mAdc	-	1.00	-	1.00	-	0.94	mAdc	2	-	-	1	11	4
Output Current	I_{A5}*	3	3.00	-	3.00	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	1,3	-	2	11	4
		3	3.00	-	3.00	-	3.00	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2,3	-	1	11	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	1,2	11	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1,2	-	-	11	4
Switching Time	t	1+3-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In: 1	2	Pulse Out: 3	-	11	4
		1-3+	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	1	2	↓	-	↓	↓
		2+3+	-	-	-		-	-		-	-	-		-	-		2	-		1		
		2-3-	-	-	-		-	-		-	-	-		-	-		2	-		1		

Ground inputs of gates not under test. Other pins not listed are left open.

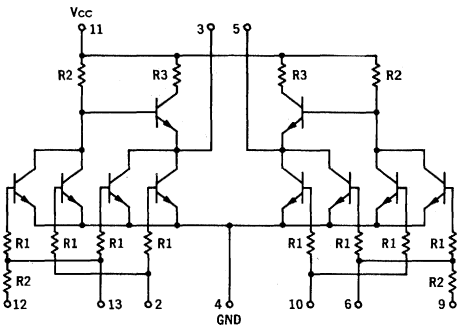
* Symbol is I_{A16} for MC771P.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

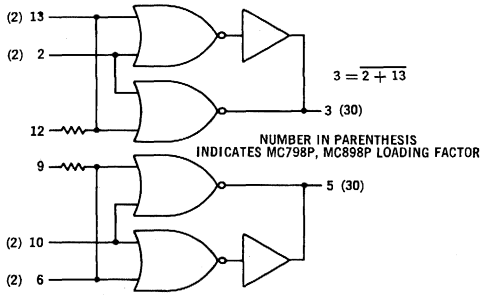


MC798P • MC898P



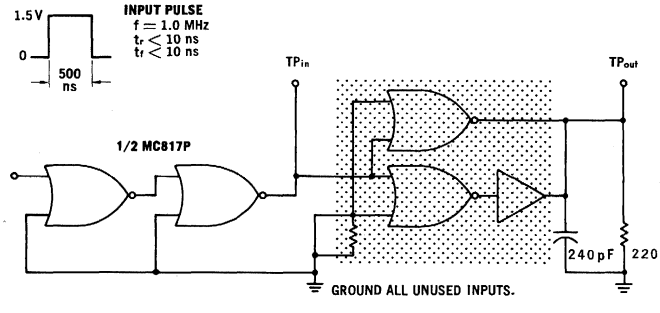
TYPICAL RESISTANCE VALUES
R1 = 1.5 k
R2 = 3.6 k
R3 = 100 Ω

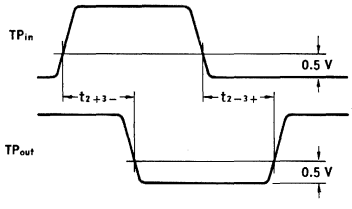
Dual 2-input buffers designed to drive a greater number of loads than the basic Resistor Transistor Logic circuit. Returning an input resistor to V_{CC} allows for capacitive coupling in multivibrator and differentiator applications.



t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

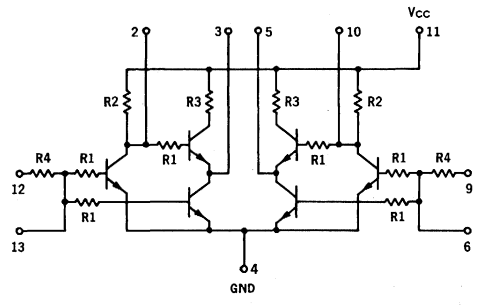
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(k Ohms) V_R*
MC898P	0°C	0.880	0.850	1.80	0.500	3.60	4.6
	+25°C	0.830	0.800	1.80	0.460	3.60	4.8
	+75°C	0.740	0.710	1.80	0.400	3.60	5.0
MC798P	+15°C	0.865	0.865	1.80	0.475	3.60	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	5.0

Characteristic	Symbol	Pin Under Test	MC898P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC798P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2\ I_{in}$	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	13	-	11	-	4
Output Current	I_{AB}	3	4.5	-	4.5	-	4.5	-	mAdc	5.0	-	5.0	-	5.0	-	mAdc	-	3	-	2,13	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	4,13
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	13	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	4,13
Switching Time	$t_{on} + t_{off}$	2,3	-	-	-	160	-	-	ns	-	-	-	160	-	-	ns	Pulse In 2	Pulse Out 3	-	-	11	-	4,13

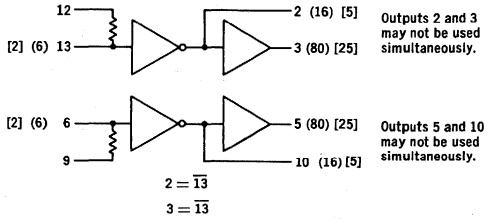
Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

MC799P • MC899P



TYPICAL RESISTANCE VALUES
R1 = 450Ω R3 = 100Ω
R2 = 640Ω R4 = 1.0 k

The dual buffer is designed to drive a greater number of load circuits than the basic RTL circuit. Because this circuit has a very low output impedance the rise times of output waveforms are maintained when driving capacitive loads. A resistor which is internally connected to the input allows for capacitive coupling to the input, the differentiation of input waveforms and various multivibrator applications.



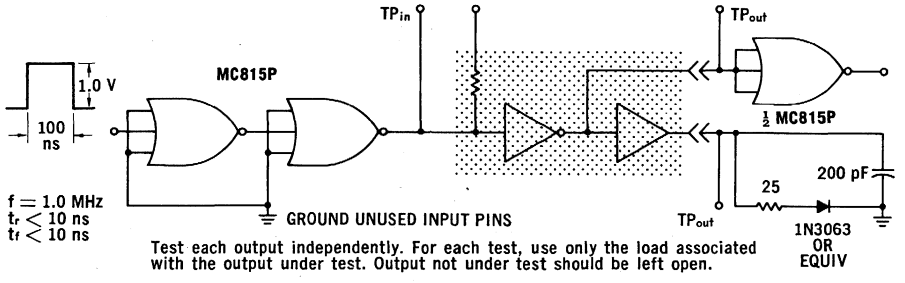
$2 = \overline{13}$

$3 = \overline{13}$

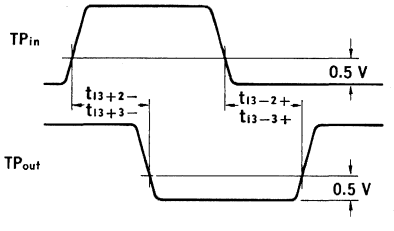
NUMBER IN PARENTHESIS INDICATES MC799P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC899P LOADING FACTOR

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test. Output not under test should be left open.



ELECTRICAL CHARACTERISTICS

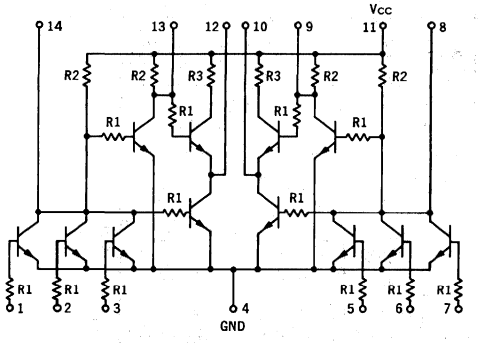
Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC899P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC899P	+25°C	0.910	0.800	1.80	0.500	3.60	640
MC899P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC799P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC799P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC799P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC899P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC799P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	13	-	1.2	-	1.2	-	1.1	mAdc	-	1.0	-	1.0	-	0.94	mAdc	13	-	-	-	11	-	4
Output Current	I_{A5}**	2	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	2	-	13	11	-	4
	I_{AB}	3	15.0	-	15.0	-	14.25	-	mAdc	13.75	-	13.75	-	12.50	-	mAdc	-	3	-	13	11	-	4
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	-	4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	3	4
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	11, 12	-	↓
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	13	-	11	3	↓
Switching Time	t	13+3-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	Pulse In 13	Pulse Out 3	-	-	11	-	4
		13-3+	-	-	-	45	-	-	↓	-	-	-	45	-	-	↓	13	3	-	-	↓	-	↓
		13+2-	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	13	2	-	-	↓	-	↓
		13-2+	-	-	-	32	-	-	↓	-	-	-	32	-	-	↓	13	2	-	-	↓	-	↓

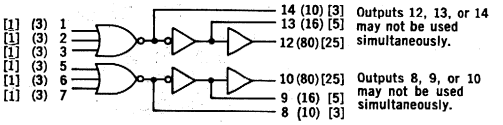
Ground all unused input pins. Other pins not listed are left open. * Resistor Value to V_{CC}. ** Symbol is I_{A16} for MC799P.

MC788P • MC888P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 100 Ω

Two 3-input positive logic NOR gates, each followed by an inverting and non-inverting high fan-out amplifier, are provided in a single package. For each section, the output from each stage is available. If more than one output is used, the full loading factors cannot be employed since each output provides the drive for the succeeding stage.

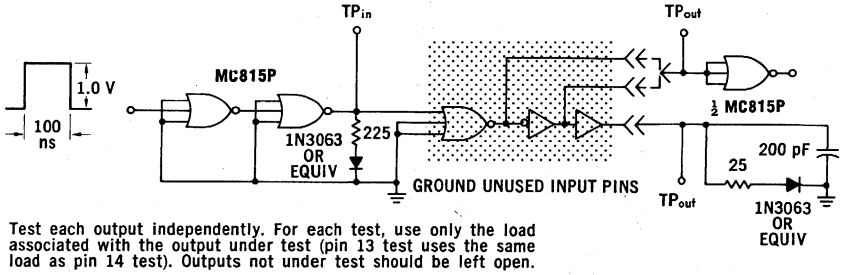


$14 = \overline{1+2+3}$ $13 = 1+2+3$ $12 = 1+2+3$

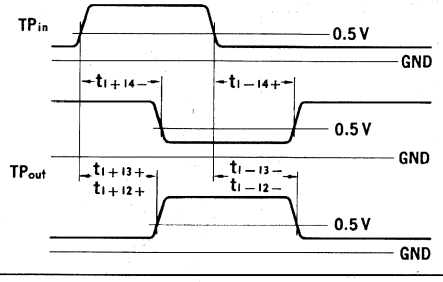
NUMBER IN PARENTHESIS INDICATES MC788P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC888P LOADING FACTOR.

t_{pd} = 24 ns
P_D = 145 mW (Input Low)
56 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



Test each output independently. For each test, use only the load associated with the output under test (pin 13 test uses the same load as pin 14 test). Outputs not under test should be left open.



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one buffer only.
The other buffer is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC888P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC788P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

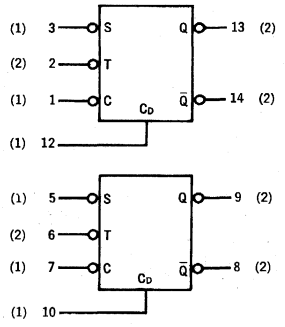
Characteristic	Symbol	Pin Under Test	MC888P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC788P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2, 3	-	11	-	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	1, 3	-	↓	-	↓
		3	-		-		-			-		-		-			3	-	1, 2	-		-	
Output Current	I_{AB} †	12	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	12	-	14	11	-	4
	I_{A5} #	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	14	↓	-	↓
	I_{A3} ‡	14	1.8	-	1.8	-	1.71	-		-	-	-	-	-	-	-	-	14	-	1, 2, 3		-	
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	12	1,2,3,4
		13	-		-		-			-		-		-			-	14	-	-		-	1,2,3,4
		14	-		-		-			-		-		-			-	1	-	-		-	2,3,4
		14	-		-		-			-		-		-			-	2	-	-		-	1,3,4
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	-	1,2,4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	12	1,2,3,4
		13	-		-		-			-		-		-			-	-	14	-		-	1,2,3,4
		14	-		—		-			-		-		-			-	-	1	-		-	2,3,4
		14	-		-		-			-		-		-			-	-	2	-		-	1,3,4
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	-	1,2,4
																	Pulse In	Pulse Out					
Switching Time	t	1+12+	-	-	-	65	-	-	-	-	-	-	65	-	-	-	1	12	-	-	11	-	2,3,4
		1-12-	-	-	-	58	-	-	-	-	-	-	58	-	-	-	1	12	-	-	↓	-	↓
		1+13+	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1-13-	-	-	-	42.5	-	-	-	-	-	-	42.5	-	-	-	1	13	-	-		-	
		1+14-	-	-	-	20	-	-	-	-	-	-	20	-	-	-	1	14	-	-		-	
		1-14+	-	-	-	28	-	-	-	-	-	-	28	-	-	-	1	14	-	-	↓	-	↓

Ground input pins of buffer not under test. Other pins not listed are left open. *Resistor value to V_{CC}.

†I_{A80} is symbol for MC788P. #I_{A16} is symbol for MC788P. ‡I_{A5} is symbol for MC788P.

MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{TOG} = 3 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (All Inputs Low)

NUMBER IN PARENTHESIS
INDICATES MC776P, MC876P LOADING FACTOR

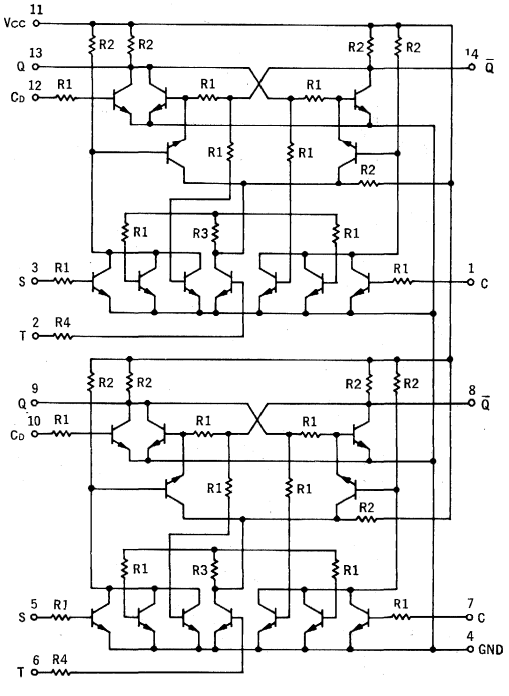
CLOCKED INPUT OPERATION①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

① Direct input (C_D) must be low.

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

③ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 1.5k R3 = 3.0k
R2 = 3.6k R4 = 750Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

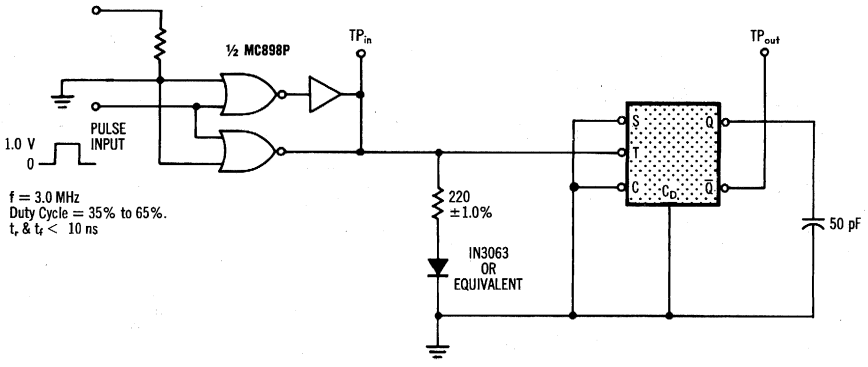
	@ Test Temperature	TEST VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	TEST VALUES (μA) I_O
MC876P	0°C	0.880	0.850	1.80	0.500	3.60	270
	+25°C	0.830	0.800	1.80	0.460	3.60	290
	+75°C	0.740	0.710	1.80	0.400	3.60	255
MC776P	+15°C	0.865	0.865	1.80	0.475	3.60	270
	+25°C	0.850	0.850	1.80	0.460	3.60	270
	+ 55°C	0.800	0.800	1.80	0.430	3.60	270

Characteristic	Symbol	Pin Under Test	MC876P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC776P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VALUES APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	I_O	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	µAdc	-	150	-	150	-	150	µAdc	1	-	13	-	11	-	4
	$2\ I_{in}$	2	-	300	-	280	-	280	↓	-	300	-	300	-	300	↓	2	-	1, 3	-	↓	-	↓
	I_{in}	3	-	150	-	140	-	140	↓	-	150	-	150	-	150	↓	3	-	14	-	↓	-	↓
	I_{in}	12	-	150	-	140	-	140	↓	-	150	-	150	-	150	↓	12	-	14	-	↓	-	↓
Output Current	I_{A2}	13	320	-	320	-	300	-	µAdc	320	-	320	-	320	-	µAdc	-	13	1	12	11	-	4, 14 §
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	-	↓
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12, 14	3	-	↓	-	↓
Output Voltage	V_{out}	13	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	↓	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	-	4, 13 §
		13*†	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	14	4, 12
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	3	↓	↓	↓
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	-	↓	-	14 §
Saturation Voltage	$V_{CE(sat)}$	13	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	-	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	-	4, 13 §
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	12	↓	-	4, 14 §
Turn On Voltage	V_{on}	13*#	850	-	800	-	710	-	mVdc	865	-	850	-	800	-	mVdc	-	1, 3	-	-	11	13	4, 12
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3	-	1	↓	↓	↓
		13*†	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	-	-	1, 3	↓	↓	↓

* Clock Pulse to pin 2
† Pin 13 = LOW } Set by a momentary ground prior to the
# Pin 14 = LOW } application of the negative-going clock.

§ ground thru diode (cathode to ground).
Ground inputs of flip-flop not under test.
Other pins not listed are left open.

TOGGLE MODE TEST CIRCUIT



1. Set up the circuit with the Input Pulse as given.
2. The circuit should toggle with an output (TP_{out}) sense frequency of 1.5 MHz as the duty cycle is varied between 35% and 65%.

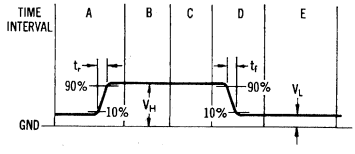
CLOCK PULSE

MC776P		
T_A	V_L	V_H
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
T_A	V_L	V_H
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

All values are ± 2.0mV

CLOCK PULSE DEFINITION

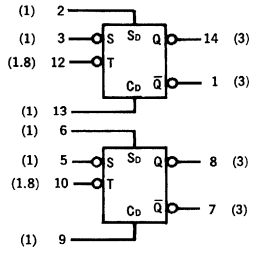


SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, but should be < 1.0 μs.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC778P • MC878P

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



DIRECT INPUT OPERATION①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION③

t_n④	t_{n+1}④	
S	Q	$\bar{Q}$
1	1	0
0	0	1

NUMBER IN PARENTHESIS INDICATES MC778P, MC878P LOADING FACTOR

P_D = 48 mW (Direct Set, S_D, and Direct Clear, C_D, Low; all other inputs high)
35 mW (All Inputs Low)

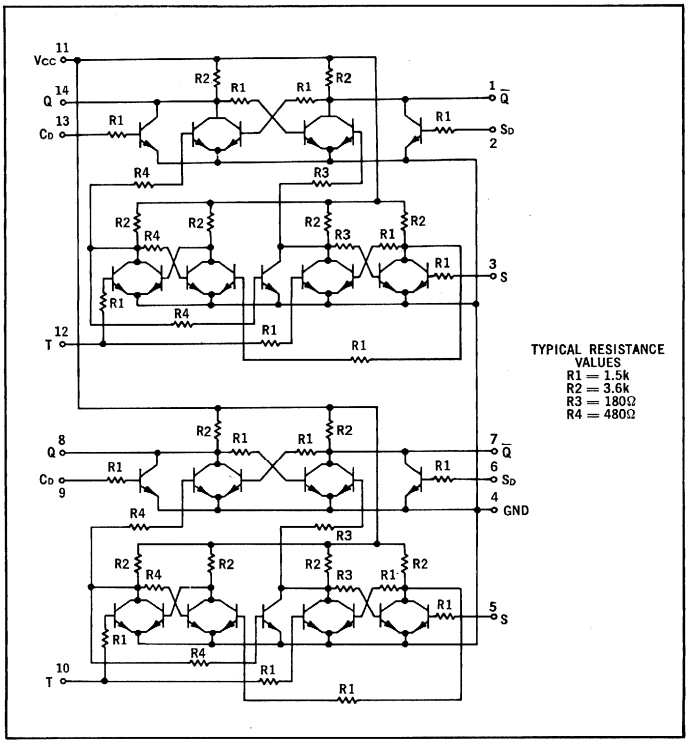
frog = 1 MHz

① Clock (T input) must be high.

② The output state will not change when the input state goes from $S_D = C_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.

③ Direct inputs (S_D and C_D) must be low.

④ The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.



TYPICAL RESISTANCE VALUES
R1 = 1.5k
R2 = 3.6k
R3 = 180Ω
R4 = 480Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

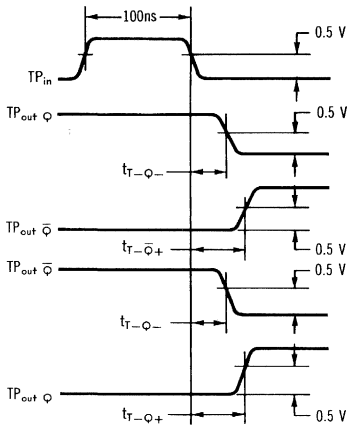
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	$K\Omega \pm 1\%$ V_R*
MC878P	0°C	0.880	0.850	1.80	0.500	3.60	0.45	4.3
	+25°C	0.830	0.800	1.80	0.460	3.60	0.40	4.3
	+75°C	0.740	0.710	1.80	0.400	3.60	0.35	4.7
MC778P	+15°C	0.865	0.865	1.80	0.475	3.60	-	4.6
	+25°C	0.850	0.850	1.80	0.460	3.60	-	4.8
	+55°C	0.800	0.800	1.80	0.430	3.60	-	5.0

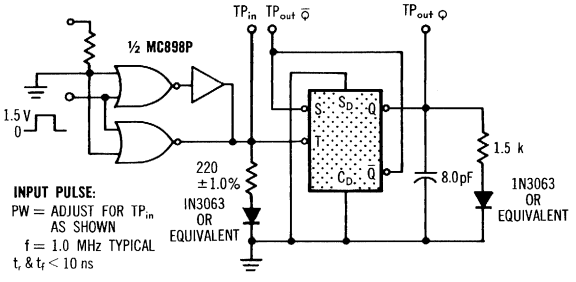
Characteristic	Symbol	Pin Under Test	MC878P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC778P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_{LL}	V_R*	Gnd
Input Current	I_{in}	2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	3	12	11	-	12	4, 13
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	-	12		-	12	2, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	-	-		-	-	2, 3, 4, 13
	1.8 I_{in}	12	-	270	-	250	-	250		-	270	-	270	-	270		12	-	3	-		-	-	2, 4, 13
	I_{in}	13	-	150	-	140	-	140		-	150	-	150	-	150		13	-	-	12		-	12	2, 3, 4
Output Current	I_{A3}	1	420	-	430	-	395	-	μAdc	420	-	420	-	420	-	μAdc	1	12	3, 13	2	11	-	-	4
		1		-		-		-			-		-		-		1	-	13	2, 12		-	12	3, 4
		14		-		-		-			-		-		-		14	12	2	13		-	-	3, 4
		14		-		-		-			-		-		-		14	3	2	12, 13		-	12	4
Output Voltage	V_{out}	1	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	12, 13	-	11	-	-	3, 4
		1	-		-		-			-		-		-			-	14	12	-		-	-	2, 3, 4, 13
		14	-		-		-			-		-		-			-	13	2, 12	-		-	-	3, 4
		14	-		-		-			-		-		-			-	1	12	-		-	-	2, 3, 4, 13
Saturation Voltage	$V_{CE(sat)}$	1	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	3	13	12	11	-	12	2, 4
		14	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	3, 12	11	-	12	4, 13
Leakage Current	I_L	11	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	μAdc	-	-	-	-	-	11	-	2, 3, 4, 12, 13

* Apply to V_{CC} thru resistor prior to applying V_{off}. Ground inputs of flip-flop not under test. Other pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

FIGURE 1

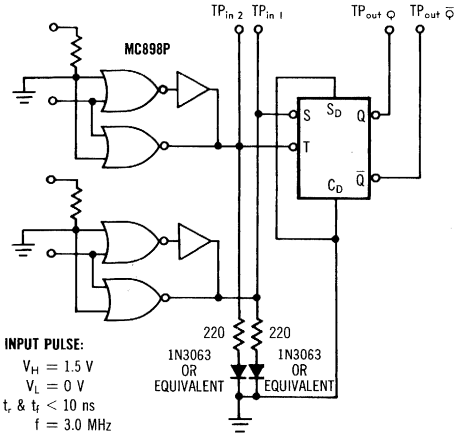




TEST	MAXIMUM (ns @ 25°C)
t_{T-Q+}	120
$t_{T-\bar{Q}-}$	80
t_{T-Q-}	80
$t_{T-\bar{Q}+}$	120

SWITCHING TIMES

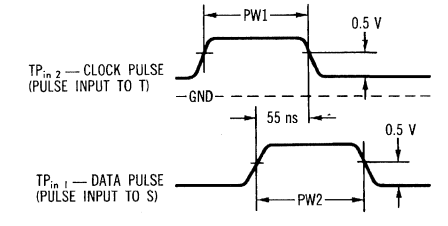
FIGURE 2A — SET-UP AND RELEASE TIMES TEST CIRCUIT



INPUT PULSES ARE ADJUSTED TO PRODUCE TP$_{in\ 1}$ AND TP$_{in\ 2}$ SHOWN IN FIGURES 2B AND 2C.

TP$_{in\ 1}$ is defined as the data pulse
TP$_{in\ 2}$ is defined as the clock pulse

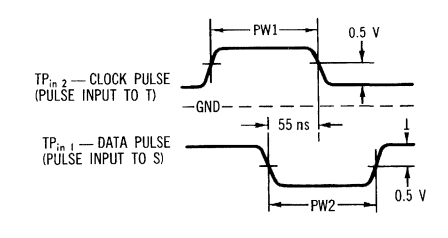
FIGURE 2B — SET-UP TIME WAVEFORMS



IF Q WAS HIGH, IT WILL REMAIN HIGH;
IF Q WAS LOW; IT WILL GO HIGH.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

FIGURE 2C — RELEASE TIME WAVEFORMS

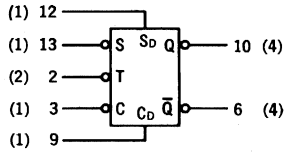


IF Q WAS LOW, IT WILL REMAIN LOW;
IF Q WAS HIGH, IT WILL GO LOW.

PW1 = 100 ns min.
PW2 = 80 ±5 ns

MC722P • MC822P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



NUMBER IN PARENTHESIS
INDICATES MC722P, MC822P LOADING FACTOR

f_{Tog} = 1.0 MHz
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The ouput state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.

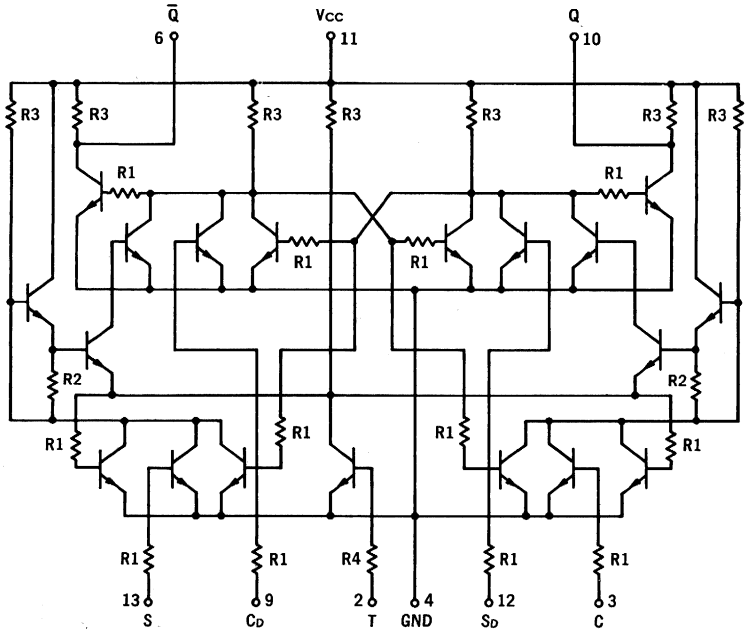
0 = low state

1 = high state

t_n = time period prior to negative transition of clock pulse

t_{n+1} = time period subsequent to negative transition of clock pulse

Q_n = state of Q output in time period t_n



TYPICAL RESISTANCE VALUES
R1 = 1.5 k R3 = 3.6 k
R2 = 2.0 k R4 = 750 Ω

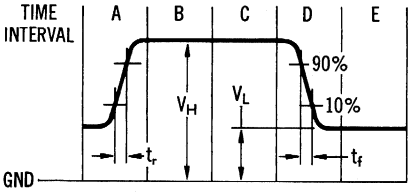
ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC822P	0°C	0.880	0.850	1.80	0.500	3.60
	+25°C	0.830	0.800	1.80	0.460	3.60
	+75°C	0.740	0.710	1.80	0.400	3.60
MC722P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC822P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC722P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	300	-	280	-	280	μAdc	-	300	-	300	-	300	μAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-	▼	-	▼	-	▼	▼	-	▼	-	▼	-	▼	▼	13	-	9	-	▼	▼
Output Current	I_{A4}	6	570	-	570	-	535	-	mAdc	570	-	570	-	570	-	μAdc	6	9	12	-	11	4
		10	570	-	570	-	535	-	mAdc	570	-	570	-	570	-	μAdc	10	12	9	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-	▼	-	▼	-	▼	▼	-	▼	-	▼	-	▼	▼	-	-	-	3, 13	▼	▼

Pins not listed are left open.
* = Clock Pulse to pin 2, see Figure 1.
# = Pin 9 HIGH, ## = Pin 12 HIGH } Set by a momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

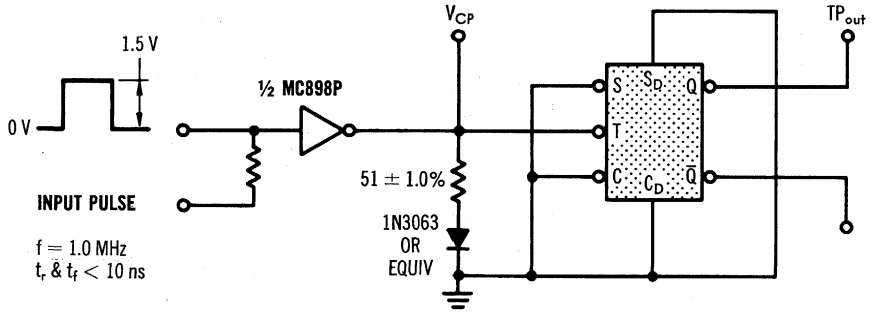
MC822P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.850 V ± 2.0 mV
0°C	+ 0.500 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 75°C	+ 0.400 V ± 2.0 mV	+ 0.760 V ± 2.0 mV

MC722P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

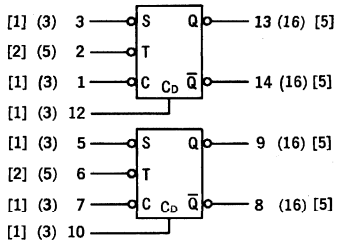
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



THE SENSE FREQUENCY AT TP_{out} (0.5 MHz) SHOULD BE ½ THE FREQUENCY AT V_{CP} WHEN THE DUTY CYCLE IS VARIED BETWEEN 25% AND 75%.

MC791P • MC891P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{tog} = 4 MHz
t_{pd} = 40 ns typ

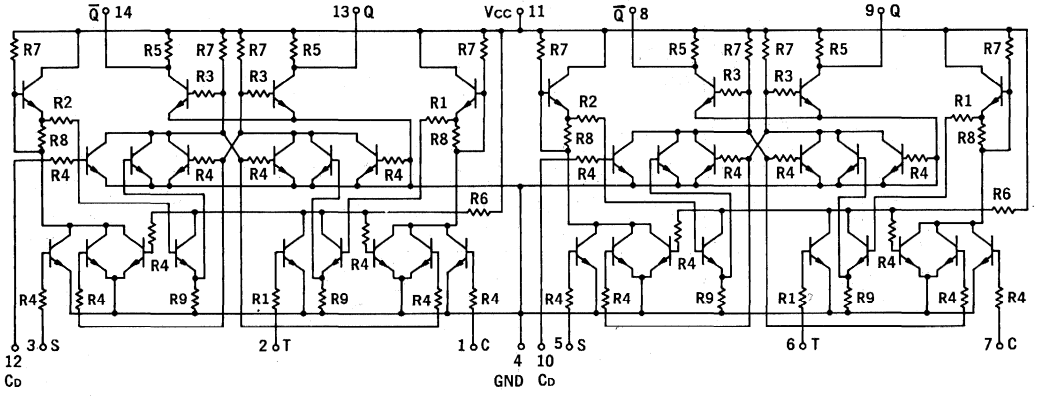
P_D = 190 mW typ (Only Clock Input High)
160 mW typ (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\bar{Q}$
1	1	Q_n③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC791P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC891P



TYPICAL RESISTANCE VALUES
R1 = 300 Ω R4 = 600 Ω R7 = 900 Ω
R2 = 500 Ω R5 = 640 Ω R8 = 2.0 k
R3 = 550 Ω R6 = 700 Ω R9 = 3.0 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC891P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC791P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC891P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC791P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1†	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	-	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		2	-	1, 3	-		
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
	I_{in}	12	-	600	-	600	-	570		-	500	-	500	-	470		12	-	-	-		
Output Current	I_{A5}‡	13†	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	13	-	-	11	-
		14	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.50	-	mAdc	-	12, 14	-	-	11	4
Output Voltage	V_{out}	13 § ⑤	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	4, 12
		13§§④	-		-		-			-		-		-			-	-	-	3		
		13 § ⑥	-		-		-			-		-		-			-	1	-	-		
		13§§⑦	-		-		-			-		-		-			-	-	-	3		
		14 § ④	-		-		-			-		-		-			-	-	-	1		
		14§§⑤	-		-		-			-		-		-			-	3	-	-		
		14 § ⑦	-		-		-			-		-		-			-	-	-	1		
		14§§⑥	-		-		-			-		-		-			-	3	-	-		
Saturation Voltage	$V_{CE(sat)}$	13†	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	-	11	4
		13*#	-		-		-			-		-		-			-	1, 3	-	-		
		13†*	-		-		-			-		-		-			-	1	-	3		
		13†*	-		-		-			-		-		-			-	-	-	1, 3		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-		-		-			-		-		-			-	-	-	1, 3		
		14†*	-		-		-			-		-		-			-	1, 3	-	-		

Ground inputs of flip-flop not under test. Other pins not listed are left open.

† Preset the flip-flop by the following procedure:
(1) Momentarily apply V_{BOT} to pin 12 to preclear flip-flop.
(2) After V_{BOT} is removed from pin 12, ground pins 1 and 3.
(3) Apply a negative-going clock pulse to pin 2 (see note*) while pins 1 and 3 are still grounded. This changes the state of the flip-flop to the SET condition.
(4) Remove grounds from pins 1 and 3, and proceed with the test.

‡ Symbol is I_{A16} for MC791P.

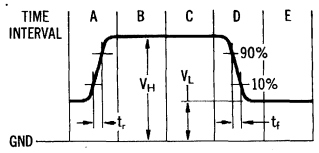
* Clock pulse to pin 2, see Figure 1.

Pin 12 = HIGH — Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

§ = Clock pulse to pin 2, data pulse to pin 3.
§§ = Clock pulse to pin 2, data pulse to pin 1.

④ = See Figure 4.
⑤ = See Figure 5.
⑥ = See Figure 6.
⑦ = See Figure 7.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

MC891P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC791P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

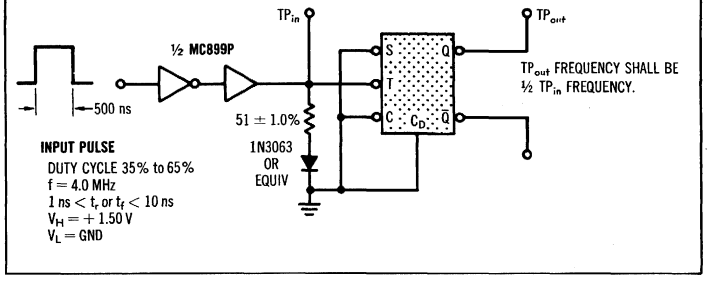


FIGURE 3 — TEST CIRCUIT

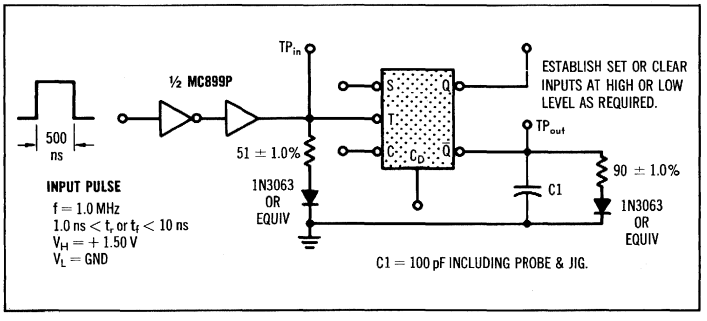


FIGURE 4 — TEST WAVEFORMS

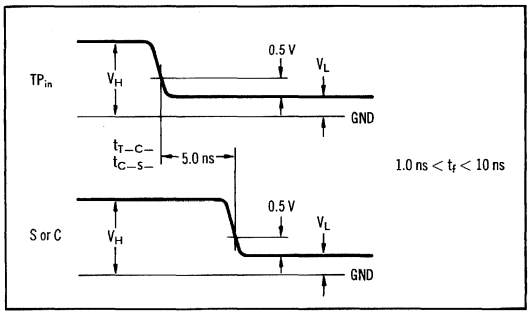


FIGURE 5 — TEST WAVEFORMS

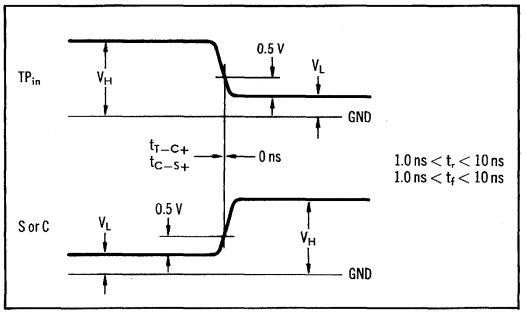


FIGURE 6 — TEST WAVEFORMS

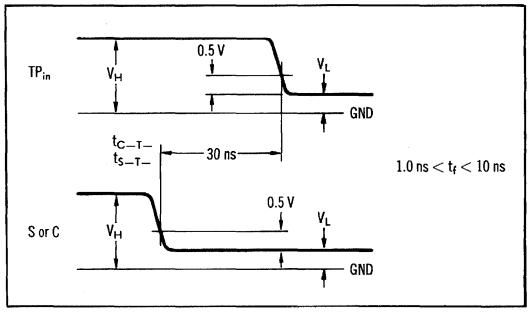
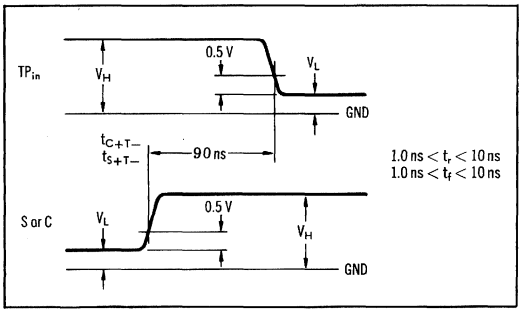
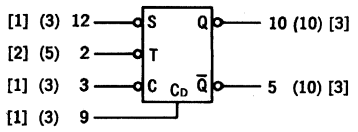


FIGURE 7 — TEST WAVEFORMS



MC723P • MC816P

J-K flip-flop with a direct clear input in addition to the clocked inputs.



$f_{Tog} = 4$ MHz

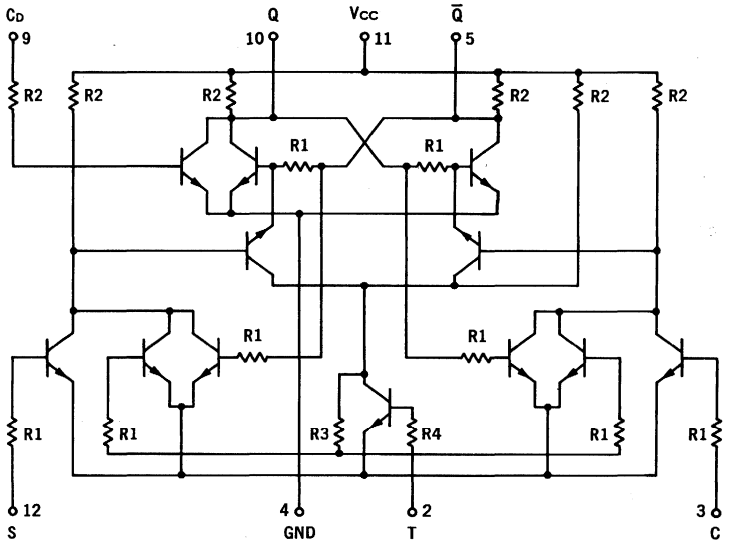
$P_D = 91$ mW (Only Clock Input High)
79 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC723P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC816P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC816P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC723P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC816P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC723P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 12	-	11	4
	I_{in}	3	-	600	-	600	-	570		-		-		-			3	-	10	-		
		9	-		-		-			-		-		-			9	-	5	-		
		12	-		-		-			-		-		-			12	-	5	-		
Output Current	I_{A3}†	5	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	5	9, 12	-	11	4
		5		-		-		-			-		-		-		-	5, 9	12	-		4
		10		-		-		-			-		-		-		-	10	3	9		4, 5§
Output Voltage	V_{out}	10	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	9	-	-	11	4, 5
		10*##	-		-		-			-		-		-			-	3, 12	-	-		4, 9
		10*	-		-		-			-		-		-			-	3	-	12		
		10*##	-		-		-			-		-		-			-	-	-	3, 12		
Saturation Voltage	$V_{CE(sat)}$	5	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	-	9	11	4, 5
		10	-		-		-			-		-		-			-	-	9	-		4, 5
		10	-		-		-			-		-		-			-	-	-	-		4, 10§
Turn-On Voltage	V_{on}	10*##Δ	930	-	880	-	790	-	mVdc	865	-	850	-	800	-	mVdc	-	3, 12	-	-	11	4, 9
		10*Δ		-		-		-			-		-		-		-	12	-	3		
		10*#Δ		-		-		-			-		-		-		-	-	-	3, 12		

Pins not listed are left open.

† = I_{A10} is symbol for MC723P

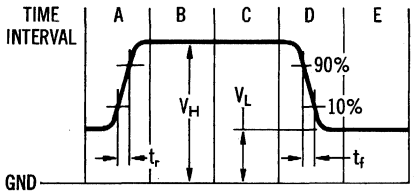
§ = Silicon diode to ground.

* = Clock Pulse to pin 2, See Figure 1.

= Pin 10 LOW, ## = Pin 5 LOW } Set by a momentary ground prior to the application of the negative-going Clock pulse.

Δ = MC816P pin 10 loaded by: 1.56 mAdc (0°C and +75°C)
1.65 mAdc (+25°C)
MC723P pin 10 loaded by: 1.56 mAdc (+15°C and +55°C)
1.65 mAdc (+25°C)

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

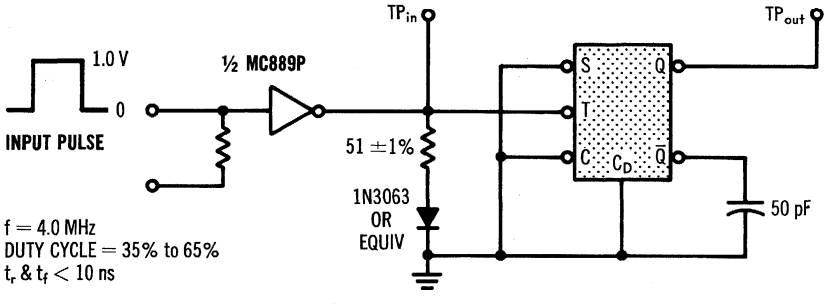
MC816P

T_A	V_L	V_H
+25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC723P

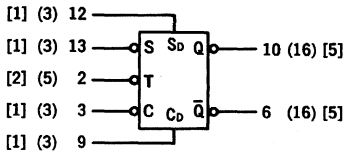
T_A	V_L	V_H
+25°C	+0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



MC726P • MC826P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



f_{TOG} = 4 MHz

P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

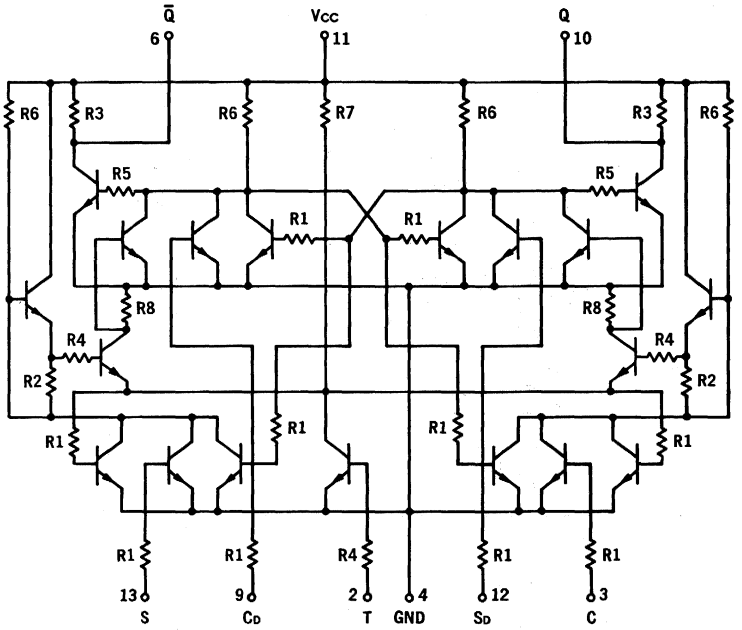
t_n ②		t_{n+1} ③	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

DIRECT INPUT OPERATION ④

S_D	C_D	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

1. Direct inputs (C_D and S_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
6. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC726P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC826P



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 k	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 k

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC826P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC726P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC826P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC726P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-		-		-			-		-		-			13	-	9	-		
Output Current	I_{A5}§	6	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	6, 12	9	-	11	4
		10	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	10, 9	12	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-		-		-			-		-		-			-	-	-	3, 13		

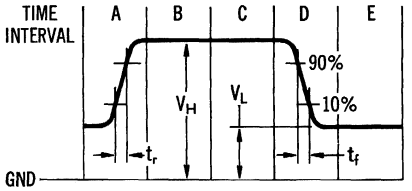
Pins not listed are left open.

* Clock Pulse to pin 2, see Figure 1.

§ I_{A16} is symbol for MC726P.

\# Pin 9 HIGH
Pin 12 HIGH
} Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

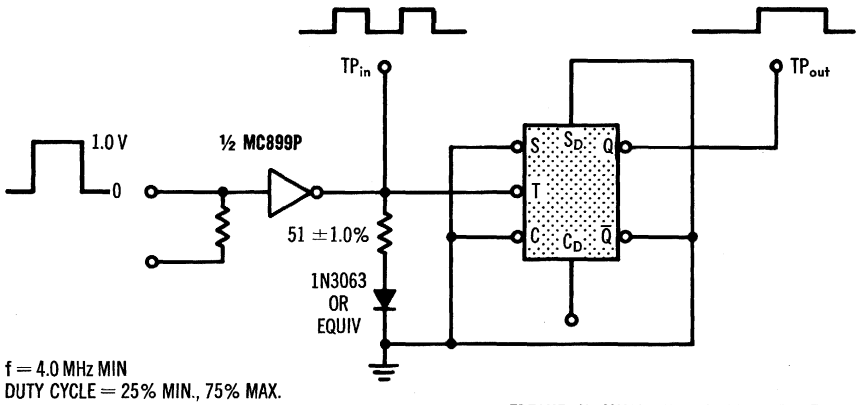
MC826P

T_A	V_L	V_H
+25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC726P

T_A	V_L	V_H
+25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

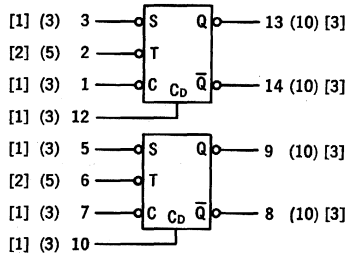


f = 4.0 MHz MIN
DUTY CYCLE = 25% MIN., 75% MAX.
t_r & t_f < 10 ns

OUTPUT FREQUENCY SHALL BE ½ OF TP_{in} FREQUENCY.

MC790P • MC890P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



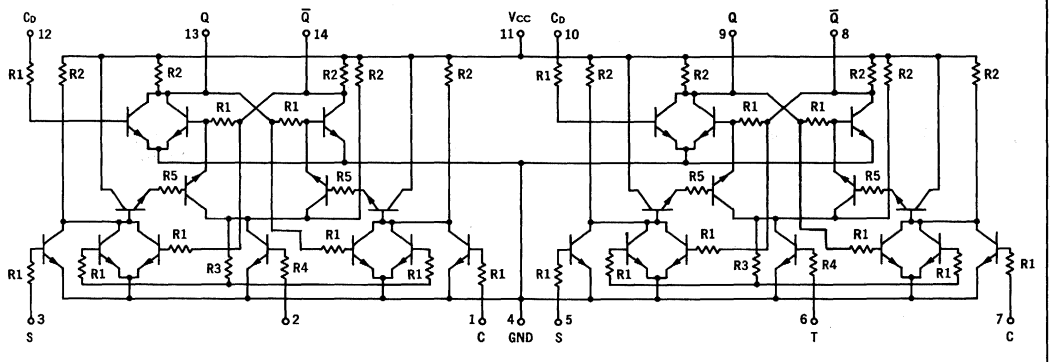
$f_{Tog} = 4$ MHz
$P_D = 182$ mW (Only Clock Input High)
158 (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be $<$ 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC790P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC890P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC890P	0°C	0.960	0.930	1.80	0.570	3.60
MC890P	+25°C	0.910	0.880	1.80	0.500	3.60
MC890P	+75°C	0.820	0.790	1.80	0.450	3.60
MC790P	+15°C	0.865	0.865	1.80	0.475	3.60
MC790P	+25°C	0.850	0.850	1.80	0.460	3.60
MC790P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC890P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC790P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	13	-	11	2, 3, 4, 12
	$2I_{in}$	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	4, 12
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	14	-		1, 2, 4, 12
	I_{in}	12	-	600	-	600	-	570		-	500	-	500	-	470		12	-	14	-		1, 2, 3, 4
Output Current	I_{A3} §	13	1.80	-	1.80	-	1.71	-	mAdc	1.65	-	1.65	-	1.56	-	mAdc	-	13	1	12	11	2, 3, 4
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	1, 2, 4
		14		-		-		-			-		-		-		-	12, 14	3	-		1, 2, 4
Output Voltage	V_{out}	13	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-	11	1,2,3,4,14
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	4, 12
		13*##	-		-		-			-		-		-			-	1	-	3		↓
		13*##	-		-		-			-		-		-			-	-	-	1, 3		
		14*##	-		-		-			-		-		-			-	1, 3	-	-		
		14*#	-		-		-			-		-		-			-	3	-	1		
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	↓	↓
Saturation Voltage	$V_{CE(sat)}$	13	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	12	-	11	1,2,3,4,14
		13#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	1,2,3,4,12
		14##	-		-		-			-		-		-			-	-	12	-		1,2,3,4

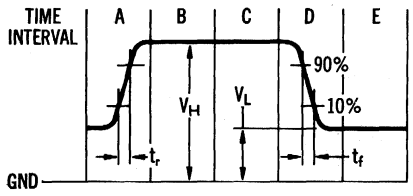
Ground unused input pins. Other pins not listed are left open.

* Clock pulse to pin 2, see Figure 1,

§ I_{A10} is symbol for MC790P.

Pin 13 = LOW
Pin 14 = LOW
} Set by a momentary ground prior to the application of the negative-going Clock Pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

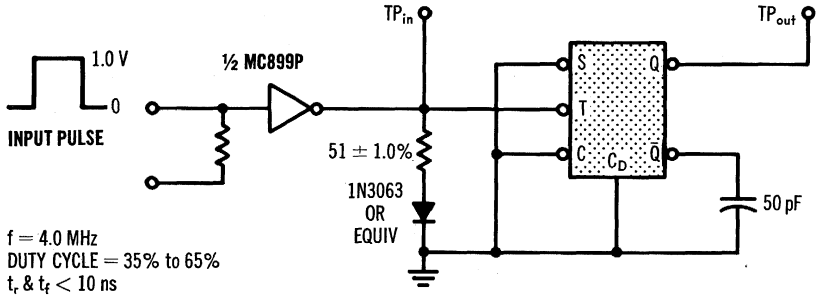
MC890P

T_A	V_L	V_H
+ 25°C	+0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+0.450 V ± 2.0 mV	+0.840 V ± 2.0 mV

MC790P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

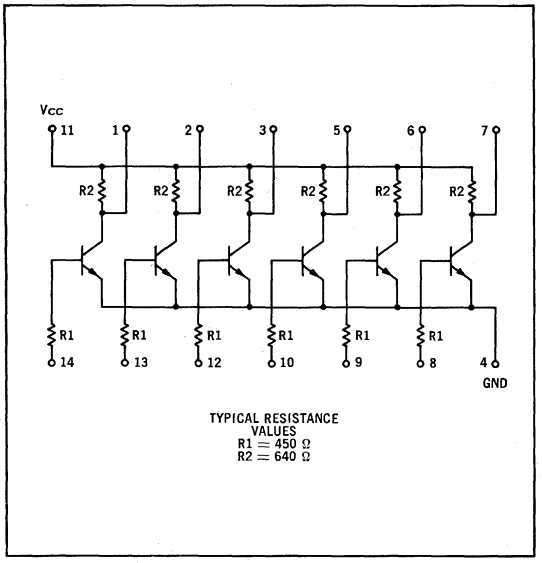
FIGURE 2 — TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz
DUTY CYCLE = 35% to 65%
t_r & $t_f < 10$ ns

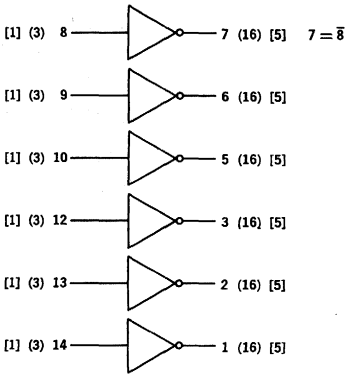
FREQUENCY AT TP_{out} SHOULD BE ½ THE FREQUENCY AT TP_{in}

MC789P • MC889P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω

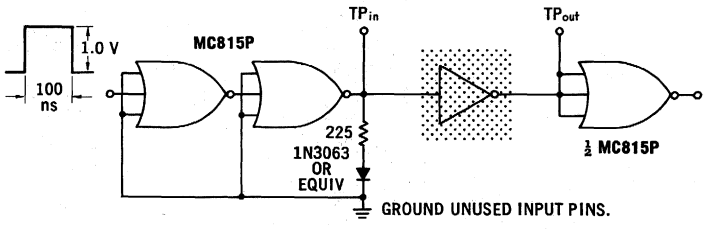
Six individual circuits are contained in a single package. Each provides the simple inversion function.

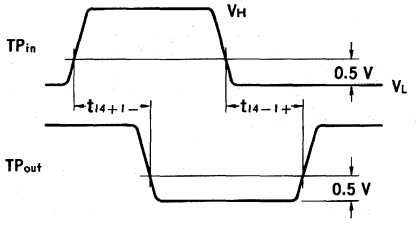


NUMBER IN PARENTHESIS INDICATES MC789P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC889P LOADING FACTOR.

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.
The other inverters are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC889P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC789P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

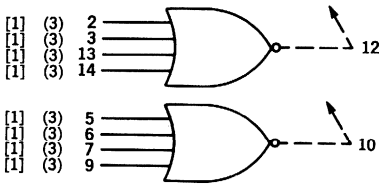
Characteristic	Symbol	Pin Under Test	MC889P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC789P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	14*	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	*	-	11	4
Output Current	I_{A5}	1	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	1	-	-	14	11	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	4
Switching Time	$t_{on} + t_{off}$	1, 14	-	-	-	48	-	-	ns	-	-	-	48	-	-	ns	Pulse In 14	Pulse Out 1	-	-	11	4

Ground inputs of inverters not under test. Other pins not listed are left open

* To simulate worse case conditions, the output of inverter under test is tied to the output of another inverter which has its input taken to V_{BOT}.

MC786P • MC886P

Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.

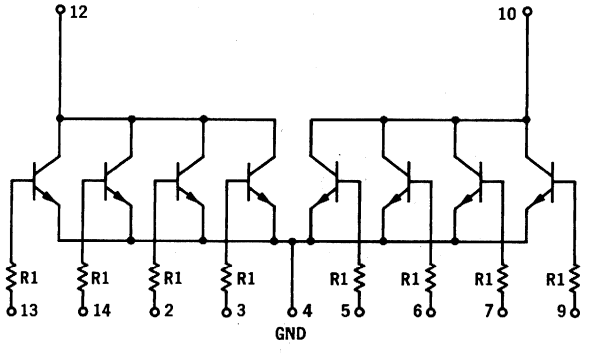


$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC786P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC886P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expander is tested in the same manner.

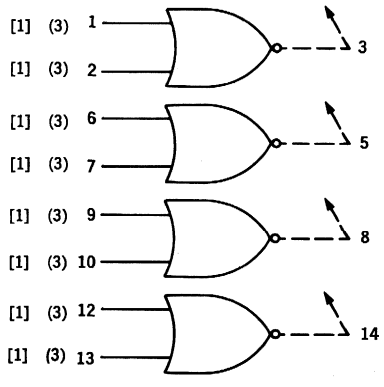
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC886P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC786P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC886P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC786P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	2	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	3,13,14	-	11	12	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	3	-	2,13,14	-	↓	↓	↓
		13	-		-		-			-		-		-			13	-	2,3,14	-			
		14	-		-		-			-		-		-			14	-	2,3,13	-			
Output Leakage Current	I_{CEX}	12	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	12	-	-	2, 3, 13, 14	11	-	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	13	-	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	14	-	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	2	-	-			3,4,13,14
		12	-		-		-			-		-		-			-	3	-	-			2,4,13,14
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	13	-	11	12	2,3,4,14
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	14	-	↓	↓	2,3,4,13
		12	-		-		-			-		-		-			-	-	2	-			3,4,13,14
		12	-		-		-			-		-		-			-	-	3	-			2,4,13,14

Ground unused input pins. Other pins not listed are left open.

MC785P • MC885P

Four 2-input expanders housed in a single package increase the input capability of MRTL gates.

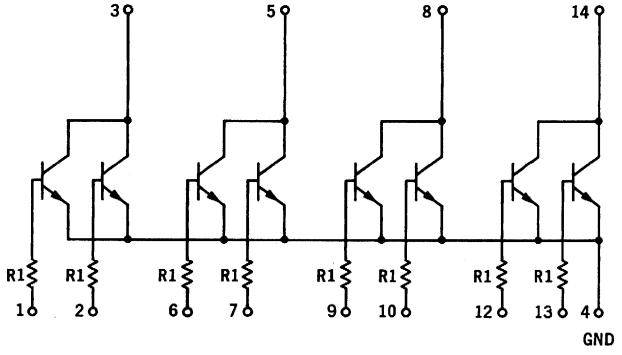


$3 = \overline{1+2}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC785P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC885P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} CONNECTION TO PIN 11 IS NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

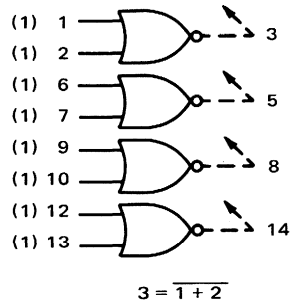
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC885P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC785P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC885P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC785P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	3	4
		2	-	600	—	600	-	570	μAdc	-	500	-	500	-	470	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	200	-	200	-	250	μAdc	-	225	-	225	-	250	μAdc	3	-	-	1, 2	11	-	4
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2, 4
		3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1, 4
Saturation Voltage	$V_{CE(sat)}$	3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	3	2, 4
		3	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	3	1, 4

Ground unused input pins. Other pins not listed are left open. * Resistor value to V_{CC}.

MC9721P • MC9821P

Four 2-input expanders housed in a single package increase the input capability of mW MRTL gates.



$3 = \overline{1 + 2}$

t_{pd} = 27 ns

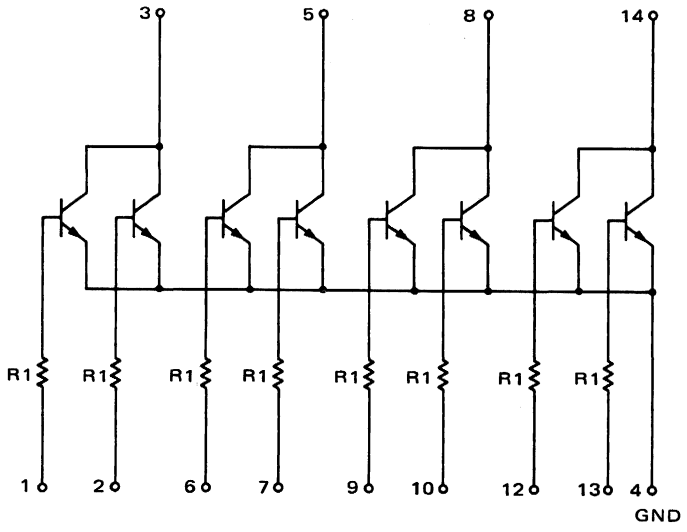
P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC9721P, MC9821P LOADING FACTOR

NOTES ON THE USE OF THE MC9721/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



V_{CC} connection to pin 11 is not shown
Typical Resistance Values
R1 = 1.5 k

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	($k\Omega$) V_R*
MC9821P	0°C	0.880	0.850	1.80	0.500	3.60	3.6
	+25°C	0.830	0.800	1.80	0.460	3.60	3.6
	+75°C	0.740	0.710	1.80	0.400	3.60	4.0
MC9721P	+15°C	0.865	0.865	1.80	0.475	3.60	3.6
	+25°C	0.850	0.850	1.80	0.460	3.60	3.6
	+55°C	0.800	0.800	1.80	0.430	3.60	3.6

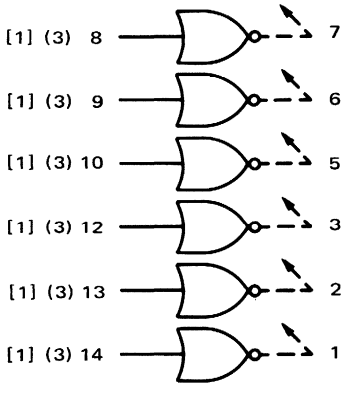
Characteristic	Symbol	Pin Under Test	MC9821P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9721P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	2	-	11	3	4
		2	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	2	-	1	-	11	3	4
Output Leakage Current	I_{CEX}	3	-	25	-	25	-	30	μAdc	-	40	-	40	-	50	μAdc	3	-	-	1,2	11	-	4
Output Voltage	V_{out}	3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	3	2,4
		3	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	3	1,4
Saturation Voltage	$V_{CE(sat)}$	3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	1	-	11	3	2,4
		3	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	2	-	11	3	1,4

Ground unused input pins. Other pins not listed are left open.

* Resistor value to V_{CC}.

MC9719P • MC9819P

Six individual expanders are contained in a single package to increase the input capability of MRTL gates.



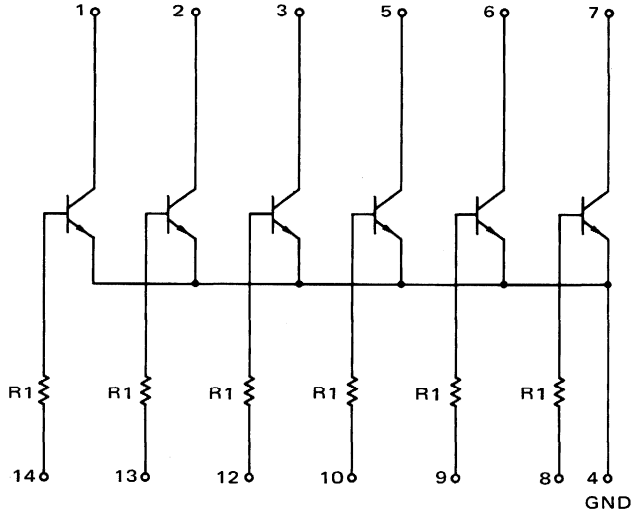
t_{pd} = 12 ns
P_D = 13 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC9719P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC9819P LOADING FACTOR

When an expander is added to a gate, subtract 0.4 load from the output of the gate for each expander circuit added.

SEE SHEET 6-158 FOR EXPANDER RULES



V_{CC} connection to pin 11 is not shown
Typical Resistance Value
R1 = 450 Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one expander only.
The other expanders are tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC9819P	0°C	0.960	0.930	1.80	0.570	3.60	640
	+25°C	0.910	0.880	1.80	0.500	3.60	640
	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC9719P	+15°C	0.865	0.865	1.80	0.475	3.60	640
	+25°C	0.850	0.850	1.80	0.460	3.60	640
	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC9819P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC9719P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	I_{in}	14	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	14	-	-	-	11	1	4
Output Leakage Current	I_{CEX}	1	-	100	-	218	-	235	μAdc	-	100	-	225	-	225	μAdc	1	-	-	14	11	-	4
Output Voltage	V_{out}	1	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	-	-	11	1	4
Saturation Voltage	$V_{CE(sat)}$	1	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	14	-	11	1	4

Ground inputs of expanders not under test. Other pins not listed are left open.

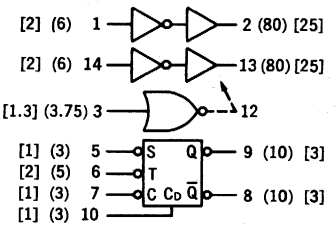
* Resistor value to V_{CC}.

MULTIFUNCTION DEVICES

(1 J-K Flip-Flop, 1 Expander, 2 Buffers)

MC779P • MC879P

A medium-power monolithic device consisting of one J-K flip-flop, one expander, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for preclearing counters, inserting parallel data into registers, and other similar applications. The MRTL expander is designed to increase the fan-in capability of gates with expander inputs, and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

	f_{Tog} MHz	t_{pd}	P_D(mW)	
			(Inputs High)	(Inputs Low)
FLIP-FLOP	4	–	91‡	79
EACH BUFFER	–	15	25	45
EXPANDER	–	12	2.5	Negligible

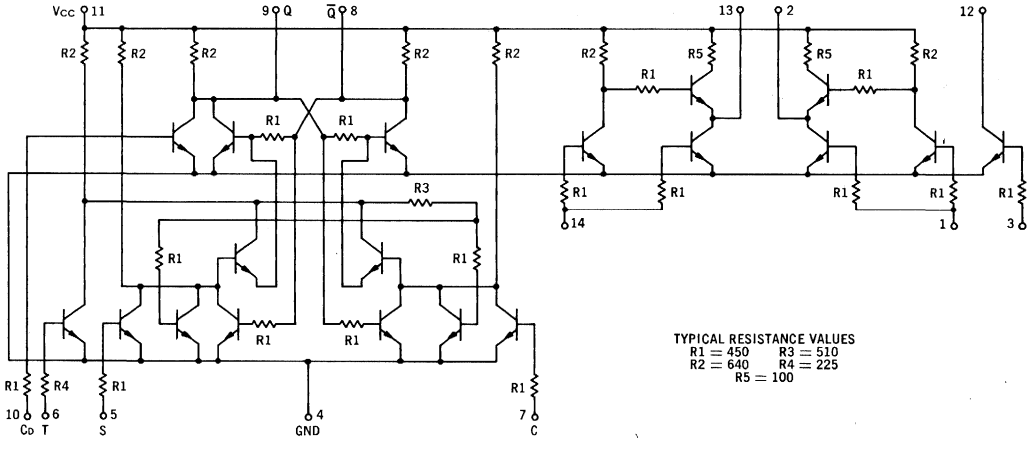
‡Only Clock Input High

CLOCKED INPUT OPERATION ①

t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC779P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC879P



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC879P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC879P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC879P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC779P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC779P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC779P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC879P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC779P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		12	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5, 7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}†	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}‡	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5, 10	-		-	1,3,4,14
	I_{A3}‡	8		-		-		-			-		-		-		-	8, 10	5	-		-	
	I_{A3}‡	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}#	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		12	1,4,5,6,7,10,14
	I_{AB}†	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5, 7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5, 7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5, 7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5, 7		-	
		12	-		-		-			-		-		-			-	3	-	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	-	3	-		12	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* = Resistor value to V_{CC}.

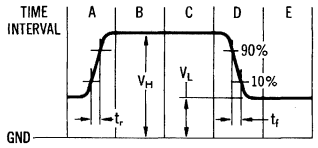
† = I_{A80} is symbol for MC779P

‡ = I_{A10} is symbol for MC779P

= I_{A16} is symbol for MC779P

Pin 8 = LOW } Set by a momentary ground prior to the application
** Pin 9 = LOW } of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.

E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

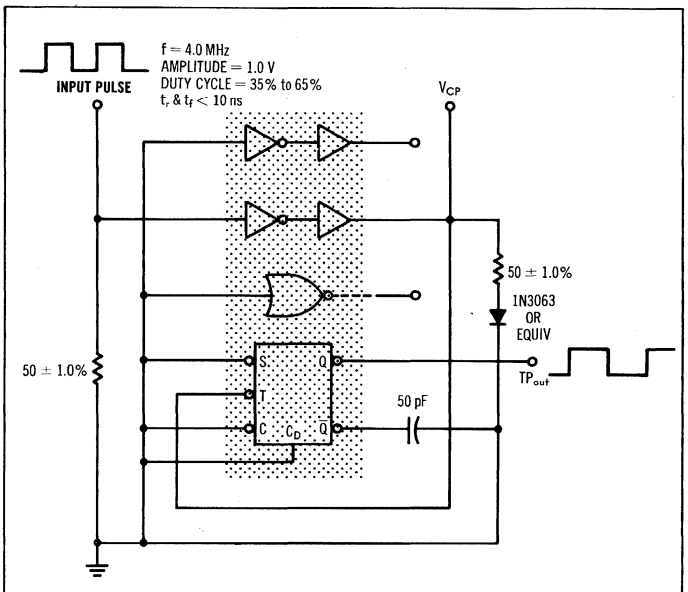
MC879P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+0.790 V ± 2.0 mV

MC779P

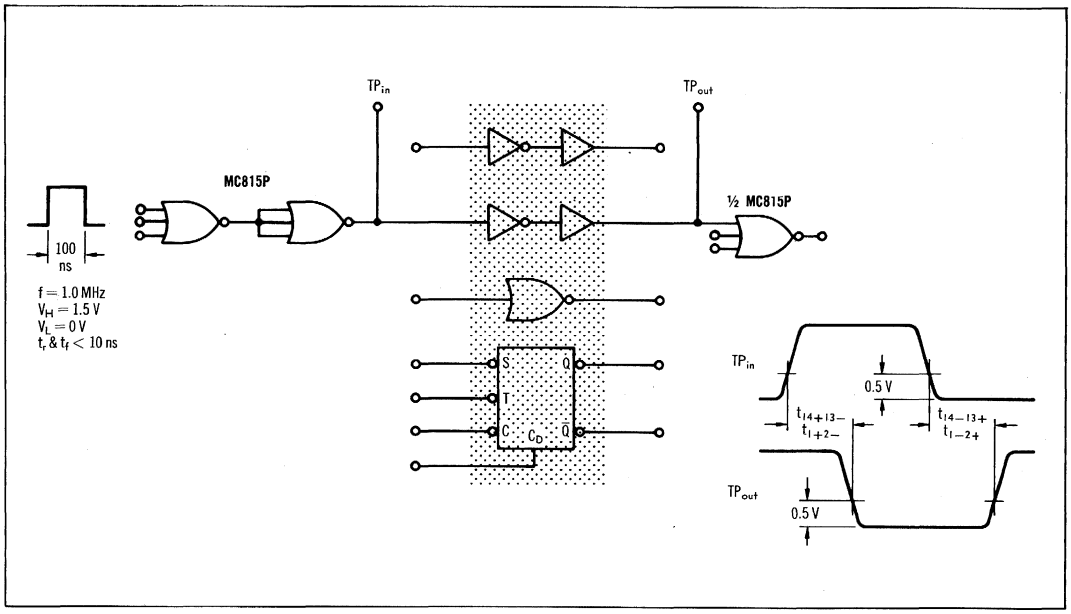
T_A	V_L	V_H
+ 25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+ 15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

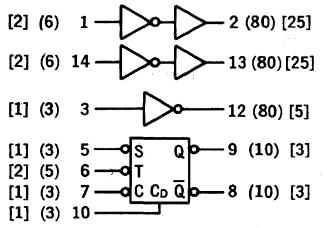


MULTIFUNCTION DEVICES

(1 J-K Flip-Flop, 1 Inverter, 2 Buffers)

MC787P • MC887P

A medium-power monolithic device consisting of one J-K flip-flop, one inverter, and two buffer circuits in a single package. This J-K flip-flop can be operated in the toggling mode. Simultaneous logic ONE pulses applied to the SET and CLEAR terminals cause the output state to reverse. A direct clear input allows asynchronous entry for pre-clearing counters, inserting parallel data into registers, and other similar applications. The inverter is a basic MRTL gate and the buffers are high fan-out gates with single inputs.



$2 = \overline{1}$

$12 = \overline{3}$

CLOCKED INPUT OPERATION ①

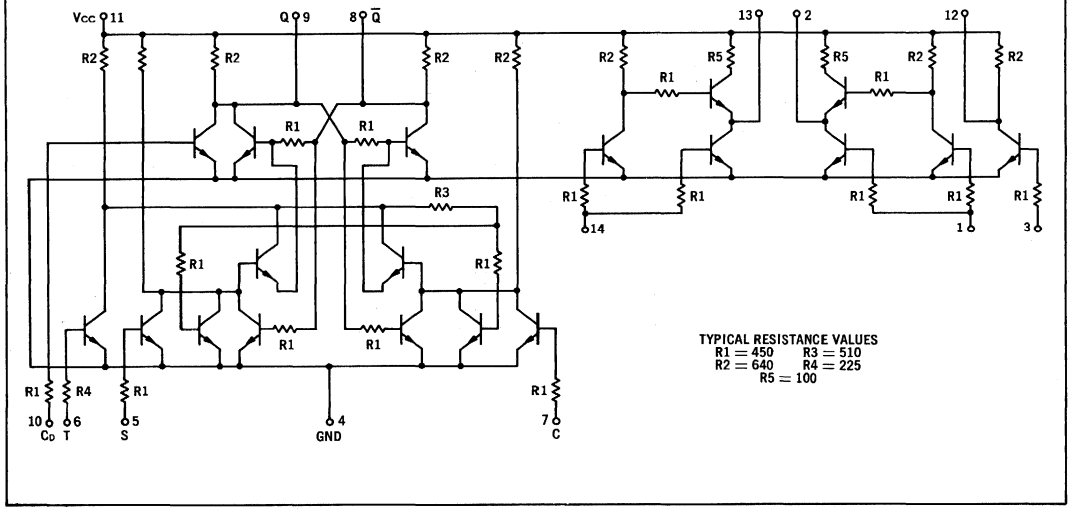
t_n②		t_{n+1}②	
S	C	Q	$\overline{Q}$
1	1	Q_n③	$\overline{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_n$	Q_n③

	f_{TOG} MHz	t_{pd} ns	P_D (mW) (Input High)	P_D (mW) (Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC787P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC887P



TYPICAL RESISTANCE VALUES
R1 = 450 R3 = 510
R2 = 640 R4 = 225
R5 = 100

ELECTRICAL CHARACTERISTICS

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	(Ohms) V_R*
MC887P	0°C	0.960	0.930	1.80	0.570	3.60	640
MC887P	+25°C	0.910	0.880	1.80	0.500	3.60	640
MC887P	+75°C	0.820	0.790	1.80	0.450	3.60	750
MC787P	+15°C	0.865	0.865	1.80	0.475	3.60	640
MC787P	+25°C	0.850	0.850	1.80	0.460	3.60	640
MC787P	+55°C	0.800	0.800	1.80	0.430	3.60	640

Characteristic	Symbol	Pin Under Test	MC887P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC787P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	V_R*	Gnd
Input Current	$2I_{in}$	1	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	1	-	-	-	11	2	3,4,5,6,7,10,14
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	-	-		-	1,4,5,6,7,10,14
	I_{in}	5	-	600	-	600	-	570		-	500	-	500	-	470		5	-	8	-		-	1,3,4,14
	$2I_{in}$	6	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		6	-	5,7	-		-	
	I_{in}	7	-	600	-	600	-	570		-	500	-	500	-	470		7	-	9	-		-	
	I_{in}	10	-	600	-	600	-	570		-	500	-	500	-	470		10	-	8	-		-	
	$2I_{in}$	14	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		14	-	-	-		13	1,3,4,5,6,7,10
Output Current	I_{AB}†	2	15.0	-	15.0	-	14.25	-	mAdc	13.50	-	13.75	-	12.50	-	mAdc	-	2	-	1	11	-	3,4,5,6,7,10,14
	I_{A3}‡	8	1.8	-	1.8	-	1.71	-		1.65	-	1.65	-	1.56	-		-	8	5,10	-		-	1,3,4,14
	I_{A3}‡	8		-		-		-			-		-		-		-	8,10	5	-		-	
	I_{A3}‡	9##		-		-		-			-		-		-		-	9	7	10		-	
	I_{A5}#	12	3.0	-	3.0	-	2.85	-		2.65	-	2.65	-	2.50	-		-	12	-	3		-	1,4,5,6,7,10,14
	I_{AB}†	13	15.0	-	15.0	-	14.25	-		13.50	-	13.75	-	12.50	-		-	13	-	14		-	1,3,4,5,6,7,10
Output Voltage	V_{out}	2	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	1	-	-	11	2	3,4,5,6,7,10,14
		8Δ##	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		8Δ**	-		-		-			-		-		-			-	5	-	7		-	
		8Δ**	-		-		-			-		-		-			-	-	-	5,7		-	
		9	-		-		-			-		-		-			-	10	-	-		-	1,3,4,8,14
		9Δ**	-		-		-			-		-		-			-	5,7	-	-		-	1,3,4,10,14
		9Δ##	-		-		-			-		-		-			-	7	-	5		-	
		9Δ##	-		-		-			-		-		-			-	-	-	5,7		-	
		12	-		-		-			-		-		-			-	3	-	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	14	-	-		13	1,3,4,5,6,7,10
Saturation Voltage	$V_{CE(sat)}$	2	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1	-	11	2	3,4,5,6,7,10,14
		8##	-		-		-			-		-		-			-	-	-	10		-	1,3,4,14
		9	-		-		-			-		-		-			-	-	10	-		-	1,3,4,8,14
		9**	-		-		-			-		-		-			-	-	-	-		-	1,3,4,14
		12	-		-		-			-		-		-			-	—	3	-		-	1,4,5,6,7,10,14
		13	-		-		-			-		-		-			-	-	14	-		13	1,3,4,5,6,7,10
																	Pulse In	Pulse Out					
Switching Time	t	1+2-	-	-	-	30	-	-	ns	-	-	-	30	-	-	ns	1	2	-	-	11	-	3,4,14
		1-2+	-	-	-	45	-	-		-	-	-	45	-	-		1	2	-	-		-	3,4,14
		14+13-	-	-	-	30	-	-		-	-	-	30	-	-		14	13	-	-		-	1,3,4
		14-13+	-	-	-	45	-	-		-	-	-	45	-	-		14	13	-	-		-	1,3,4

Pins not listed are left open.

Δ = Clock Pulse to pin 6, see Figure 1.

* Resistor value to V_{CC}.

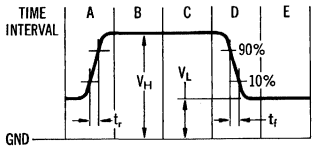
† = I_{A80} is symbol for MC787P

‡ = I_{A10} is symbol for MC787P

\# = I_{A16} is symbol for MC787P

Pin 8 = LOW } Set by a momentary ground prior to the application of the negative-going clock pulse.
** Pin 9 = LOW }

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

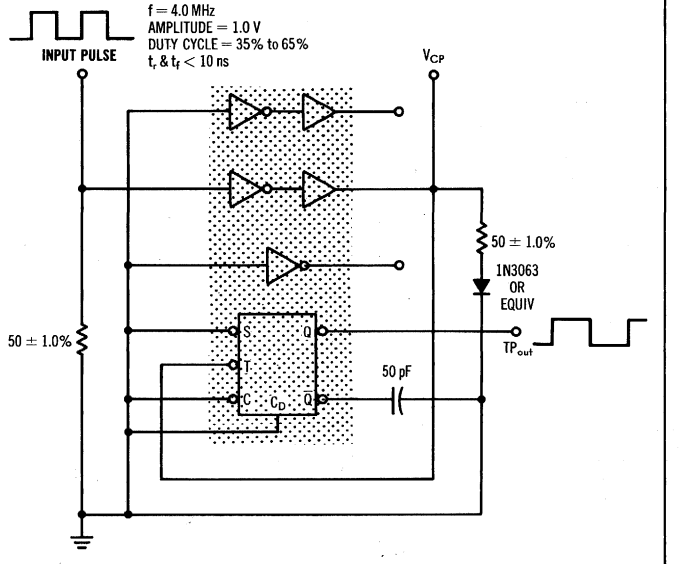
MC887P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.790 V ± 2.0 mV

MC787P

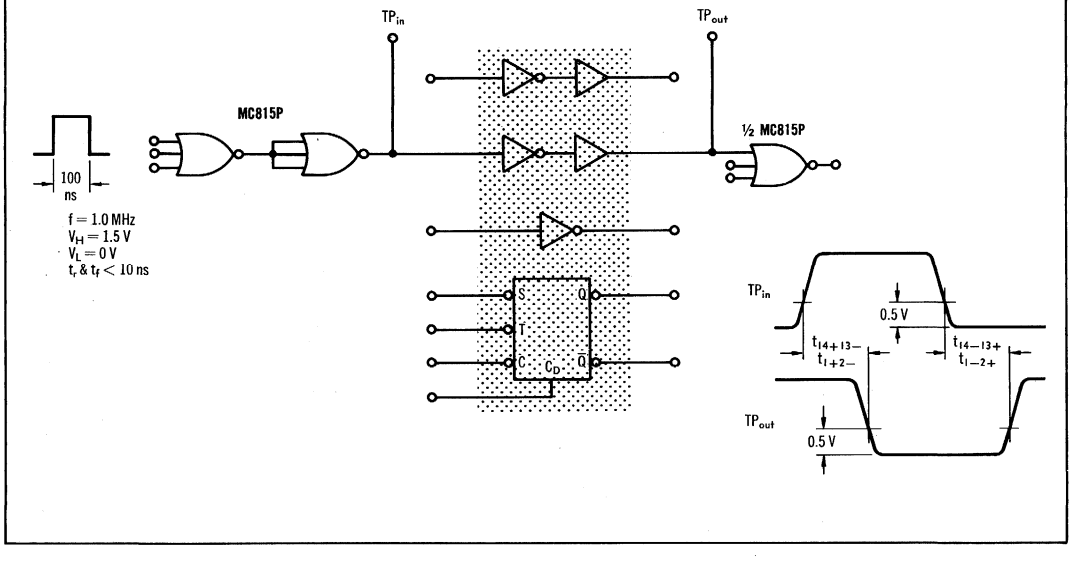
T_A	V_L	V_H
+ 25°C	−0.460 V ± 2.0 mV	−0.900 V ± 2.0 mV
+ 15°C	+0.475 V ± 2.0 mV	+0.915 V ± 2.0 mV
+ 55°C	+0.430 V ± 2.0 mV	+0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT

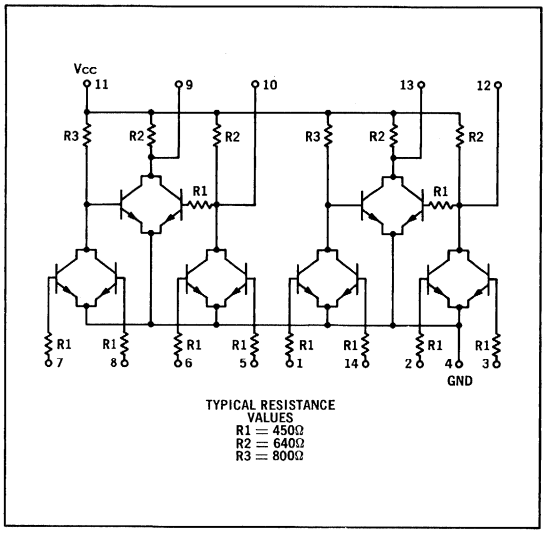


TP_{out} SHOULD HAVE A FREQUENCY OF ½ V_{CP} (2.0 MHz) WHEN THE DUTY CYCLE IS VARIED FROM 35% to 65%.

FIGURE 3 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

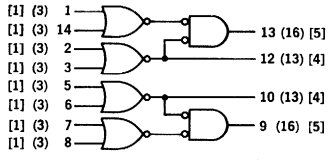


MC775P • MC875P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-adder devices in a single package. Each device can be used to supply the SUM and CARRY operations on two input signals. E g.,if the inputs are applied to pins 1 and 14, and their complements to pins 2 and 3, the SUM of the inputs appears on pin 13 while the CARRY appears on pin 12.

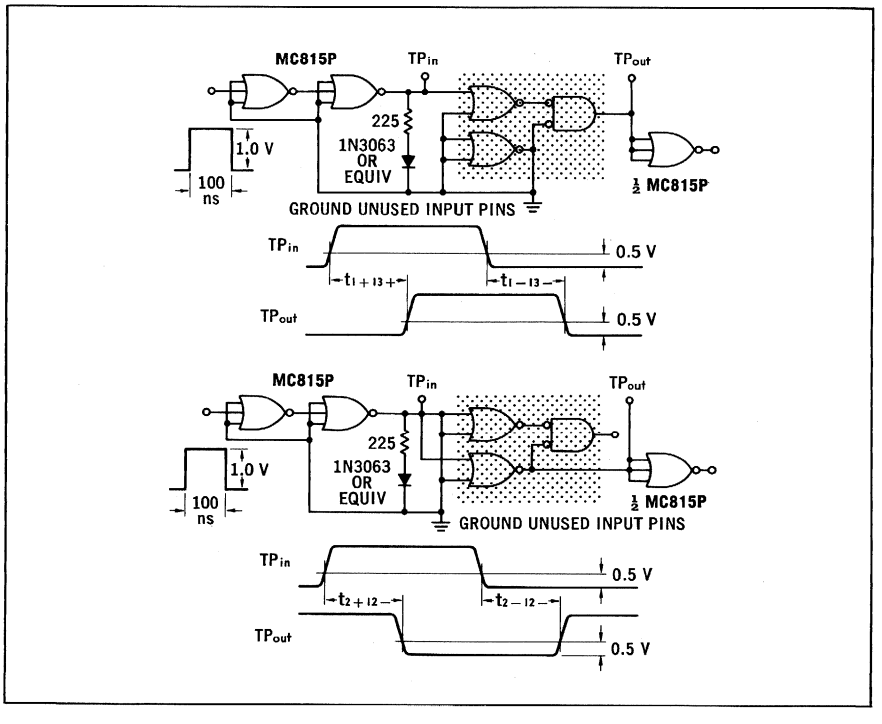


IF: $2 = \overline{1}$, & $3 = \overline{14}$
THEN: $12 = 1 \cdot 14$, & $13 = 1 \cdot \overline{14} + \overline{1} \cdot 14$

t_{pd} = 20 ns typ
P_D = 120 mW typ

NUMBER IN PARENTHESIS INDICATES MC775P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC875P LOADING FACTOR.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-adder only.
The other half-adder is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC875P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC775P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC875P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC775P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	14	-	11	4
		2	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	2	-	3	-	↓	↓
		3	-		-		-			-		-		-			3	-	2	-		
		14	-		-		-			-		-		-			14	-	14	-		
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	-	-	-	-	-	-	-	-	12	-	2, 3	11	4
	I_{A5}†	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	1, 2, 13	-	-	↓	↓
	I_{A5}†	13	3.0	-	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	mAdc	-	3,13,14	-	-	↓	↓
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2	-	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	↓	↓
		13	-		-		-			-		-		-			-	12	1, 13	-		
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	2	-	11	4
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	3	-	↓	↓
		13	-		-		-			-		-		-			-	-	1, 14	2, 3		
		13	-		-		-			-		-		-			-	-	2, 3	1, 14		
Switching Time	t																Pulse In	Pulse Out				
		2+12-	-	-	-	20	-	-	ns	-	-	-	20	-	-	ns	2	12	-	-	11	4
		2-12+	-	-	-	30	-	-	↓	-	-	-	30	-	-	↓	2	12	-	-	↓	4
		1+13+	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12
		1-13-	-	-	-	36	-	-		-	-	-	36	-	-		1	13	-	-		4, 12

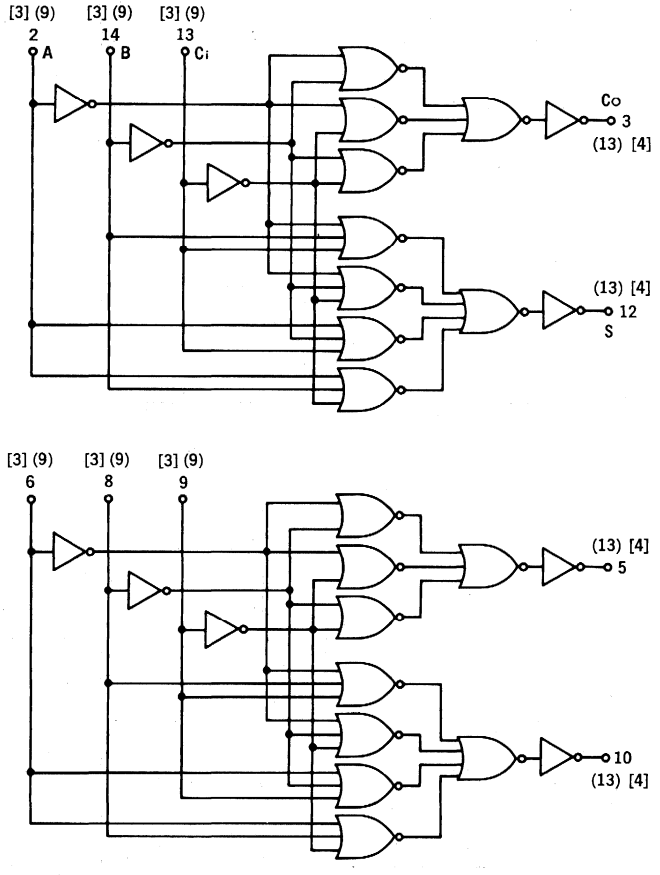
Ground inputs of half-adder not under test. Other pins not listed are left open.

* I_{AB} is symbol for MC775

† I_{A16} is symbol for MC775

MC796P • MC896P

Provides the SUM and CARRY functions while requiring only the AUGEND (A) and ADDEND (B) inputs with CARRY IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

POSITIVE LOGIC

$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + A\overline{B}\overline{C_i} + \overline{A}\overline{B}C_i + \overline{A}B\overline{C_i}$

$t_{pd} = 60$ ns typ

$P_D = 84$ mW typ

NUMBER IN PARENTHESIS INDICATES M796P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC896P LOADING FACTOR.

ELECTRICAL CHARACTERISTICS

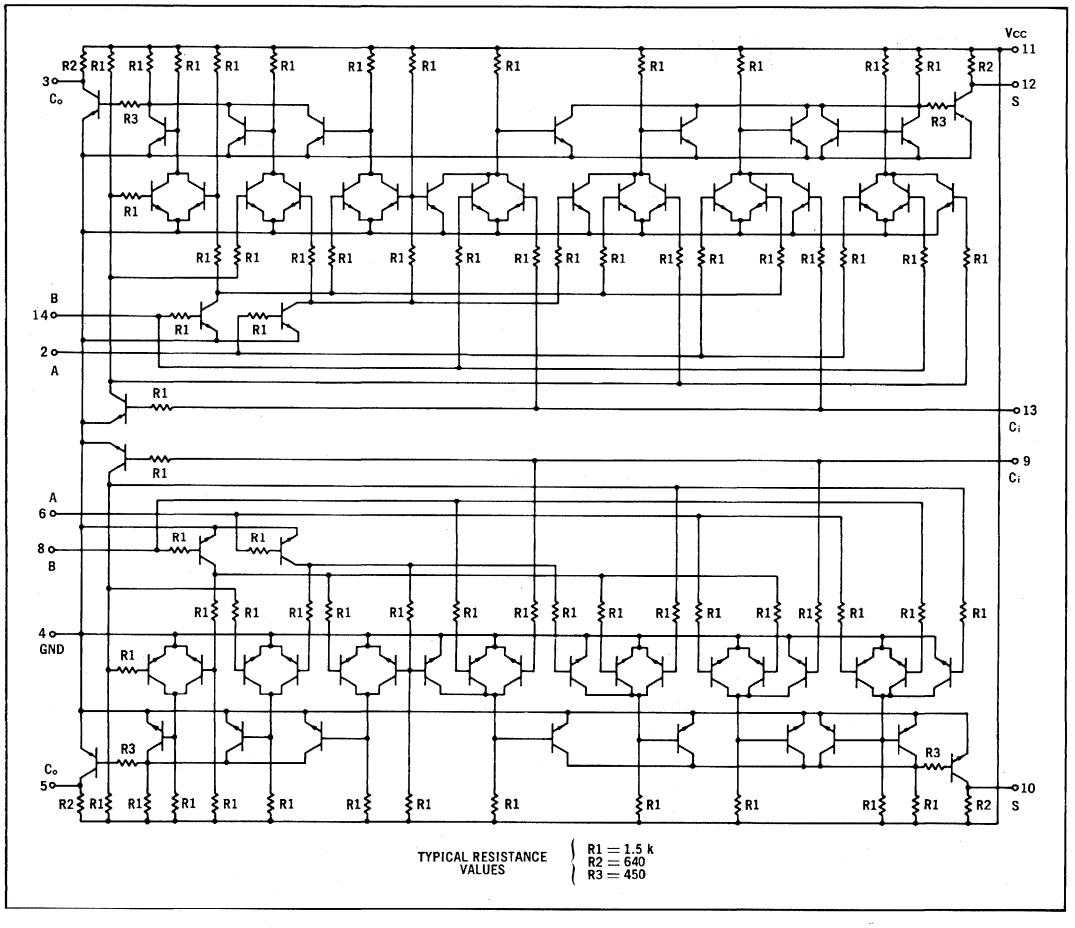
Test procedures are shown for one full adder only.
The other full adder is tested in the same manner.

	@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC896P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC796P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

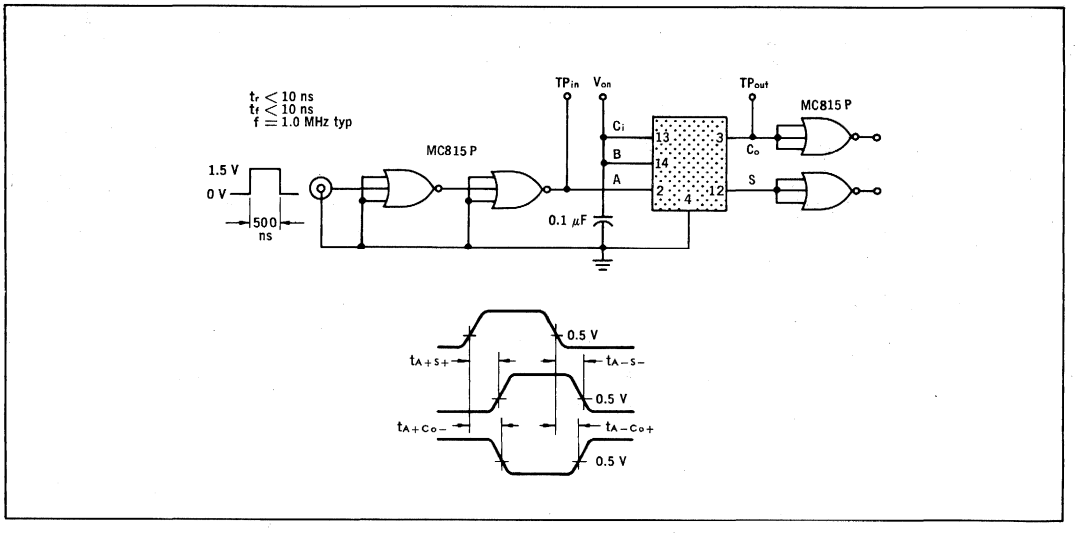
Characteristic	Symbol	Pin Under Test	MC896P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC796P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1800	-	1800	-	1710	μAdc	-	1500	-	1500	-	1410	μAdc	2	-	-	-	11	4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	-	-	↓	↓
		14	-		-		-			-		-		-			14	-	-	-		
Output Current	I_{A4}*	3	2.40	-	2.40	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	3,13,14	-	2	11	4
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	2,3,13	-	14	↓	↓
				-		-		-			-		-		-		-	2,3,14	-	13		
				-		-		-			-		-		-		-	(2,3,) (13,14)	-	-		
		12		-		-		-			-		-		-		-	12,13	-	2,14		
				-		-		-			-		-		-		-	12,14	-	2,13		
				-		-		-			-		-		-		-	2,12	-	13,14		
				-		-		-			-		-		-		-	(2,12,) (13,14)	-	-		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	-	-	2,13,14	11	4
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	13	-	2,14	↓	↓
			-		-		-			-		-		-			-	14	-	2,13		
			-		-		-			-		-		-			-	2	-	13,14		
		12	-		-		-			-		-		-			-	-	-	2,13,14		
			-		-		-			-		-		-			-	13,14	-	2		
			-		-		-			-		-		-			-	2,14	-	13		
			-		-		-			-		-		-			-	2,14	-	13		
Switching Time																	Pulse In		Pulse Out			
	t	2+12+	-	-	-	75	-	-	ns	-	-	-	75	-	-	ns	2	13,14	12	-	11	4
		2-12-	-	-	-	75	-	-	↓	-	-	-	75	-	-	↓	↓	-	12	-	↓	↓
		2+3+	-	-	-	85	-	-		-	-	-	85	-	-			13	3	14		
		2-3-	-	-	-	65	-	-		-	-	-	65	-	-		↓	13	3	14		
		14+12+	-	-	-	75	-	-		-	-	-	75	-	-		14	-	12	2,13		
		14-12-	-	-	-	75	-	-		-	-	-	75	-	-		↓	-	12	2,13		
		14+3+	-	-	-	85	-	-		-	-	-	85	-	-			13	3	2		
		14-3-	-	-	-	65	-	-		-	-	-	65	-	-			13	3	↓		
		13+12-	-	-	-	70	-	-		-	-	-	70	-	-		13	14	12			
		13-12+	-	-	-	80	-	-		-	-	-	80	-	-		↓	↓	12			
		13+3+	-	-	-	70	-	-		-	-	-	70	-	-				3			
		13-3-	-	-	-	80	-	-	↓	-	-	-	80	-	-	↓	↓	↓	3	↓	↓	↓

* Symbol is I_{A13} for MC796P.

Ground inputs of full adder not under test.
Other pins not listed are left open.

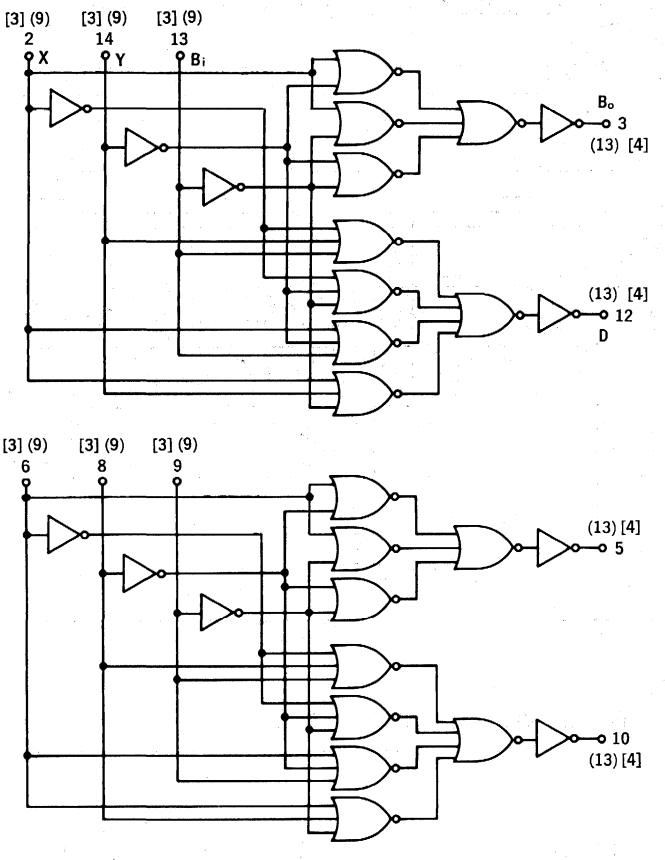


SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



MC797P • MC897P

Provides the DIFFERENCE and BORROW functions while requiring only MINUEND (X) and SUBTRAHEND (Y) inputs with BORROW IN.



TRUTH TABLE				
INPUT LOGIC LEVEL			OUTPUT LOGIC LEVEL	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

POSITIVE LOGIC

$D = YXB_i + Y\bar{X}\bar{B}_i + \bar{Y}X\bar{B}_i + \bar{Y}\bar{X}B_i$

$B_o = \bar{Y}\bar{X}B_i + Y\bar{X}\bar{B}_i + \bar{Y}\bar{X}B_i + YXB_i$

$t_{pd} = 60$ ns typ

$P_D = 84$ mW typ

NUMBER IN PARENTHESIS INDICATES MC797P LOADING FACTOR.

NUMBER IN BRACKETS INDICATES MC897P LOADING FACTOR.

ELECTRICAL CHARACTERISTICS

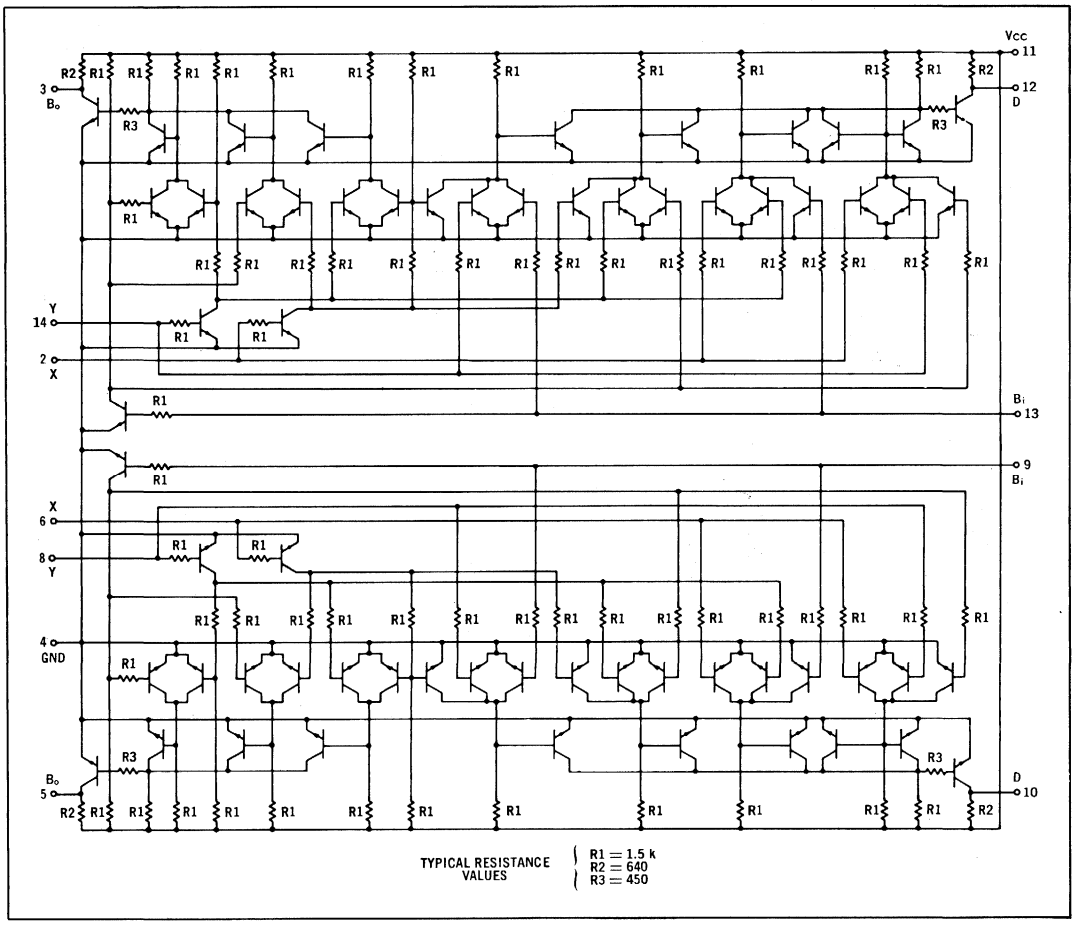
Test procedures are given for only one subtractor.
The other subtractor is tested in the same manner.

@Test Temperature		TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC897P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.800	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC797P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

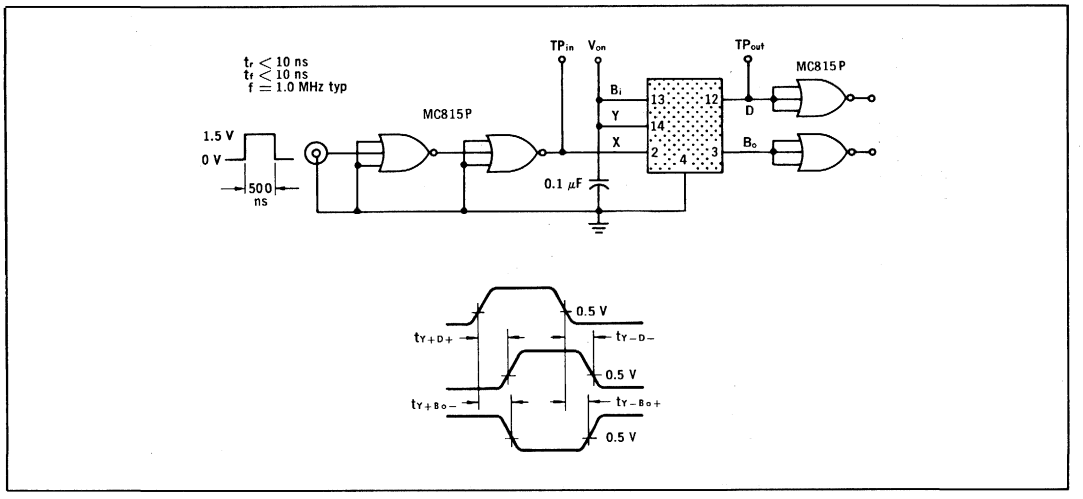
Characteristic	Symbol	Pin Under Test	MC897P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC797P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$3\ I_{in}$	2	-	1800	-	1800	-	1710	μAdc	-	1500	-	1500	-	1410	μAdc	2	-	-	-	11	4
		3	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	13	-	-	-	↓	↓
		14	-		-		-			-		-		-			14	-	-	-		
Output Current	I_{A4}*	3	2.40	-	2.40	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2,3, 13,14	-	-	11	4
		↓	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	3,13	-	2,14	↓	↓
				-		-		-			-		-		-		-	3,14	-	2,13		
		12		-		-		-			-		-		-		-	12,13	-	2,14		
		↓		-		-		-			-		-		-		-	12,14	-	2,13		
				-		-		-			-		-		-		-	2,12	-	13,14		
				-		-		-			-		-		-		-	2,12, 13,14	-	-		
Output Voltage	V_{out}	3	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	2,13	-	14	11	4
		↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,14	-	13	↓	↓
			-		-		-			-		-		-			-	-	-	2,13,14		
		12	-		-		-			-		-		-			-	-	-	2,13,14		
		↓	-		-		-			-		-		-			-	13,14	-	2		
			-		-		-			-		-		-			-	2,14	-	13		
			-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2,13	-	14	↓	↓
Switching Time																	Pulse In		Pulse Out			
	t	2+12+	-	-	-	60	-	-	ns	-	-	-	60	-	-	ns	2	13,14	12	-	11	4
		2-12-	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	12	-	↓	↓
		2+3+	-	-	-	65	-	-		-	-	-	65	-	-				3	-		
		2-3-	-	-	-	60	-	-		-	-	-	60	-	-				3	-		
		14+12+	-	-	-	↓	-	-		-	-	-	↓	-	-		14	-	12	2,13		
		14-12-	-	-	-		-	-		-	-	-		-	-		↓	-	12	2,13		
		14+3-	-	-	-	65	-	-		-	-	-	65	-	-			13	3	2		
		14-3+	-	-	-	60	-	-		-	-	-	60	-	-		↓	↓	3	↓		
		13+12-	-	-	-	↓	-	-		-	-	-	↓	-	-		13		12			
		13-12+	-	-	-		-	-		-	-	-		-	-			↓	12			
		13+3+	-	-	-		-	-		-	-	-		-	-		↓	2,14	3	-		
		13-3-	-	-	-	↓	-	-	↓	-	-	-	↓	-	-	↓	↓	2,14	3	-	↓	↓

* Symbol for MC797P is I_{A13}.

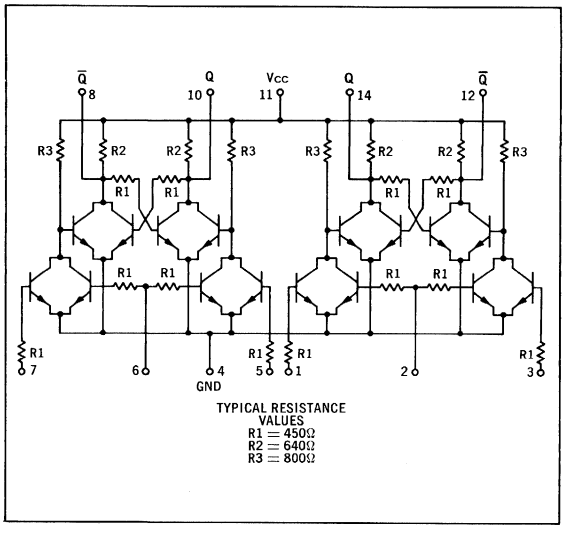
Ground input pins of subtractor not under test.
Other pins not listed are left open.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

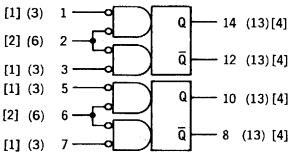


MC784P • MC884P



TYPICAL RESISTANCE VALUES
R1 = 450Ω
R2 = 640Ω
R3 = 800Ω

Two half-shift registers in a single package. Each is a bistable storage element. Eg., information coming in on pins 1 and 3 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 14 and 12, will both be low.

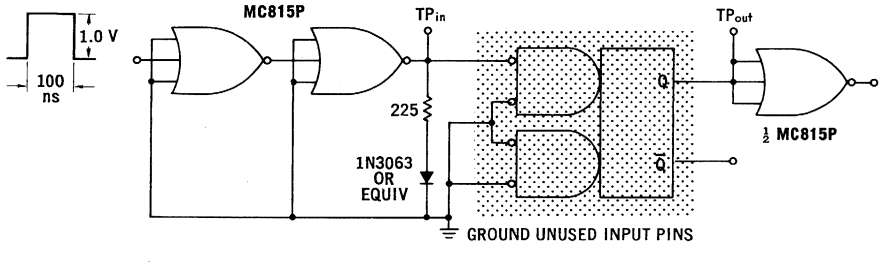


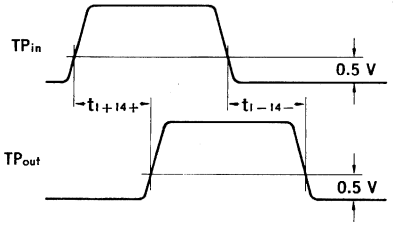
NUMBER IN PARENTHESIS INDICATES MC784P LOADING FACTOR

NUMBER IN BRACKETS INDICATES MC884P LOADING FACTOR

t_{pd} = 22 ns typ
P_D = 120 mW typ

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

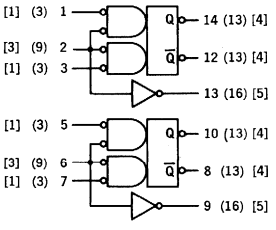
	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC884P	0°C	0.960	0.930	1.80	0.570	3.60
MC884P	+25°C	0.910	0.880	1.80	0.500	3.60
MC884P	+75°C	0.820	0.790	1.80	0.450	3.60
MC784P	+15°C	0.865	0.865	1.80	0.475	3.60
MC784P	+25°C	0.850	0.850	1.80	0.460	3.60
MC784P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC884P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC784P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$2I_{in}$	2	-	1200	-	1200	-	1140		-	1000	-	1000	-	940		2	-	1, 3	-		
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	2	-		
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
		12		-		-		-			-		-		-		-	3, 12	-	-		4
		14		-		-		-			-		-		-		-	2, 14	-	-		4, 12†
		14		-		-		-			-		-		-		-	1, 14	-	-		4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		14	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	12	1, 2	-	11	4
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-		-		-			-		-		-			-	-	-	2, 3		4, 14
		14	-		-		-			-		-		-			-	-	1, 2, 3	-		4, 14†
		14	-		-		-			-		-		-			-	-	-	1, 2		4
Switching Time	t	1+14+	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 1	Pulse Out 14	-	-	11	4, 12
		1-14-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	1	14	-	-	11	4, 12

Ground input pins of half-register not under test. Other pins not listed are left open. † Silicon diode to ground. * Symbol is I_{A13} for the MC784P.

MC783P • MC883P

Dual half-shift registers each with built-in inverter, in a single package. Information coming in on pins 1 and 2 will be transferred to pins 14 and 12 when the gating signal, pin 2, goes low. If all three inputs, 1, 2, and 3, are low, the outputs, 12 and 14, will both be low.

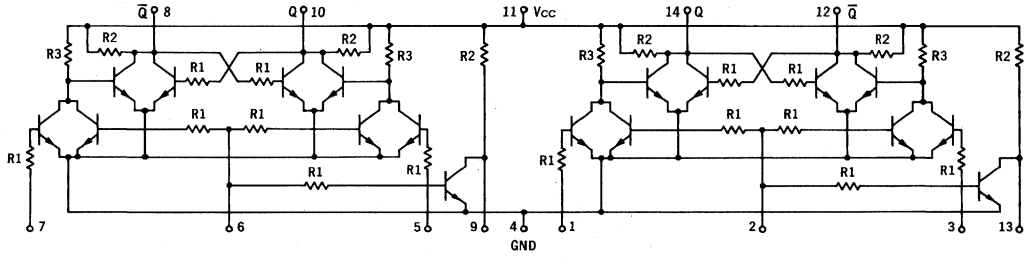


$14 = \overline{12}\ (1 + 2)$
$12 = \overline{14}\ (3 + 2)$

t_{pd} = 22 ns typ
P_D = 140 mW typ

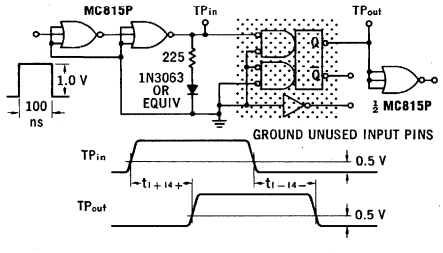
NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC783P

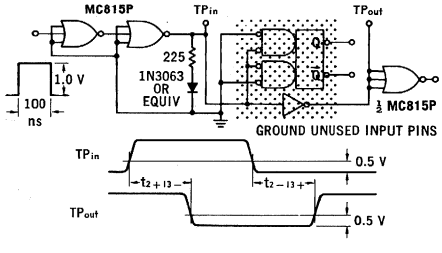
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC883P



TYPICAL RESISTANCE VALUES
R1 = 450 Ω
R2 = 640 Ω
R3 = 800 Ω

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half-shift register only.
The other half-shift register is tested in the same manner.

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC883P	0°C	0.960	0.930	1.80	0.570	3.60
MC883P	+25°C	0.910	0.880	1.80	0.500	3.60
MC883P	+75°C	0.820	0.790	1.80	0.450	3.60
MC783P	+15°C	0.865	0.865	1.80	0.475	3.60
MC783P	+25°C	0.850	0.850	1.80	0.460	3.60
MC783P	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC883P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC783P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	I_{in}	1	-	600	-	600	-	570	μAdc	-	500	-	500	-	470	μAdc	1	-	2	-	11	4
	$3I_{in}$	2	-	1800	-	1800	-	1710	↓	-	1500	-	1500	-	1410	↓	2	-	1, 3	-	↓	↓
	I_{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	2	-	↓	↓
Output Current	I_{A4}*	12	2.4	-	2.4	-	2.28	-	mAdc	2.15	-	2.15	-	2.03	-	mAdc	-	2, 12	-	-	11	4, 14†
	I_{A4}*	12	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	3, 12	-	-	↓	4
	I_{A5}**	13	3.0	—	3.0	-	2.85	-	↓	2.65	-	2.65	-	2.5	-	↓	-	13	-	2	↓	4
	I_{A4}*	14	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	2, 14	-	-	↓	4, 12†
	I_{A4}*	14	2.4	-	2.4	-	2.28	-	↓	2.15	-	2.15	-	2.03	-	↓	-	1, 14	-	-	↓	4
Output Voltage	V_{out}	12	-	500	-	400	-	400	mVdc	-	400	-	300	-	320	mVdc	-	14	2, 3	-	11	4
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	2	-	-	↓	↓
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	12	1, 2	-	↓	↓
Saturation Voltage	$V_{CE(sat)}$	12	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	-	1, 2, 3	-	11	4, 12†
		12	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	2, 3	↓	4, 14
		13	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	2	-	↓	4
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	1, 2, 3	-	↓	4, 14†
		14	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 2	↓	4, 12
Switching Time	t	2+13-	-	-	-	40	-	-	ns	-	-	-	40	-	-	ns	Pulse In 2	Pulse Out 13	-	-	11	4
		2-13+	-	-	-	40	-	-	↓	-	-	-	40	-	-	↓	2	13	-	-	↓	4
		1+14+	-	-	-	28	-	-	↓	-	-	-	28	-	-	↓	1	14	-	-	↓	4, 12
		1-14-	-	-	-	24	-	-	↓	-	-	-	24	-	-	↓	1	14	-	-	↓	4, 12

Ground input pins of half-shift register not under test. Other pins not listed are left open. * Symbol is I_{A13} for MC783P. ** Symbol is I_{A16} for MC783P †Silicon diode to ground.

ADDITIONS AND MODIFICATIONS

COMMERCIAL

MRTL

INTEGRATED CIRCUITS

LOW-POWER
AND
MEDIUM-POWER

MC700 SERIES

MILLIWATT AND MEDIUM-POWER

COMMERCIAL MRTL

INTEGRATED CIRCUITS

INDEX

In this series of MRTL logic circuits, medium and low-power devices are combined and specified for compatible application in commercial usages. Medium-power devices have loading factors normalized for compatibility with low-power for ease of mixing the two power levels in a system.

INDEX

	Page No.
General Information	6-246
Summary of Devices Available in Metal Cans (G Suffix)	6-248
Summary of Devices Available in Flat Packages (F Suffix)	6-251

DEVICE		POWER	PACKAGE
GATES			
MC703	3-Input Gates	MRTL	F, G
MC707	4-Input Gates	MRTL	F, G
MC711	4-Input Gates	mW MRTL	F, G
MC728	5-Input Gates	mW MRTL	F, G
MC729	5-Input Gates	MRTL	F, G
MC710	Dual 2-Input Gates	mW MRTL	F, G
MC714	Dual 2-Input Gates	MRTL	F, G
MC715	Dual 3-Input Gates	MRTL	F, G
MC718	Dual 3-Input Gates	mW MRTL	F, G
MC719	Dual 4-Input Gate	mW MRTL	F
MC725	Dual 4-Input Gate	MRTL	F
MC792	Triple 3-Input Gate	MRTL	F
MC793	Triple 3-Input Gate	mW MRTL	F
MC717	Quad 2-Input Gate	mW MRTL	F
MC724	Quad 2-Input Gate	MRTL	F
BUFFERS			
MC700	Buffers	MRTL	F, G
MC709	Buffers	mW MRTL	F, G
MC781	Dual Buffer	mW MRTL	G
MC799	Dual Buffers	MRTL	F, G
MC798	Dual 2-Input Buffer	mW MRTL	F
MC788	Dual 3-Input Buffer	MRTL	F
INVERTERS			
MC727	Quad Inverters	MRTL	F, G
MC789	Hex Inverter	MRTL	F
EXPANDERS			
MC721	Dual 2-Input Expanders	mW MRTL	F, G
MC786	Dual 4-Input Expander	MRTL	F
MC785	Quad 2-Input Expander	MRTL	F

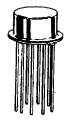
DEVICE		POWER	PACKAGE
COUNTER ADAPTERS			
MC701	Counter Adapter	MRTL	G
ADDERS			
MC704	Half Adders	MRTL	F, G
MC708	Half Adders	mW MRTL	F, G
MC712	Half Adders	mW MRTL	F, G
MC775	Dual Half Adder	MRTL	F
HALF-SHIFT REGISTERS			
MC705	Half-Shift Registers with Inverter	MRTL	F, G
MC706	Half-Shift Registers without Inverter	MRTL	F, G
MC783	Dual Half-Shift Register with Inverter	MRTL	F
MC784	Dual Half-Shift Register without Inverter	MRTL	F
FLIP-FLOPS			
MC702	R-S Flip-Flop	MRTL	G
MC720	J-K Flip-Flops	mW MRTL	F, G
MC722	J-K Flip-Flops	mW MRTL	F, G
MC723	J-K Flip-Flops	MRTL	F, G
MC726	J-K Flip-Flops	MRTL	F, G
MC774	J-K Flip-Flop	MRTL	G
MC782	J-K Flip-Flop	mW MRTL	G
MC776	Dual J-K Flip-Flop	mW MRTL	F
MC790	Dual J-K Flip-Flop	MRTL	F
MC791	Dual J-K Flip-Flop	MRTL	F
MC713	Type D Flip-Flops	mW MRTL	F, G
MC778	Dual Type D Flip-Flop	mW MRTL	F

NUMERICAL INDEX
(Functions and Characteristics)

V_{CC} = 3.6 V ±10%, T_A = 25°C

Function	Type ① +15 to +55°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
MRTL					
Buffer	MC700	72,96	80	20	25/50 ②
Counter Adapter	MC701	96	16	22	80
R-S Flip-Flop	MC702	96	13	14	32
3-Input NOR Gate	MC703	72,96	16	12	28/7.5 ②
Half Adder	MC704	72,96	16	14	65
Half-Shift Register	MC705	72,96	13	22	75
Half-Shift Register (w/o Inverter)	MC706	72,96	13	22	52
4-Input NOR Gate	MC707	72,96	16	12	30/7.5 ②
Dual 2-Input NOR Gate	MC714	72,96	16	12	50/15 ②
Dual 3-Input NOR Gate	MC715	72,96A	16	12	55/15 ②
J-K Flip-Flop	MC723	72,96	10	35	91/79 ④
Quad 2-Input NOR Gate	MC724	83	16	12	100/30 ②
Dual 4-Input NOR Gate	MC725	83	16	12	60/15 ②
J-K Flip-Flop	MC726	72,96A	16	35	100/86 ④
Quad Inverter	MC727	72,96A	16	12	87/30 ②
5-Input NOR Gate	MC729	72,96	16	12	33/7.5 ②
Quad Exclusive OR Gate	MC771	83	16	12	87
J-K Flip-Flop	MC774	96	16	35	100/86 ④
Dual Half Adder	MC775	83	16	20	120
Dual Half Shift Register	MC783	83	13	22	140
Dual Half Shift Register w/Inverter	MC784	83	13	22	100
Quad 2-Input Expander	MC785	83	–	12	20/ – ②
Dual 4-Input Expander	MC786	83	–	12	20/ – ②
Dual 3-Input Buffer, non-inverting	MC788	83	80	24	145/56 ②
Hex Inverter	MC789	83	16	12	130/15 ②
Dual J-K Flip-Flop	MC790	83	10	35	182/158 ④
Dual J-K Flip-Flop	MC791	83	16	40	190/160 ④
Triple 3-Input NOR Gate	MC792	83	16	12	82/24 ②
Dual Full Adder	MC796	83	13	60	84
Dual Full Subtractor	MC797	83	13	60	84
Dual Buffer	MC799	72,96A	80	20	50/100 ②
Hex Expander	MC9719	83	–	12	13/ – ②
mW MRTL					
Half Adder	MC708	72,96	4	60	19/12.5 ②
2-Input Buffer	MC709	72,96	30	57	7.0/23 ②
Dual 2-Input NOR Gate	MC710	72,96	4	27	10/2.5 ②
Dual 4-Input OR/NOR Gate	MC711	72,96	4	60	8.0/5.5 ②
Half Adder	MC712	72,96	4	66	15.5/10.5 ②
Type D Flip-Flop	MC713	72,96	3	75	24/17.5 ③
Quad 2-Input NOR Gate	MC717	83	4	27	20/5.0 ②
Dual 3-Input NOR Gate	MC718	72,96A	4	27	12/2.5 ②
Dual 4-Input NOR Gate	MC719	83	4	27	13/2.5 ②
J-K Flip-Flop	MC720	72,96	2	50	20.5/14.5 ④
Dual 2-Input Gate Expander	MC721	72,96	–	27	3.0/ – ②
J-K Flip-Flop	MC722	72,96A	4	70	24/20 ④
5-Input NOR Gate	MC728	72,96	4	27	7.5/1.0 ②
Dual J-K Flip-Flop	MC776	83	2	50	41/29 ④
Dual Type D Flip-Flop	MC778	83	3	60	48/35 ③
Dual Buffer	MC781	96	30	57	14/46 ②
J-K Flip-Flop	MC782	96	2	80	23/21 ④
Triple 3-Input NOR Gate	MC793	83	4	27	18/3.5 ②
Dual 2-Input Buffer	MC798	83	30	57	14/46 ②
Quad 2-Input Expander	MC9721	83	–	27	20/ – ②

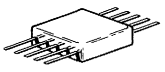
① G suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC718G = Metal Can, MC718F = Flat Package.
② Inputs High/Inputs Low.
③ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low
④ Only Clock Input High/Inputs Low



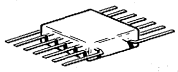
TO-99



TO-100

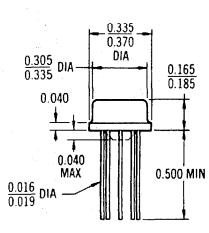


TO-91

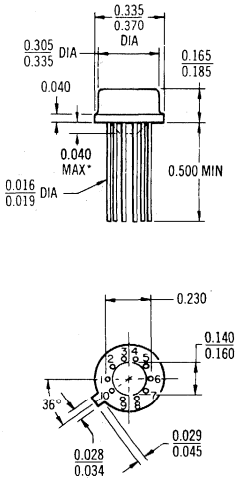


TO-86

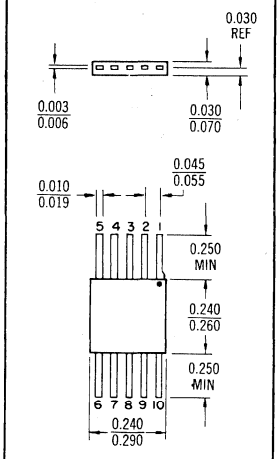
OUTLINE DIMENSIONS



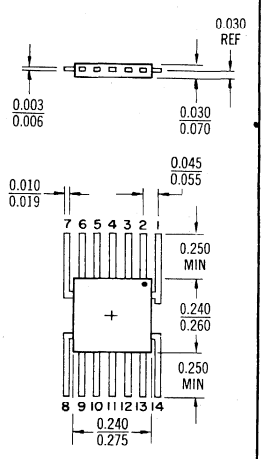
Pin 4 connected to case.



Pin 5 connected to case.



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TEST CONDITION TOLERANCES $V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_R = \pm 1\%$ $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

GENERAL RULES

- Testing tables shown in the MC900/800 MRTL and the MC908/808 mW MRTL sections of this volume may be utilized for testing MC700F and G commercial series devices. Pin number configurations are the same. MC700 series forcing functions and test limits are shown on page 6-247.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- For ease of mixing MRTL and mW MRTL in the same system, the loading factors are normalized in accordance with the input currents being driven.
- Any number of gates may be paralleled; the input loading is increased by 1/4 load if only one gate is connected to V_{CC}.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled, increasing the input loading factor by 2.33.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by two loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused input pins should be returned to ground.
- EXPANDER RULES:
  1. The MC785F, MC786F and MC9719F MRTL expanders can be used to expand medium-power MRTL output nodes only.
  2. When using the MC785F, MC786F or MC9719F subtract 0.5 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 1.33.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Logic Input Voltage		±4.0	Vdc
Power Supply Voltage (Pulsed ≤1 second)		+12	Vdc
Operating Temperature Range MC700G/F Series	T_A	+15 to +55	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Milliwatt MRTL			MRTL			Unit
	+15°C	+25°C	+55°C	+15°C	+25°C	+55°C	
I_{A3}	0.420	0.420	0.420	–	–	–	mAdc min
I_{A4}	0.570	0.570	0.570	–	–	–	mAdc min
I_{A10}	–	–	–	1.65	1.65	1.65	mAdc min
I_{A13}	–	–	–	2.15	2.15	2.03	mAdc min
I_{A16}	–	–	–	2.65	2.65	2.5	mAdc min
I_{AB}	5.0	5.0	5.0	13.5	13.75	12.5	mAdc min
I_{CEX}	50	50	100	225	225	250	μAdc max
I_{in}	0.150	0.150	0.150	0.500	0.500	0.470	mAdc max
2 I_{in}	0.300	0.300	0.300	1.0	1.0	0.94	mAdc max
V_{out}	0.400	0.300	0.320	0.400	0.300	0.320	Vdc max
V_{CE}	0.220	0.230	0.320	0.300	0.290	0.320	Vdc max
TEST CONDITIONS							
V_{BOT}	1.8	1.8	1.8	1.8	1.8	1.8	Vdc
V_{CC}	3.6	3.6	3.6	3.6	3.6	3.6	Vdc
V_{in}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_{off}	0.475	0.460	0.430	0.475	0.460	0.430	Vdc
V_{on}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_R*	4600	4800	5000	640	640	640	Ohms

*Resistor value to V_{CC}

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{on}.

I_{AB} Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} The maximum available current from the output of a Dual Gate.

I_{CEX} Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

1.8 I_{in} Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

2 I_{in} Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L Isolation leakage current.

I_O Output load current.

V_{BOT} A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} Supply voltage.

$V_{CE(sat)}$ Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} Minimum high level voltage applied to the input of a device.

V_{LL} A supply voltage low enough to allow flow of leakage currents only.

V_{off} The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} The maximum output voltage with V_{on} applied to the input.

V_R Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

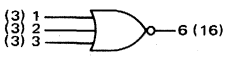
COMMERCIAL MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these pages describe the MC700 Series Commercial MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

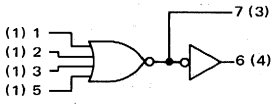
MC703G 3-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

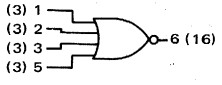
MC711G 4-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 3 + 5}$
$6 = 1 + 2 + 3 + 5$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

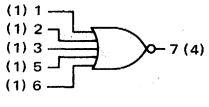
MC707G 4-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

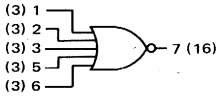
MC728G 5-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

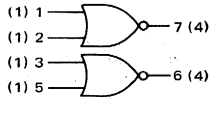
MC729G 5-Input Gate
(medium-power)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

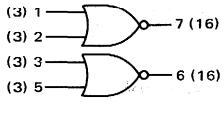
MC710G Dual 2-Input Gate
(milliwatt)



$7 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

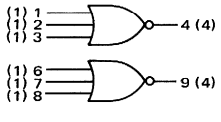
MC714G Dual 2-Input Gate
(medium-power)



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

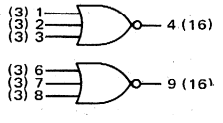
MC718G Dual 3-Input Gate
(milliwatt)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

MC715G Dual 3-Input Gate
(medium-power)

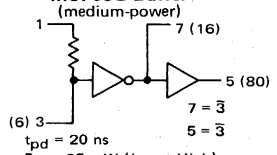


$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

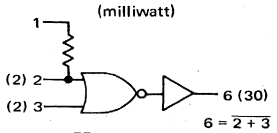
BUFFERS

MC700G Buffer
(medium-power)



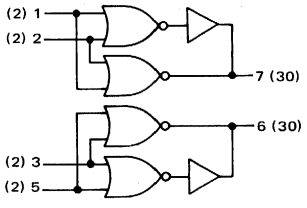
$7 = \overline{3}$
$5 = \overline{3}$
t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

MC709G Buffer
(milliwatt)



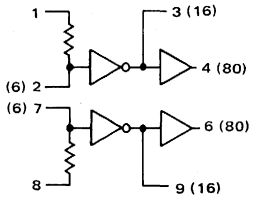
$6 = \overline{2 + 3}$
t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

MC781G Dual Buffer
(milliwatt)



$7 = \overline{1 + 2}$
t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

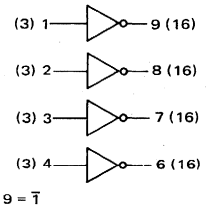
MC799G Dual Buffer
(medium-power)



$3 = \overline{2}$
$4 = \overline{2}$
t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

INVERTER

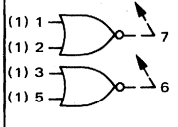
MC727G Quad Inverter
(medium-power)



$9 = \overline{1}$
t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

EXPANDER

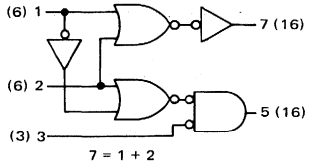
MC721G
Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

COUNTER ADAPTER

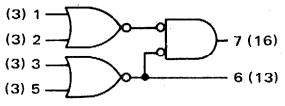
MC701G Counter Adapter
(medium-power)



$7 = 1 + 2$
$5 = (\overline{1} + 2)\,\overline{3}$
t_{pd} = 22 ns
P_D = 80 mW

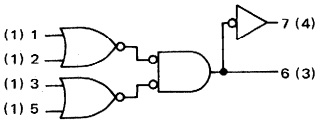
HALF ADDERS

MC704G Half Adder
(medium-power)



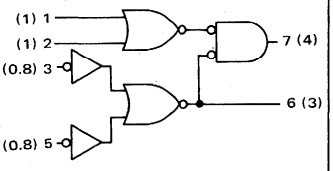
IF: $3 = \overline{1}$, & $5 = \overline{2}$
THEN: $6 = 1 \cdot 2$
$7 = 1 \cdot \overline{2} + \overline{1} \cdot 2$
$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{3 + 5}$
t_{pd} = 14 ns
P_D = 65 mW

MC712G Half Adder
(milliwatt)



$7 = (1 + 2)\,(3 + 5)$
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$
t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

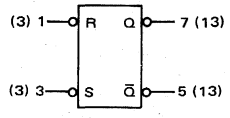
MC708G Half Adder
(milliwatt)



$7 = (\overline{\overline{3} + \overline{5}})$
$6 = (1 + 2)\,(\overline{3} + \overline{5})$
t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

FLIP-FLOPS

MC702G R-S Flip-Flop
(medium-power)



t_{pd} = 14 ns
P_D = 32 mW

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

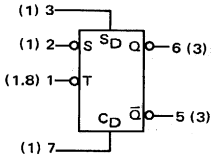
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC713G Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

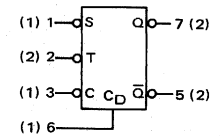
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

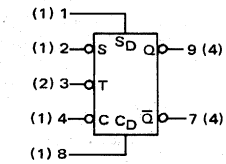
1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

MC720G J-K Flip-Flop
(milliwatt)



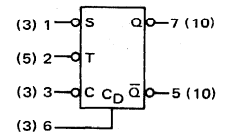
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722G J-K Flip-Flop
(milliwatt)



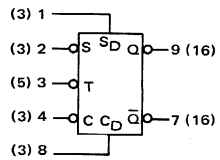
t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC723G J-K Flip-Flop
(medium-power)



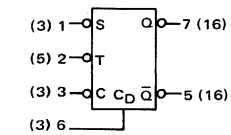
f_{Tog} = 4.0 MHz
t_{pd} = 30 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726G J-K Flip-Flop
(medium-power)



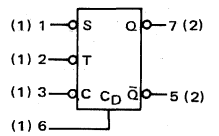
f_{Tog} = 4.0 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

MC774G J-K Flip-Flop
(medium-power)



t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

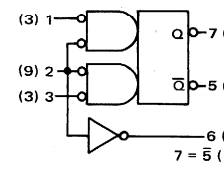
MC782G J-K Flip-Flop
(milliwatt)



t_{pd} = 80 ns
P_D = 23 mW (Only Clock Input High)
21 mW (Inputs Low)

HALF-SHIFT REGISTERS

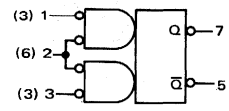
MC705G Half-Shift Register
(medium-power)



7 = $\bar{5}$ (1 + 2)
5 = $\bar{7}$ (2 + 3)
6 = $\bar{2}$

t_{pd} = 22 ns
P_D = 75 mW

MC706G Half-Shift Register
(without inverter—medium-power)



7 = $\bar{5}$ (1 + 2)
5 = $\bar{7}$ (2 + 3)

t_{pd} = 22 ns
P_D = 52 mW

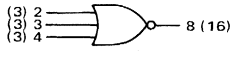
COMMERCIAL MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams shown on these pages describe the MC700 Series Commercial MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

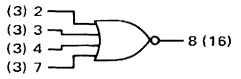
MC703F 3-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

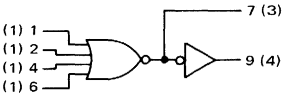
MC707F 4-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

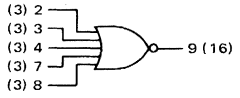
MC711F 4-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 4 + 6}$
$9 = 1 + 2 + 4 + 6$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

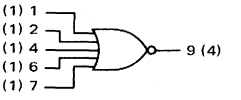
MC729F 5-Input Gate
(medium-power)



$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

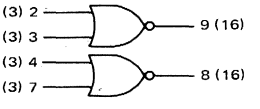
MC728F 5-Input Gate
(milliwatt)



$9 = \overline{1 + 2 + 4 + 6 + 7}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

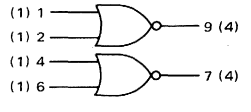
MC714F Dual 2-Input Gate
(medium-power)



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

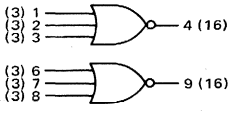
MC710F Dual 2-Input Gate
(milliwatt)



$9 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

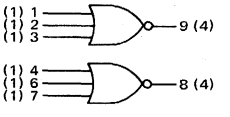
MC715F Dual 3-Input Gate
(medium-power)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

MC718F Dual 3-Input Gate
(milliwatt)



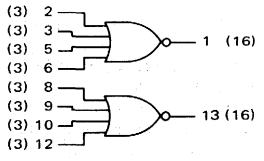
$9 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

(continued)

GATES (continued)

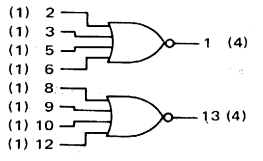
MC725F Dual 4-Input Gate
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

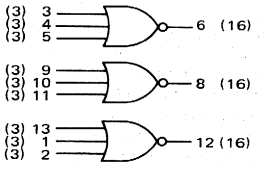
MC719F Dual 4-Input Gate
(milliwatt)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

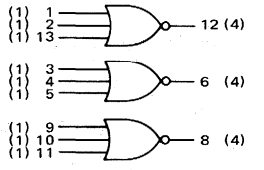
MC792F Triple 3-Input Gate
(medium-power)



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

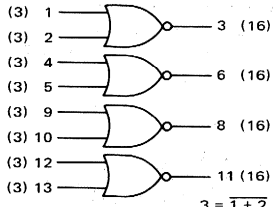
MC793F Triple 3-Input Gate
(milliwatt)



$12 = \overline{1 + 2 + 13}$

t_{pd} = 27 ns
P_D = 18 mW (Inputs High)
3.5 mW (Inputs Low)

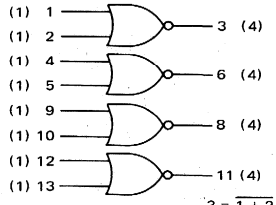
MC724F Quad 2-Input Gate
(medium-power)



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

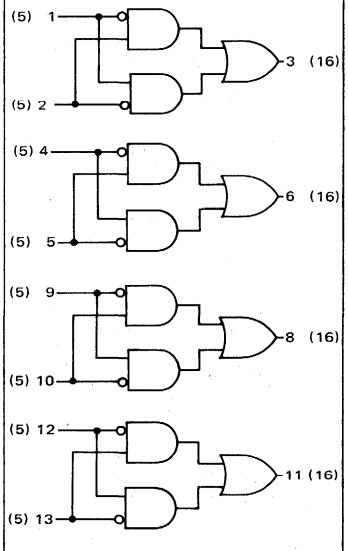
MC717F Quad 2-Input Gate
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

MC771F Quad Exclusive "OR" Gate
(medium-power)

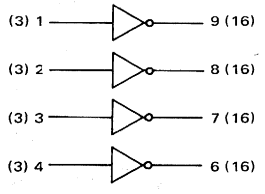


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

INVERTERS

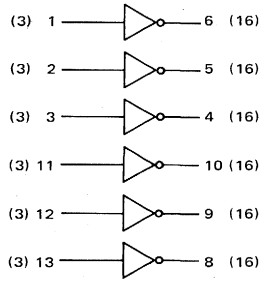
MC727F Quad Inverter
(medium-power)



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

MC789F Hex Inverter
(medium-power)

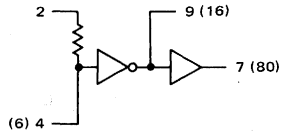


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

BUFFERS

MC700F Buffer
(medium-power)

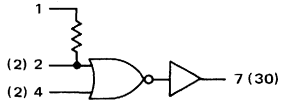


$9 = \overline{4}$

$7 = \overline{4}$

t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

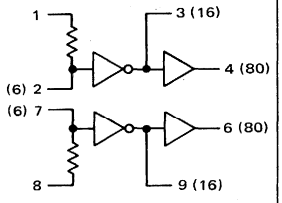
MC709F BUFFER
(milliwatt)



$7 = \overline{2 + 4}$

t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

MC799F Dual Buffer
(medium-power)

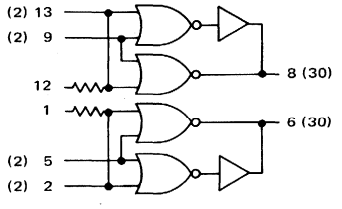


$3 = \overline{2}$

$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

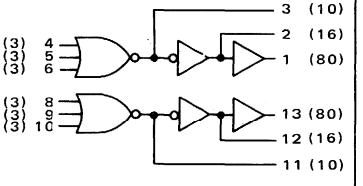
MC798F Dual 2-Input Buffer
(milliwatt)



$8 = \overline{9 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

MC788F Dual 3-Input Buffer
(non-inverting—medium-power)



t_{pd} = 24 ns
P_D = 145 mW (Input High)
56 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$

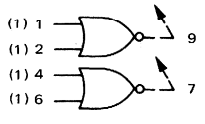
$2 = 4 + 5 + 6$

$1 = 4 + 5 + 6$

Outputs 1, 2 or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

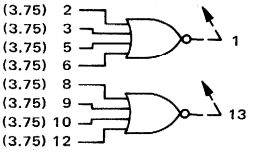
EXPANDERS

MC721F Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

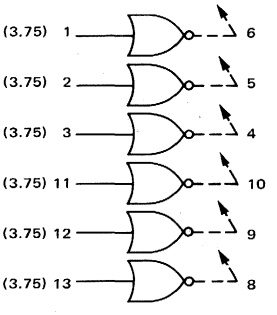
MC786F Dual 4-Input Expander
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

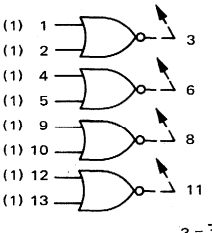
MC9719F Hex Expanders
(medium-power)



$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

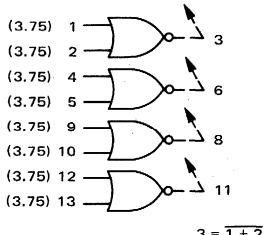
MC9721F Quad 2-Input Expander
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC785F Quad 2-Input Expander
(medium-power)

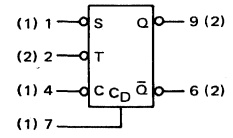


$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

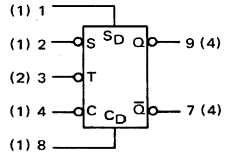
FLIP-FLOPS

MC720F J-K Flip-Flop
(milliwatt)



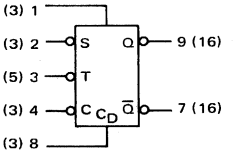
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722F J-K Flip-Flop
(milliwatt)



t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC726F J-K Flip-Flop
(medium-power)



f_{Tog} = 4.0 MHz
t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

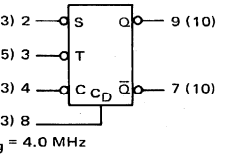
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\bar{Q}$
1	1	Q_n ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ⑤

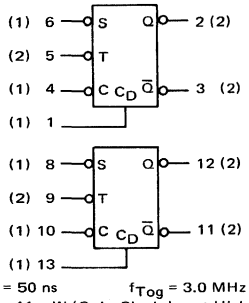
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC723F J-K Flip-Flop
(medium-power)



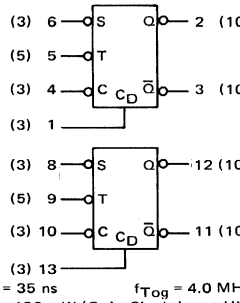
f_{Tog} = 4.0 MHz
t_{pd} = 35 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC776F Dual J-K Flip-Flop
(milliwatt)



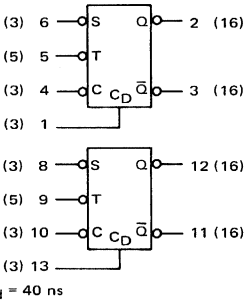
t_{pd} = 50 ns f_{Tog} = 3.0 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

MC790F Dual J-K Flip-Flop
(medium-power)



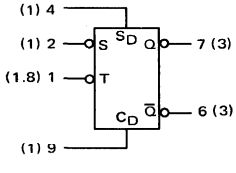
t_{pd} = 35 ns f_{Tog} = 4.0 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MC791F Dual J-K Flip-Flop
(medium-power)



t_{pd} = 40 ns
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC713F Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

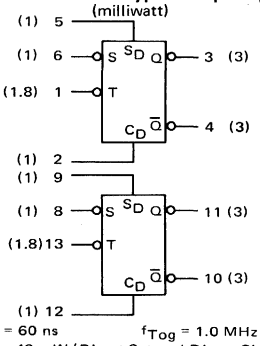
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

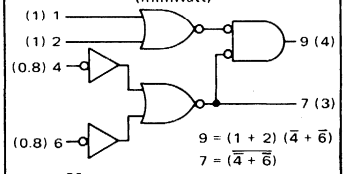
MC778F Dual Type D Flip-Flop
(milliwatt)



t_{pd} = 60 ns f_{Tog} = 1.0 MHz
P_D = 48 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
35 mW (All Inputs Low)

HALF ADDERS

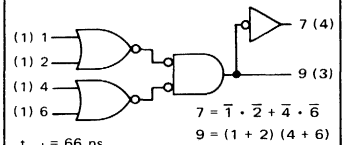
MC708F Half-Adder
(milliwatt)



$9 = (1 + 2)(\overline{4} + \overline{6})$
$7 = \overline{(\overline{4} + \overline{6})}$

t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

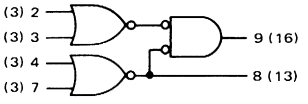
MC712F Half-Adder
(milliwatt)



$7 = \overline{1} \cdot \overline{2} + \overline{4} \cdot \overline{6}$
$9 = (1 + 2)(4 + 6)$

t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

MC704F Half Adder
(medium-power)

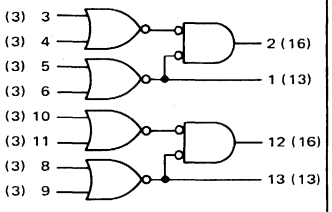


$9 = (2+3)(4 + 7)$
$8 = \overline{4 + 7}$

IF: $4 = \overline{2}$, & $7 = \overline{3}$
THEN: $8 = 2 \cdot 3$
$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

t_{pd} = 14 ns
P_D = 65 mW

MC775F Dual Half Adder
(medium-power)

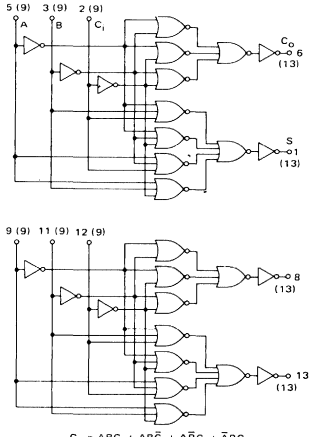


$2 = (3 + 4)(5 + 6)$
$1 = \overline{5 + 6}$

t_{pd} = 20 ns
P_D = 120 mW

FULL ADDER

MC796F Dual Full Adder



$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$
$S = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}B\overline{C_i}$

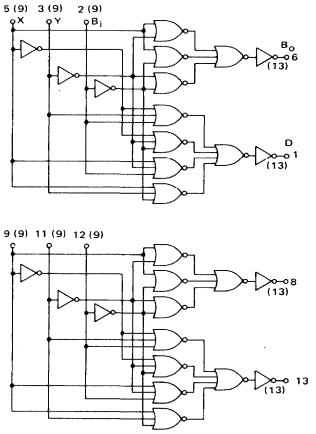
t_{pd} = 60 ns
P_D = 84 mW

TRUTH TABLE

Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC797F Dual Full Subtractor



$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$
$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + YXB_i$

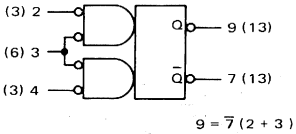
t_{pd} = 60 ns
P_D = 84 mW

TRUTH TABLE

Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

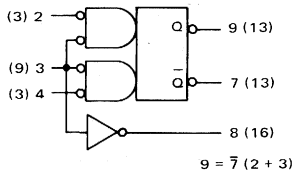
MC706F Half-Shift Register
(without inverter—medium-power)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$

t_{pd} = 22 ns
P_D = 52 mW

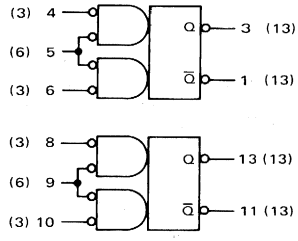
MC705F Half-Shift Register
(with inverter—medium-power)



$9 = \overline{7}\ (2 + 3)$
$7 = \overline{9}\ (3 + 4)$
$8 = \overline{3}$

t_{pd} = 22 ns
P_D = 75 mW

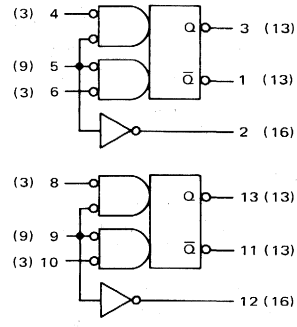
MC784F Dual Half-Shift Register
(without inverter—medium-power)



$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

t_{pd} = 22 ns
P_D = 100 mW

MC783F Dual Half-Shift Register
(with inverter—medium-power)



$3 = \overline{1}\ (4 + 5)$
$1 = \overline{3}\ (6 + 5)$

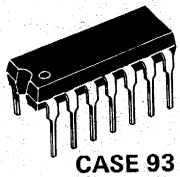
t_{pd} = 22 ns
P_D = 140 mW

MOS

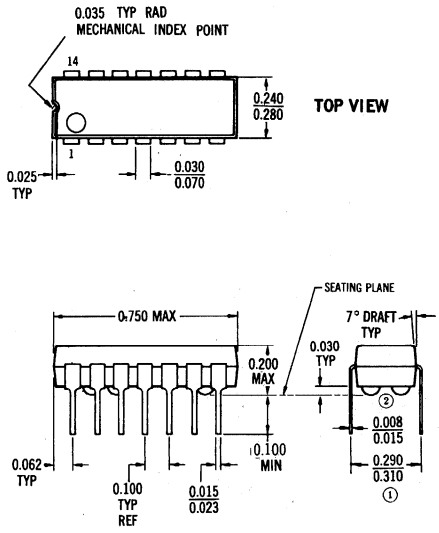
INTEGRATED CIRCUITS

MC1120P SERIES

This low-cost MOS integrated circuit series is designed specifically for electronic organ applications.



CASE 93
(TO-116)



FUNCTIONS AND CHARACTERISTICS ($V_S = -10$ V, $T_A = 25°C$)

FUNCTION	TYPE CASE 93 0 to +75°C	Output Loading Factor Each Output	Output Voltage Swing Volts	Operating Frequency kHz	Total Power Dissipation mW typ/pkg
Dual Keyer Gate with Snub Inputs	MC1120	5	12	0 to 100	10
Frequency Divider (Four Stage)	MC1124	5	10	0 to 100	190

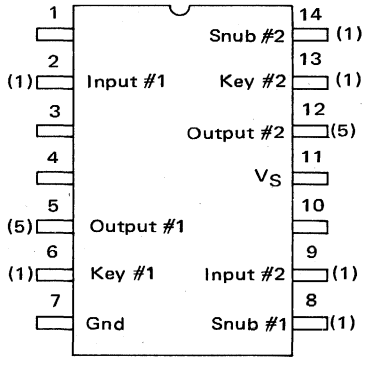
MAXIMUM RATINGS

RATING	VALUE	UNIT
Power Supply Voltage	−40 to +0.3	Vdc
Input Voltage — MC1120P MC1124P	−40 to +0.3 −30 to +0.3	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	−55 to +125	°C

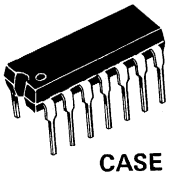
MC1120P

A monolithic circuit consisting of two gates with key and snub inputs.

- Noise Immunity = 1.0 Volt
- Minimum Fan-Out = 5
- Temperature Range = 0 to +75°C

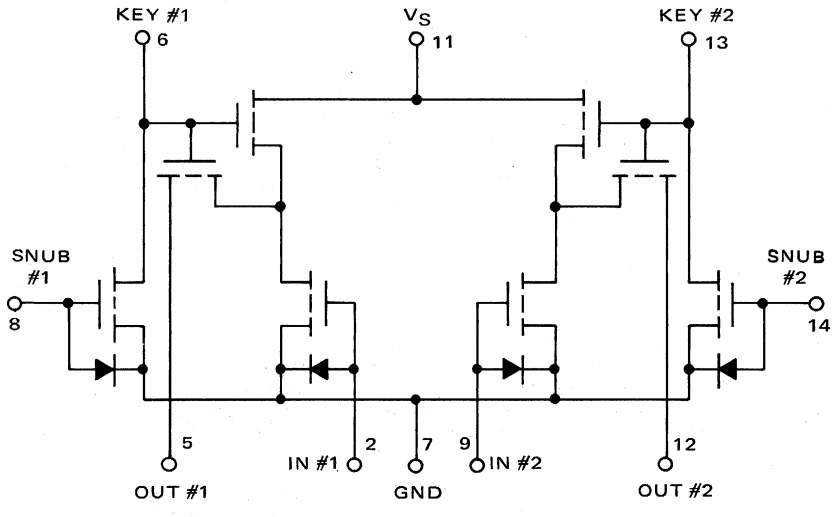


Number in parenthesis = loading factor



CASE 93
(TO-116)

CIRCUIT SCHEMATIC



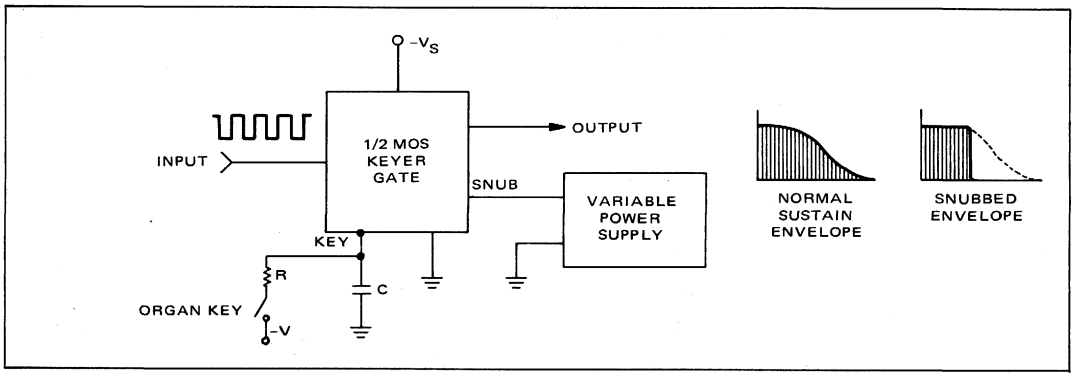
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Source Voltage	V_S	-40 to +0.3	Vdc
Input, Snub, Key Voltages	V_{in}, V_{SN}, V_K	-40 to +0.3	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Test Conditions Vdc ± 1% V_{IL} -2.5	V_{IH} -15	V_K -20	V_{max} -40	V_S -10	Ground
						Applied to pins listed below:					
Source Supply Drain Current	I_S	11	-	1.0	mAdc	-	9,2	6,13	-	11	7,8,14
Input Current	I_{in}	2	-	100	μAdc	-	-	-	2	-	6,7
		9	-	100	μAdc	-	-	-	9	-	7,13
Snub Current	I_{SN}	8	-	100	μAdc	-	-	-	8	-	6,7
		14	-	100	μAdc	-	-	-	14	-	7,13
Key Current	I_K	6	-	100	μAdc	-	-	-	6	-	2,7,8
		13	-	100	μAdc	-	-	-	13	-	7,9,14
Key Current (Snub On)	$I_{K(on)}$	6	70	-	μAdc	-	8	6	-	-	2,7
		13	70	-	μAdc	-	14	13	-	-	7,9
Key Current (Snub Off)	$I_{K(off)}$	6	-	1.0	μAdc	8	-	6	-	-	2,7
		13	-	1.0	μAdc	14	-	13	-	-	7,9
Logical "1" Output Voltage	V_{OL}	5	-	-2.0	Vdc	-	-	2,6	-	11	7
		12	-	-2.0	Vdc	-	-	9,13	-	11	7
Logical "0" Output Voltage	V_{OH}	5	-9.0	-	Vdc	-	-	6	-	11	2,7
		12	-9.0	-	Vdc	-	-	13	-	11	7,9

TYPICAL APPLICATION



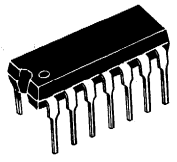
Closing of the organ key "enables" the KEYER GATE, permitting subsequent pulses applied to the signal input to pass through the gate, and simultaneously charges capacitor C. When the key is released the stored charge maintains the gate conduction until charge is removed. The SNUB line provides a means of varying the total resistance in parallel with the capacitor by controlling the series impedance of the MOS transistor. Therefore the length of time that the note is sustained after the key is released depends upon the snub voltage.

FREQUENCY DIVIDER

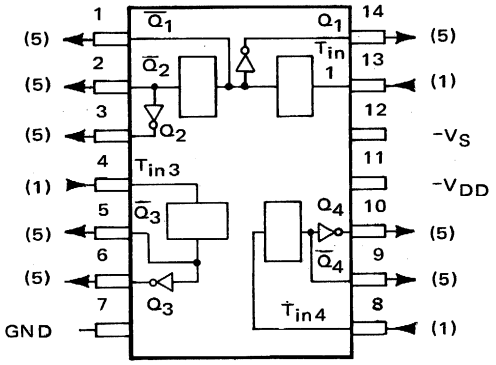
MC1124P

A monolithic circuit consisting of four flip-flops with single rail inputs and Q and $\bar{Q}$ outputs.

- Toggle Frequency = DC to 500 kHz
- Noise Immunity = 1.0 Volt
- Minimum Fan-Out = 5
- Temperature Range = 0 to +75°C



CASE 93
(TO-116)

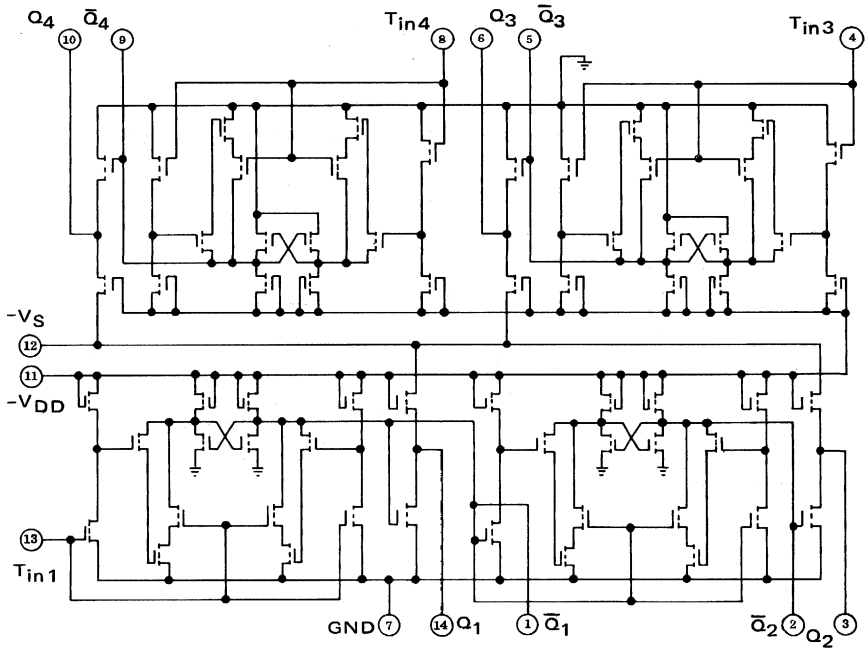


Number in parenthesis = loading factor

NOTE:

To cascade flip-flop stages, connect $\bar{Q}$ (trigger out) to T_{in} (trigger in) of the next stage.

CIRCUIT SCHEMATIC



MAXIMUM RATINGS

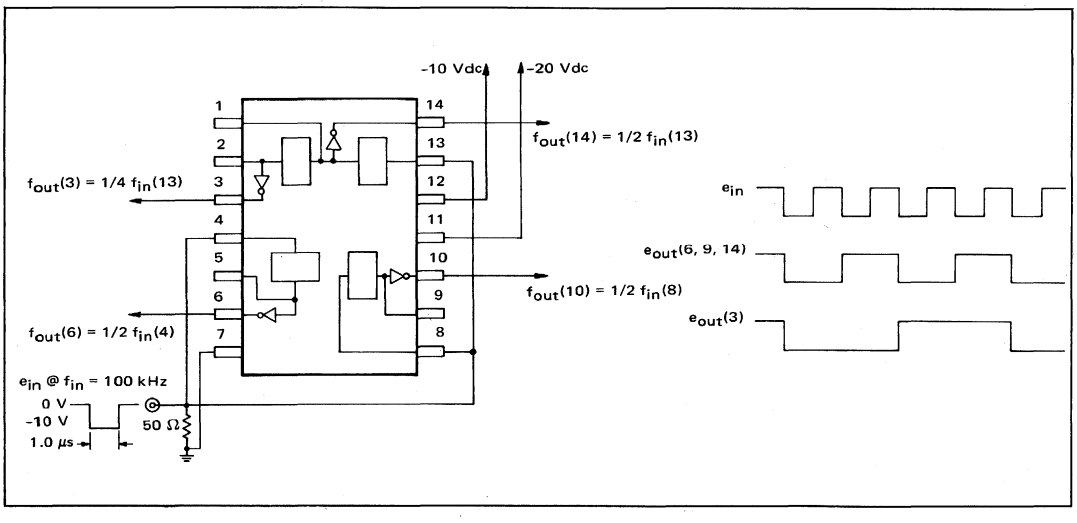
Rating	Symbol	Value	Unit
Drain Voltage	V_{DD}	-40 to +0.3	Vdc
Trigger Input Voltage	V_{in}	-30 to +0.3	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Min	Max	Unit	Test Voltages @ T_A = 25°C			Ground
						VT_{in} *	V_{DD} -30 ± 1 Vdc	V_S -10 ±0.5 Vdc	
						Applied to pins listed below:			
Drain Supply Drain Current	I_{DD}	11	-	2.5	mAdc	-	11	12	1,4,7,8,13
Source Supply Drain Current	I_{DS}	12	-	17	mAdc	-	1,2,5,9,11	12	4,7,8,13
Source Supply Leakage Current	I_{SS}	12	-	5.0	μAdc	-	-	12	1,2,3,4,5 6,7,8,9,10 11, 13, 14
"Q" Logical "0" Output Voltage	V_{OH}	3	-9.0	-	Vdc	1	11	12	7
		6	-9.0	-		4	11	12	7
		10	-9.0	-		8	11	12	7
		14	-9.0	-		13	11	12	7
"Q" Logical "1" Output Voltage	V_{OL}	3	-	-2.5	Vdc	1	11	12	7
		6	-	-2.5		4	11	12	7
		10	-	-2.5		8	11	12	7
		14	-	-2.5		13	11	12	7
"$\overline{Q}$" Logical "0" Output Voltage	V_{OH}	1	-10	-	Vdc	13	11	12	7
		2	-10	-		1	11	12	7
		5	-10	-		4	11	12	7
		9	-10	-		8	11	12	7
"$\overline{Q}$" Logical "1" Output Voltage	V_{OL}	1	-	-2.5	Vdc	13	11	12	7
		2	-	-2.5		1	11	12	7
		5	-	-2.5		4	11	12	7
		9	-	-2.5		8	11	12	7
Toggle Frequency	f_{Tog}		100	-	kHz		See Test Diagram		

*VT_{in} — Preset to desired output level by applying -20 Vdc to input then open.

TOGGLE FREQUENCY TEST DIAGRAMS AND WAVEFORMS

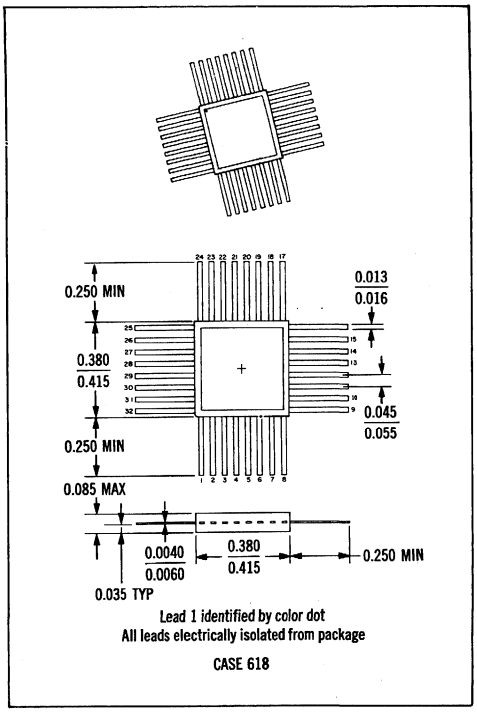


COMPLEX ARRAYS

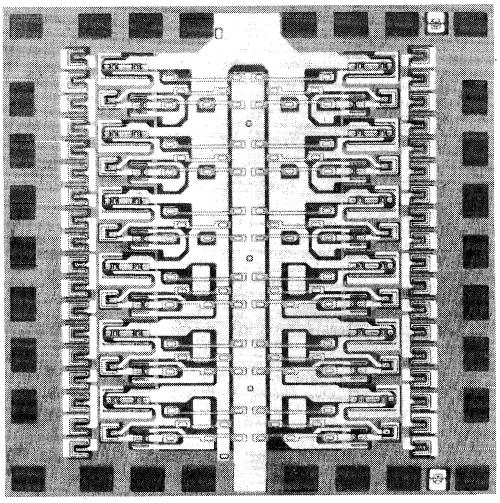
XC157

FOR COMPLEX FUNCTIONS USING CUSTOM 2nd LAYER METALIZATION

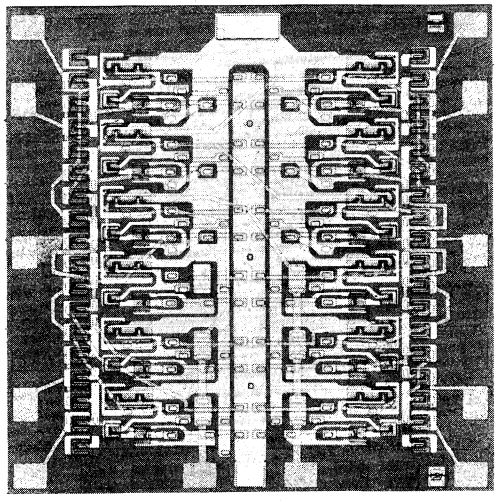
The XC157 is a monolithic 12-gate array developed to introduce a form of custom MSI. This array also serves as a vehicle for establishing customer-supplier interfaces which will ultimately lead toward more complex MSI and LSI systems. Each gate is intraconnected with a first layer of metalization but contains uncommited input logic diodes and output load resistors for increased design flexibility. The diode and load resistor intraconnections and the subsequent gate-to-gate interconnections are made with your custom-designed second layer of metalization.



From this silicon monolithic circuit array of 12 MDTL gates . . . XC157



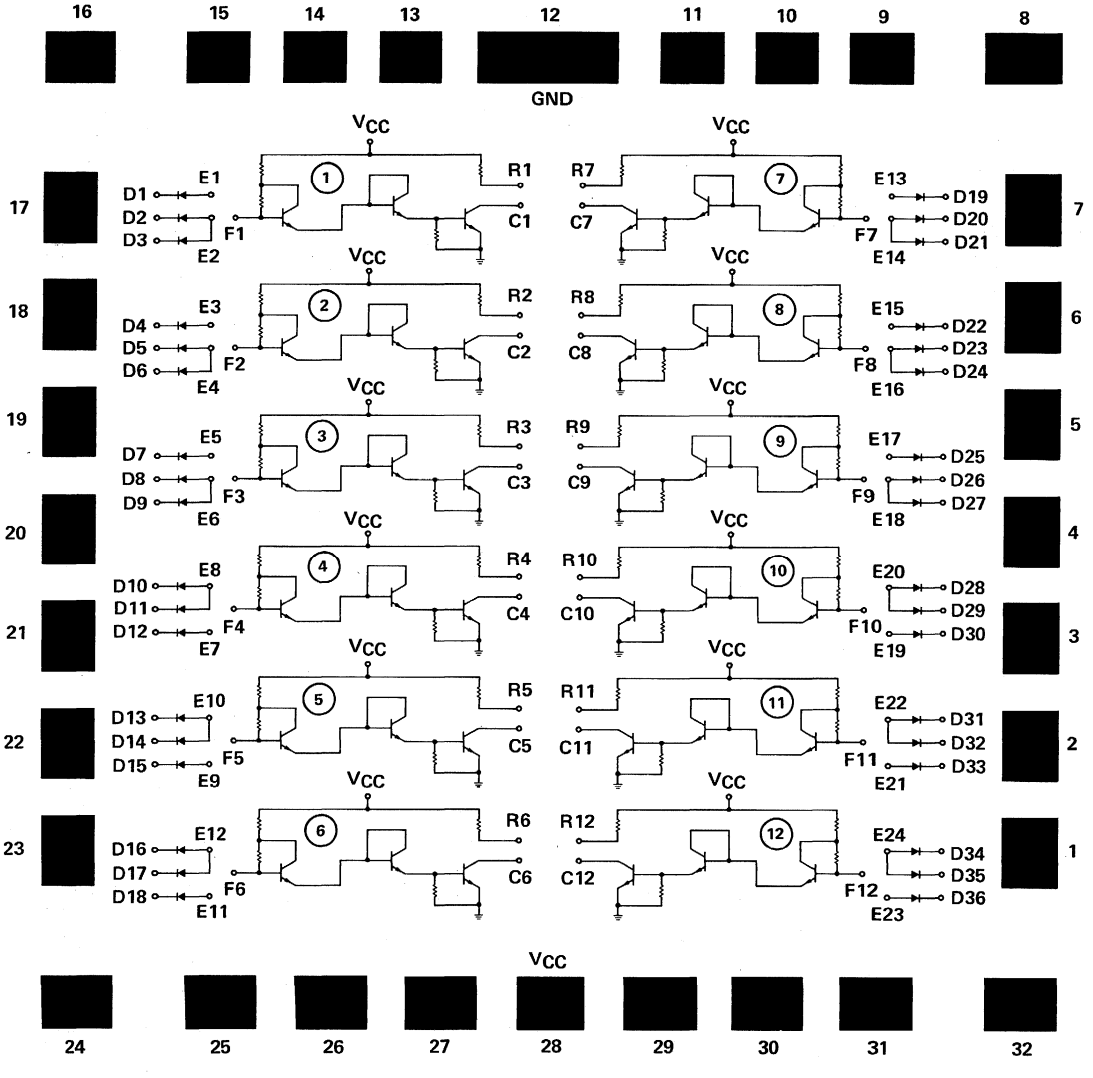
. . . you can design custom complex circuit functions such as . . . 4-CHANNEL CLOCKED LATCH WITH 2ND METALIZATION



SECOND METAL LAYER DESIGN PROCEDURE:

1. Sketch desired logic configuration, such as shown by Custom Design Examples. Consult CIRCUIT RULES and use the schematic diagram, Figure 1, as a reference.
2. Show desired interconnections on the circuit schematic (Figure 1). Prepare a preliminary layout, on Figure 2, of the required interconnections for a second layer metalization using the connection points designated on Figure 1.
3. Transfer resultant circuit connections to a node routing list (see example on page 8-8) for use as a guide, using the pad designations shown on Figure 2. On the same routing list indicate interconnection pads not used.
4. Prepare test specification, including test sequence, for acceptance testing of the final product in accordance with the electrical characteristics given for the individual gate. State logic equation to define required input-output relationships. When logic is sequential in nature, (i.e., flip-flops, counting elements, etc.) include timing diagram.
5. Forward items 1 thru 4 to your nearest Motorola Sales Office for product price and delivery quotation.

FIGURE 1 – CHIP SCHEMATIC



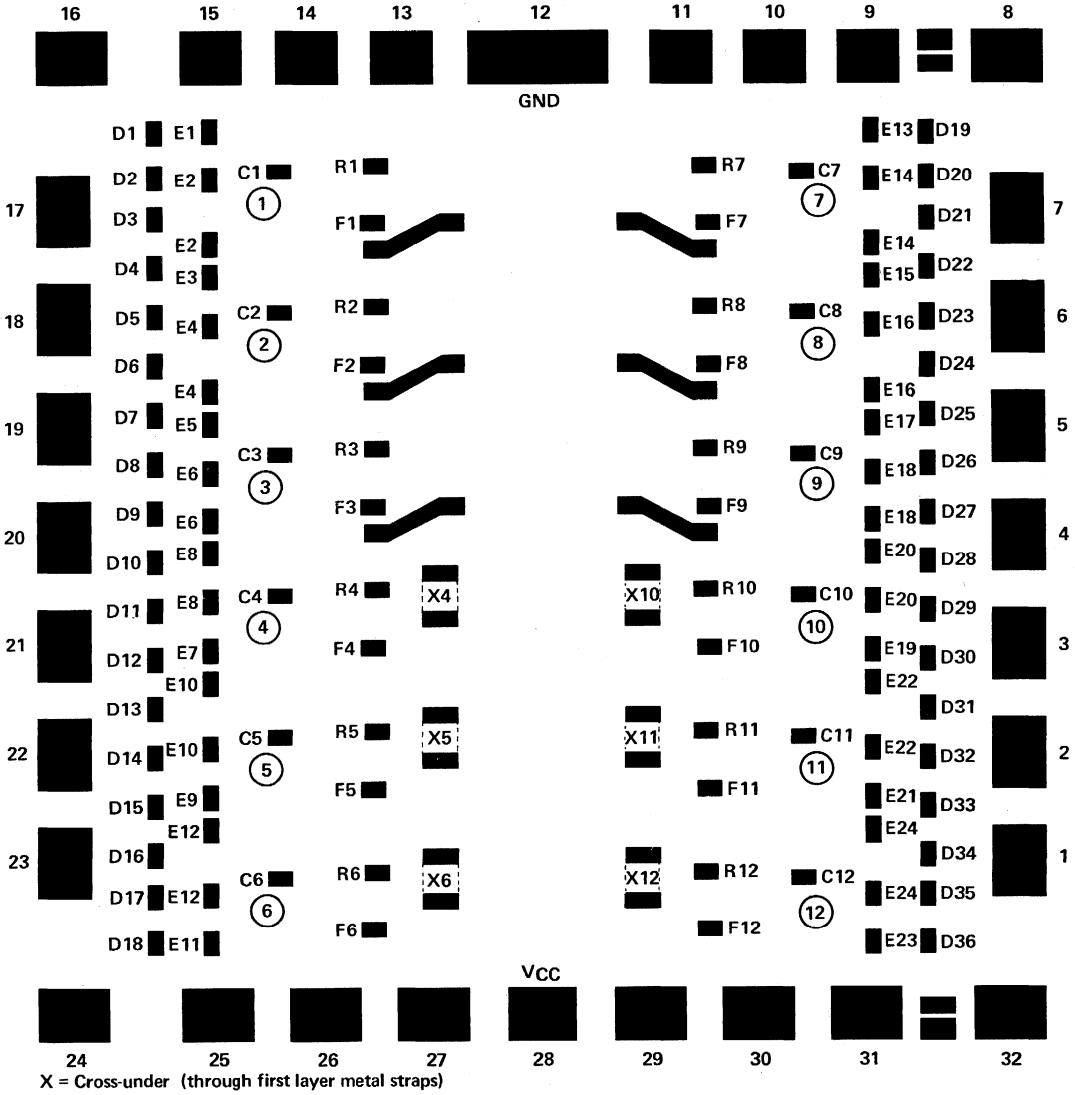
Cross-unders available as shown in Figure 2

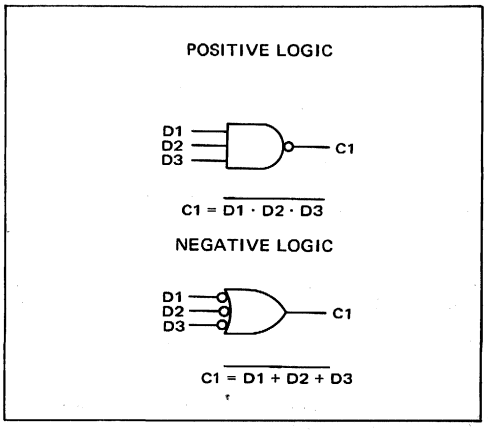
CIRCUIT RULES:

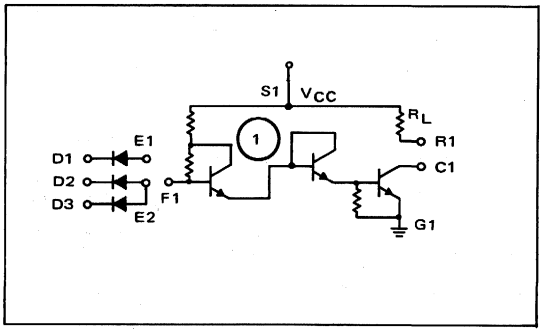
1. The number of inputs to any individual gate may be expanded to a maximum of 10 diodes.
2. For any individual gate the maximum allowable fan-out external to the package is limited to 5 loads. However, fan-out of any individual gate is allowable up to 10, if 5 of the fan-outs are internal and on the same side of the chip as the driver (e.g., Gate 1 must not drive Gates 7 thru 12); otherwise each internal fan-out must be subtracted from the allowable external fan-out of 5.
3. Each load resistor (R_L) used represents a fan-out load of one (1).
4. Collector ORing is allowable. Where one common load resistor is used, six gate outputs may be tied together.

FIGURE 2 – INTERCONNECTION PAD LAYOUT

Points on the first metalization layer are made available through pads designated by letters with numbers on both Figures 1 and 2 (e.g., R1, D22, etc.). These pads are used to make the circuit interconnections discussed in the sections on design procedure and circuit rules, through use of a second layer of metalization. The bonding pads are designated by number only and correspond to the number system of the 32-pin flat package. Connection to these bonding pads must also be shown for the interconnecting metalization.







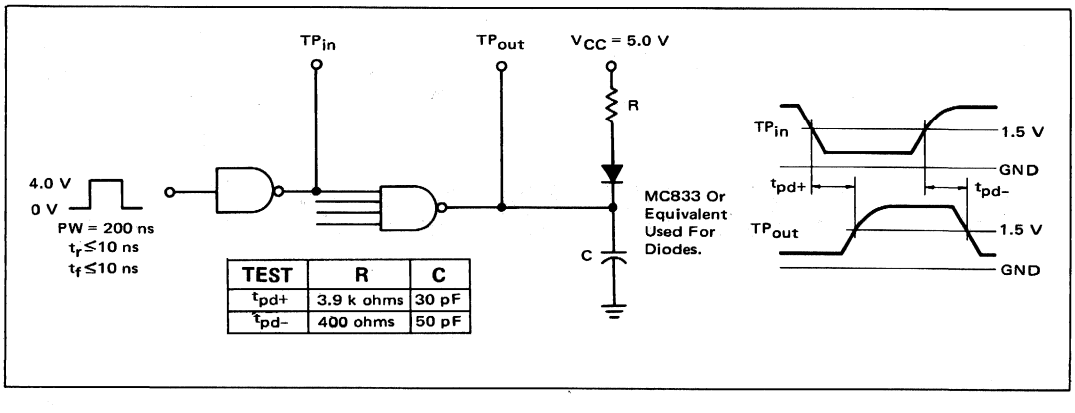
ELECTRICAL CHARACTERISTICS FOR INDIVIDUAL GATES

E1 and E2 are connected to F1; R1 is connected to C1; S1 and G1 are connected to pads 28 and 12 through the 1st layer of metalization.

NOTE: These characteristics are given to assist the user in specifying the input-output characteristics of the required complex function.

						TEST CURRENT / VOLTAGE VALUES @ T_A=25°C										
						mA		Volts								
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCH}	V_{max}	
						15.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	5.50	8.00	
		Pad Under Test	Test Limits +25°C			TEST CURRENT / VOLTAGE APPLIED TO PADS LISTED BELOW:										
Characteristic	Symbol		Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	C1	-	0.45	Vdc	C1	-	-	D1,D2,D3	-	-	-	S1	-	-	G1
	V_{OH}	C1	2.60	-	↓	-	C1	D1	-	-	-	-	↓	-	-	↓
				-		-	↓	D2	-	-	-	-		-	-	
				-		-		D3	-	-	-	-		-	-	
Short-Circuit Current	I_{SC}	C1	-	-1.63	mAdc	-	-	-	-	-	-	-	-	S1	-	D1,C1,G1
Reverse Current	I_R	D1	-	5.0	μAdc	-	-	-	-	-	D1	-	-	S1	-	D2,D3,G1
		D2	-	↓	↓	-	-	-	-	-	D2	-	-	↓	-	D1,D3,G1
		D3	-			-	-	-	-	-	D3	-	-		-	D1,D2,G1
Output Leakage Current	I_{CEX}	C1	-	50	μAdc	-	-	-	-	-	-	C1,S1	-	-	-	D1,G1
Forward Current	I_F	D1	-	-1.5	mAdc	-	-	-	-	D1	D2,D3	-	-	S1	-	G1
		D2	-	↓	↓	-	-	-	-	D2	D1,D3	-	-	↓	-	↓
		D3	-			-	-	-	-	D3	D1,D2	-	-		-	
Drain Current per Gate	I_{PDH}	S1	-	4.0	mAdc	-	-	-	-	-	-	-	S1	-	-	G1
	I_{max}	S1	-	6.8	mAdc	-	-	-	-	-	-	-	-	-	S1	D1,G1
Switching Times						Pulse In	Pulse Out									
	t_{pd+}	C1	25	80	ns	D1	C1	-	-	-	-	-	S1	-	-	G1
	t_{pd-}	C1	10	35	ns	D1	C1	-	-	-	-	-	S1	-	-	G1

EQUIVALENT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

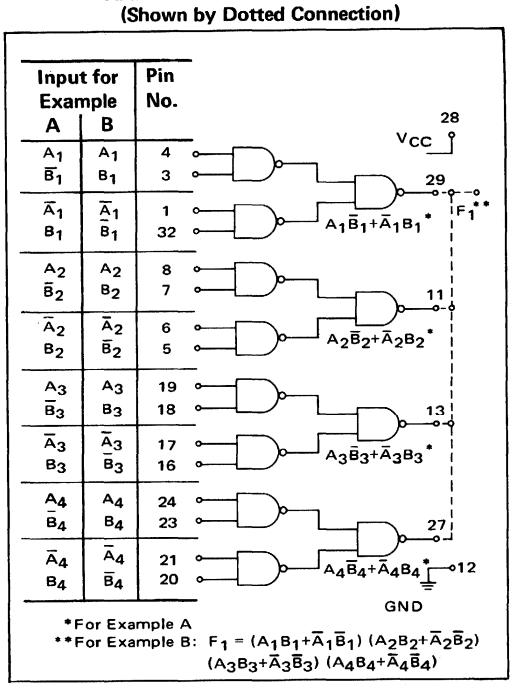


TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	50 pF

CUSTOM DESIGN EXAMPLES

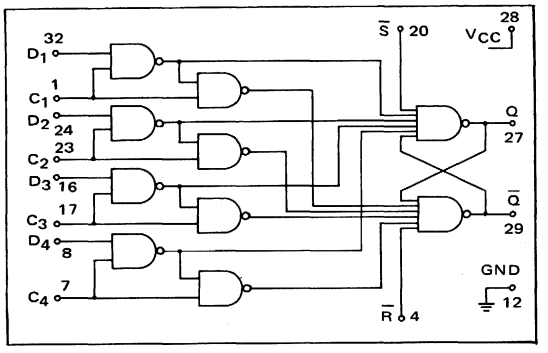
EXAMPLE A – QUAD EXCLUSIVE "OR" GATE
or
EXAMPLE B – 4-BIT COMPARATOR
(Shown by Dotted Connection)

Input for Example A	Input for Example B	Pin No.
A_1	A_1	4
$\bar{B}_1$	B_1	3
$\bar{A}_1$	$\bar{A}_1$	1
B_1	$\bar{B}_1$	32
A_2	A_2	8
$\bar{B}_2$	B_2	7
$\bar{A}_2$	$\bar{A}_2$	6
B_2	$\bar{B}_2$	5
A_3	A_3	19
$\bar{B}_3$	B_3	18
$\bar{A}_3$	$\bar{A}_3$	17
B_3	$\bar{B}_3$	16
A_4	A_4	24
$\bar{B}_4$	B_4	23
$\bar{A}_4$	$\bar{A}_4$	21
B_4	$\bar{B}_4$	20

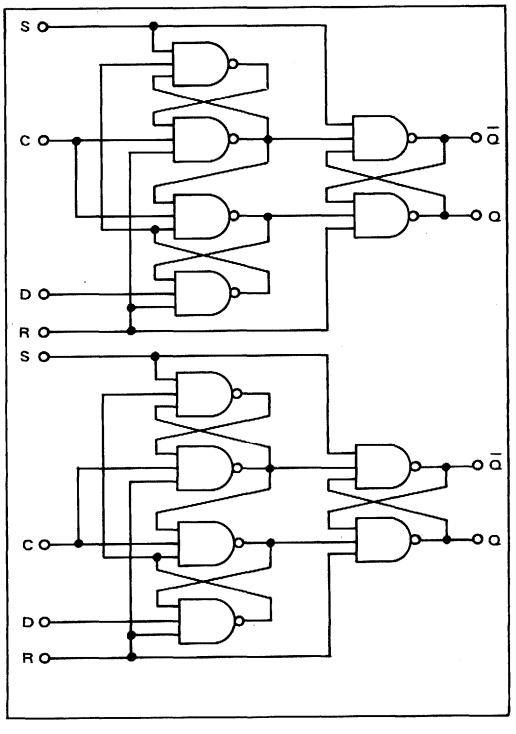


*For Example A
**For Example B: $F_1 = (A_1B_1+\bar{A}_1\bar{B}_1)(A_2B_2+\bar{A}_2\bar{B}_2)(A_3B_3+\bar{A}_3\bar{B}_3)(A_4B_4+\bar{A}_4\bar{B}_4)$

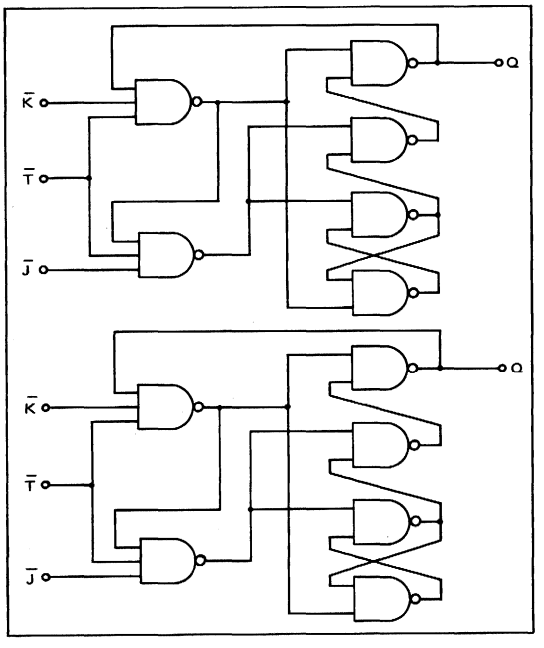
EXAMPLE C – 4-CHANNEL CLOCKED LATCH



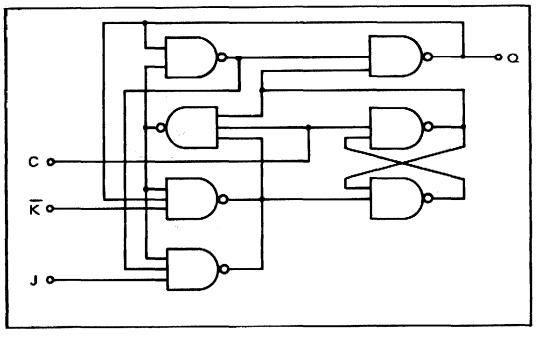
EXAMPLE D – DUAL TYPE "D" FLIP-FLOP



EXAMPLE E – DUAL TYPE "T" FLIP-FLOP



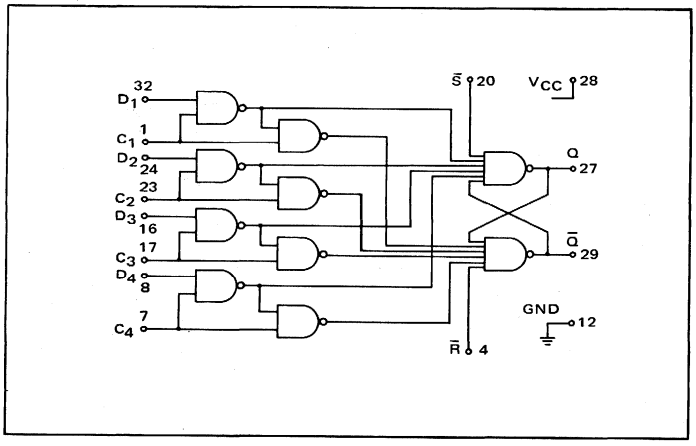
EXAMPLE F – J-K̄ FLIP-FLOP



EXAMPLE OF PROCEDURE TO BE FOLLOWED

(USING CUSTOM DESIGN EXAMPLE C: 4-CHANNEL CLOCKED LATCH)

LOGIC DIAGRAM



NODE ROUTING LIST

D2-16	E12-F6
D3-D5-17	D12-R12-C12-D32
R1-C1-D6-D8	D35-32
D9-20	E24-F12
E5-E6-E7-E8-F3	D33-D34-1
D11-D13-C6-R6	F11-E21-E22
D14-D16-23	E17-E18-E19-E20-F9
D17-24	C11-R11-D29
E2-F1	D28-R3-C3-27 (thru X5, X6)
D7-R7-C7-D24	E16-F8
C2-R2-D26	D25-C8-R8
E4-F2	D21-D23-7
D10-R9-C9-29 (thru X10, X11, X12	D20-8
C5-R5-D30	E14-F7
E10-F5	D27-4

NODES NOT USED

D1	E11
D4	E13
D15	E15
D18	E23
D19	C4
D22	C10
D31	R4
D36	R10
E1	F4
E3	F10
E9	X4

ACCEPTANCE SPECIFICATION

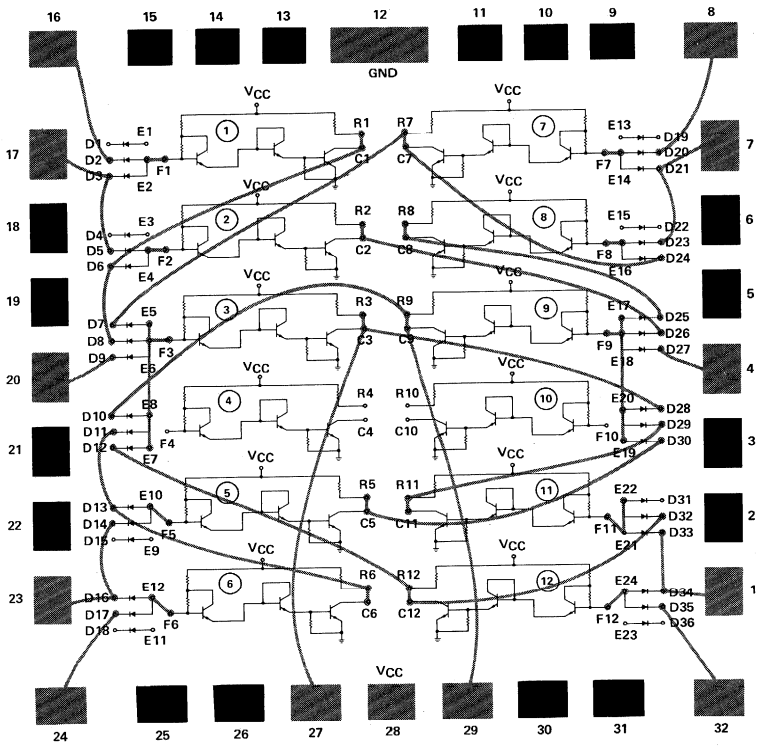
. . . to be prepared with format similar to that shown on page 8-6.

LOGIC EQUATION
and/or
TIMING DIAGRAM (when applicable)

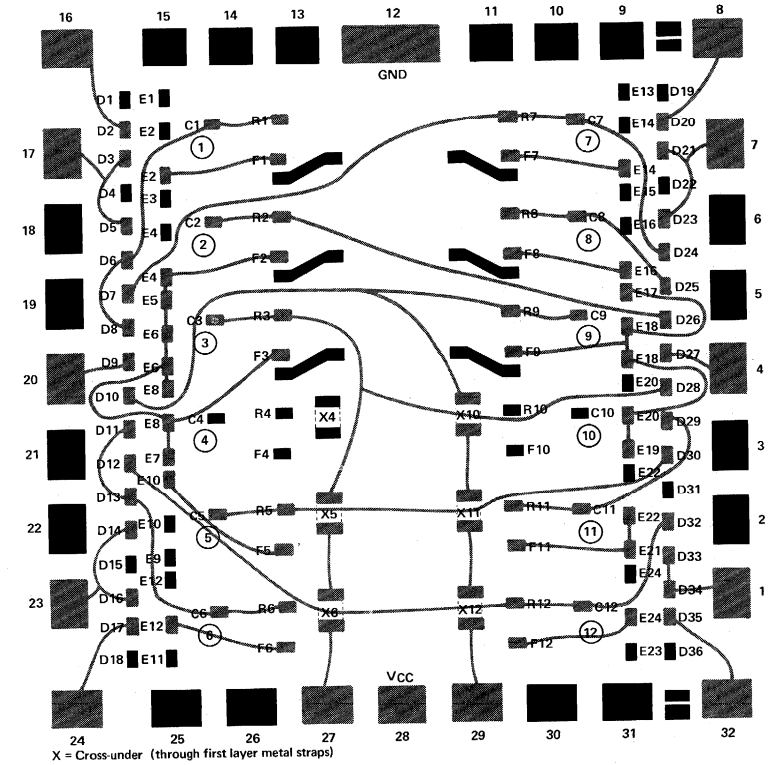
The process technology represented by the XC157 is a significant and necessary step for large-scale integration. It is, however, just a forerunner of the more complex arrays presently in development. Arrays with greater complexities and logic power utilizing other logic circuitry will soon become available. From these arrays circuits such as multiple independent Type D flip-flops, decade counters, shift registers, and complex ripple counters can be derived.

EXAMPLE OF PROCEDURE (continued)

CIRCUIT SCHEMATIC



INTERCONNECTION PAD LAYOUT



X = Cross-under (through first layer metal straps)

LINEAR

INTEGRATED CIRCUITS

LINEAR

INTEGRATED CIRCUITS

INDEX

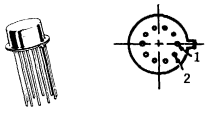
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LINEAR INTEGRATED CIRCUITS

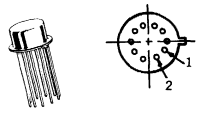
APPLICATION SELECTOR GUIDE

LINEAR integrated circuits offer the design engineer a variety of functions for analog applications. This line includes operational, differential, high frequency, power, and sense amplifiers with a broad selection of operating characteristics and packaging.

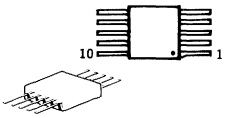
LINEAR IC PACKAGES



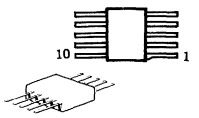
CASE 71 — 10 PIN
Suffix G after type number



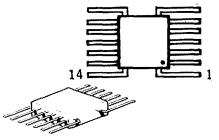
CASE 71A — 10 PIN
Suffix G after type number



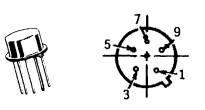
CASE 72 (TO-91)
Suffix F after type number



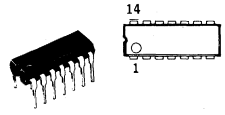
CASE 73
Suffix F after type number



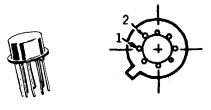
CASE 83 (TO-86)
Suffix F after type number



CASE 89 — 5 PIN
Suffix G after type number



CASE 93 (TO-116)
Suffix P after type number



CASE 96 — 8 PIN (TO-99)
Suffix G after type number

At a Glance

OPERATIONAL AMPLIFIERS

TYPE				Open Loop Voltage Gain (A_{VOL})	Output Voltage Swing (V_{out}, V_P)	Common Mode Rejection Ratio (CM_{rej}, dB)
Temperature Range						
−55 to +125°C	Case	0 to +75°C	Case			
MC1520	71A,72	–	–	1,500	± 4.0	−90
MC1530	71,72	MC1430	71,72,93	5,000	± 5.0	−75
MC1531	71,72	MC1431	71,72,93	3,500	± 5.0	−75
MC1533	71,72	MC1433	71,72,93	60,000*	± 12	−100
MC1535**	71,83	MC1435**	71,83,93	7,000	± 3.6	−90
–	–	MC1437**	93	45,000	± 14	−100
MC1539	96	MC1439	96	MC1539 120,000 MC1439 100,000	± 14	−100
MC1709	96,72	MC1709C	96,72,93	45,000	± 14	−90
MC1712	96,72	MC1712C	96,72,93	3,600	± 5.3	−100

*Adjustable **Dual

HIGH FREQUENCY AMPLIFIERS

TYPE	Temperature	Case	Small-Signal Voltage Gain (A_V, dB)	Bandwidth (MHz)	Noise Figure (dB)	Comments
MC1110	−55 to +125°C	89	26② @ 100 MHz	300②	4.0 @ 100 MHz	High stability through low internal feedback for RF-IF applications.
MC1509	−55 to +125°C	73	40	40	4.5μV(5Hz-10MHz)①	Ideal for wideband video applications.
MC1510	−55 to +125°C	73, 96	40	40	4.5μV(5Hz-10MHz)①	
MC1550	−55 to +125°C	71	26 @ 60 MHz	200②	5.0 @ 60 MHz	Constant input impedance over entire AGC range. RF-IF amplifier for communications equipment.
MC1552	−55 to +125°	71	34	40	5.0 @ 30 MHz	Three stage direct coupled common emitter cascade circuit with series feedback achieving extremely stable gain.
MC1553	−55 to +125°C	71	52	35	5.0 @ 30 MHz	Same as MC1552 except higher gain.

① Noise Voltage referred to input
② Useful transducer power gain

POWER AMPLIFIERS

TYPE	Temperature	Case	Output Power (W)	Voltage Gain (A_V, V/V)	Total Harmonic Distortion (%)	Comments
MC1524	−55 to +125°C	71	1.0	38	0.6	Complementary output, low standby current drain.
MC1554	−55 to +125°C	71	1.0	10,18,36	0.4	Capable of single or split supply operation.

DIFFERENTIAL AMPLIFIERS

TYPE	Temperature	Case	Differential Voltage Gain (A_{dd}, dB)	Output Voltage Swing (V_{out}, V_{p-p})	Common Mode Rejection (CM_{rej}, dB)	Differential Input Impedance (Z_{in}, kΩ)	Comments
MC1429	0 to +75°C	71	38	6.0	−75	40	Darlington inputs (high impedance).
MC1519	−55 to +125°C	71	73	14	−89	2.6	NPN inputs, PNP outputs, 1 MHz BW.
MC1525	−55 to +125°C	71	43	8.0	−85	3.0	Conventional differential inputs, high gain, built-in temperature compensated current source.
MC1526	−55 to +125°C	71	36	8.0	−85	70	Same as MC1525 except Darlington inputs.
MC1529	−55 to +125°C	71	38	6.0	−75	50	Same as MC1429—specified over full temperature range.

SENSE AMPLIFIERS

TYPE	Temperature	Case	Input Threshold (V_{th}, mVdc)	Voltage Gain (A_V, V/V)	Response Time (t_R, ns)	Comments
MC1440	0 to +75°C	71,72,93	17	85	50	Designed to detect bipolar differential signals derived by a core memory with cycle times as short as 0.5 μs.
MC1540	−55 to +125°C	71,72	17	85	30	
MC1541	−55 to +125°C	83	17	85	15	A dual-channel gated sense amplifier with separate wide band differential input amplifiers.
MC1710	−55 to +125°C	72,96	0	1700†	40	A differential comparator providing accuracy and fast response time.
MC1710C	0 to +75°C	72,96,93	0	1700†	40	Same as MC1710—specified over limited temperature range.
MC1711	−55 to +125°C	71A,72	0	1500†	40	A dual differential comparator providing accuracy and fast response time.
MC1711C	0 to +75°C	71A,72,93	0	1500†	40	Same as MC1711—specified over limited temperature range.

† Avol

STEREO PREAMPLIFIERS

TYPE	Temperature	Case	Open Loop Voltage Gain (A_{VOL})	Input Offset Voltage (mV)	Output Voltage Swing (V_{rms})	Channel Separation (dB)	Comments
MC1303	0 to +75°C	93	10,000	3.0	5.5	70	Two amplifiers on a single monolithic chip.

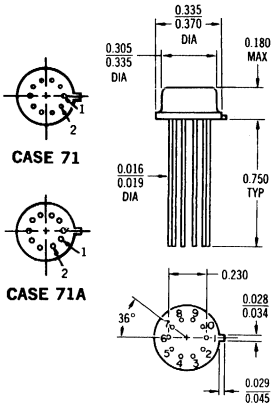
LINEAR IC SYMBOLS AND DEFINITIONS

A_{dd}	Differential Voltage Gain (dB)
A_p	Transducer Power Gain (dB)
A_V	Voltage Gain (dB or V/V, as specified)
A_{VOL}	Open Loop Voltage Gain (V/V)
$A_{V(s.e.)}$	Single-Ended Voltage Gain (dB)
CM_{rej}	Common Mode Rejection Ratio (dB)
CMV_{in}	Input Common Mode Voltage Swing (V_{pk} or V_{p-p}, as specified)
TCV_{io}	Temperature Coefficient of Input Offset Voltage (μV/°C)
TCV_{th}	Threshold Voltage Temperature Coefficient (μV/°C)
THD	Total Harmonic Distortion (%)
t_{pd}	Propagation Delay Time (ns)
t_R	Response Time (ns)
V_{io}	Input Offset Voltage (mV)
V_{OH}	Output Voltage, High (Vdc)
V_{OL}	Output Voltage, Low (Vdc)
V_{out}	Output Voltage Swing (V_{pk} or V_{p-p}, as specified)
V_{out} (CM)	Common Mode Output Voltage (Vdc)
V_{out} (dc)	DC Output Voltage (Vdc)
V_{th}	Input Threshold Voltage (mVdc)

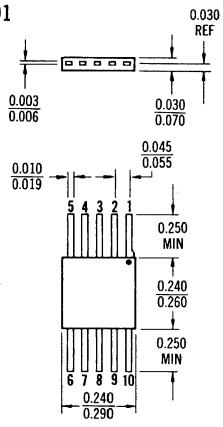
CASE OUTLINES

CASE 71, 71A

CASE 71A – PIN 10 UNDER TAB

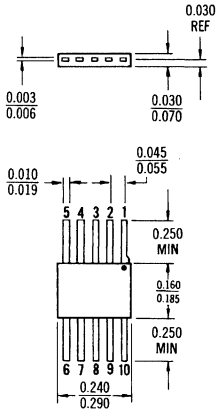


CASE 72 10-LEAD FLAT PACKAGE TO-91



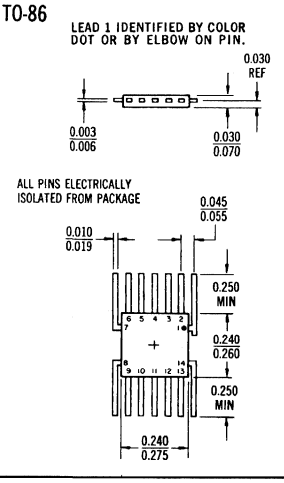
Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

CASE 73 10-LEAD FLAT PACKAGE



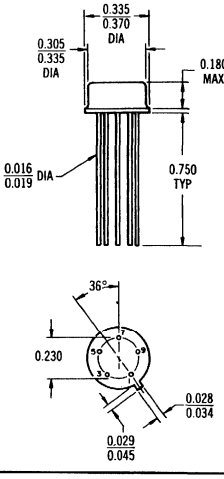
Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

CASE 83 14-LEAD FLAT PACKAGE TO-86

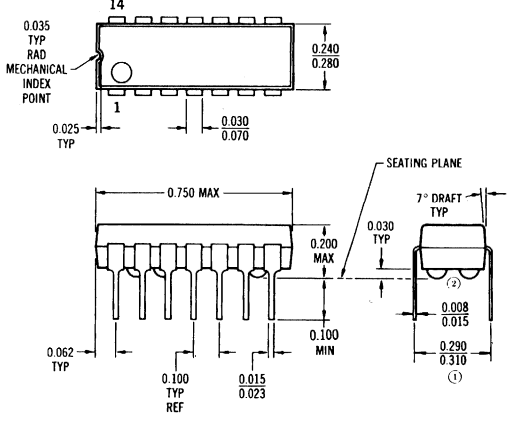


All dimensions are in inches

CASE 89

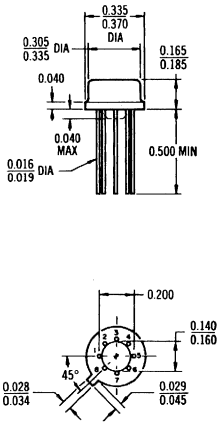


CASE 93 TO-116 PACKAGE



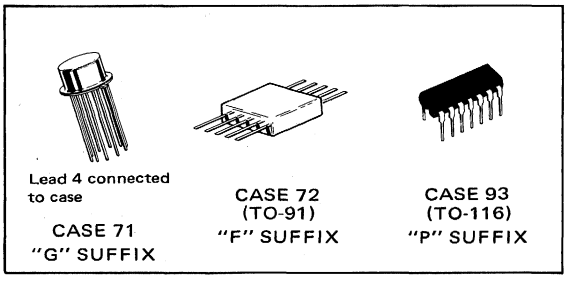
① This dimension is measured at the seating plane.
② 4 insulating stand-offs are provided.

CASE 96 TO-99 PACKAGE



MC1430
MC1431

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



Lead 4 connected to case

CASE 71
"G" SUFFIX

CASE 72
(TO-91)
"F" SUFFIX

CASE 93
(TO-116)
"P" SUFFIX

Typical Amplifier Features:

- High Open Loop Gain — A_{VOL} = 74 dB typical
- Large Output Voltage Swing — Typically ±5.0 V @ ±6.0 V Supply
- Low Output Impedance — Z_{out} = 25 ohms typical
- High Slew Rate — Typically 4.5 V/μs

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+8	Vdc
Power Supply Voltage	V^-	-8	Vdc
Differential Input Signal	V_{in}	±5	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25°C		4.6	mW/°C
Flat Package		500	mW
Derate above 25°C		3.3	mW/°C
Plastic Package		400	mW
Derate above 25°C		3.3	mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}		°C
Metal Can and Flat Package		-55 to +150	
Plastic Package		-55 to +125	

*For full temperature range (-55°C to +125°C) see MC1530-MC1531 data sheet.

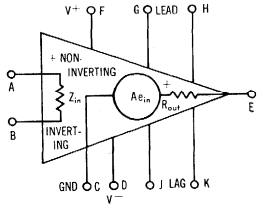


FIGURE 1 - EQUIVALENT CIRCUIT BOTH TYPES

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"F" & "G" Pkgs.	1	2	3	4	5	6	7	8	9	10
"P" Package	4	6	8	7	11	12	13	14	1	2

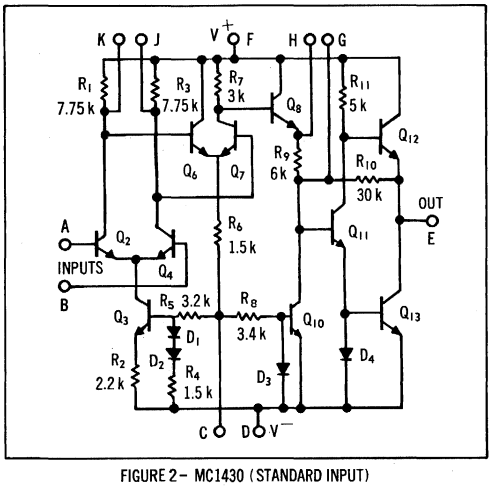


FIGURE 2 - MC1430 (STANDARD INPUT)

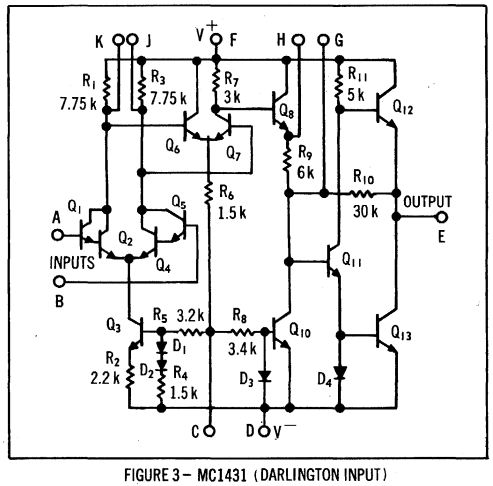
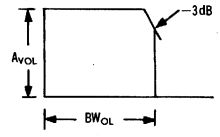
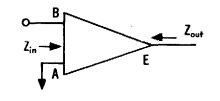
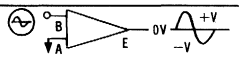
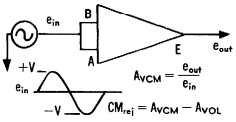
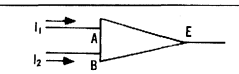
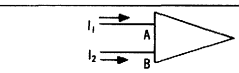
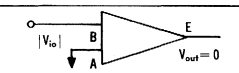


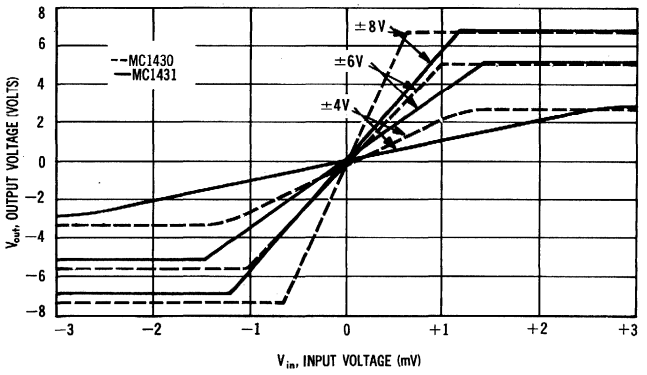
FIGURE 3 - MC1431 (DARLINGTON INPUT)

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions*	Characteristic		Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	MC1430	A_{VOL}	69	74	—	dB
		MC1431		62	71	—	dB
		MC1430		3000	5000	—	V/V
		MC1431		1500	3500	—	V/V
	Open Loop Bandwidth (no roll-off capacitance)	MC1430	BW_{OL}	1.0	1.2	—	MHz
		MC1431		0.15	0.4	—	
	Output Impedance (f = 20 Hz)	MC1430, MC1431	Z_{out}	—	25	50	ohms
	Input Impedance (f = 20 Hz)	MC1430	Z_{in}	5k	15k	—	ohms
		MC1431		300k	600k	—	
	Output Voltage Swing (1000 ohm Load)	MC1430, MC1431	V_{out}	±4.0	±5.0	—	V_{peak}
	Input Common Mode Voltage Swing	MC1430	CMV_{in}	±2.0	±2.5	—	V_{peak}
		MC1431		±2.0	±2.2	—	
	Common Mode Rejection Ratio	MC1430	CM_{rej}	65	75	—	dB
		MC1431		60	75	—	
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$	MC1430	I_b	—	5	15	μA
		MC1431		—	0.1	0.3	
	Input Offset Current $I_{io} = I_1 - I_2$	MC1430	I_{io}	—	0.4	4	μA
		MC1431		—	0.01	0.1	
	Input Offset Voltage	MC1430	$\|V_{io}\|$	—	2	10	mV
		MC1431		—	5	15	
	DC Power Dissipation (Power Supply = ±6 V, V_{out} = 0)		P_D	—	110	150	mW
	Input Offset Voltage						mV
	+75°C	MC1430	$\|V_{io}\|$	—	3.0	12.0	
	0°C			—	3.0	11.0	
	+75°C	MC1431		—	6.0	18.0	
	0°C			—	6.0	16.5	

*All definitions imply linear operation (V_{io} = 0)

FIGURE 4 — NORMALIZED DC OPEN LOOP TRANSFER CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

1. For High Slew Rate use Circuit A, Figure 9
2. For Minimum Noise use Circuit B, Figure 9
3. For operational stability Power Supply decoupling should be employed at all times.
4. Self Biasing network used to hold output voltage less than ±1 volt dc (quiescent)

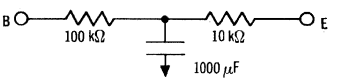
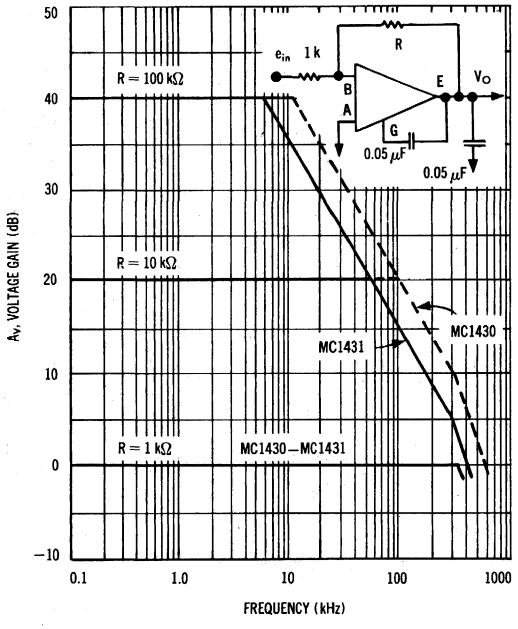


FIGURE 5 — VOLTAGE GAIN versus FREQUENCY

(Rolloff Applied To Output Amplifier)



(Rolloff Applied To Input Differential Amplifier)

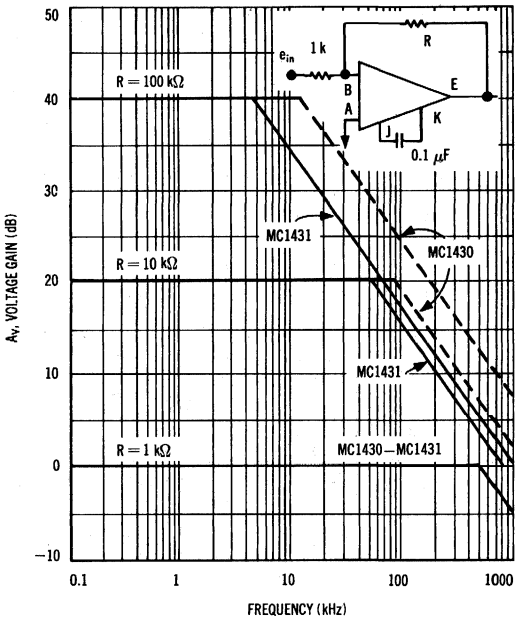


FIGURE 6 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

(Rolloff Applied To Input Differential Amplifier)

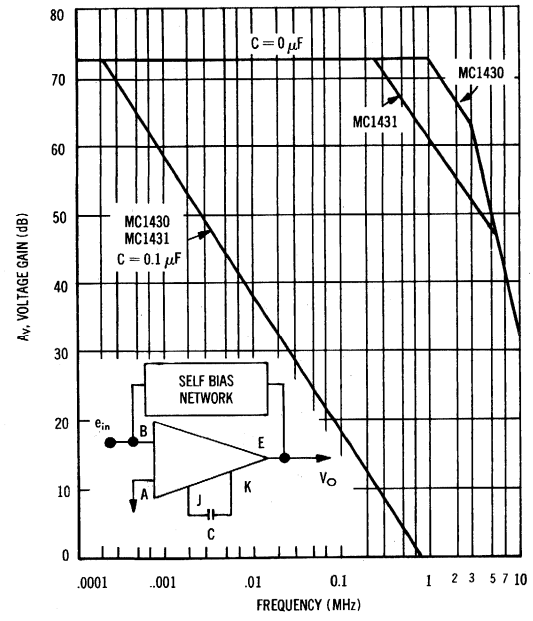


FIGURE 7 — VOLTAGE GAIN versus MINIMUM ROLLOFF CAPACITANCE

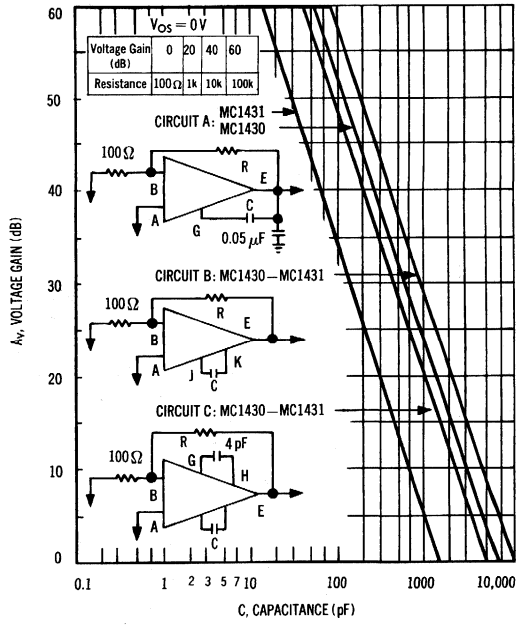
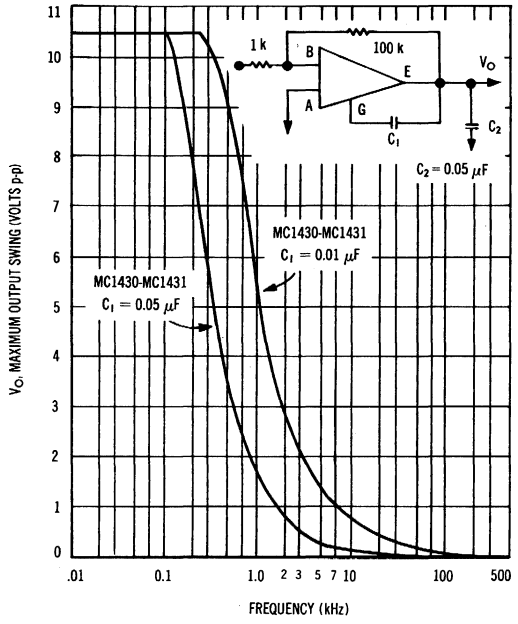


FIGURE 8 — MAXIMUM OUTPUT VOLTAGE SWING versus FREQUENCY

(Rolloff Applied To Output Amplifier)



(Rolloff Applied To Input Differential Amplifier)

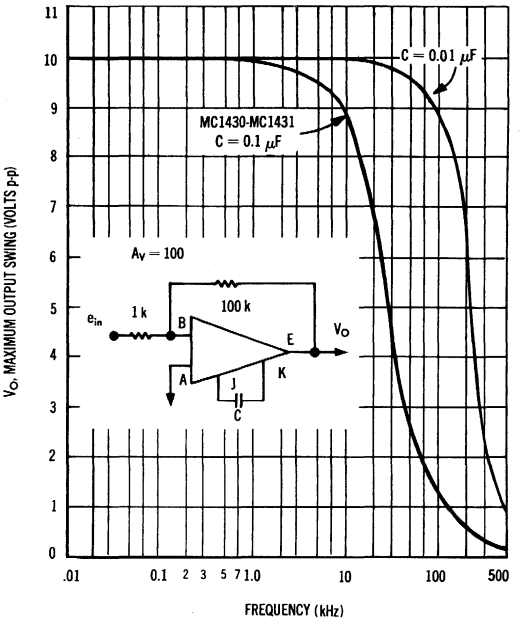


FIGURE 9 — SLEW RATE versus ROLLOFF CAPACITANCE

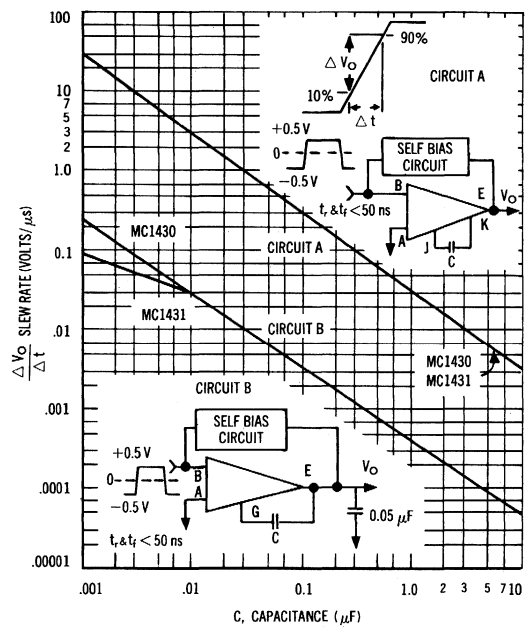
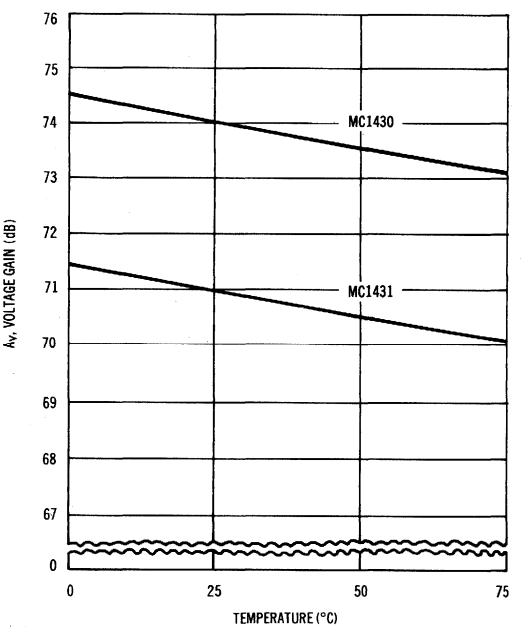
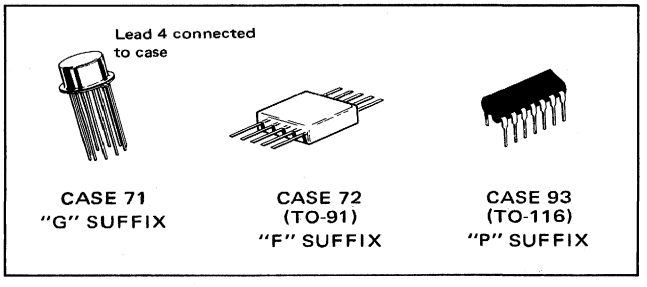


FIGURE 10 — OPEN LOOP VOLTAGE GAIN



MC1433

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



Typical Amplifier Features:

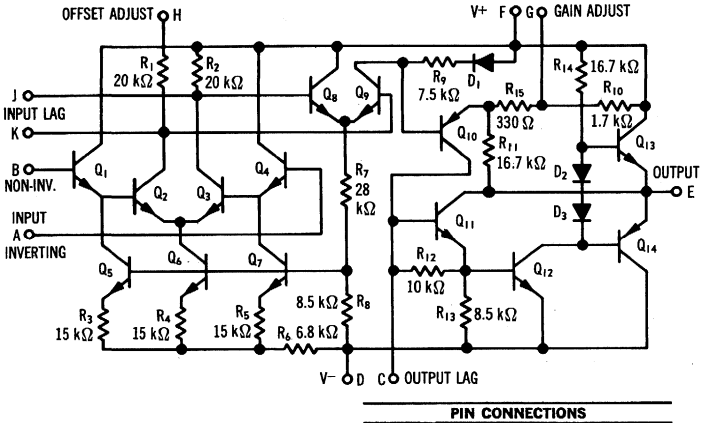
- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 60,000 typical
- Low Temperature Drift – ±8.0 μV/°C
- Large Output Voltage Swing – ±13 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 100 ohms typical
- Input Offset Voltage Adjustable to Zero

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+ V−	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±10	Volts
Common Mode Input Swing	CMV_{in}	±V+	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	1.0	s
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

*For full temperature range (-55°C to +125°C) and characteristic curves, see MC1533 data sheet.

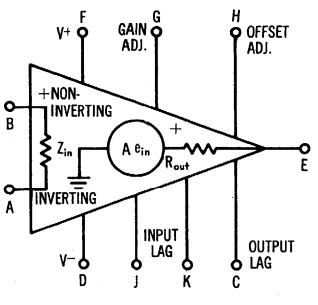
CIRCUIT SCHEMATIC



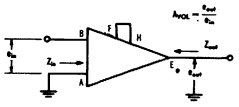
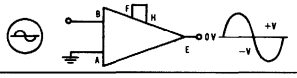
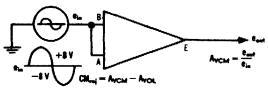
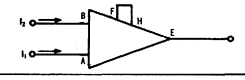
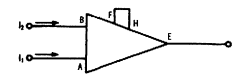
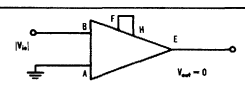
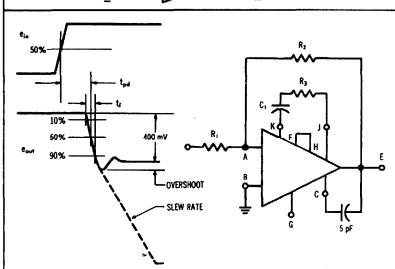
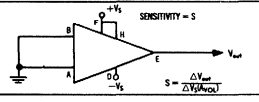
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9
"P" Package	4	5	6	7	11	12	13	14	2	3

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (V @ Pin G = +15 Vdc) (Pin G open) (V @ Pin G = +15 Vdc, $T_A = 0°C$, $+75°C$) (Pin G open, $T_A = 0°C$, $+75°C$)	A_{VOL}	30,000 10,000 20,000 5,000	60,000 30,000 50,000 25,000	- - - -	-
	Output Impedance (Pin G open, f = 20 Hz)	Z_{out}	-	100	150	Ω
	Input Impedance (Pin G open, f = 20 Hz)	Z_{in}	300	600	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±10	±13 ±12	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8	±9	-	V_{peak}
	Common Mode Rejection Ratio (V @ Pin G = +15 Vdc) (Pin G open)	CM_{rej}	80 70	100 94	- -	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$, ($T_A = +25°C$) ($T_A = 0°C$)	I_b	- -	0.5 -	2.0 4.0	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, $T_A = 0°C$) ($I_{io} = I_1 - I_2$, $T_A = +75°C$)	I_{io}	- - -	0.1 - -	0.50 0.75 0.75	μA
	Input Offset Voltage ② ($T_A = 25°C$) ($T_A = 0°C$, $+75°C$)	V_{io}	- -	1.0 -	7.5 10.0	mV
	Step Response Gain = 100, 15% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 100 Ω, C_1 = 0.02 μF Gain = 10, no overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 10 Ω, C_1 = 0.05 μF Gain = 1, 20% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5 Ω, C_1 = 0.1 μF	t_f t_{pd} dV_{out}/dt ③ t_f t_{pd} dV_{out}/dt ③ t_f t_{pd} dV_{out}/dt ③	- - - - - - - - -	0.15 0.06 11.0 0.3 0.1 1.5 0.2 0.3 0.8	- - - - - - - - -	μs μs V/μs μs μs V/μs μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage ($T_A = 0°C$ to $+25°C$) ($T_A = +25°C$ to $+75°C$)	TC_{Vio}	- -	10 8	- -	μV/°C
	Average Temperature Coefficient of Input Offset Current ($T_A = 0°C$ to $+25°C$) ($T_A = +25°C$ to $+75°C$)	TC_{Iio}	- -	0.1 0.05	- -	nA/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	125	240	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	200	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	200	μV/V

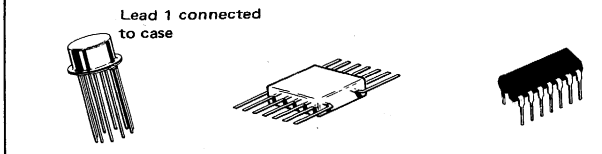
① All definitions imply linear operation

② Input offset voltage (V_{io}) may be adjusted to zero by varying the potential on pin H

③ dV_{out}/dt = Slew Rate

MC1435

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.



CASE 71 "G" SUFFIX

CASE 83 (TO-86) "F" SUFFIX

CASE 93 (TO-116) "P" SUFFIX

Typical Amplifier Features:

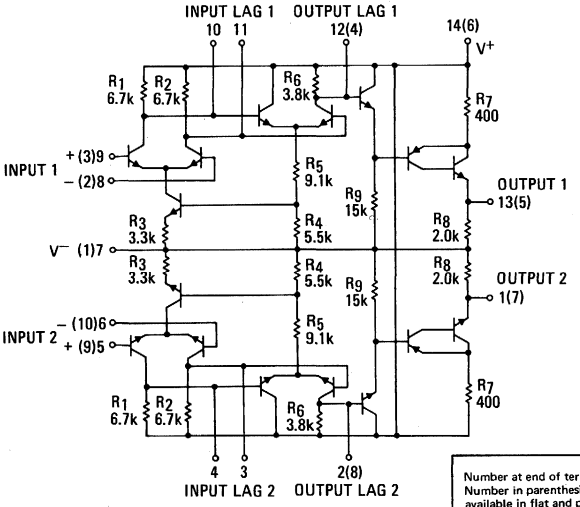
- High Open Loop Gain Characteristics — A_{VOL} = 7,000 typical
- Low Temperature Drift — ±10 μV/°C
- Large Output Voltage Swing — ±3.6 V typ @ ±6.0 V supply
- Low Input Offset Voltage — 1.0 mV
- Low Input Noise Voltage — 0.5 μV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

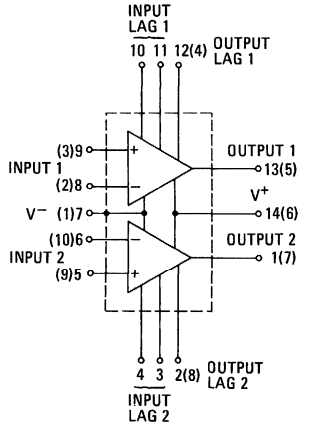
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+9.0 -9.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+5.0 -4.0	Volts
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (package limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

*For full temperature range (-55°C to +125°C) and characteristic curves, see MC1535 data sheet.

CIRCUIT SCHEMATIC

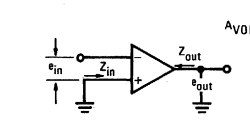
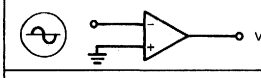
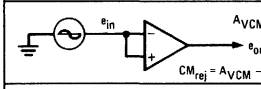
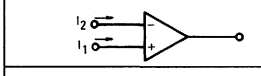
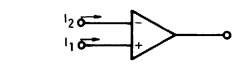
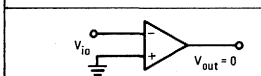
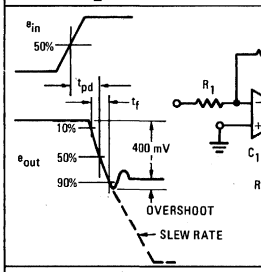
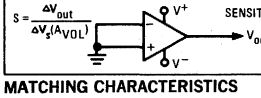


EQUIVALENT CIRCUIT



Number at end of terminal is pin number for both flat and plastic packages. Number in parenthesis is pin number for metal can package. Input lag available in flat and plastic packages.

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V^+ = +6.0Vdc, V^- = −6.0Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (T_A = 0°C to +75°C)	A_{VOL}	3,500 71	7,000 77	- -	V/V dB
	Output Impedance (f = 20 Hz)	Z_{out}	-	1.7	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	10	45	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	5.0	7.0	-	V_{p-p}
	Input Common Mode Voltage Swing	CMV_{in}	+3.0 -2.0	+3.9 -2.7	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	60	90	-	dB
	Input Bias Current $\left(I_b=\frac{I_1+I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	- -	1.2 3.6	5.0 10	μA
	Input Offset Current ($I_{io}=I_1-I_2$) ($I_{io}=I_1-I_2$, T_A = 0°C) ($I_{io}=I_1-I_2$, T_A = +75°C)	I_{io}	- - -	0.05 - -	0.5 1.5 1.5	μA
	Input Offset Voltage (T_A = 25°C) R_S = 50Ω (T_A = 0°C to + 75°C)	V_{io}	- -	1.0 -	5.0 7.5	mV
	Step Response Gain = 100, 30% overshoot, R_1 = 4.7 kΩ, R_2 = 470 kΩ, R_3 = 150 Ω, C_1 = 1,000 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.8 0.1 7.0	- - -	μs μs V/μs
	Gain = 10, 10% overshoot, R_1 = 47 kΩ, R_2 = 470 kΩ, R_3 = 47 Ω, C_1 = 0.01 μF	t_f t_{pd} dV_{out}/dt ①	- - -	0.4 0.3 4.0	- - -	μs μs V/μs
	Gain = 1, 5% overshoot, R_1 = 47 kΩ, R_2 = 47 kΩ R_3 = 4.7 Ω, C_1 = 0.1 μF	t_f t_{pd} dV_{out}/dt ①	- - -	0.5 0.25 0.67	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C)	TC_{Vio}	-	3.0	-	μV/°C
	Average Temperature Coefficient of Input Offset Current (T_A = 0°C to +75°C)	TC_{Iio}		2.0		nA/°C
	DC Power Dissipation (Power Supply = ± 6.0 V, V_{out} = 0)	P_D	-	100	180	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	-	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	100	-	μV/V

MATCHING CHARACTERISTICS

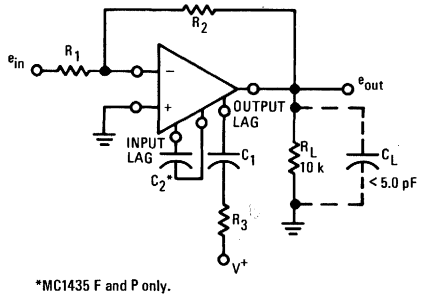
Same characteristic definitions as shown for each amplifier above.	Open Loop Voltage Gain	$A_{VOL1}-A_{VOL2}$	-	±1.0	-	dB
	Input Bias Current	$I_{b1}-I_{b2}$	-	±0.15	-	μA
	Input Offset Current	$I_{io1}-I_{io2}$	-	±0.02	-	μA
	Average Temperature Coefficient	$TC_{Iio1}-TC_{Iio2}$		±0.1		nA/°C
	Input Offset Voltage	$V_{io1}-V_{io2}$	-	±0.1	-	mV
	Average Temperature Coefficient	$TC_{Vio1}-TC_{Io2}$		±0.5		μV/°C
	Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	-	-60	-	dB

① dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

V^+ = +6.0 Vdc, V^- = −6.0 Vdc, T_A = 25°C

FIGURE 1 – TEST CIRCUIT



*MC1435 F and P only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE (mV rms)
2	1	100	4.7 k	470 k	1,000	150	0	1.7
	1A	or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
	2A	or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
		or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
		or 1	47 k	47 k	0	∞	50,000	0.46
4	1	AVOL	100	∞	1,000	150	0	8.1
		or AVOL	100	∞	0	∞	510	8.1
	2	AVOL	100	∞	10,000	47	0	5.5
		or AVOL	100	∞	0	∞	5,000	5.5
	3	AVOL	100	∞	100,000	4.7	0	4.4
		or AVOL	100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

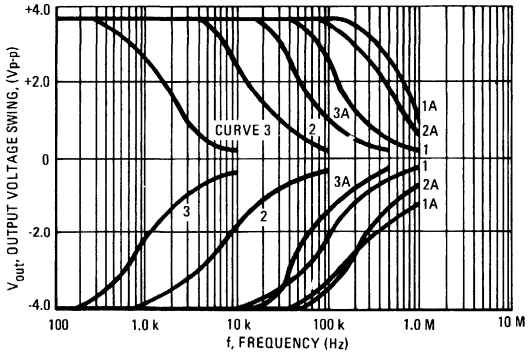


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

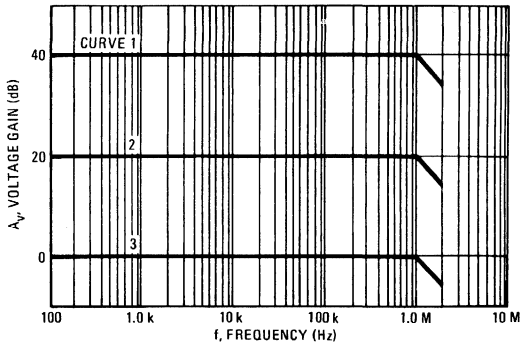


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

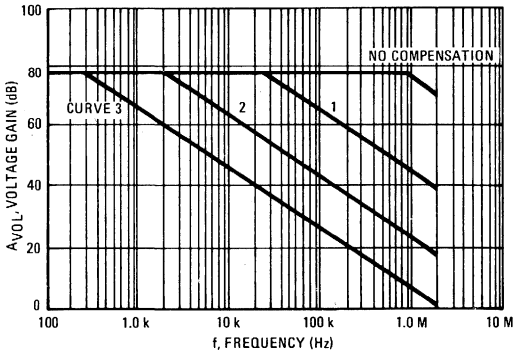


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

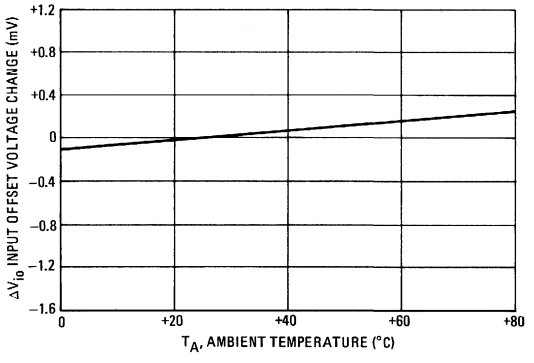


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

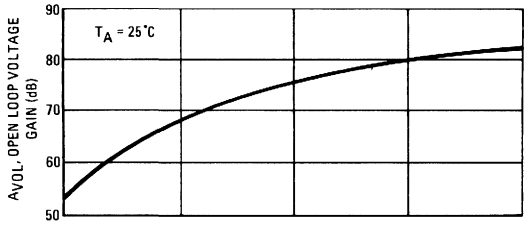


FIGURE 1 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

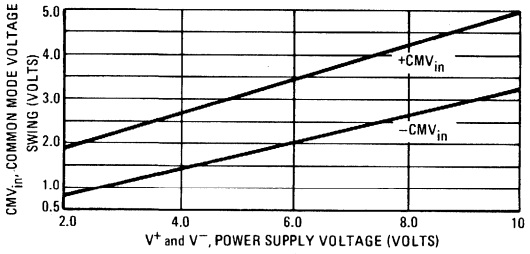


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

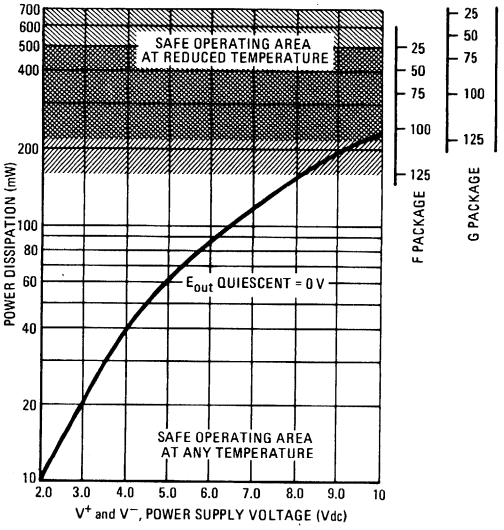
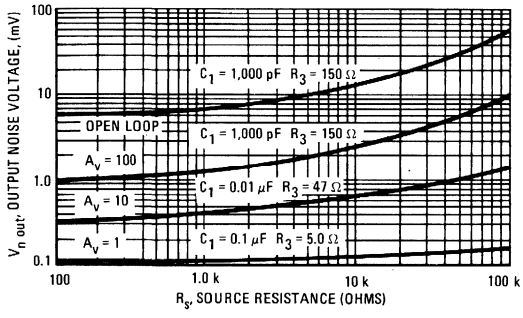


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



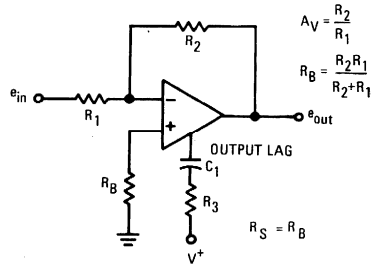
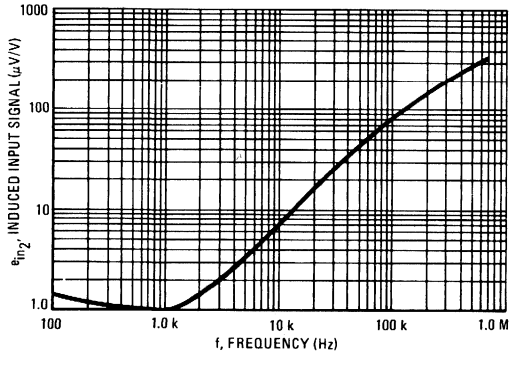
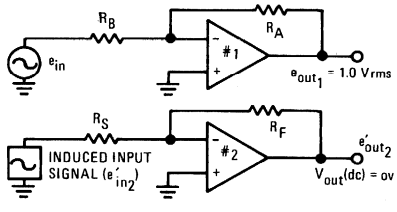


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

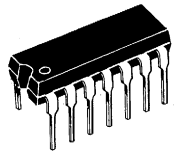
$e'_{out_2} = e'_{in_2} \times \frac{R_F}{R_S}$, where e'_{out_2} is the component of e_{out_2} due only to lack of perfect separation between the two amplifiers.

MC1437P
(DUAL MC1709CP)

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing –
  ±14 V typical @ ±15 V Supply
- Low Output Impedance – Z_{out} = 30 ohms typical

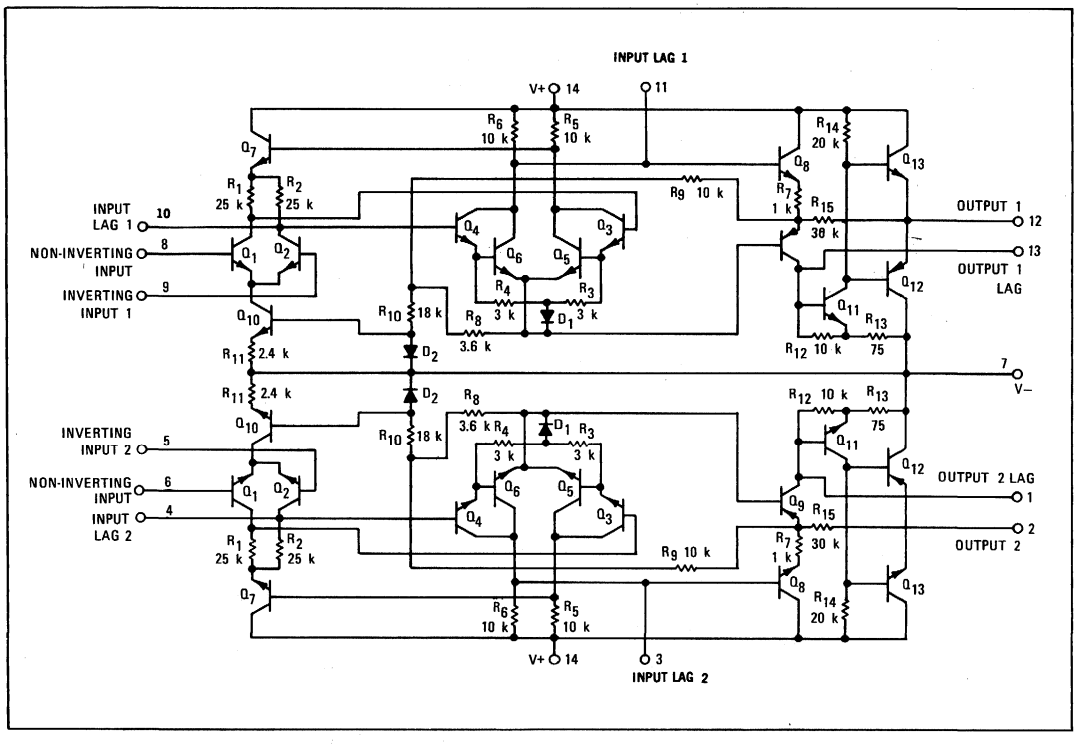


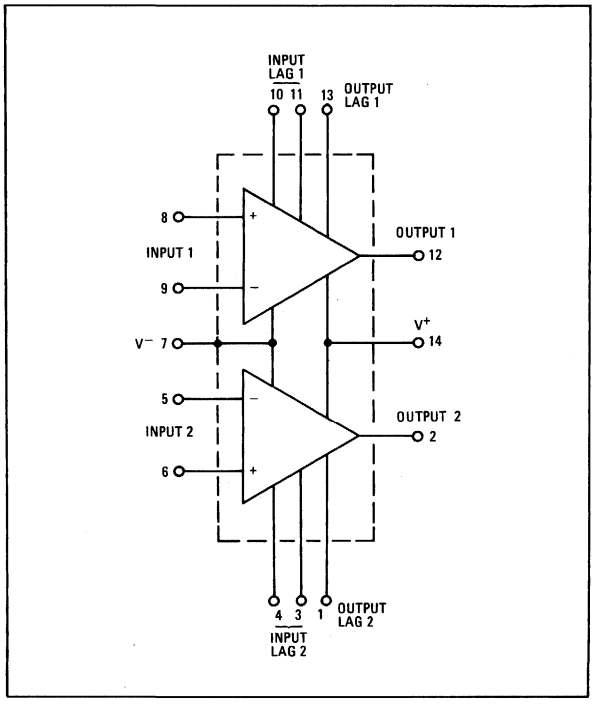
CASE 93
(TO-116)
"P" SUFFIX

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Plastic Package Derate above 25° C	P_D	 415 3.3	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range Plastic Package	T_{stg}	 -65 to +125	°C

CIRCUIT SCHEMATIC

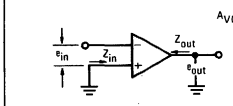
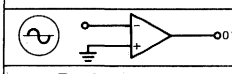
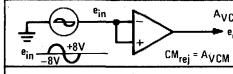
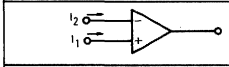
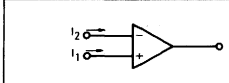
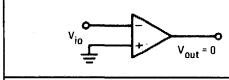
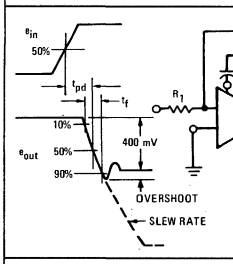
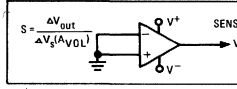




EQUIVALENT CIRCUIT

ELECTRICAL CHARACTERISTICS (each amplifier)

(V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L = 5.0 kΩ, V_{out} = ±10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	45,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	30	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	50	150	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	±12	±14	-	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8.0	±10	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	65	100	-	dB
	Input Bias Current $\left(I_b=\frac{I_1+I_2}{2}\right)$, ($T_A$ = +25°C)	I_b	-	0.4	1.5	μA
	(T_A = 0°C)		-	-	2.0	
	Input Offset Current ($I_{io}=I_1-I_2$)	I_{io}	-	0.05	0.5	μA
	($I_{io}=I_1-I_2$, T_A = 0°C)		-	-	0.75	
	($I_{io}=I_1-I_2$, T_A = +75°C)		-	-	0.75	
	Input Offset Voltage (T_A = 25°C)	V_{io}	-	1.0	7.5	mV
	(T_A = 0°C, +75°C)		-	-	10	
	Step Response					
	Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_f	-	0.8	-	μs
		t_{pd}	-	0.38	-	μs
		dV_{out}/dt ①	-	12	-	V/μs
	Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f	-	0.6	-	μs
		t_{pd}	-	0.34	-	μs
		dV_{out}/dt ①	-	1.7	-	V/μs
	Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f	-	2.2	-	μs
		t_{pd}	-	1.3	-	μs
		dV_{out}/dt ①	-	0.25	-	V/μs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C)	TC_{Vio}	-	1.5	-	μV/°C
	(R_S ≦ 10 kΩ, T_A = 0°C to +75°C)		-	3.0	-	
	Average Temperature Coefficient of Input Offset Current (T_A = 0° to +25°C)	TC_{Iio}	-	0.7	-	nA/°C
	(T_A = +25°C to +75°C)		-	0.7	-	
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	150	225	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	10	200	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	10	200	μV/V

① dV_{out}/dt = Slew Rate

MATCHING CHARACTERISTICS

Same characteristic definitions as shown for each amplifier above.	Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	-	±1.0	-	dB
	Input Bias Current	I_{b1}-I_{b2}	-	±0.15	-	μA
	Input Offset Current	I_{io1}-I_{io2}	-	±0.02	-	μA
	Average Temperature Coefficient	TC_{Iio1}-TC_{Iio2}	-	±0.2		nA/°C
	Input Offset Voltage	V_{io1}-V_{io2}	-	±0.2	-	mV
	Average Temperature Coefficient	TC_{Vio1}-TC_{Io2}		±0.5		μV/°C
	Channel Separation (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	-	90	-	dB

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1–TEST CIRCUIT

$V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25^oC$

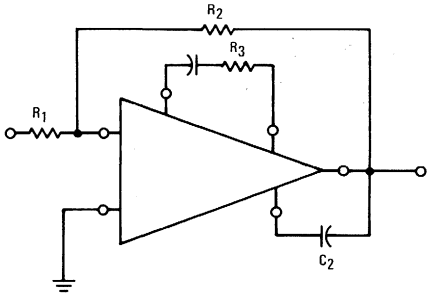


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS					OUTPUT NOISE (mV rms)
			$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)	
2	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
3	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
4	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 2–LARGE SIGNAL SWING versus FREQUENCY

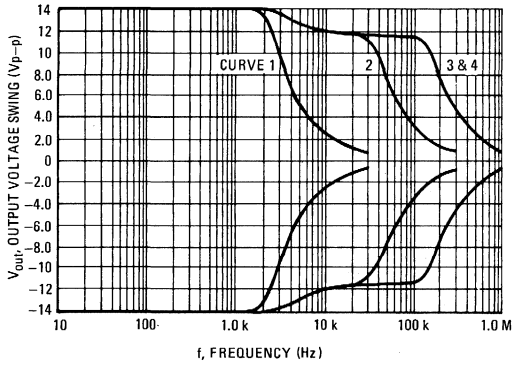


FIGURE 3–VOLTAGE GAIN versus FREQUENCY

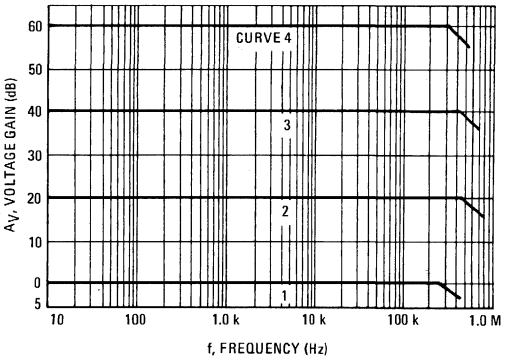


FIGURE 4–OPEN LOOP VOLTAGE GAIN versus FREQUENCY

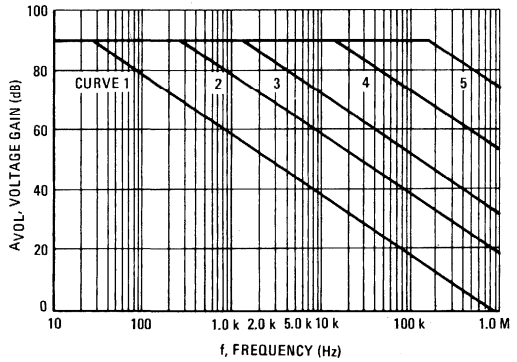


FIGURE 5–POWER DISSIPATION versus POWER SUPPLY VOLTAGE

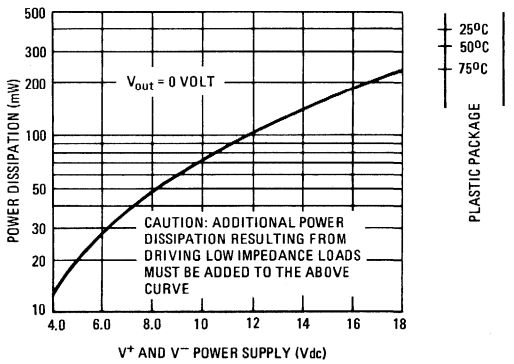


FIGURE 6–VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

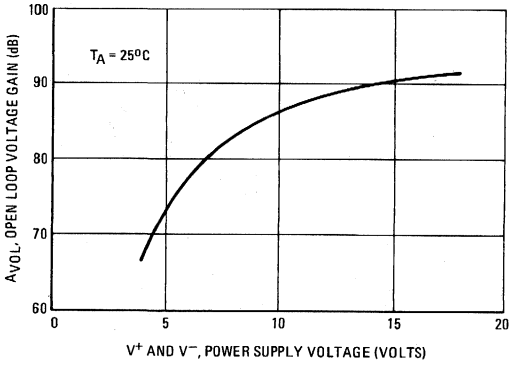


FIGURE 7–COMMON SWING versus POWER SUPPLY VOLTAGE

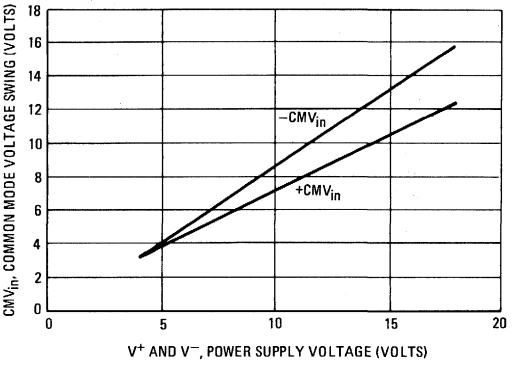


FIGURE 8–INPUT OFFSET VOLTAGE versus TEMPERATURE

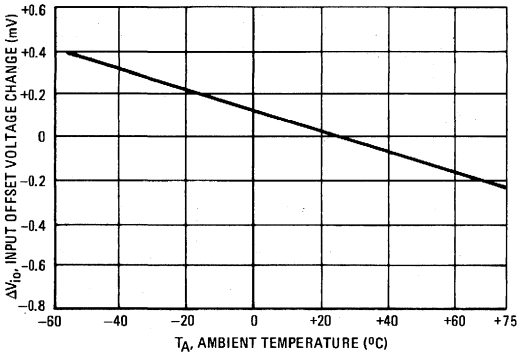


FIGURE 9–OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

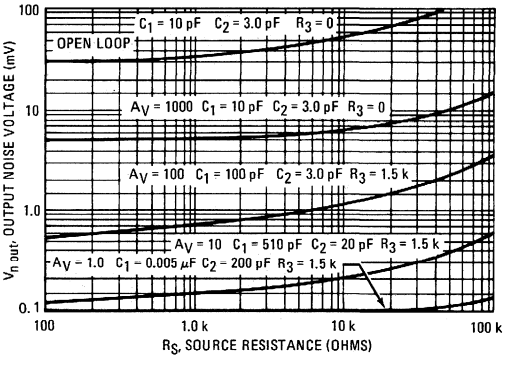
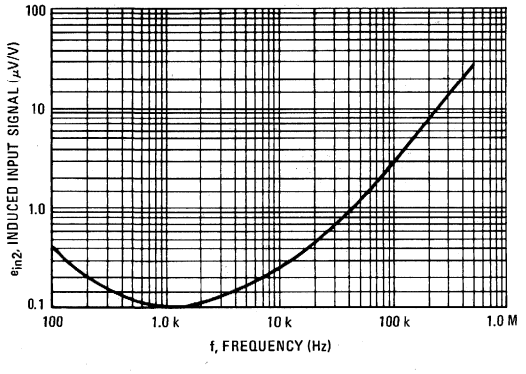
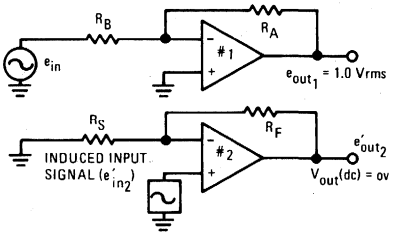


FIGURE 10–INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{out_2} = e'_{in_2}(1 + \frac{R_F}{R_S})$, where e'_{out_2} is the component of e_{out_2} due only to lack of perfect separation between the two amplifiers.

OPERATIONAL AMPLIFIER

MC1439G

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

Typical Amplifier Features:

- Low Input Offset Voltage — 2.0 mV typ
- Low Input Offset Current — 100 nA max
- Large Power-Bandwidth — 20 V_{p-p} Output Swing at 10 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate — 34 V/μs typ



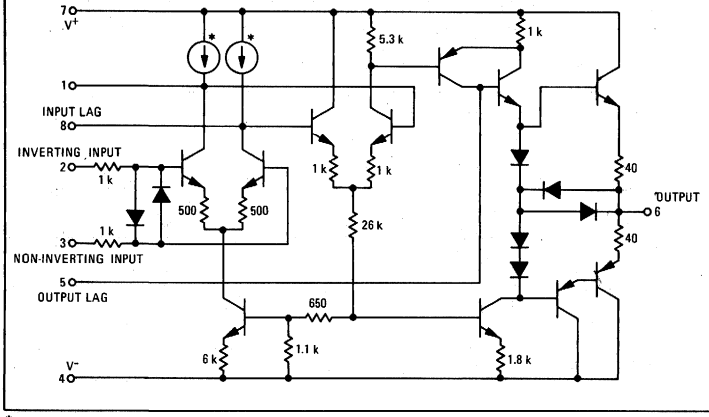
Lead 4 connected to case

CASE 96
(TO-99)
"G" SUFFIX

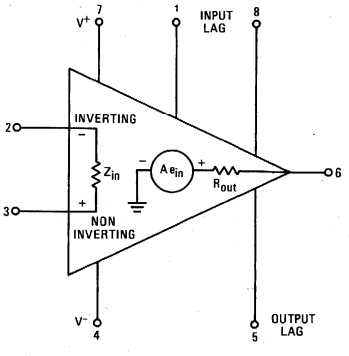
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm V^+$	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC

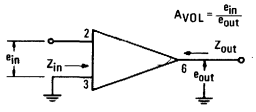
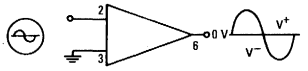
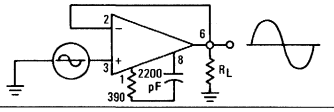
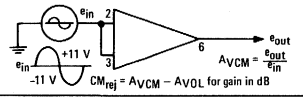
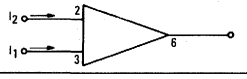
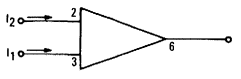
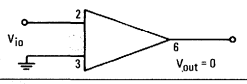
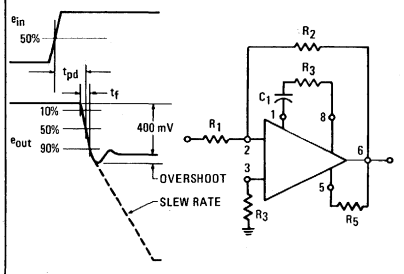
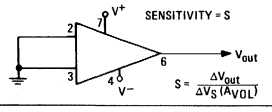


EQUIVALENT CIRCUIT



*PATENT PENDING

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L = 2.0 kΩ, V_{out} = ±10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	100,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	4.0	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	100	300	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2.0 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Power Bandwidth (A_v = 1, R_L = 2.0 kΩ, THD ≦ 5%, V_o = 20 V_{p-p})	P_{BW}	10	50	-	kHz
	Input Common Mode Voltage Swing	CMV_{in}	±11	±12	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	80	100	-	dB
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$, (T_A = +25°C) (T_A = 0°C)	I_b	- -	0.20 0.23	1.0 1.5	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	- - -	20 - -	100 150 150	nA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	- -	2.0 -	7.5 10	mV
	Step Response Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	700 100 34	- - -	ns ns V/μs
	Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = ∞,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	700 100 1.7	- - -	ns ns V/μs
	Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	600 80 6.25	- - -	ns ns V/μs
	Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = ∞,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	600 80 1.7	- - -	ns ns V/μs
	Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = 10 kΩ,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	400 80 4.2	- - -	ns ns V/μs
	Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = ∞,* C_1 = 2200 pF	t_f t_{pd} dV_{out}/dt‡	- - -	400 80 1.4	- - -	ns ns V/μs
	Equivalent Input Noise Voltage (Open Loop) (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	-	30	-	$nV/(Hz)^{1/2}$
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50Ω, T_A = 0°C to +75°C) (R_S ≦ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	- -	3.0 5.0	- -	μV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	90	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	200	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	200	μV/V

*To improve performance, development is in process to include resistor $R_5 \approx 10$ kΩ on the device chip. Available after September 1968.

‡dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = 25°C)

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 1)					
			$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	$R_4(\Omega)$	R_5*(Ω)	C_1(pF)
2	1	1.0	10 k	10 k	5.0 k	390	10 k	2200
	2	1.0	10 k	10 k	5.0 k	390	∞	2200
3	1	A_{VOL}	0	∞	0	∞	∞	0
	2	1000	1000	1.0 M	1000	0	∞	10
	3	100	1000	100 k	1000	10 k	∞	2200
	4	10	1000	10 k	1000	1.0 k	∞	2200
	5	1.0	10 k	10 k	5.0 k	390	∞	2200
4	1	A_{VOL}	0	∞	0	∞	∞	0
	2	A_{VOL}	0	∞	0	10 k	∞	2200
	3	A_{VOL}	0	∞	0	390	∞	2200

*To improve performance, development is in process to include resistor $R_5 \approx 10\ k\Omega$ on the device chip. Available after September 1968.

FIGURE 1 – TEST CIRCUIT

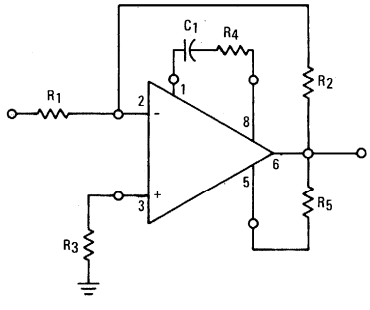


FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

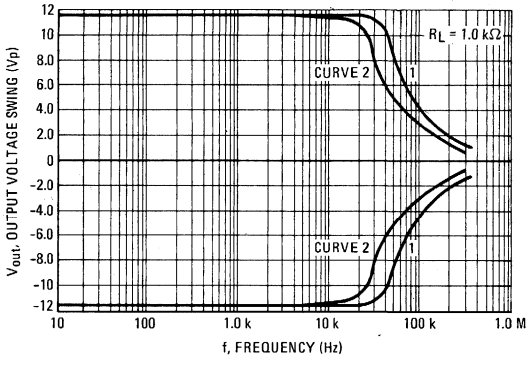


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

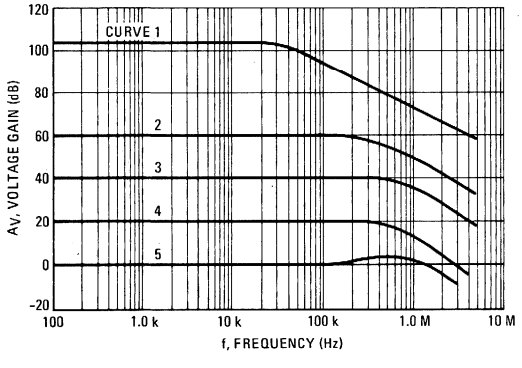


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

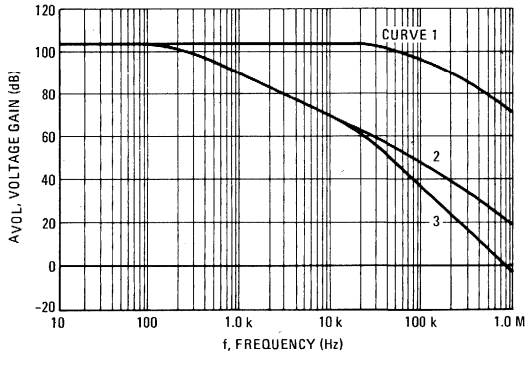


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

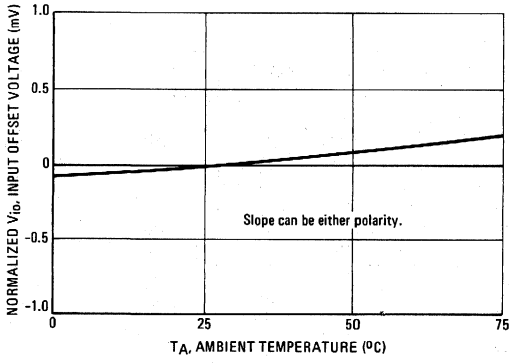


FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

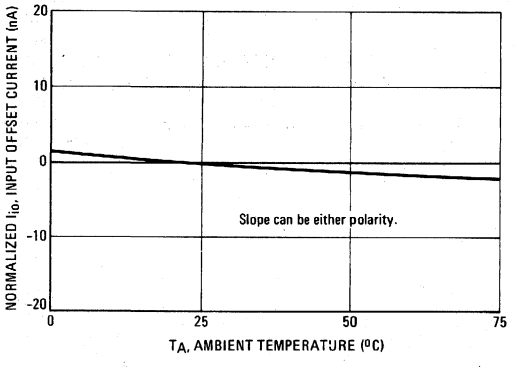


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

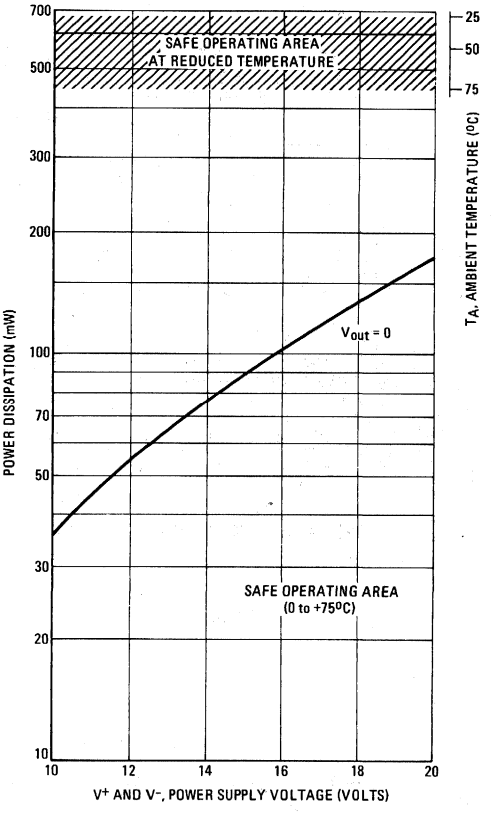


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

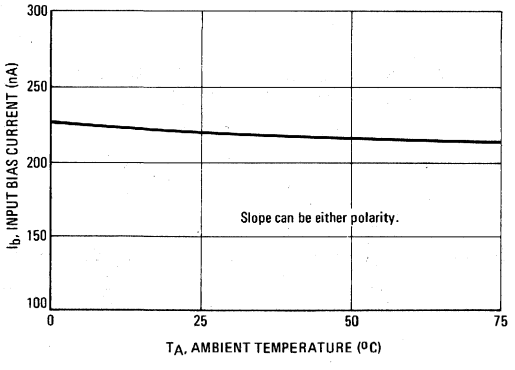
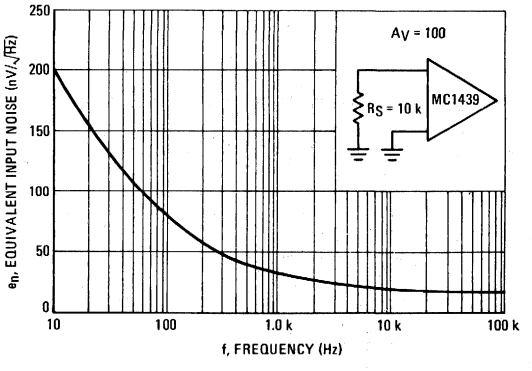


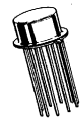
FIGURE 9 – SPECTRAL NOISE DENSITY



OPERATIONAL AMPLIFIER

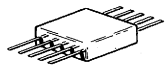
MC1520

. . . designed for use in general-purpose or wide band differential amplifier applications, especially those requiring differential outputs.



Lead 3 connected to case

CASE 71A
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

Typical Characteristics:

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 megohms
- Low Output Impedance; 50 ohms

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Vdc
Differential Input Signal	V_{in}	±8.0	Vdc
Load Current	I_{L1}, I_{L2}	15	mA
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC

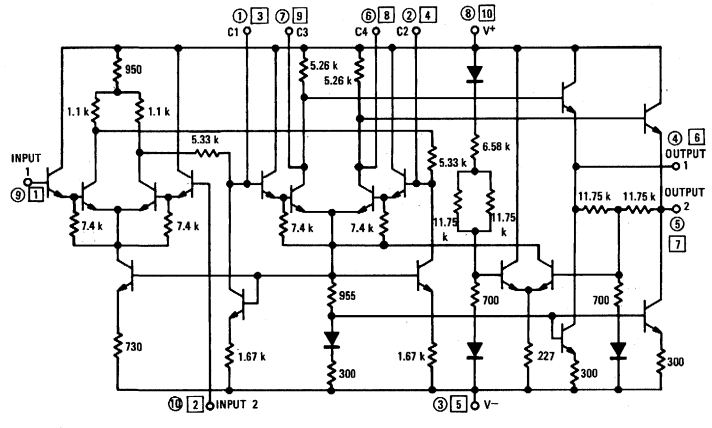
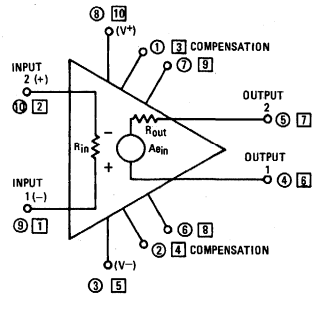
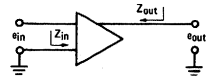
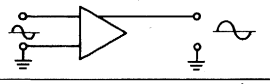
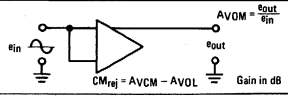
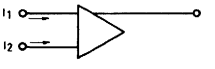
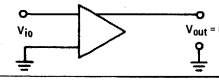
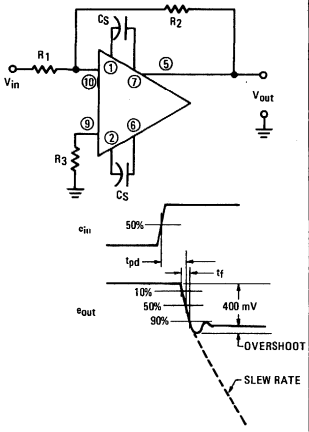
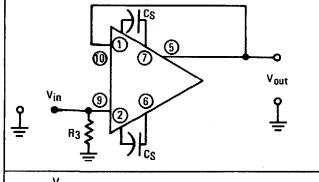
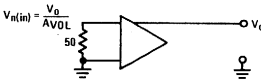


FIGURE 2 – EQUIVALENT CIRCUIT



SINGLE-ENDED ELECTRICAL CHARACTERISTICS

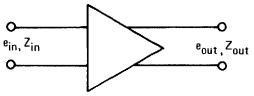
(V^+ = + 6.0 Vdc, V^- = –6.0 Vdc, T_A =25°C unless otherwise noted)

Characteristic Definitions ①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (-55°C ≦ T_A ≦ +125°C)	A_{VOL}	1000 60	1500 64	2500 68	V/V dB
	Output Impedance (f = 20 Hz)	Z_{out}	-	50	100	ohms
	Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	-	megohms
	Output Voltage Swing R_L = 7.0 kΩ (Figure 8)	V_{out}	±3.5	±4.0	-	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±2.0	±3.0	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	75	90	-	dB
	Input Bias Current ($I_b = \frac{I_1 + I_2}{2}$), T_A = +25°C	I_b	-	0.8	2.0	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = -55°C) ($I_{io} = I_1 - I_2$, T_A = +125°C)	I_{io}	- - -	30 - -	100 200 200	nA
	Input Offset Voltage T_A = 25°C	V_{io}	-	5.0	10	mV
	Step Response Gain = 1.0, 10% Overshoot R_1 = 10 kΩ R_2 = 10 kΩ R_3 = 5.0 kΩ C_s = 39 pF	t_f t_{pd} dV_{out}/dt ②	- - -	80 70 5.0	- - -	ns ns V/μs
	Gain = 10, 10% Overshoot R_1 = 10 kΩ R_2 = 100 kΩ R_3 = 10 kΩ C_s = 10 pF	t_f t_{pd} dV_{out}/dt ②	- - -	80 70 15	- - -	ns ns V/μs
	Gain = 100, No Overshoot R_1 = 1.0 kΩ R_2 = 100 kΩ R_3 = 1.0 kΩ C_s = 1.0 pF	t_f t_{pd} dV_{out}/dt ②	- - -	80 70 30	- - -	ns ns V/μs
	Open Loop, No Overshoot R_1 = 50 Ω R_2 = ∞ R_3 = 50 Ω C_s = 0	t_f t_{pd} dV_{out}/dt ②	- - -	180 70 35	- - -	ns ns V/μs
	Bandwidth: Open Loop (Figure 4) Closed Loop (Unity Gain) (Figure 5)	-	- -	2.0 10	- -	MHz
	Input Noise Voltage (Open Loop) (5.0 Hz - 5.0 MHz)	$V_{n(in)}$	-	11	15	μV(rms)
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = -55°C to +125°C)	TCV_{io}	-	2.0	-	μV/°C
	DC Power Dissipation V_{out} = 0	P_D	-	120	240	mW
	Power Supply Sensitivity (V± Constant)	$S^{\pm}$	-	250	450	μV/V

① All definitions imply linear operation. ② dV_{out}/dt = Slew Rate

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

(V^+ = + 6.0 Vdc, V^- = –6.0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Gain (Open Loop)	A_{VOL}	2000 66	3000 70	5000 74	-
	Input Impedance (f = 20 Hz)	Z_{in}	0.5	2.0	-	megohms
	Output Impedance (f = 20 Hz)	Z_{out}	-	100	200	ohms
	Common Mode Output Voltage	$V_{out(CM)}$	-0.5	0	+0.5	Vdc
	Output Voltage Swing R_L = 7.0 kΩ	V_{out}	±7.0	±8.0	-	V_{peak}

TYPICAL OUTPUT CHARACTERISTICS (V^+ = +6.0 Vdc, V^- = –6.0 Vdc, unless otherwise noted)

FIGURE 3 - LARGE SIGNAL SWING versus FREQUENCY

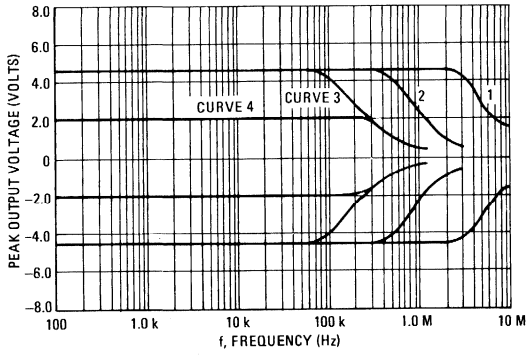
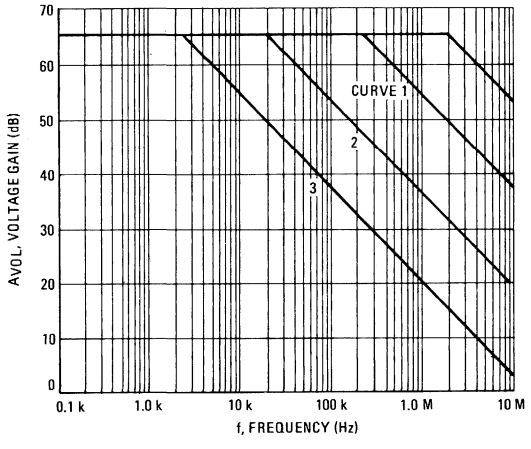


FIGURE 4 - OPEN LOOP VOLTAGE GAIN



TEST CIRCUIT

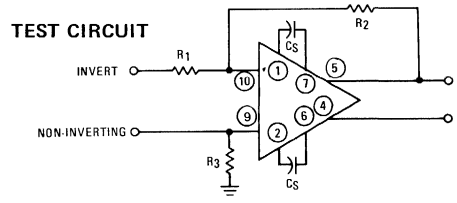
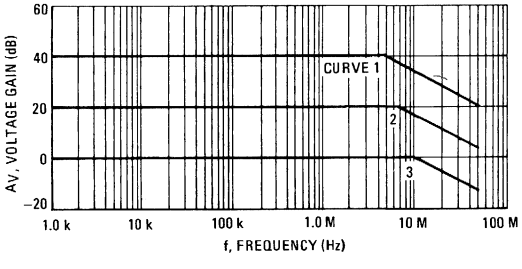


FIGURE NO.	CURVE NO.	MODE	VOLTAGE GAIN	TEST CONDITIONS R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_S (pF)	NOISE OUTPUT mV, rms
3	1	INVERTING	100	1.0 k	100 k	1.0 k	1.0	2.0
	2	INVERTING	10	10 k	100 k	10 k	10	0.55
	3	INVERTING	1.0	10 k	10 k	5.0 k	39	0.17
	4	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17
4	1	NON-INVERTING	A_{VOL}	0	∞	50	1.0	1.0
	2	NON-INVERTING	A_{VOL}	0	∞	50	10	2.0
	3	NON-INVERTING	A_{VOL}	0	∞	50	39	5.2
5	1	NON-INVERTING	100	100	10 k	100	1.0	2.0
	2	NON-INVERTING	10	1.0 k	9.1 k	910	10	0.55
	3	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17

FIGURE 5 - CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



TYPICAL CHARACTERISTICS

FIGURE 6 - POWER DISSIPATION versus POWER SUPPLY VOLTAGE

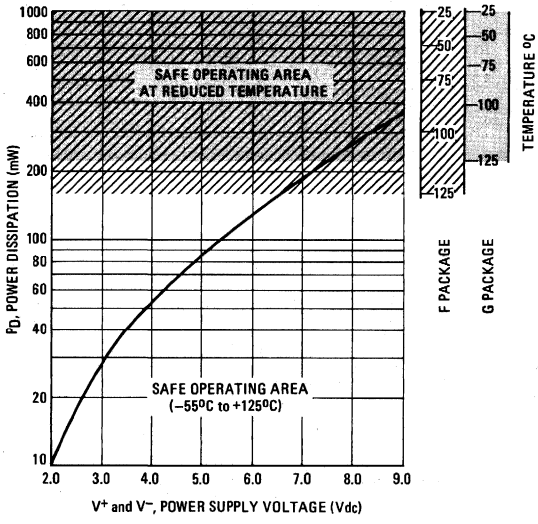


FIGURE 7 - OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

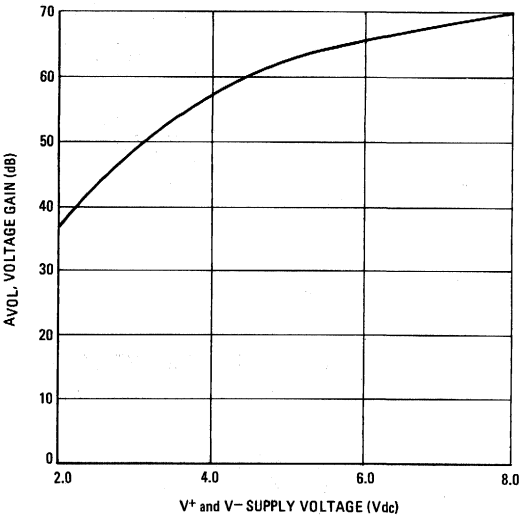


FIGURE 8 - SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

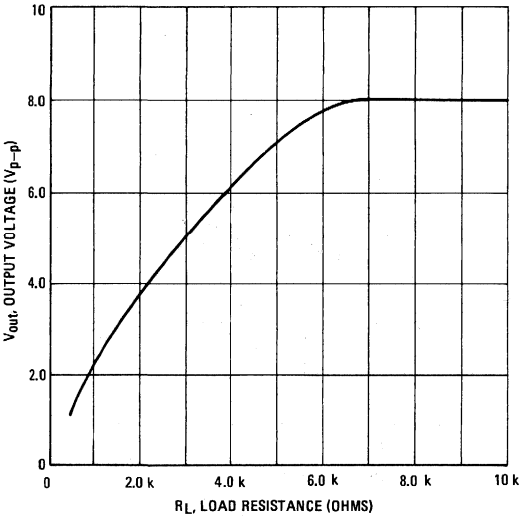
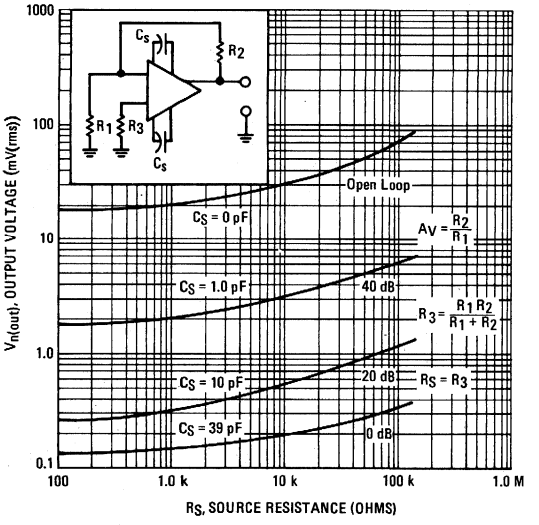
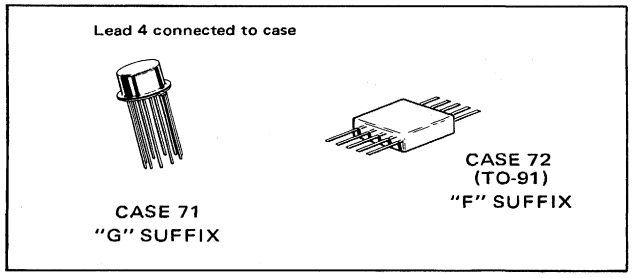


FIGURE 9 - OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



MC1530
MC1531

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



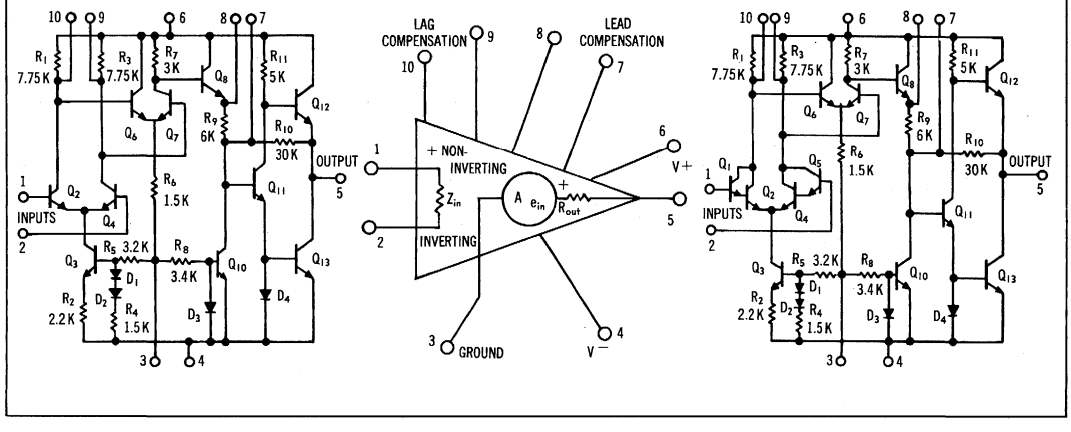
Typical Amplifier Features:

- Excellent Open Loop Gain Characteristics
  A_{VOL} = 74 dB typical
  A_{VOL} stability = ±1.5 dB from -55°C to +125°C
- Low Temperature Drift — ±3.0 μV/°C
- Large Output Voltage Swing — Typically ±5.0 V @ ±6.0 V Supply
- Low Output Impedance — Z_{out} = 25 ohms typical
- High Slew Rate — typically 4.5 V/μs @ A_V = 10

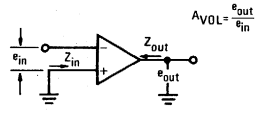
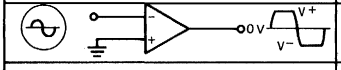
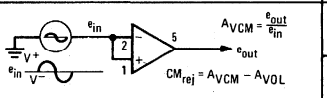
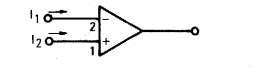
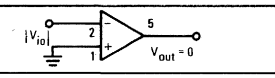
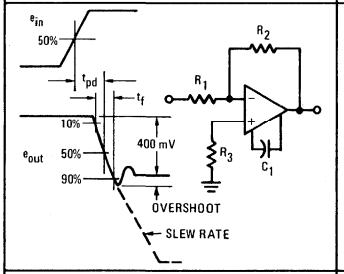
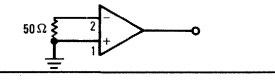
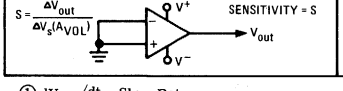
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+9.0	Vdc
Power Supply Voltage	V-	-9.0	Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25+ C		4.6	mW/°C
Flat Package		500	mW
Derate above 25° C		3.3	mW/°C
Operating Temperature Range	T_A	-55 to + 125	°C
Storage Temperature Range	T_{stg}	-65 to + 175	°C

MC1530 (STANDARD INPUT) **EQUIVALENT CIRCUIT (BOTH TYPES)** **MC1531 (DARLINGTON INPUT)**



ELECTRICAL CHARACTERISTICS (V^+ = +6.0Vdc, V^- = −6.0Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic		Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (T_A = -55 to + 125° C)	MC1530 MC1531	A_{VOL}	4500 2500	5000 3500	12500 7000	V/V
		MC1530 MC1531		73 68	74 71	82 77	dB
	Output Impedance (f = 20 Hz)	MC1530 MC1531	Z_{out}	-	25	50	ohms
	Input Impedance (f = 20 Hz)	MC1530 MC1531	Z_{in}	10k 1.0M	20k 2.0M	- -	ohms
	Output Voltage Swing (R_L = 1.0 k ohm)	MC1530 MC1531	V_{out}	±4.5	±5.2	-	V_{peak}
	Input Common Mode Voltage Swing	MC1530 MC1531	CMV_{in}	±2.0 ±2.0	±2.7 ±2.4	- -	V_{peak}
	Common Mode Rejection Ratio	MC1530 MC1531	CM_{rej}	70 65	75 65	- -	dB
	Input Bias Current ($I_b=\frac{I_1+I_2}{2}$)	MC1530 MC1531	I_b	- -	3.0 0.025	10 0.150	µA
	Input Offset Current $I_{io}=I_1-I_2$	MC1530 MC1531	I_{io}	- -	0.200 0.003	2.0 0.025	µA
	Input Offset Voltage	MC1530 MC1531	$\|V_{io}\|$	- -	1.0 3.0	5.0 10	mV
	Step Response Gain = 100, 0% overshoot R_1 = 1.0 k ohm R_2 = 100 k ohm R_3 = 1.0 k ohm C_1 = 1800 pF		t_f t_{pd} dV_{out}/dt ①	- - -	0.60 0.30 17	- - -	µs µs V/µs
	Gain = 10, 10% overshoot R_1 = 10 k ohm R_2 = 100 k ohm R_3 = 10 k ohm C_1 = 6800 pF		t_f t_{pd} dV_{out}/dt ①	- - -	0.24 0.18 4.5	- - -	µs µs V/µs
	Gain = 1.0, 5.0% overshoot R_1 = 10 k ohm R_2 = 10 k ohm R_3 = 5.0 k ohm C_1 = 33,000 pF		t_f t_{pd} dV_{out}/dt ①	- - -	0.20 0.16 1.0	- - -	µs µs V/µs
	Input Noise Voltage (Open Loop, 50 ohm source, BW_{OL} = 5.0 MHz)	MC1530 MC1531	$V_{n(in)}$	- -	10 20	- -	μV_{rms}
	Average Temperature Coefficient of Input Offset Voltage 25°C to + 125° C -55° C to + 25° C 25°C to + 125° C -55° C + 25° C	MC1530 MC1531 	TC_{Vio}	- - - -	3.8 8.0 11 20	- - - -	µV/°C
	D. C. Power Dissipation (Power Supply = ±6.0 V, V_{out} = 0)		P_D	-	110	150	mW
	Positive Supply Sensitivity (V^- constant) Negative Supply Sensitivity (V^+ constant)		S^+ S^-	- -	100 100	- -	µV/V µV/V

① dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

V^+ = +6.0 Vdc, V^- = −6.0 Vdc, T_A = 25°C)

FIGURE 1 – TEST CIRCUIT

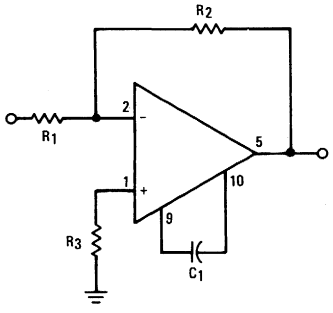


FIG. NO.	CURVE NO.	VOLTAGE GAIN	DEVICE	TEST CONDITIONS				OUTPUT NOISE (mV rms)
				R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	
2	1	100	MC1530	1.0 k	100 k	1.0 k	1800	3.5
		100	MC1531	1.0 k	100 k	1.0 k	1800	3.4
	2	10	MC1530	10 k	100 k	10 k	6800	4.8
		10	MC1531	10 k	100 k	10 k	6800	4.8
	3	1.0	MC1530	10 k	10 k	5.0 k	33000	3.4
		1.0	MC1531	10 k	10 k	5.0 k	33000	7.0
3	1	100	MC1530	1.0 k	100 k	1.0 k	1800	3.5
		100	MC1531	1.0 k	100 k	1.0 k	1800	3.4
	2	10	MC1530	10 k	100 k	10 k	6800	4.8
		10	MC1531	10 k	100 k	10 k	6800	4.8
	3	1.0	MC1530	10 k	10 k	5.0 k	33000	3.4
		1.0	MC1531	10 k	10 k	5.0 k	33000	7.0
4	1	A_{VOL}	MC1530	0	∞	0	1800	7.6
		A_{VOL}	MC1531	0	∞	0	1800	19.0
	2	A_{VOL}	MC1530	0	∞	0	6800	5.5
		A_{VOL}	MC1531	0	∞	0	6800	15.0
	3	V_{VOL}	MC1530	0	∞	0	33000	5.0
		A_{VOL}	MC1531	0	∞	0	33000	11.0

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

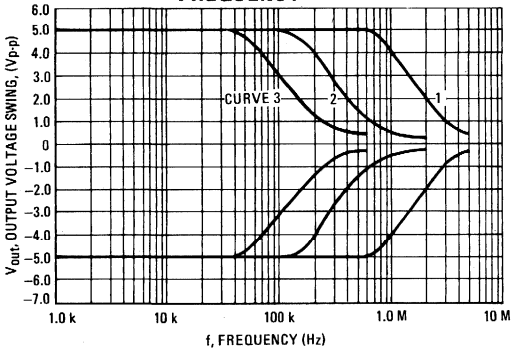


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

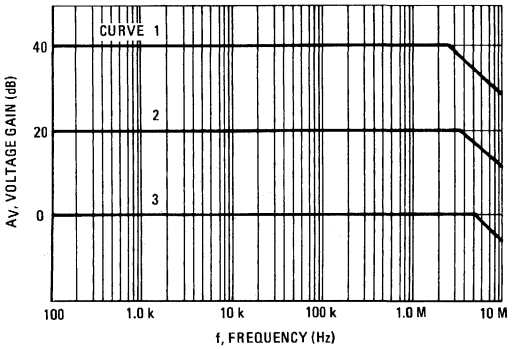


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

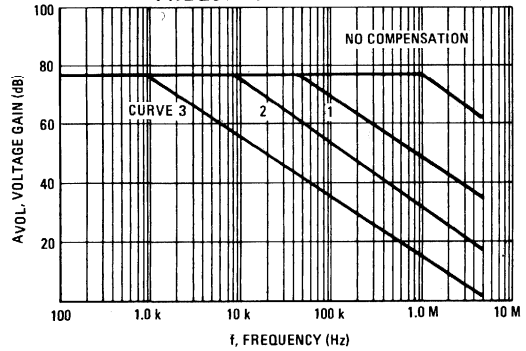


FIGURE 5 – SLEW RATE versus ROLLOFF CAPACITANCE

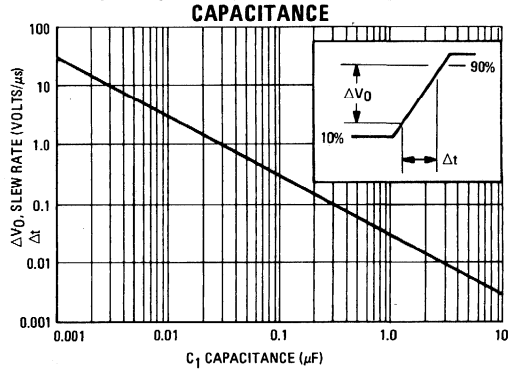


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

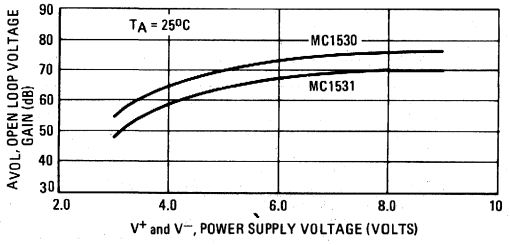


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

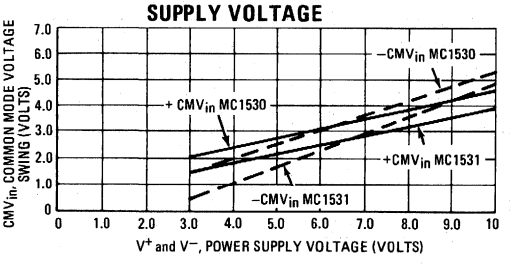


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

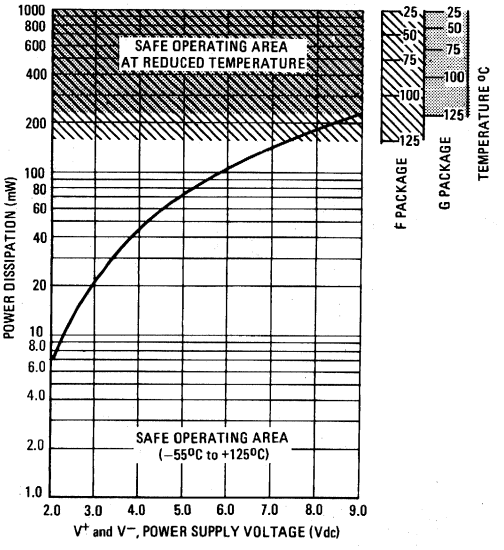
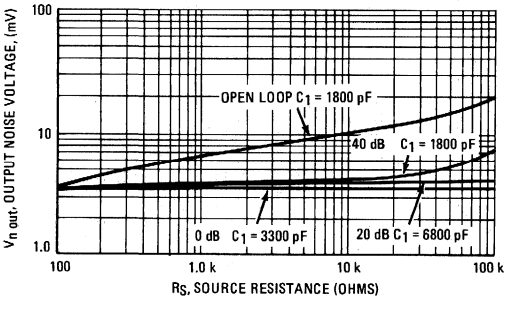


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



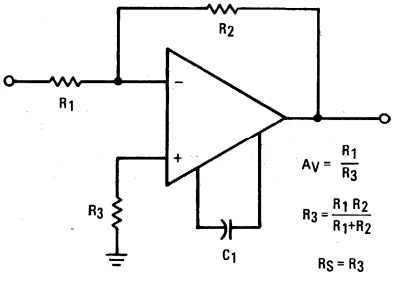
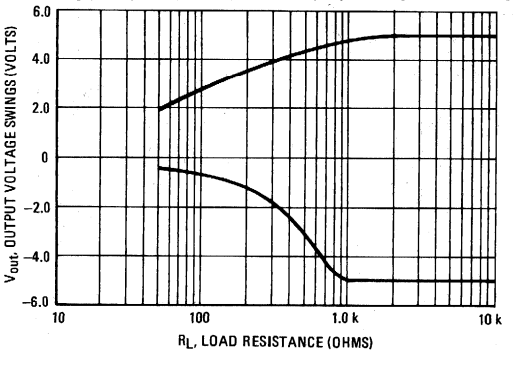
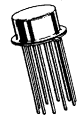


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



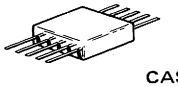
MC1533

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



Lead 4 connected to case

CASE 71
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

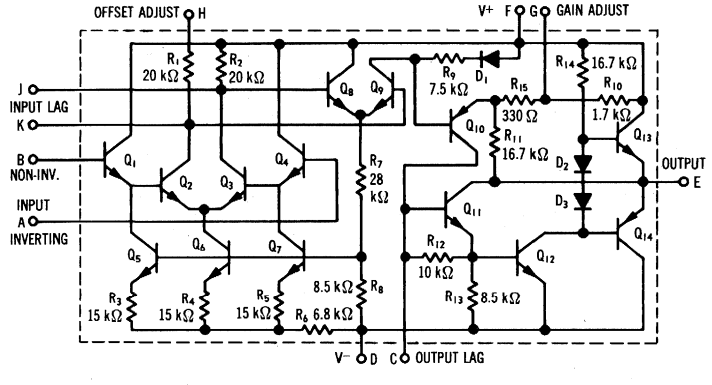
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 60,000 typical
- Low Temperature Drift — ±5.0 μV/°C
- Large Output Voltage Swing — ±13 V Typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 100 ohms typical
- Input Offset Voltage Adjustable to Zero

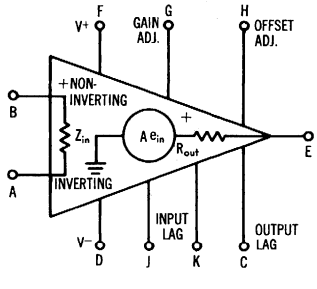
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+20 -20	Vdc Vdc
Differential Input Signal	V_{in}	±10	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	1.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



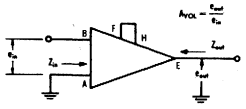
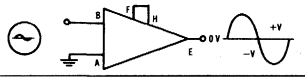
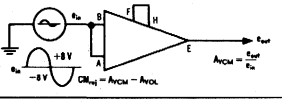
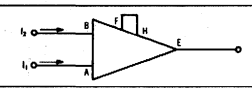
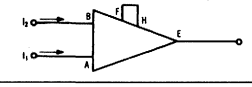
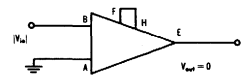
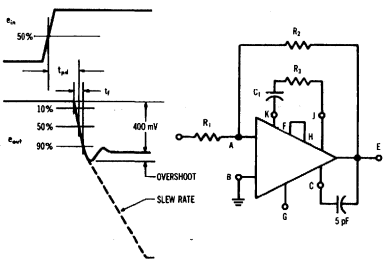
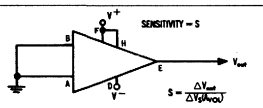
EQUIVALENT CIRCUIT



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions ①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (V @ Pin G = +15 Vdc) (Pin G open) (V@Pin G = +15 Vdc, T_A = -55°C, +125°C) (Pin G open, T_A = -55°C, +125°C)	A_{VOL}	40,000 15,000 35,000 12,000	60,000 30,000 50,000 25,000	150,000 60,000 150,000 60,000	-
	Output Impedance (Pin G open, f = 20 Hz)	Z_{out}	-	100	150	Ω
	Input Impedance (Pin G open, f = 20 Hz)	Z_{in}	500	1000	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±11	±13 ±12	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	+9 -8	+10 -9	- -	V_{peak}
	Common Mode Rejection Ratio (V @ Pin G = +15 Vdc) (Pin G open)	CM_{rej}	90 80	100 94	- -	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C) (T_A = -55°C)	I_b	- -	0.5 -	1.0 3.0	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = -55°C) ($I_{io} = I_1 - I_2$, T_A = +125°C)	I_{io}	- - -	0.03 - -	0.15 0.5 0.2	μA
	Input Offset Voltage ② (T_A = 25°C) (T_A = -55°C, + 125°C)	V_{io}	- -	1.0 -	5.0 6.0	mV
	Step Response {Gain = 100, 15% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 100 Ω, C_1 = 0.002 μF}	t_f t_{pd} dV_{out}/dt ③	- - -	0.15 0.06 11.0	- - -	μs μs V/μs
	{Gain = 10, no overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 10 Ω, C_1 = 0.05 μF}	t_f t_{pd} dV_{out}/dt ③	- - -	0.3 0.1 1.5	- - -	μs μs V/μs
	{Gain = 1, 20% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5 Ω, C_1 = 0.1 μF}	t_f t_{pd} dV_{out}/dt ③	- - -	0.2 0.3 0.8	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage (T_A = -55°C to +25°C) (T_A = +25°C to +125°C)	TC_{Vio}	- -	8.0 5.0	- -	μV/°C
	Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C) (T_A = +25°C to +125°C)	TC_{Iio}	- -	0.1 0.05	- -	nA/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	120	170	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	150	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	150	μV/V

① All definitions imply linear operation

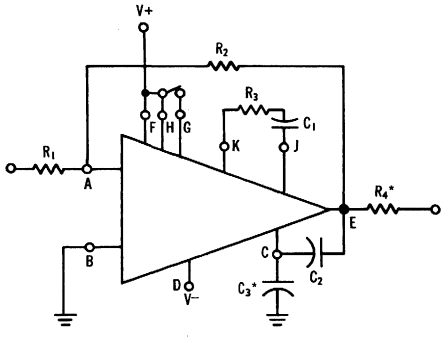
② Input offset voltage (V_{io}) may be adjusted to zero by varying the potential on pin H

③ dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1 — TEST CIRCUIT

$V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$



*FOR CAPACITIVE LOADS, $R_4 = 47\ \Omega$ OR $C_3 = 47$ pF

Fig. No.	Curve No.	Test Conditions					
		$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1	C_2(pF)	C_3(pF)
2	1	10k	10k	5	1 μF	10	47
	2	10k	100k	10	0.1 μF	10	47
	3	1k	1M	510	820 pF	10	47
	3	10k	1M	100	0.05 μF	10	47
	4	1k	1M	100	0.05 μF	3	47
	4	1k	1M	510	820 pF	3	47
3	1 (Low Gain)	1k	1M	10	1000 pF	10	47
	1 (High Gain)	1k	1M	510	820 pF	10	47
	2 (Low Gain)	10k	1M	10	0.01 μF	10	47
	2 (High Gain)	10k	1M	100	0.01 μF	10	47
	3 (Low Gain)	10k	100k	10	0.1 μF	10	47
	3 (High Gain)	10k	100k	10	0.1 μF	10	47
	4 (Low Gain)	10k	10k	10	1 μF	10	47
	4 (High Gain)	10k	10k	5	1 μF	10	47
4	1	0	∞	10	1 μF	10	47
	2	0	∞	10	0.1 μF	10	47
	3	0	∞	10	0.01 μF	10	47
	4	0	∞	10	1000 pF	10	47
	5	0	∞	10	100 pF	10	47
5	1	0	∞	10	1 μF	10	47
	2	0	∞	10	0.1 μF	10	47
	3	0	∞	10	0.01 μF	10	47
	4	0	∞	10	1000 pF	10	47
	5	0	∞	10	100 pF	10	47

FIGURE 2 — LARGE-SIGNAL SWING versus FREQUENCY

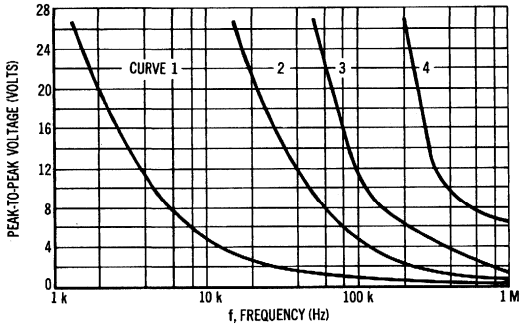


FIGURE 3 — VOLTAGE GAIN versus FREQUENCY

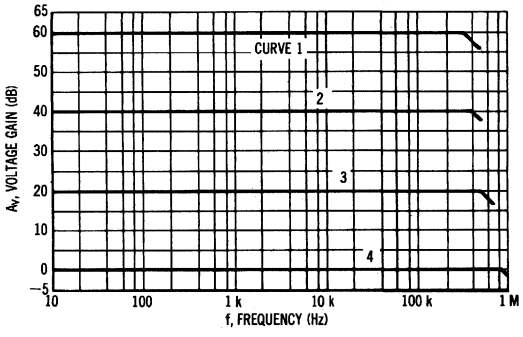


FIGURE 4 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(LOW GAIN CONFIGURATION)

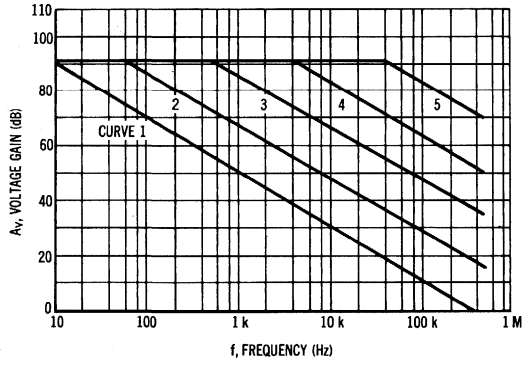
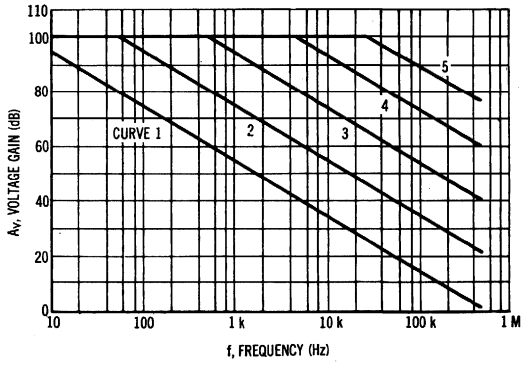


FIGURE 5 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(HIGH GAIN CONFIGURATION)



TYPICAL CHARACTERISTICS

FIGURE 6 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

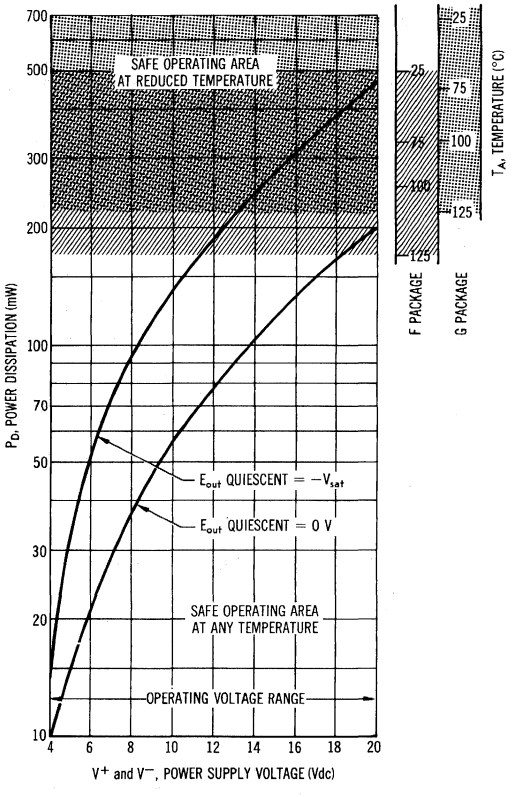


FIGURE 7 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

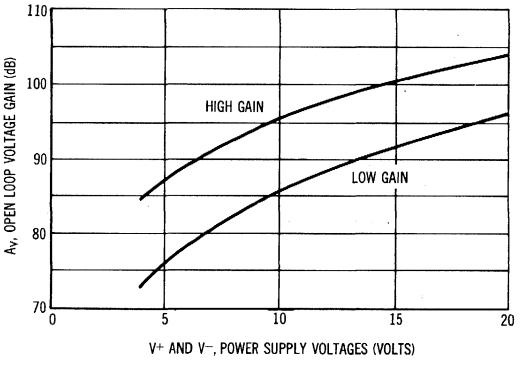


FIGURE 8 — COMMON MODE SWING versus POWER SUPPLY VOLTAGE

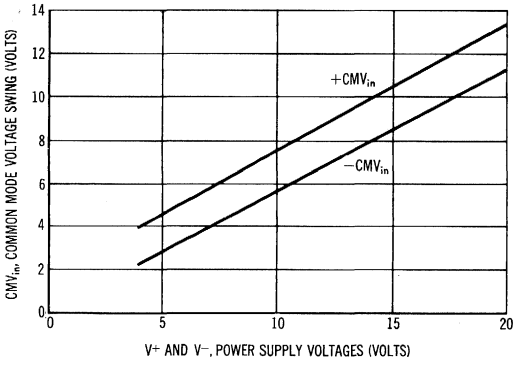


FIGURE 9 — INPUT OFFSET VOLTAGE versus TEMPERATURE

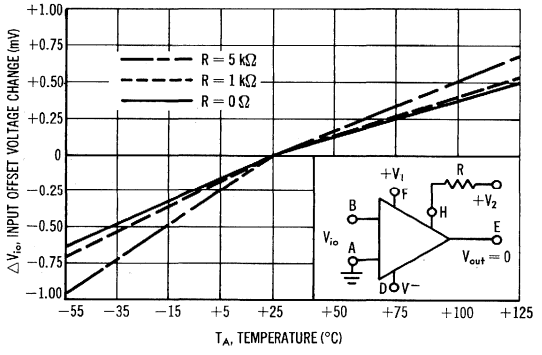
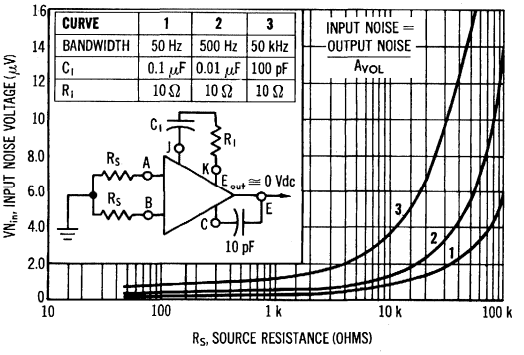
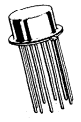


FIGURE 10 — INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



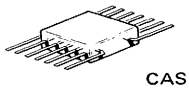
MC1535

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.



Lead 1 connected to case

CASE 71
"G" SUFFIX



CASE 83
(TO-86)
"F" SUFFIX

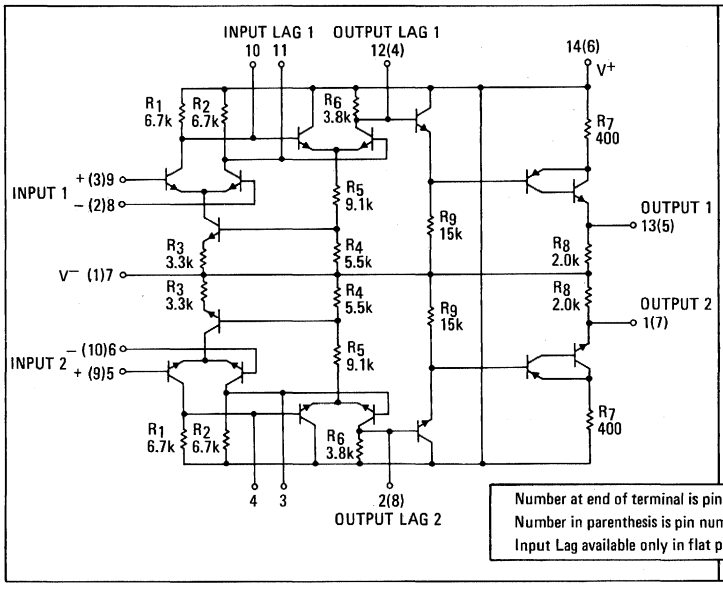
Typical Amplifier Features:

- High Open Loop Gain Characteristics – A_{VOL} = 7,000 typical
- Low Temperature Drift – ±10 μV/°C
- Large Output Voltage Swing – ±3.6 V Typ @ ±6.0 V supply
- Low Input Offset Voltage – 1.0 mV
- Low Input Noise Voltage – 0.5 μV

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

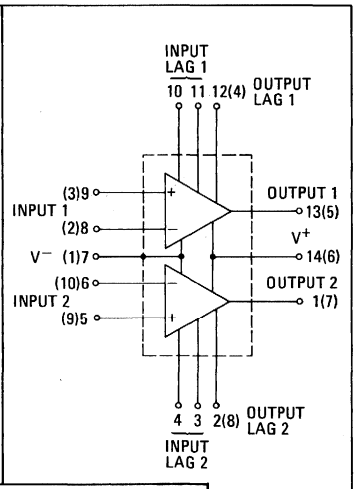
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC

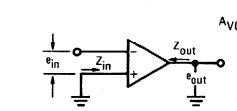
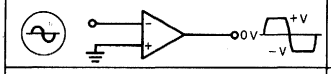
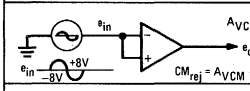
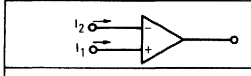
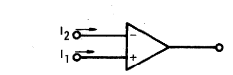
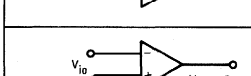
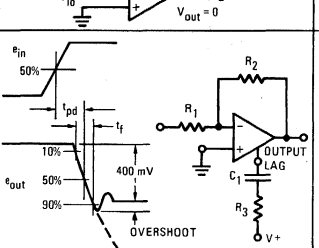
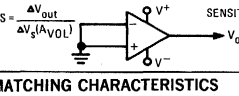


Number at end of terminal is pin number for flat package.
Number in parenthesis is pin number for metal can package.
Input Lag available only in flat package.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Each Amplifier) (V^+ = +6.0Vdc, V^- = −6.0Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (T_A = -55°C to +125°C)	A_{VOL}	4,000 72	7,000 77	10,000 80	V/V dB
	Output Impedance (f = 20 Hz)	Z_{out}	-	1.7	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	10	45	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	±3.3	±3.6	-	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	+3.0 -2.0	+3.9 -2.7	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	70	90	-	dB
	Input Bias Current $\left(I_b=\frac{I_1+I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = -55°C)	I_b	- -	1.2 3.6	3.0 6.0	μA
	Input Offset Current ($I_{io}=I_1-I_2$) ($I_{io}=I_1-I_2$, T_A = -55°C) ($I_{io}=I_1-I_2$, T_A = +125°C)	I_{io}	- - -	0.05 - -	0.3 0.9 0.3	μA
	Input Offset Voltage (T_A = 25°C) (T_A = -55°C + 125°C)	V_{io}	- -	1.0 -	3.0 5.0	mV
	Step Response Gain = 100, 30% overshoot, R_1 = 4.7 kΩ, R_2 = 470 kΩ, R_3 = 150 Ω, C_1 = 1,000 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.8 0.1 7.0	- - -	μs μs V/μs
	Gain = 10, 10% overshoot, R_1 = 47 kΩ, R_2 = 470 kΩ, R_3 = 47 Ω, C_1 = 0.01 μF	t_f t_{pd} dV_{out}/dt ①	- - -	0.4 0.3 4.0	- - -	μs μs V/μs
	Gain = 1, 5% overshoot, R_1 = 47 kΩ, R_2 = 47 kΩ R_3 = 4.7 Ω, C_1 = 0.1 μF	t_f t_{pd} dV_{out}/dt ①	- - -	0.5 0.25 0.67	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 55°C to +125°C)	TC_{Vio}	-	3.0	-	μV/°C
	Average Temperature Coefficient of Input Offset Current (T_A =-55°C to +125°C)	TC_{Iio}		2.0		nA/°C
	DC Power Dissipation (Power Supply = ± 6.0 V, V_{out} = 0)	P_D	-	100	150	mW
$S=\frac{\Delta V_{out}}{\Delta V_s(A_{VOL})}$ 	Positive Supply Sensitivity (V^- constant)	S^+	-	50	-	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	100	-	μV/V

MATCHING CHARACTERISTICS

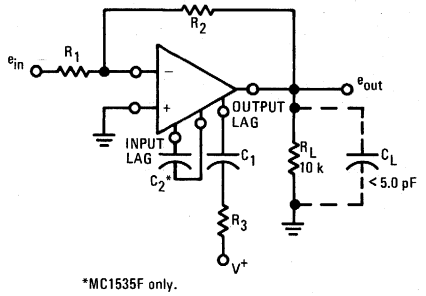
Same characteristic definitions as shown for each amplifier above.	Open Loop Voltage Gain	$A_{VOL1}-A_{VOL2}$	-	±1.0	-	dB
	Input Bias Current	$I_{b1}-I_{b2}$	-	±0.15	-	μA
	Input Offset Current	$I_{io1}-I_{io2}$	-	±0.02	-	μA
	Average Temperature Coefficient	$TC_{Iio1}-TC_{Iio2}$		±0.1		nA/°C
	Input Offset Voltage	$V_{io1}-V_{io2}$	-	±0.1	-	mV
	Average Temperature Coefficient	$TC_{Vio1}-TC_{Vio2}$		±0.5		mV/°C
	Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{out\ 1}}{e_{out\ 2}}$	-	-60	-	dB

① dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

$V^+ = +6.0$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25°C$

FIGURE 1 – TEST CIRCUIT



*MC1535F only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	C_1(pF)	$R_3(\Omega)$	C_2(pF)	OUTPUT NOISE (mV rms)
2	1	100	4.7 k	470 k	1,000	150	0	1.7
	1A	or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
	2A	or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
	1A	or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
	2A	or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
4	1	AVOL	100	∞	1,000	150	0	8.1
	1A	or AVOL	100	∞	0	∞	510	8.1
	2	AVOL	100	∞	10,000	47	0	5.5
	2A	or AVOL	100	∞	0	∞	5,000	5.5
	3	AVOL	100	∞	100,000	4.7	0	4.4
	3A	or AVOL	100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

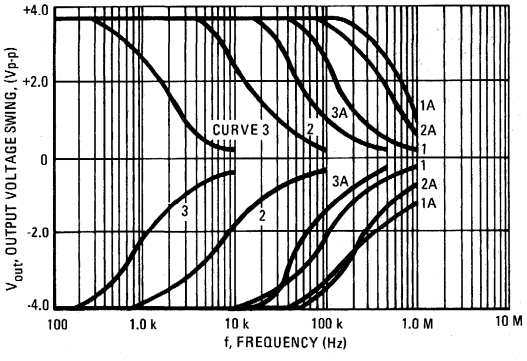


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

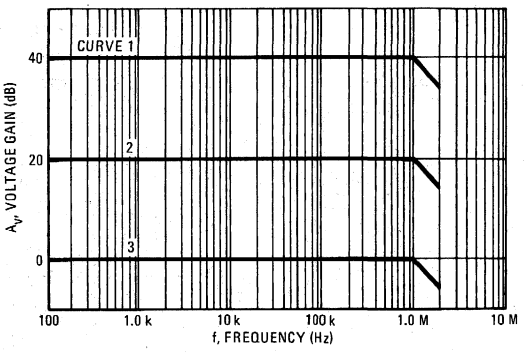


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

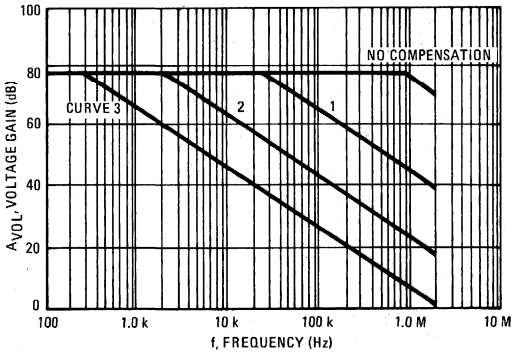


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

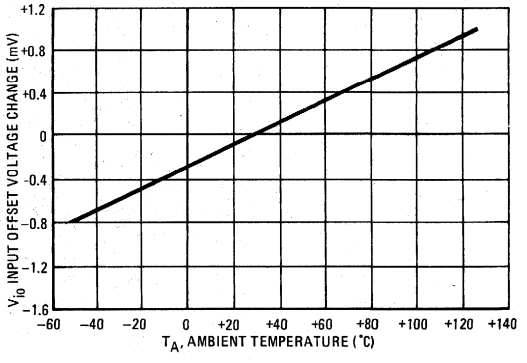


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

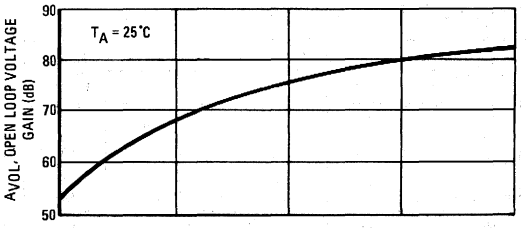


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

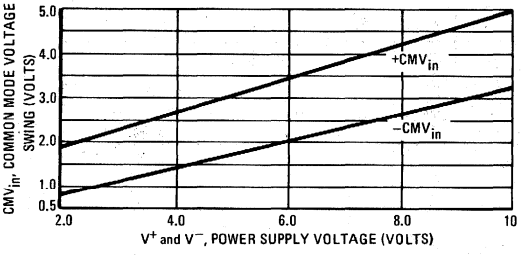


FIGURE 8 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

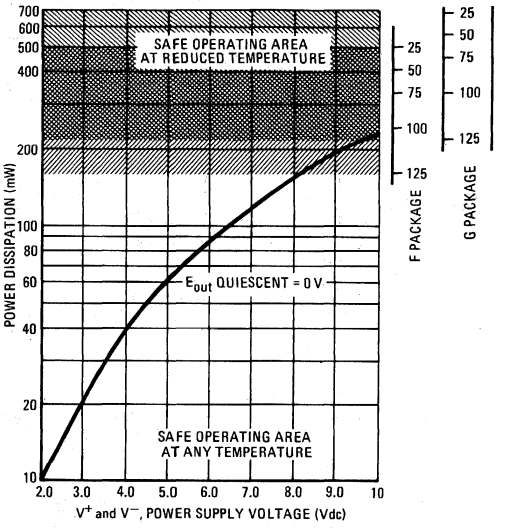
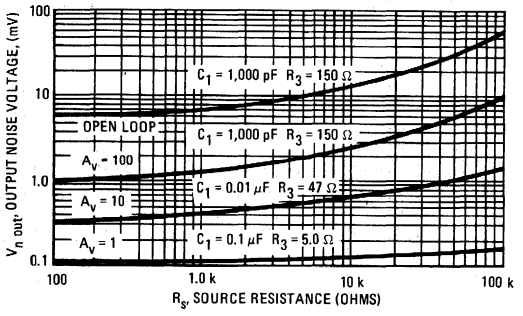


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



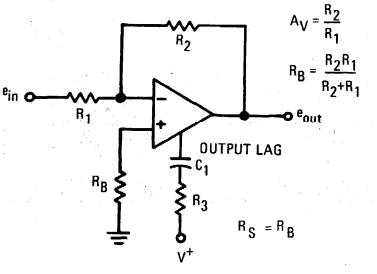
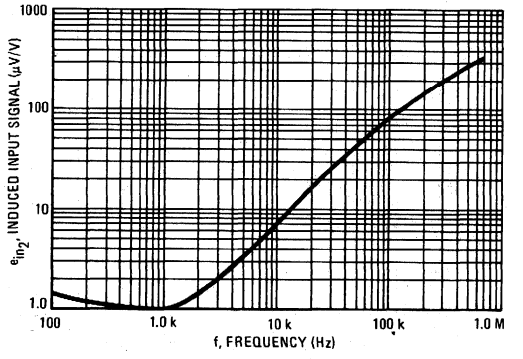
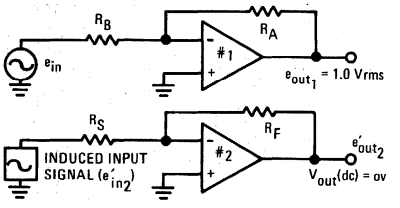


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e'_{out_2} = e'_{in_2}\left(1 + \frac{R_F}{R_S}\right)$, where e'_{out_2} is the component of e_{out_2} due only to lack of perfect separation between the two amplifiers.

MC1539G

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

Typical Amplifier Features:

- Low Input Offset Voltage — 3.0 mV max
- Low Input Offset Current — 60 nA max
- Large Power-Bandwidth — 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- Slew Rate — 34 V/μs typ



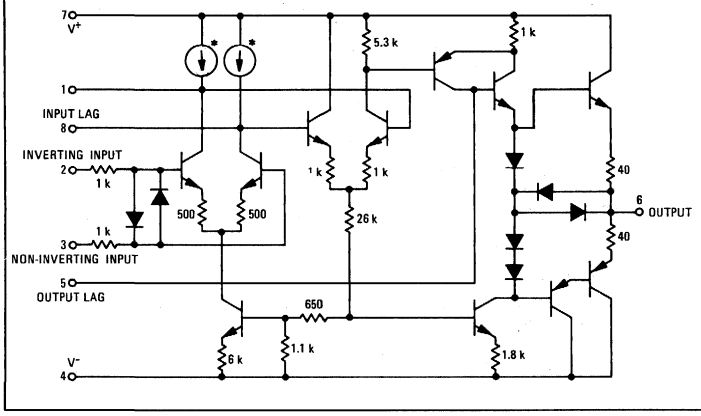
Lead 4 connected to case

CASE 96
(TO-99)
"G" SUFFIX

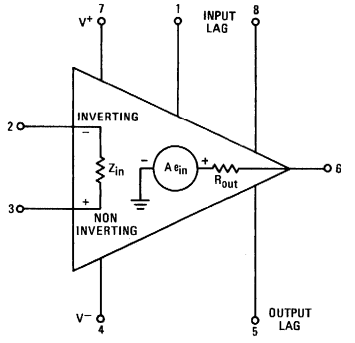
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm V^+$	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	15	mA
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Derate above T_A = 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC

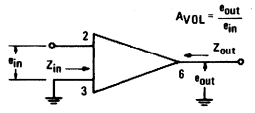
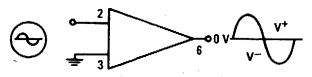
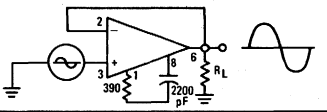
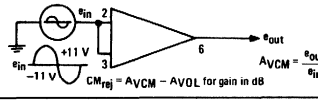
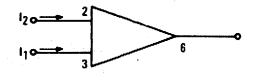
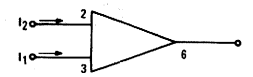
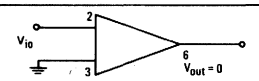
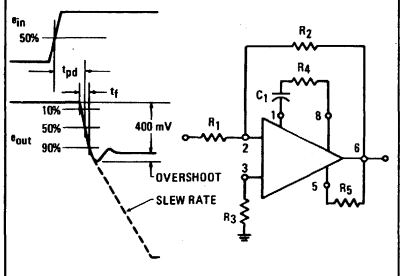
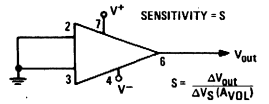


EQUIVALENT CIRCUIT



*PATENT PENDING

ELECTRICAL CHARACTERISTICS (V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (V_{out} = ±10 V, T_A = −55°C to +125°C)	A_{VOL}	50,000	120,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	4.0	-	kΩ
	Input Impedance (f = 20 Hz)	Z_{in}	150	300	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 1.0 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Power Bandwidth (A_v = 1, R_L = 1.0 kΩ, THD ≦ 5%, V_o = 20 V_{p-p})	P_{BW}	20	50	-	kHz
	Input Common Mode Voltage Swing	CMV_{in}	±11	±12	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	80	100	-	dB
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_b	- -	200 230	500 700	nA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = −55°C) ($I_{io} = I_1 - I_2$, T_A = +125°C)	I_{io}	- - -	20 - -	60 75 75	nA
	Input Offset Voltage (T_A = 25°C) (T_A = −55°C + 125°C)	V_{io}	- -	1.0 -	3.0 4.0	mV
	Step Response {Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF} {Gain = 100, no overshoot, R_1 = 1.0 kΩ, R_2 = 100 kΩ, R_3 = 1.0 kΩ, R_4 = 10 kΩ, R_5 = ∞,* C_1 = 2200 pF} {Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = 10 kΩ,* C_1 = 2200 pF} {Gain = 10, 15% overshoot, R_1 = 1.0 kΩ, R_2 = 10 kΩ, R_3 = 1.0 kΩ, R_4 = 1.0 kΩ, R_5 = ∞,* C_1 = 2200 pF} {Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = 10 kΩ,* C_1 = 2200 pF} {Gain = 1, 15% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5.0 kΩ, R_4 = 390 Ω, R_5 = ∞,* C_1 = 2200 pF}	t_f t_{pd} dV_{out}/dt‡ t_f t_{pd} dV_{out}/dt‡ t_f t_{pd} dV_{out}/dt‡ t_f t_{pd} dV_{out}/dt‡ t_f t_{pd} dV_{out}/dt‡ t_f t_{pd} dV_{out}/dt‡	- - - - - - - - - - - - - - - - - -	700 100 34 700 100 1.7 600 80 6.25 600 80 1.7 400 80 4.2 400 80 1.4	- - - - - - - - - - - - - - - - - -	ns ns V/μs ns ns V/μs ns ns V/μs ns ns V/μs ns ns V/μs ns ns V/μs
	Equivalent Input Noise Voltage (Open Loop) (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	-	30	-	$nV/(Hz)^{1/2}$
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = −55°C to +125°C) (R_S = 10 kΩ, T_A = −55°C to +125°C)	TC_{Vio}	- -	3.0 5.0	- -	μV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	90	150	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	150	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	150	μV/V

*To improve performance, development is in process to include resistor $R_5 \approx 10$ kΩ on the device chip. Available after September 1968.

‡dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

(V^+ = +15 Vdc, V^- = -15 Vdc, T_A = 25°C)

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 1)					
			$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	$R_4(\Omega)$	R_5*(Ω)	C_1(pF)
2	1	1.0	10 k	10 k	5.0 k	390	10 k	2200
	2	1.0	10 k	10 k	5.0 k	390	∞	2200
3	1	A_{VOL}	0	∞	0	∞	∞	0
	2	1000	1000	1.0 M	1000	0	∞	10
	3	100	1000	100 k	1000	10 k	∞	2200
	4	10	1000	10 k	1000	1.0 k	∞	2200
	5	1.0	10 k	10 k	5.0 k	390	∞	2200
4	1	A_{VOL}	0	∞	0	∞	∞	0
	2	A_{VOL}	0	∞	0	10 k	∞	2200
	3	A_{VOL}	0	∞	0	390	∞	2200

*To improve performance, development is in process to include resistor $R_5 \approx 10\ k\Omega$ on the device chip. Available after September 1968.

FIGURE 1 – TEST CIRCUIT

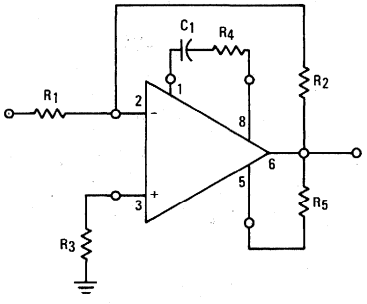


FIGURE 2 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

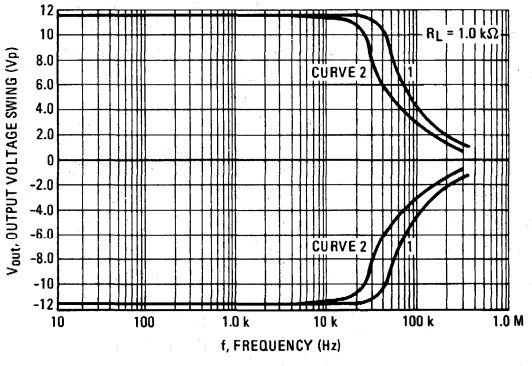


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

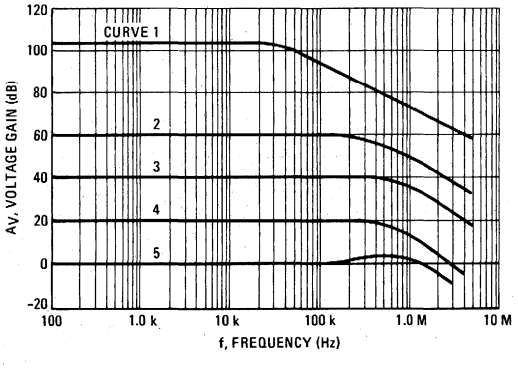


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

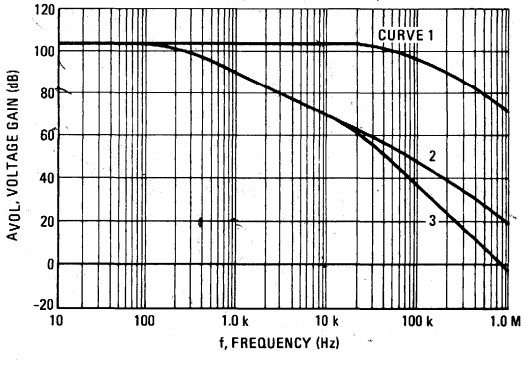


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE

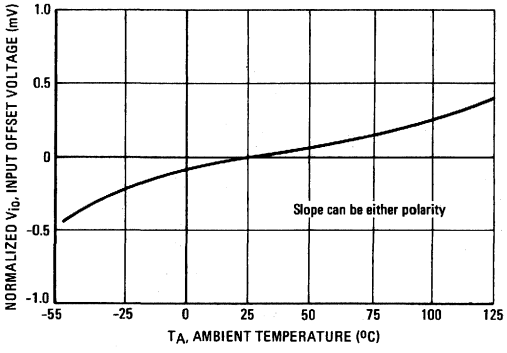


FIGURE 6 – INPUT OFFSET CURRENT versus TEMPERATURE

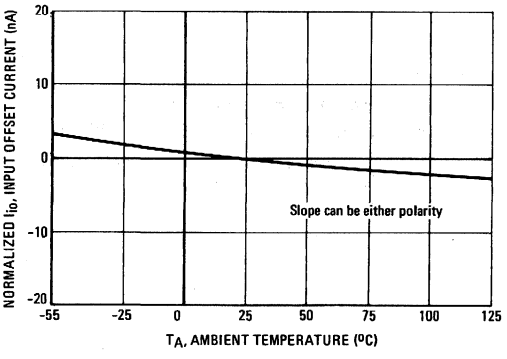


FIGURE 7 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

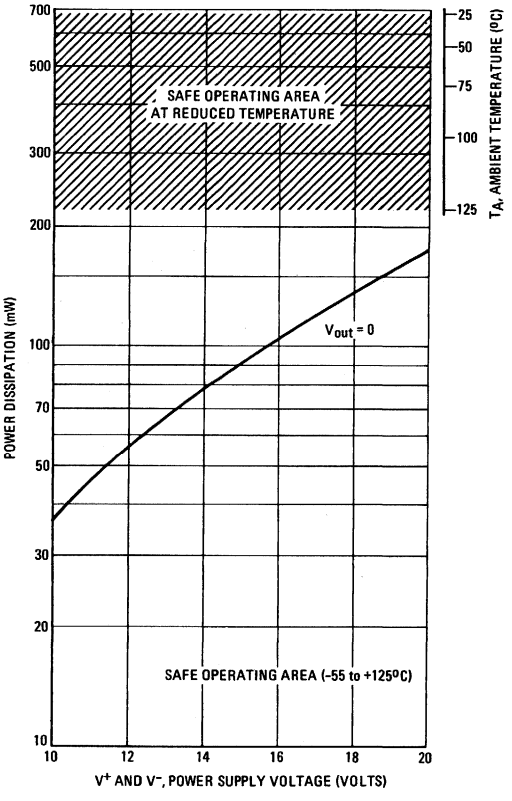


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

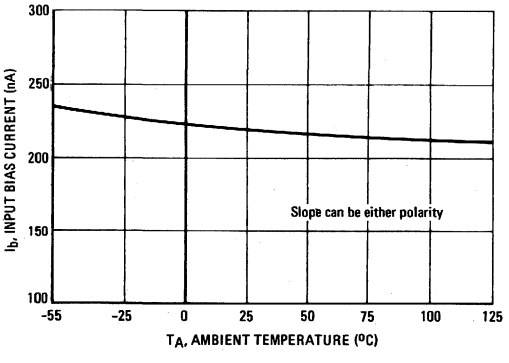
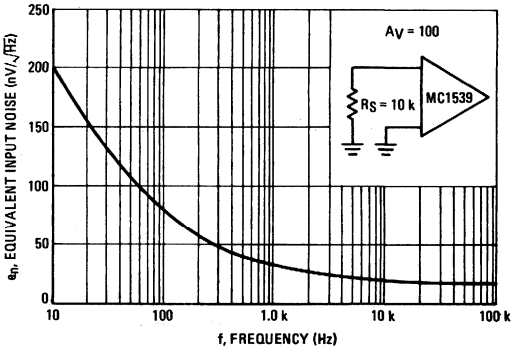


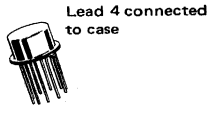
FIGURE 9 – SPECTRAL NOISE DENSITY



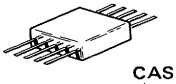
OPERATIONAL AMPLIFIER

MC1709

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



CASE 96
(TO-99)
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

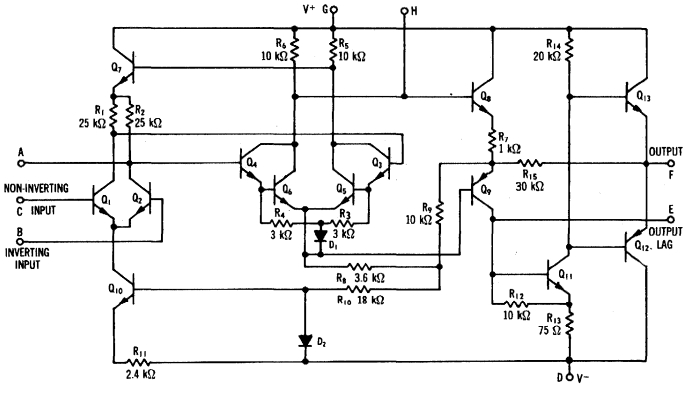
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3.0 μV/°C
- Large Output Voltage Swing –
  ±14 V typical @ ±15 V Supply
- Low Output Impedance –
  Z_{out} = 150 ohms typical

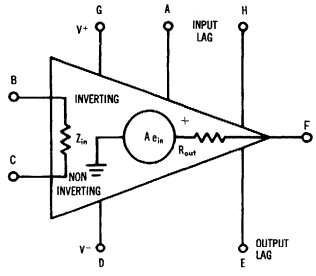
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



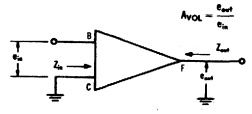
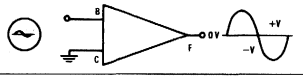
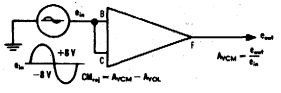
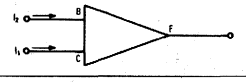
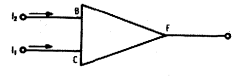
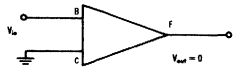
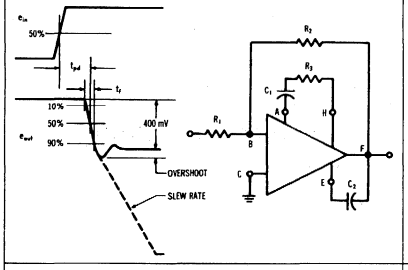
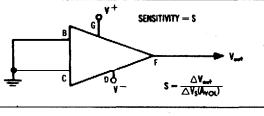
EQUIVALENT CIRCUIT



PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain ($V_{out} = \pm 10$ V, $T_A = -55°C$ to $+125°C$)	A_{VOL}	25,000	45,000	70,000	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	150	400	-	kΩ
	Output Voltage Swing ($R_L = 10$ kΩ) ($R_L = 2$ kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8	±10	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	70	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ ($T_A = +25°C$) ($T_A = -55°C$)	I_b	- -	0.2 0.5	0.5 1.5	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, $T_A = -55°C$) ($I_{io} = I_1 - I_2$, $T_A = +125°C$)	I_{io}	- - -	0.05 - -	0.2 0.5 0.2	μA
	Input Offset Voltage ($T_A = 25°C$) ($T_A = -55°C$ + 125°C)	V_{io}	- -	1.0 -	5.0 6.0	mV
	Step Response Gain = 100, 5% overshoot, $R_1 = 1$ kΩ, $R_2 = 100$ kΩ, $R_3 = 1.5$ kΩ, $C_1 = 100$ pF, $C_2 = 3$ pF	t_f t_{pd} dV_{out}/dt ②	- - -	0.8 0.38 12.0	- - -	μs μs V/μs
	Gain = 10, 10% overshoot, $R_1 = 1$ kΩ, $R_2 = 10$ kΩ, $R_3 = 1.5$ kΩ, $C_1 = 500$ pF, $C_2 = 20$ pF	t_f t_{pd} dV_{out}/dt ②	- - -	0.6 0.34 1.7	- - -	μs μs V/μs
	Gain = 1, 5% overshoot, $R_1 = 10$ kΩ, $R_2 = 10$ kΩ, $R_3 = 1.5$ kΩ, $C_1 = 5000$ pF, $C_2 = 200$ pF	t_f t_{pd} dV_{out}/dt ②	- - -	2.2 1.3 0.25	- - -	μs μs V/μs
	Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω, $T_A = -55°C$ to $+125°C$) ($R_S \leq 10$ kΩ, $T_A = -55°C$ to $+125°C$)	TC_{Vio}	- -	3.0 6.0	- -	μV/°C
	DC Power Dissipation (Power Supply = ±15 V, $V_{out} = 0$)	P_D	-	80	165	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	150	μV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	150	μV/V

① All definitions imply linear operation

② dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1 — TEST CIRCUIT
$V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$

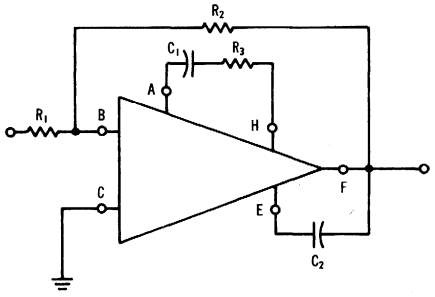


Fig. No.	Curve No.	Test Conditions				
		$R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)
2	1	10 k	10 k	1.5 k	5 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1M	1.5 k	100	3
	4	1 k	1M	0	10	3
3	1	1 k	1M	0	10	3
	2	10 k	1M	1.5 k	100	3
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5 k	200
4	1	0	∞	1.5 k	5 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3
	4	0	∞	0	10	3

FIGURE 2 — LARGE SIGNAL SWING versus FREQUENCY

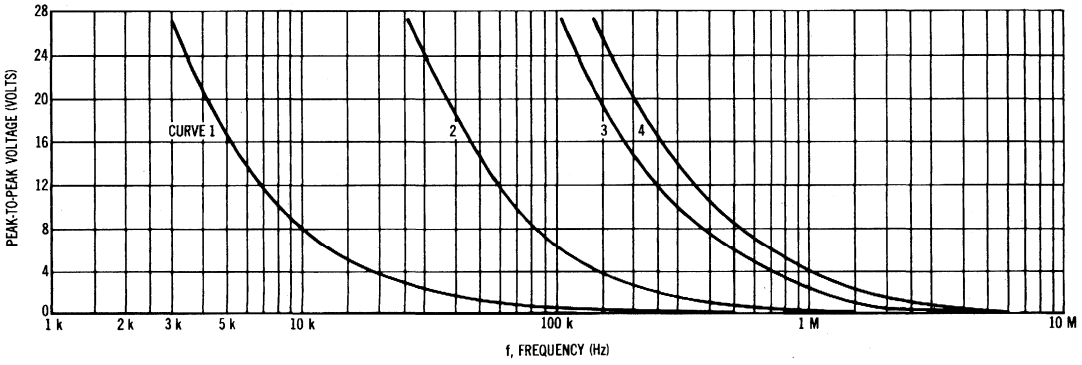


FIGURE 3 — VOLTAGE GAIN versus FREQUENCY

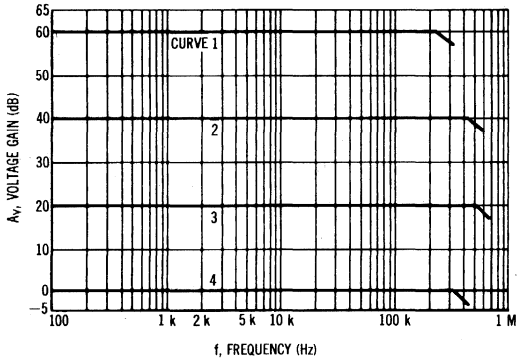


FIGURE 4 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

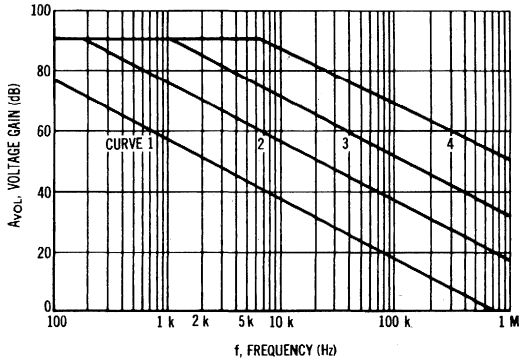


FIGURE 5 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

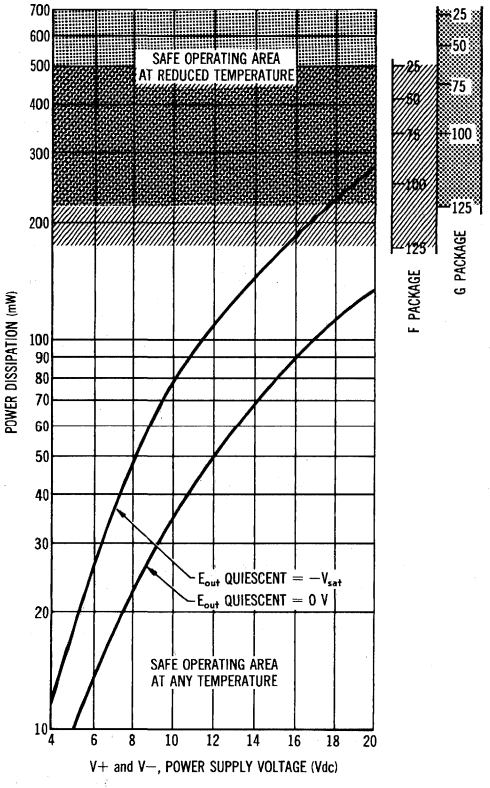


FIGURE 6 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

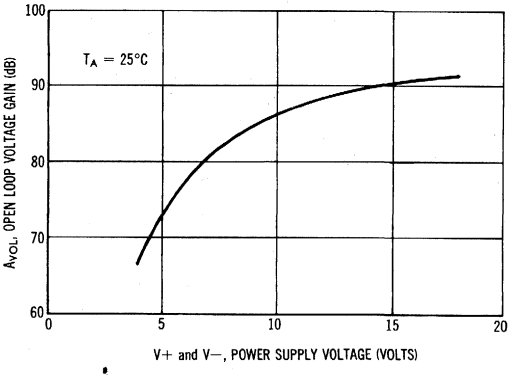


FIGURE 7 — COMMON SWING versus POWER SUPPLY VOLTAGE

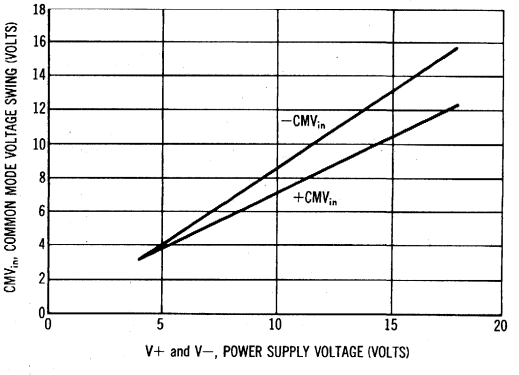


FIGURE 8 — INPUT OFFSET VOLTAGE versus TEMPERATURE

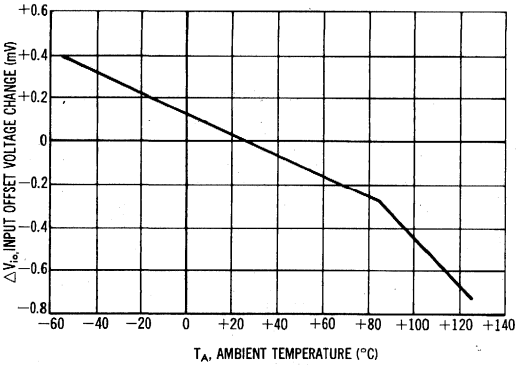
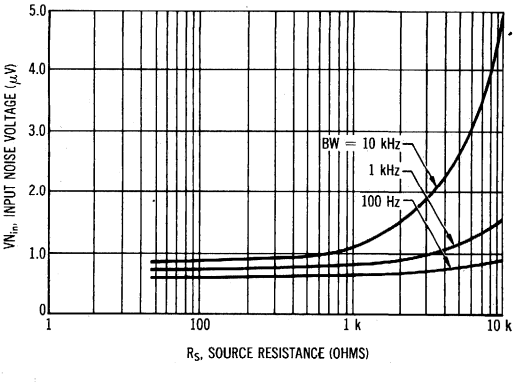


FIGURE 9 — INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



OPERATIONAL AMPLIFIER

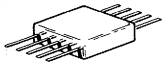
MC1709C

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



Lead 4 connected to case

CASE 96
(TO-99)
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX



CASE 93
(TO-116)
"P" SUFFIX

Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift — ±3.0 μV/°C
- Large Output Voltage Swing — ±14 V typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 150 ohms typical

PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P" Package	3	4	5	6*	9	10	11	12

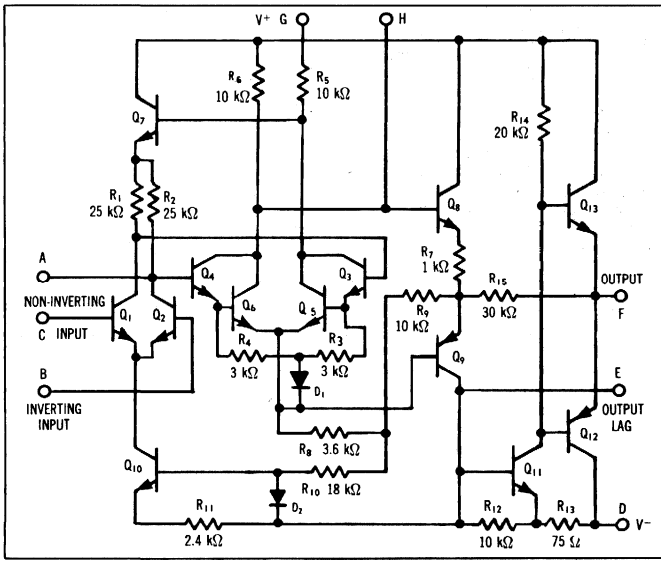
*Pin 7 is electrically connected to substrate and V^-

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

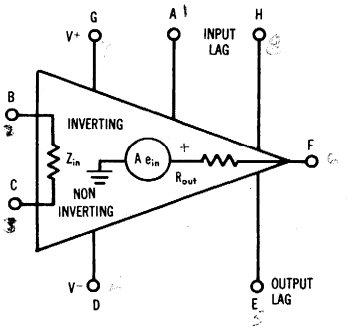
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

* For full temperature range (-55°C to +125°C) and characteristic curves, see MC1709 data sheet.

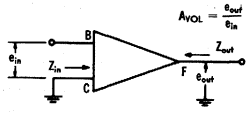
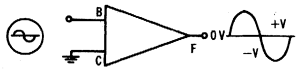
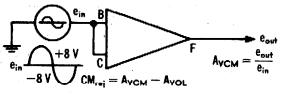
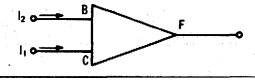
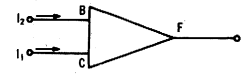
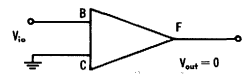
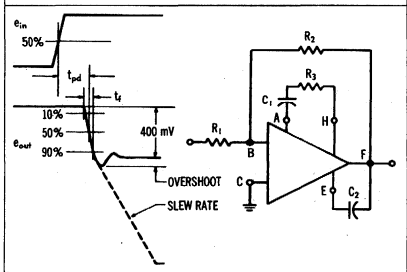
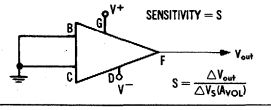
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

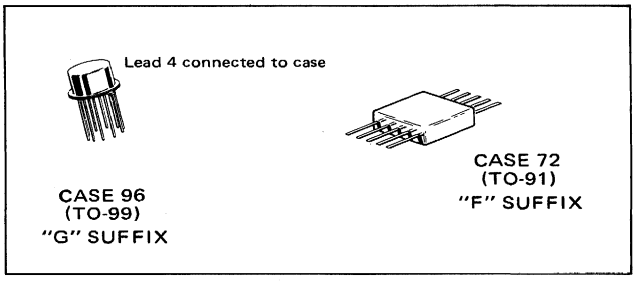
Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L=2 kΩ, V_{out} = ± 10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	45,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	50	250	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8.0	±10	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	65	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	- -	0.3 -	1.5 2.0	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	- - -	0.1 - -	0.5 0.75 0.75	µA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	- -	2.0 -	7.5 10	mV
	Step Response Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3 pF Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt ①	- - -	0.8 0.38 12 0.6 0.34 1.7 2.2 1.3 0.25	- - - - - - - - -	µs µs V/µs µs µs V/µs µs µs V/µs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C) ($R_S \leq$ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	- -	3.0 6.0	- -	µV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	80	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	200	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	200	µV/V

① dV_{out}/dt = Slew Rate

WIDEBAND DC AMPLIFIER

MC1712

. . . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.



Typical Amplifier Features:

- Open Loop Gain A_{VOL} = 3600 typical
- Low Temperature Drift – ±2.5 μV/°C
- Output Swing – ±5.3 V typical @ +12 V and -6.0 V Supplies
- Low Output Impedance – Z_{out} = 200 ohms typical

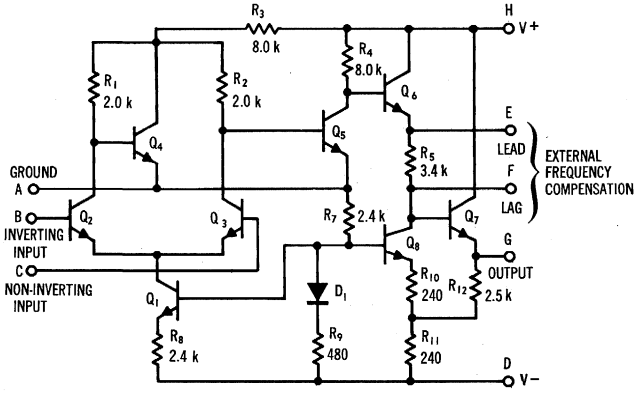
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V^+ and V^- terminals)	$\|V^+\|+\|V^-\|$	21	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

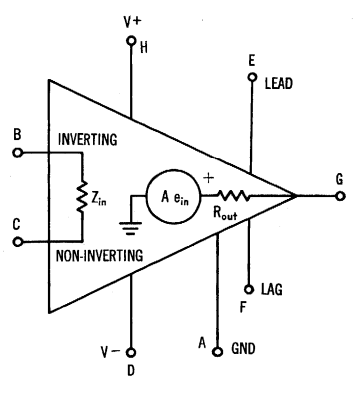
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	10

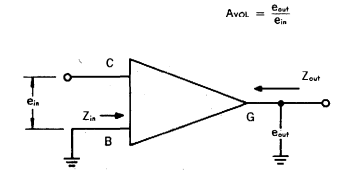
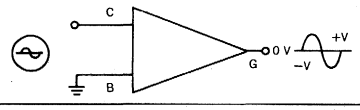
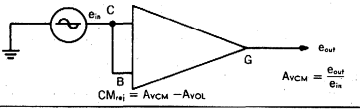
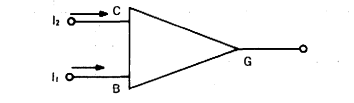
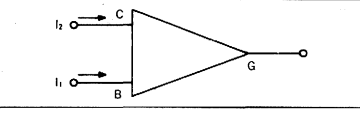
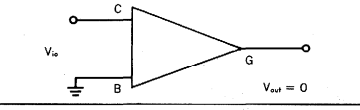
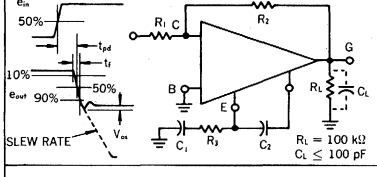
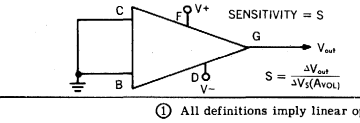
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic Definitions ①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain R_L = 100 kΩ	A_{VOL}				V/V
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, V_{out} = ± 2.5 V)		600	900	1500	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, V_{out} = ± 5.0 V)		2500	3600	6000	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, V_{out} = ± 5.0 Vdc, T_A = -55, +125°C)		2000		7000	
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, V_{out} = ± 2.5 V, T_A = -55 to +125°C)		500		1750	
	Output Impedance	Z_{out}				ohms
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f = 20 Hz)		-	300	700	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, f = 20 Hz)		-	200	500	
	Input Impedance	Z_{in}				k ohms
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f = 20 Hz)		22	70	-	
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f = 20 Hz, T_A = -55°C, +125°C)		8.0	-	-	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, f = 20 Hz)		16	40	-	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, f = 20 Hz, T_A = -55°C, +125°C)		6.0	-	-	
	Output Voltage Swing	V_{out}				V_{peak}
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, R_L = 100 kΩ)		±2.5	±2.7	-	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, R_L = 100 kΩ)		±5.0	±5.3	-	
	(V^+ = +6.0 Vdc, V^- = -3.0 Vdc, R_L = 10 kΩ)		± 1.5	± 2.0		
	(V^+ = +12 Vdc, V^- = -6.0 Vdc, R_L = 10 kΩ)		± 3.5	± 4.0		
	Input Common Mode Voltage Swing	CMV_{in}				V_{peak}
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		+0.5 -1.5	-	-	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc)		+0.5 -4.0	-	-	
	Common Mode Rejection Ratio	CM_{rej}				dB
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f ≤ 1.0 kHz)		80	100	-	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, f ≤ 1.0 kHz)		80	100	-	
	Input Bias Current	I_b				μA
	T_A = 25°C					
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		-	1.2	3.5	
	$I_b = \frac{I_1 + I_2}{2}$, ($V^+$ = 12 Vdc, V^- = -6.0 Vdc)		-	2.0	5.0	
	T_A = -55°C					
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		-	2.5	7.5	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc)		-	4.0	10	
	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}				μA
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		-	0.1	0.5	
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, T_A = -55 to +125°C)		-	-	1.5	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc)		-	0.2	0.5	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, T_A = -55 to +125°C)		-	-	1.5	
	Input Offset Voltage R_S = 2.0 kΩ	V_{io}				mV
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		-	1.3	3.0	
	(V^+ = 6.0 Vdc, V^- = -3.0 Vdc, T_A = -55°C, +125°C)		-	-	4.0	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc)		-	1.1	2.0	
	(V^+ = 12 Vdc, V^- = -6.0 Vdc, T_A = -55°C, +125°C)		-	-	3.0	
	Step Response	V_{os}	-	20	40	%
	V^+ = 12 Vdc, V^- = -6.0 Vdc		-	10	30	ns
	Gain = 100, V_{in} = 1.0 mV,	t_f	-	10	-	ns
	R_1 = 1.0 kΩ, R_2 = 100 kΩ,	t_{pd}	-	12	-	V/μs
	C_2 = 50 pF, R_3 = ∞, C_1 = open	dV_{out}/dt ②				
	V^+ = 12 Vdc, V^- = -6.0 Vdc	V_{os}	-	10	50	%
	Gain = 1.0, V_{in} = 10 mV,	t_f	-	25	120	ns
	R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	-	16	-	ns
	C_1 = 0.01 μF, R_3 = 20Ω, C_2 = open	dV_{out}/dt ②	-	1.5	-	V/μs
	Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω	TC_{Vio}				μV/°C
	(T_A = +25 to +125°C)		-	2.5	-	
	(T_A = -55 to +25°C)		-	2.0	-	
	Average Temperature Coefficient Input Offset Current	TC_{Iio}				nA/°C
	(T_A = +25°C to +125°C)		-	0.05	-	
	(T_A = -55 to +25°C)		-	1.5	-	
	DC Power Dissipation	P_D				mW
	(V_{out} = 0, V^+ = 6.0 Vdc, V^- = -3.0 Vdc)		-	17	30	
	(V_{out} = 0, V^+ = 12 Vdc, V^- = -6.0 Vdc)		-	70	120	
	Positive Supply Sensitivity (V^- constant = -6.0 Vdc, V^+ = 12 Vdc to 6.0 Vdc)	S^+	-	60	200	μV/V
	Negative Supply Sensitivity (V^+ constant = 12 Vdc, V^- = -6.0 Vdc to -3.0 Vdc)	S^-	-	60	200	μV/V

① All definitions imply linear operation. ② dV_{out}/dt = Slew Rate

TYPICAL OUTPUT CHARACTERISTICS

V+ = 12 Vdc, V− = −6.0 Vdc, T_A = 25°C

FIGURE 1 — OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

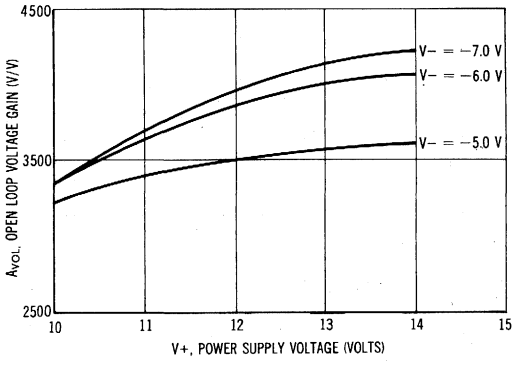


FIGURE 2 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

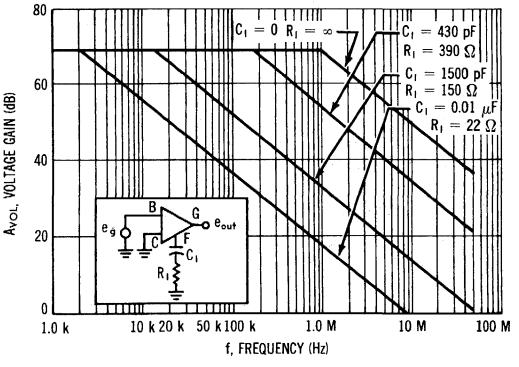


FIGURE 3 — VOLTAGE GAIN versus FREQUENCY

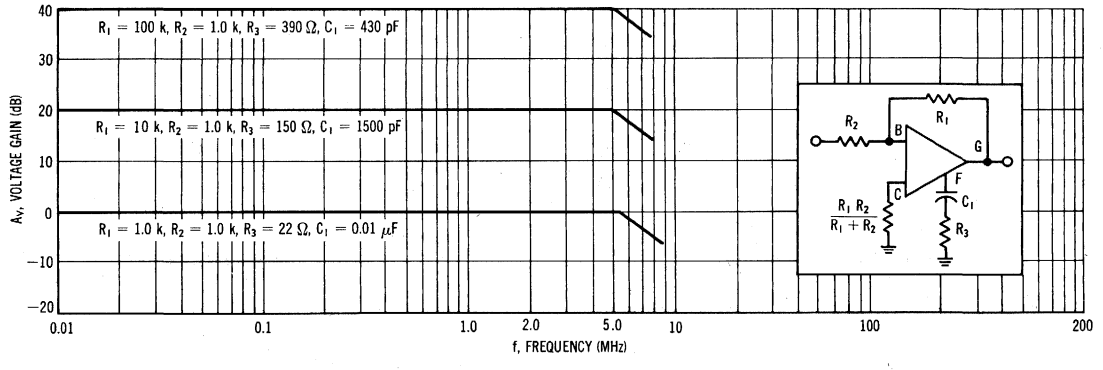
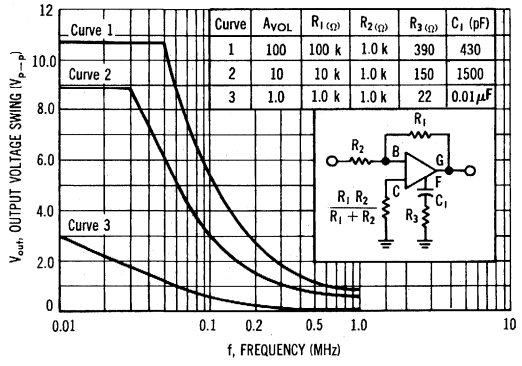


FIGURE 4 — MAXIMUM OUTPUT SWING versus FREQUENCY



Curve	A_{VOL}	$R_{1(\Omega)}$	$R_{2(\Omega)}$	$R_{3(\Omega)}$	C_1 (pF)
1	100	100 k	1.0 k	390	430
2	10	10 k	1.0 k	150	1500
3	1.0	1.0 k	1.0 k	22	0.01 μF

FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

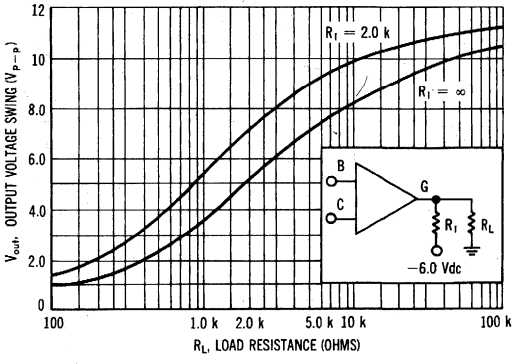


FIGURE 6 — INPUT BIAS CURRENT versus TEMPERATURE

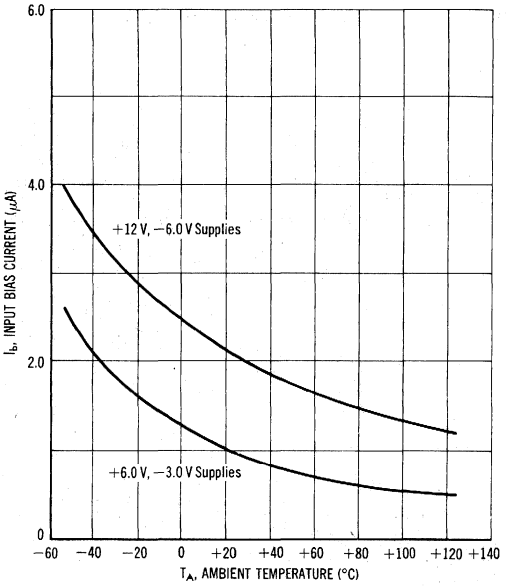


FIGURE 7 — INPUT OFFSET CURRENT versus TEMPERATURE

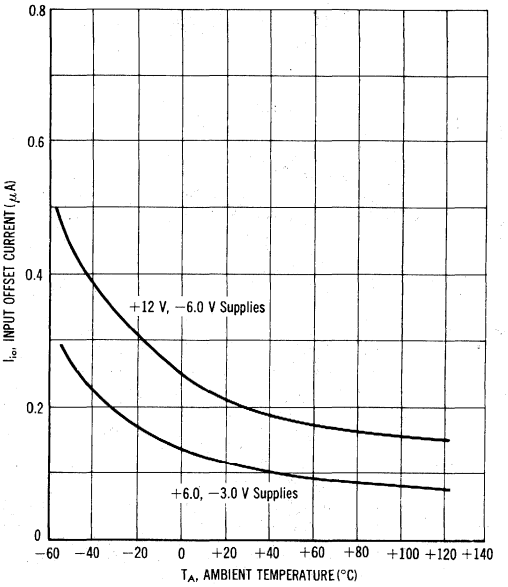


FIGURE 8 — INPUT OFFSET VOLTAGE versus TEMPERATURE

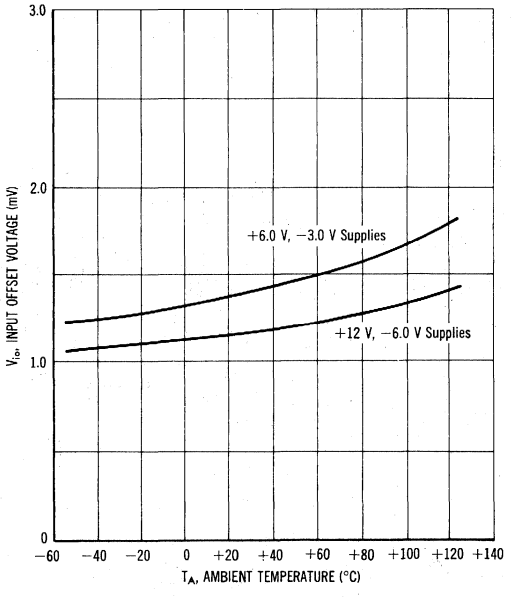
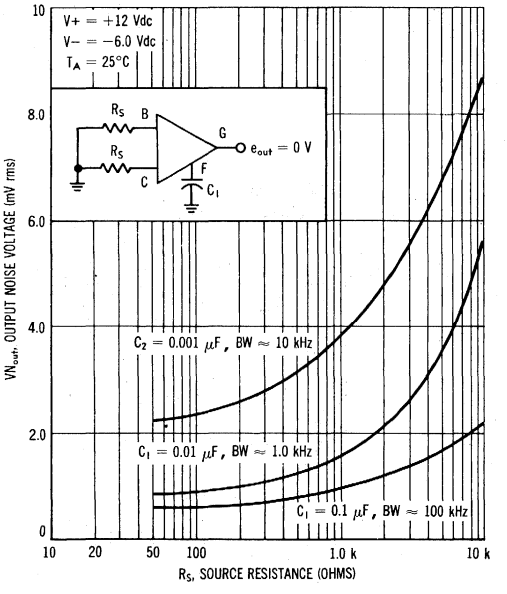
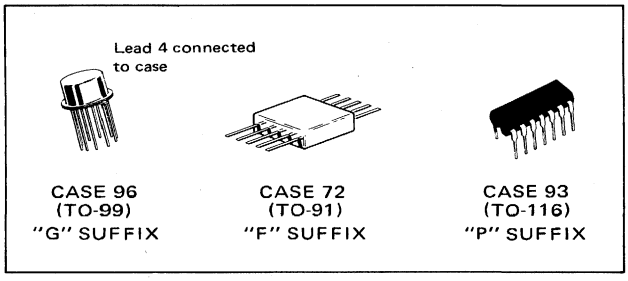


FIGURE 9 — OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



MC1712C

. . . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.



CASE 96 (TO-99) "G" SUFFIX

CASE 72 (TO-91) "F" SUFFIX

CASE 93 (TO-116) "P" SUFFIX

Typical Amplifier Features:

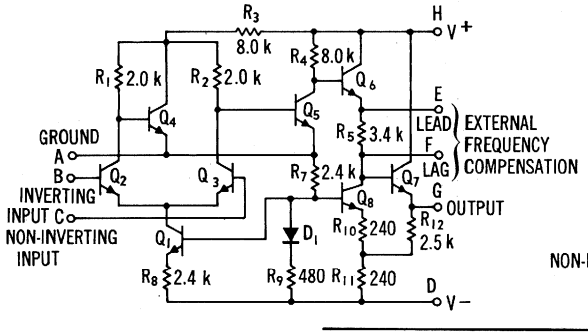
- Open Loop Gain A_{VOL} = 3400 typical
- Low Temperature Drift – ±5.0 μV/°C
- Output Voltage Swing – ±5.3 V typical @ +12 V and -6.0 V Supplies
- Low Output Impedance – Z_{out} = 200 ohms typical

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

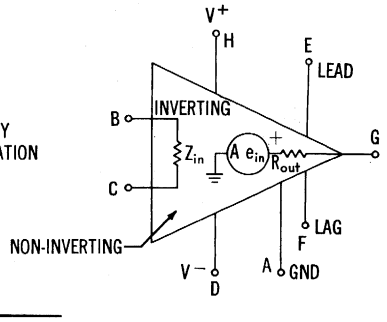
Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V+ and V− terminals)	$\|V^+\|+\|V^-\|$	21	Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C

* For full temperature range (-55°C to +125°C) and characteristic curves, see MC1712 data sheet.

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

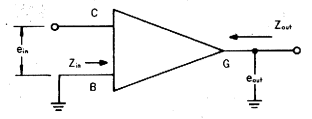
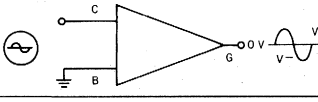
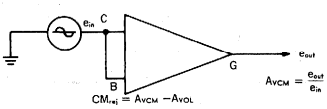
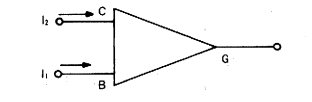
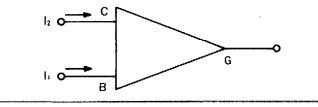
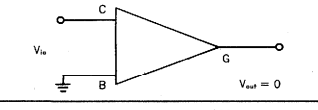
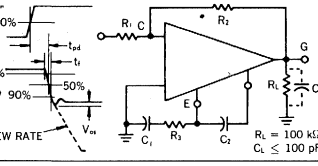
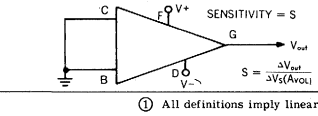


PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	10
"P" Package	3	4	5	6*	9	10	12	13

* Pin 7 is electrically connected to substrate and to V−

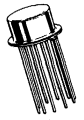
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic Definitions ①	Characteristic	Symbol	Min	Typ	Max	Unit
$A_{VOL} = \frac{e_{out}}{e_{in}}$ 	Open Loop Voltage Gain R_L = 100 kΩ (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, V_{out} = ± 2.5 V) (V^+ = 12 Vdc, V^- = -6.0 Vdc, V_{out} = ± 5.0 V) (V^+ = 12 Vdc, V^- = -6.0 Vdc, V_{out} = ± 5.0 Vdc, T_A = 0, +75°C) (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, V_{out} = ± 2.5 V, T_A = 0, +75°C)	A_{VOL}	500 2000 1500 400	800 3400 – –	1500 6000 7000 1750	V/V
	Output Impedance (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f = 20 Hz) (V^+ = 12 Vdc, V^- = -6.0 Vdc, f = 20 Hz)	Z_{out}	– –	300 200	800 600	ohms
	Input Impedance (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f = 20 Hz) (V^+ = 12 Vdc, V^- = -6.0 Vdc, f = 20 Hz)	Z_{in}	16 10	55 32	–	k ohms
	Output Voltage Swing (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, R_L = 100 kΩ) (V^+ = 12 Vdc, V^- = -6.0 Vdc, R_L = 100 kΩ) (V^+ = +6.0 Vdc, V^- = -3.0 Vdc, R_L = 10 kΩ) (V^+ = +12 Vdc, V^- = -6.0 Vdc, R_L = 10 kΩ)	V_{out}	±2.5 ±5.0 ± 1.5 ± 3.5	±2.7 ±5.3 ± 2.0 ± 4.0	– – – –	V_{peak}
 $A_{VCM} = \frac{e_{out}}{e_{in}}$ $CM_{rej} = A_{VCM} - A_{VOL}$	Input Common Mode Voltage Swing (V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V^+ = 12 Vdc, V^- = -6.0 Vdc)	CMV_{in}	+0.5 -1.5 +0.5 -4.0	– – – –	– – – –	V_{peak}
	Common Mode Rejection Ratio (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, f ≤ 1.0 kHz) (V^+ = 12 Vdc, V^- = -6.0 Vdc, f ≤ 1.0 kHz)	CM_{rej}	70 70	95 95	–	dB
 $I_b = \frac{I_1 + I_2}{2}$	Input Bias Current T_A = 25°C (V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V^+ = 12 Vdc, V^- = -6.0 Vdc) T_A = 0°C to +75°C) (V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V^+ = 12 Vdc, V^- = -6.0 Vdc) T_A = 0°C to +75°C)	I_b	– – – –	1.5 2.5 2.5 4.0	5.0 7.5 8.0 12	μA
	Input Offset Current ($I_{io} = I_1 - I_2$) (V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, T_A = 0°C to +75°C) (V^+ = 12 Vdc, V^- = -6.0 Vdc) (V^+ = 12 Vdc, V^- = -6.0 Vdc, T_A = 0°C to +75°C)	I_{io}	– – – –	0.3 – 0.5 –	2.0 2.5 2.0 2.5	μA
	Input Offset Voltage R_S = 2.0 kΩ (V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V^+ = 6.0 Vdc, V^- = -3.0 Vdc, T_A = 0°C to +75°C) (V^+ = 12 Vdc, V^- = -6.0 Vdc) (V^+ = 12 Vdc, V^- = -6.0 Vdc, T_A = 0°C to +75°C)	V_{io}	– – – –	1.7 – 1.5 –	6.0 7.5 5.0 6.5	mV
	Step Response (V^+ = 12 Vdc, V^- = -6.0 Vdc Gain = 100, V_{in} = 1.0 mV, R_1 = 1.0 kΩ, R_2 = 100 kΩ, C_2 = 50 pF, R_3 = ∞, C_1 = open) (V^+ = 12 Vdc, V^- = -6.0 Vdc Gain = 1.0, V_{in} = 10 mV, R_1 = 10 kΩ, R_2 = 10 kΩ, C_1 = 0.01 μF, R_3 = 20Ω, C_2 = open)	V_{os} t_f t_{pd} dV_{out}/dt② V_{os} t_f t_{pd} dV_{out}/dt②	– – – – – – – –	20 10 10 12 10 25 16 1.5	40 30 – – 50 120 – –	% ns ns V/μs % ns ns V/μs
	Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω (T_A = 0, +75°C)	TC_{Vio}	–	5.0	–	μV/°C
	Average Temperature Coefficient Input Offset Current (T_A = +25°C to +75°C) (T_A = 0 to +25°C)	TC_{Iio}	– –	4.0 6.0	– –	nA/°C
	DC Power Dissipation (V_{out} = 0, V^+ = 6.0 Vdc, V^- = -3.0 Vdc) (V_{out} = 0, V^+ = 12 Vdc, V^- = -6.0 Vdc)	P_D	– –	17 70	30 120	mW
 $S = \frac{\Delta V_{out}}{\Delta V_S(A_{VOL})}$	Positive Supply Sensitivity (V^- constant = -6.0 Vdc, V^+ = 12 Vdc to 6.0 Vdc) Negative Supply Sensitivity (V^+ constant = 12 Vdc, V^- = -6.0 Vdc to -3.0 Vdc)	S^+ S^-	– –	60 60	300 300	μV/V μV/V

① All definitions imply linear operation. ② dV_{out}/dt = Slew Rate

EMITTER COUPLED AMPLIFIER

MC1110



CASE 89

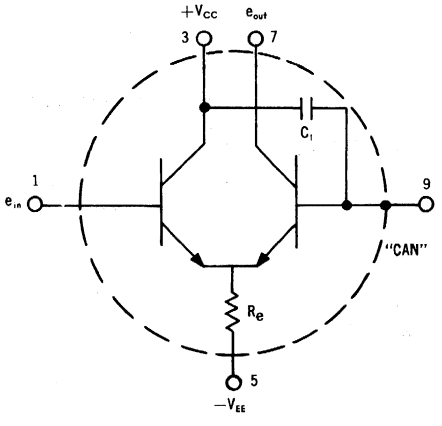
Typical Amplifier Features:

- DC – 300 MHz Performance
- Intended for IF and RF Applications
- 26 dB typ. Gain at 100 MHz
- High Stability Through Low Internal Feedback

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Power Supply Voltage	V_{EE}	14	Vdc
Total Power Dissipation (Derate 5 mW/°C above T_A = 25°C)	P_D	0.5	Watt
Operating Temperature Range	T_j	-55 to+125	°C
Storage Temperature Range	T_{stg}	-65 to+200	°C
Maximum Input Level (RMS)	V_{in}	2	V (RMS)

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

CIRCUIT OPERATION

The input terminal (Pin 1) of the device should be DC ground for optimum DC operating point. Pin 3 is to be supplied with a positive voltage (V_{CC}) for transistor collector and Pin 5 with a negative voltage (V_{EE}) to supply emitter bias current. AGC may be accomplished by variation of V_{EE}. The output of the circuit (Pin 7) should be operated at the same DC potential as is Pin 3. Pin 9 should be AC and DC grounded. Resistor R_e is a diffused silicon resistor, and C_1 is a silicon oxide capacitor.

ELECTRICAL CHARACTERISTICS (at T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS						
Input Leakage Current (V_3 = 5 Vdc; I_5, I_7, I_9 = 0)		I_1	---	---	10	nAdc
Output Leakage Current (V_7 = 5 Vdc; I_1, I_3, I_5 = 0)		I_9	---	---	10	nAdc
Operating Current (V_{CC} = 5 Vdc, V_{EE} = -4.7 Vdc, V_{in} = 0)	Figure 1	I_{CT}	3.8	4	4.2	mAdc
Input Operating Current V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0)	Figure 1	I_1	---	---	250	μAdc
Reference Operating Current V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0)	Figure 1	I_9	---	---	250	μAdc
Current Balance V_{CC} = 5 Vdc, (V_{EE} = -10 Vdc, V_{in} = 0) V_{CC} = 5 Vdc, V_{EE} = -4.7 Vdc, V_{in} = 0)	 Figure 1 Figure 1	I_3/I_7	 0.90 0.90	 --- ---	 1.10 1.10	---
Large Signal Transconductance (V_{CC} = 5 Vdc, V_{EE} = -4 Vdc, ΔV_{in} = 50 mV)		G_{21}	26	28	---	m-mhos
SMALL-SIGNAL CHARACTERISTICS						
Small Signal Current Gain (V_{CC} = 5 V, I_E = -4 mA, f = 100 MHz)		h_{21}	6.0	9.0	---	---
Short Circuit Admittances (V_{CC} = 5 V, V_{EE} = -4V, f = 100 MHz) Input Admittance Reverse Transfer Admittance Forward Transfer Admittance Output Admittance	Figure 2	--- $\|y_{11}\|$ $\|y_{12}\|$ $\|y_{21}\|$ $\|y_{22}\|$	 --- --- --- ---	 2.0 0.064 16.3 1.2	 --- --- --- ---	m-mhos
Transducer Power Gain (V_{CC} = 5V, V_{EE} = -4V, f = 100 MHz, BW = 3 MHz) (V_{CC} = 5V, V_{EE} = -4V, f = 200 MHz, BW = 6 MHz)	Figure 20 Figure 21	G_T	22 15	26 18	--- ---	dB
Noise Figure (V_{CC} = 5V, V_{EE} = -4V, f = 100 MHz, R_g = R_{SO})		NF	---	4	6	dB

FIGURE 1 — DC CHARACTERISTICS TEST CIRCUIT

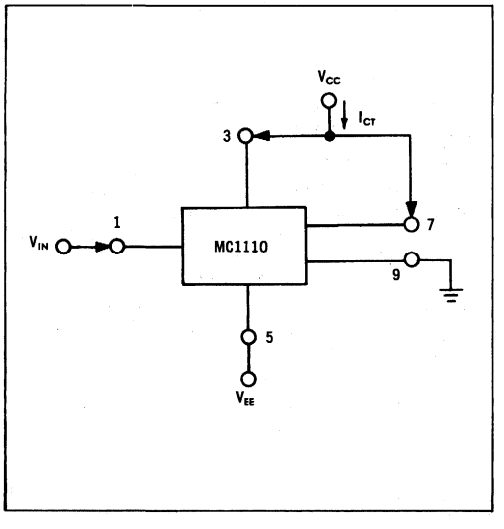
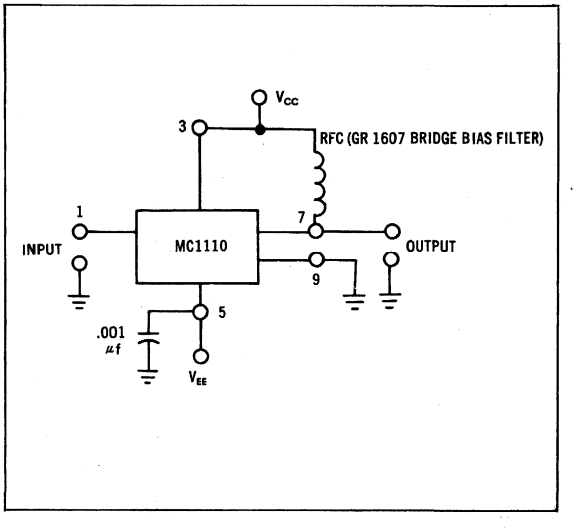
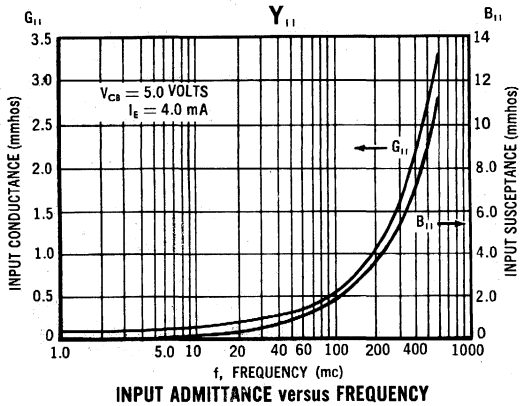


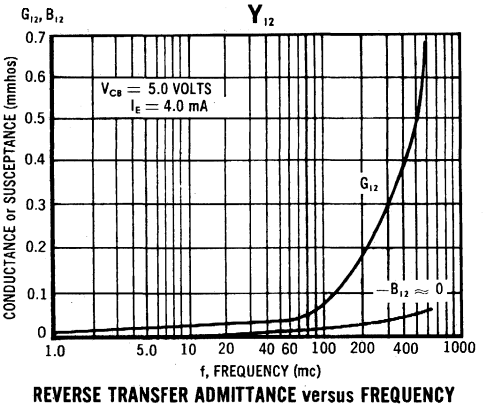
FIGURE 2 — SHORT CIRCUIT ADMITTANCE TEST CIRCUIT
(GENERAL RADIO 1607 A BRIDGE)





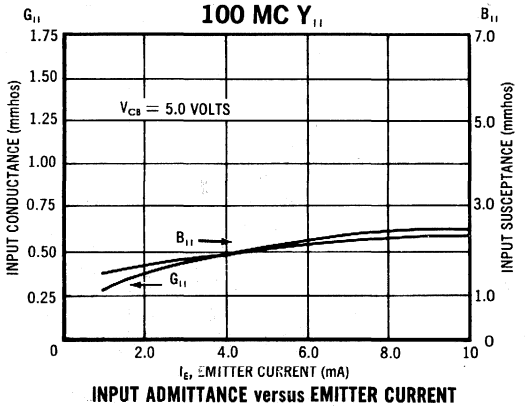
INPUT ADMITTANCE versus FREQUENCY

FIGURE 3



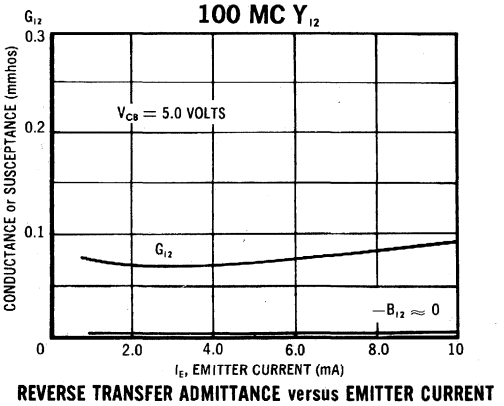
REVERSE TRANSFER ADMITTANCE versus FREQUENCY

FIGURE 6



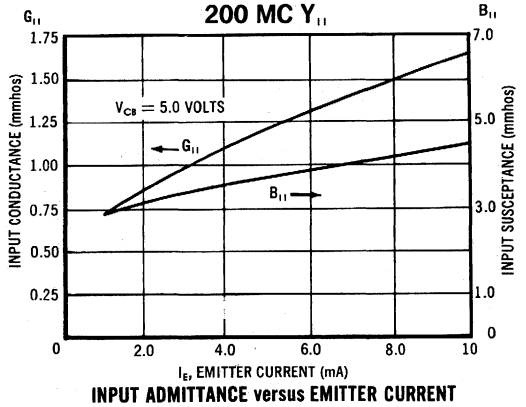
INPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 4



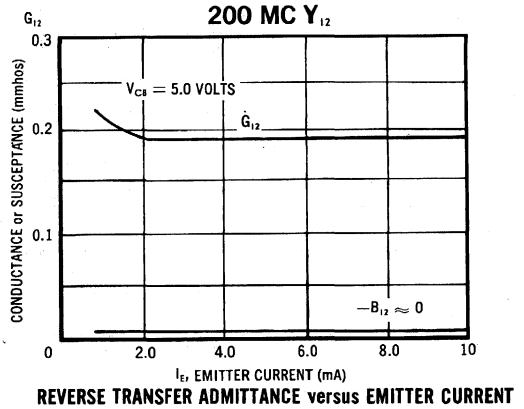
REVERSE TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 7



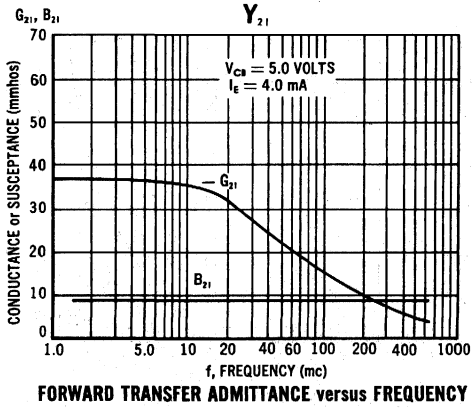
INPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 5



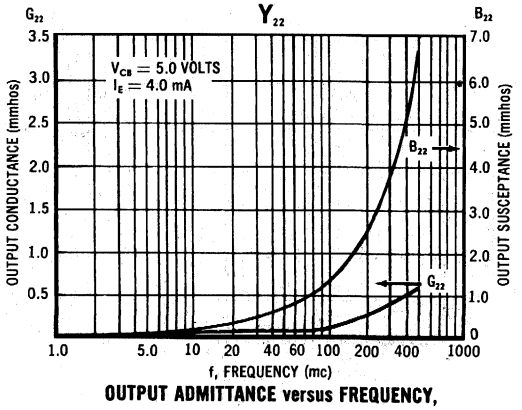
REVERSE TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 8



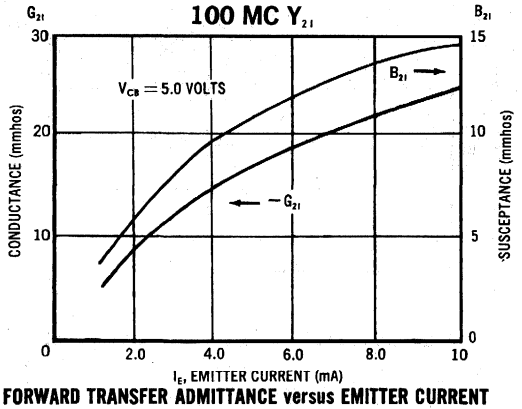
FORWARD TRANSFER ADMITTANCE versus FREQUENCY

FIGURE 9



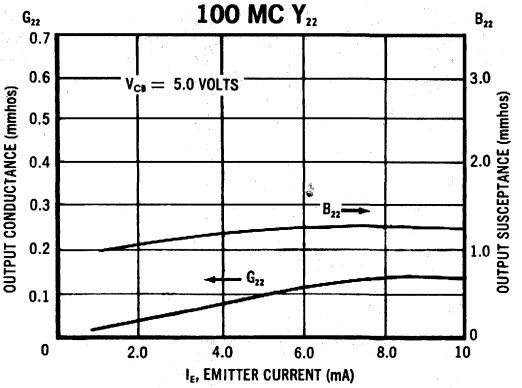
OUTPUT ADMITTANCE versus FREQUENCY,

FIGURE 12



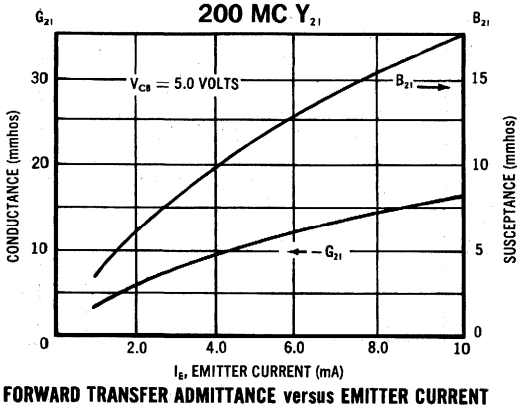
FORWARD TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 10



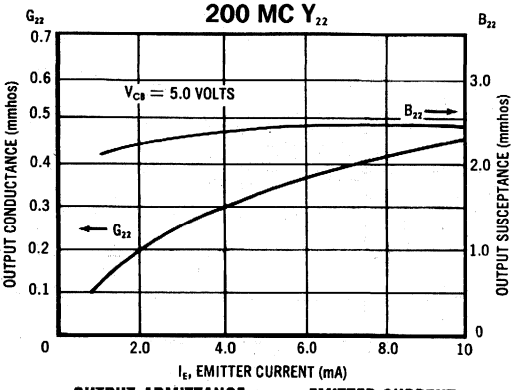
OUTPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 13



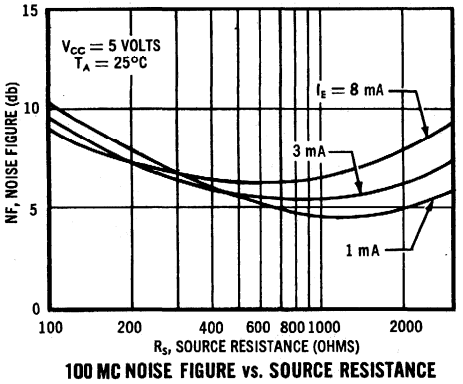
FORWARD TRANSFER ADMITTANCE versus EMITTER CURRENT

FIGURE 11



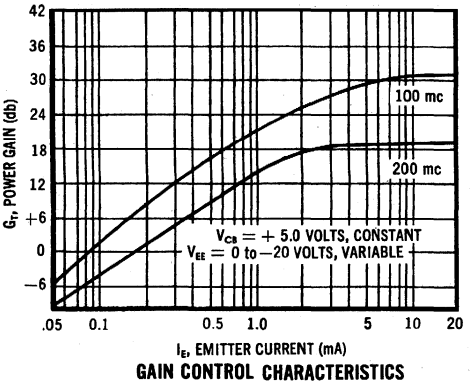
OUTPUT ADMITTANCE versus EMITTER CURRENT

FIGURE 14



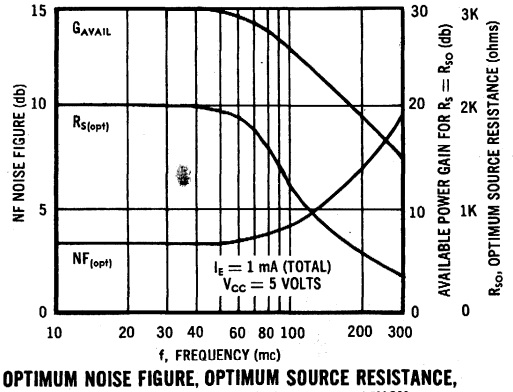
100 MC NOISE FIGURE vs. SOURCE RESISTANCE

FIGURE 15



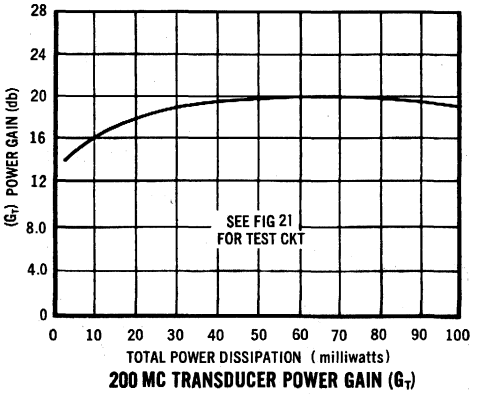
GAIN CONTROL CHARACTERISTICS

FIGURE 16



OPTIMUM NOISE FIGURE, OPTIMUM SOURCE RESISTANCE, AND AVAILABLE POWER GAIN vs. FREQUENCY

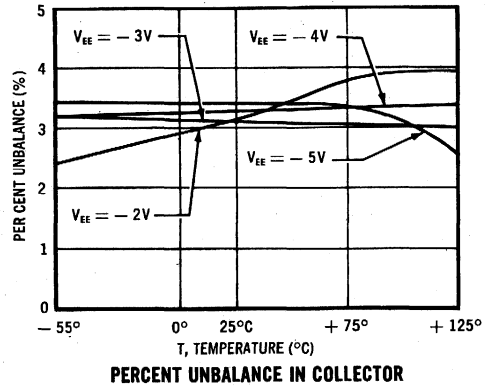
FIGURE 17



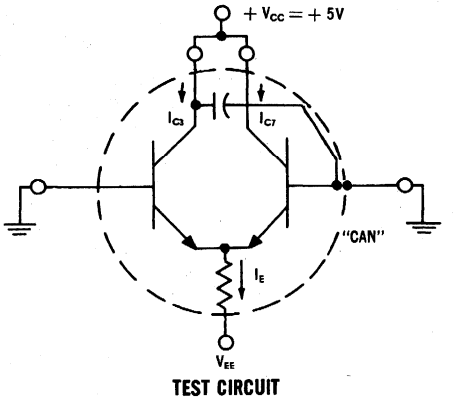
200 MC TRANSDUCER POWER GAIN (G_T) vs. POWER DISSIPATION

FIGURE 18

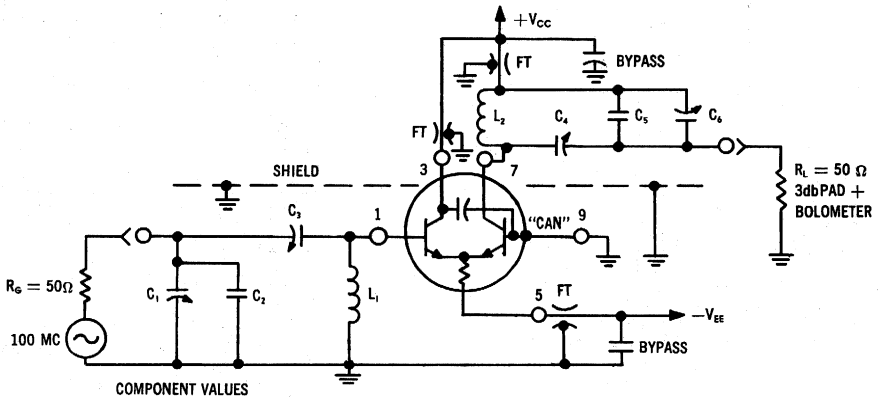
FIGURE 19



PERCENT UNBALANCE IN COLLECTOR CURRENTS (I_{C3}/I_{C7}) vs. TEMPERATURE



TEST CIRCUIT

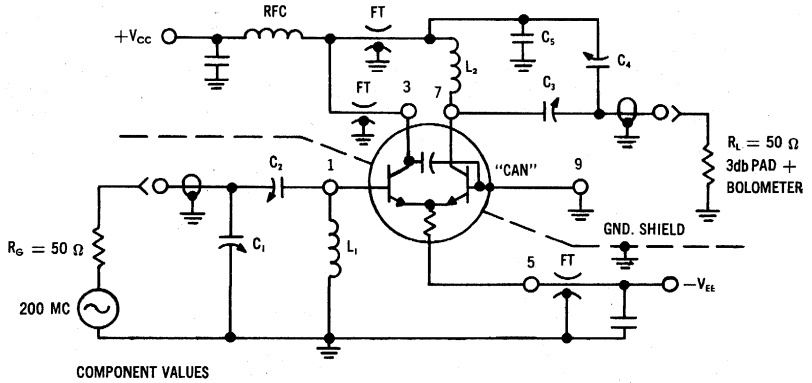


COMPONENT VALUES

C_1, C_6	VARIABLE CERAMIC CAPACITOR	9-35 $\mu\mu$f
C_3	VARIABLE CERAMIC CAPACITOR	5.5-18 $\mu\mu$f
C_4	VARIABLE CERAMIC CAPACITOR	2-8 $\mu\mu$f
C_2, C_5	FIXED MICA CAPACITOR	50 $\mu\mu$f
FT ALL	FEED THROUGH CAPACITORS	1200 $\mu\mu$f
Bypass	CAPACITORS, DISC CERAMIC	0.1 μf, 75 Vdc
L_1	INPUT INDUCTOR, 0.15 μh Q > 50	
L_2	OUTPUT INDUCTOR, 0.25 μh Q > 50	

V_{CC} = 5.0 Vdc
V_{EE} = −4 VOLTS

FIGURE 20 — 100 MC POWER GAIN TEST SET



COMPONENT VALUES

C_1, C_4	VARIABLE CERAMIC CAPACITOR	5.5-18 $\mu\mu$f
C_2, C_3	VARIABLE CERAMIC CAPACITOR	2-8 $\mu\mu$f
C_5	FIXED MICA CAPACITOR	300 $\mu\mu$f
FT ALL	FEED THROUGH CAPACITORS	1200 $\mu\mu$f
BYPASS	CAPACITORS, DISC CERAMIC	0.1 μf, 75 Vdc
L_1	INPUT INDUCTOR	30 nhy Q > 100, 2T #16 AWG ¼" FORM
L_2	OUTPUT INDUCTOR	50 nhy Q > 100, 4T #16 AWG ¼" FORM
RFC	JEFFERS MOLDED CHOKE	0.68 μh

V_{CC} = 5.0 Vdc
V_{EE} = −4 VOLTS

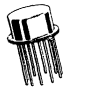
FIGURE 21— 200 MC POWER GAIN TEST SET

MC1510
MC1509

. . . designed for use as a high-frequency differential amplifier with operating characteristics that provide a flat frequency response from dc to 40 MHz.

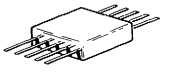
Typical Amplifier Features:

- High Gain Characteristics
  A_V = 93 typical
- Wide Bandwidth — dc to 40 MHz
- Large Output Voltage Swing —
  4.5 V p-p typical @ ±6.0 V Supply
- Low Output Distortion —
  THD ≦ 1.5%



Lead 4 connected to case

CASE 96
(TO-99)
MC1510G

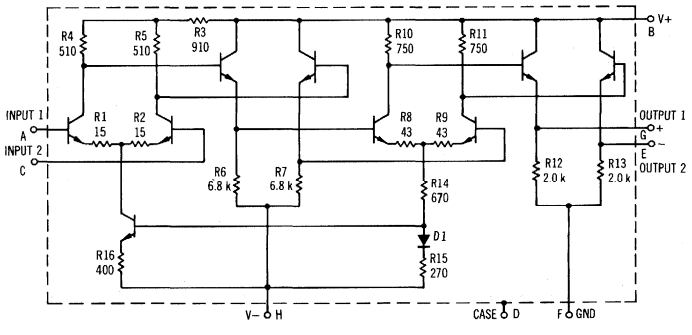


CASE 73
(TO-90)
MC1510F
MC1509F

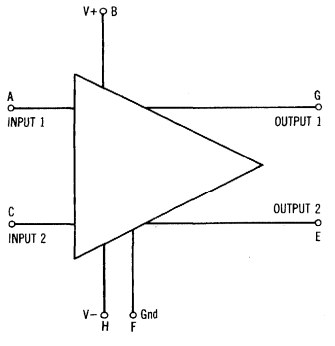
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8.0 -8.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±6.0	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



PIN CONNECTIONS								
Schematic	A	B	C	D	E	F	G	H
MC1510G	1	2	3	4	5	6	7	8
MC1510F	10	9	1	—	4	5	7	8
MC1509F	1	3	5	—	6	7	9	10

ELECTRICAL CHARACTERISTICS ($V+ = +6$ Vdc, $V- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

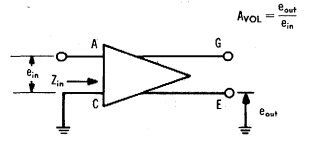
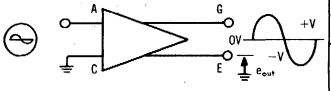
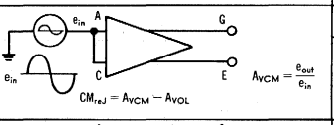
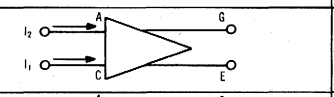
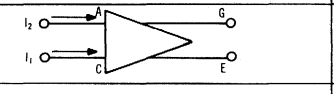
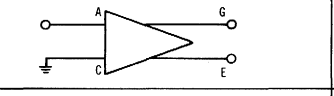
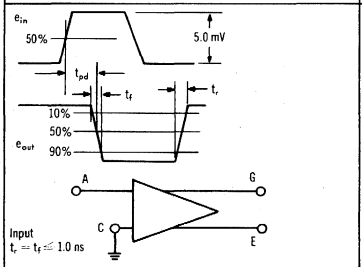
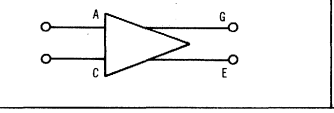
Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Single Ended Voltage Gain	$A_{V(se)}$	75	93	110	-
	Output Impedance (f = 20 kHz)	Z_{out}	-	35	-	Ω
	Input Impedance (f = 20 kHz)	Z_{in}	-	6.0	-	kΩ
	Bandwidth (-3.0 dB)	BW	-	40	-	MHz
	Output Voltage Swing (R_L = 5.0 kΩ, f = 100 kHz)	V_{out}	-	4.5	-	Vp-p
	Single Ended Output Distortion (e_{in} < 0.2% Distortion)	THD	-	1.5	5.0	%
	Input Common Mode Voltage Swing	CMV_{in}	-	±1.0	-	V_{peak}
	Common Mode Voltage Gain (R_L = 5 kΩ, e_{in} = 0.3 V rms, f = 100 kHz)	AVCM	-30	-45	-	dB
	Common Mode Rejection Ratio	CM_{rej}	-	-85	-	
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ Differential Output = 0	I_b	-	20	80	μA
	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}	-	3.0	20	μA
	Output Offset Voltage Differential Mode (V_{in} = 0)	$V_{out(DM)}$	-	0.5	1.3	Vdc
	Common Mode (Differential Output = 0)	$V_{out(CM)}$	2.6	3.1	3.5	
	Step Response	t_f t_{pd} t_r	- - -	9.0 9.0 9.0	12 - 12	ns
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = -55°C to +125°C)	TC_{Vio}	-	3.0	-	μV/°C
	($R_S \leq$ 10 kΩ, T_A = -55°C to +125°C)		-	6.0	-	
	DC Power Dissipation (Power Supply = ± 6.0 V)	P_D	-	150	220	mW
	Input Noise Voltage (f = 5.0 Hz to 10 MHz)	V_n	-	4.5	-	μV

FIGURE 1 — VOLTAGE GAIN versus FREQUENCY

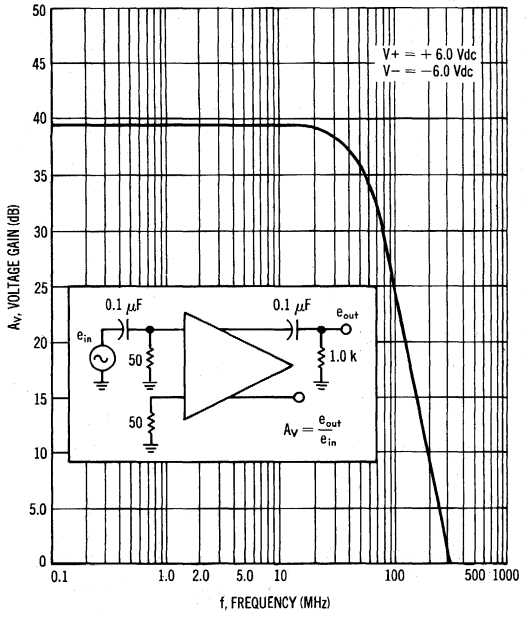


FIGURE 2 — VOLTAGE GAIN versus SUPPLY VOLTAGE

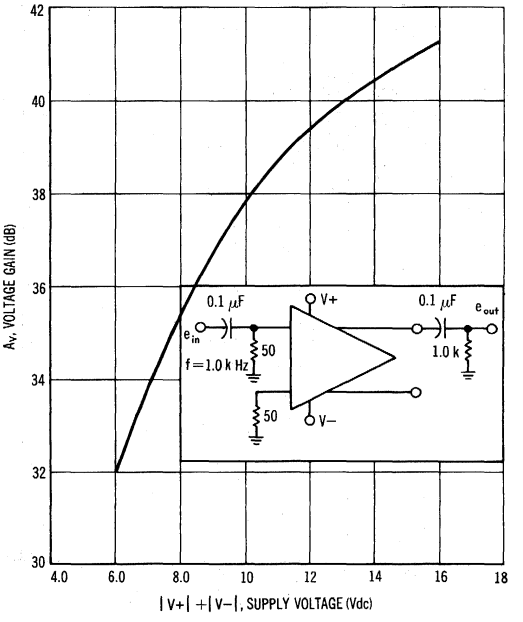


FIGURE 3 — VOLTAGE GAIN versus TEMPERATURE

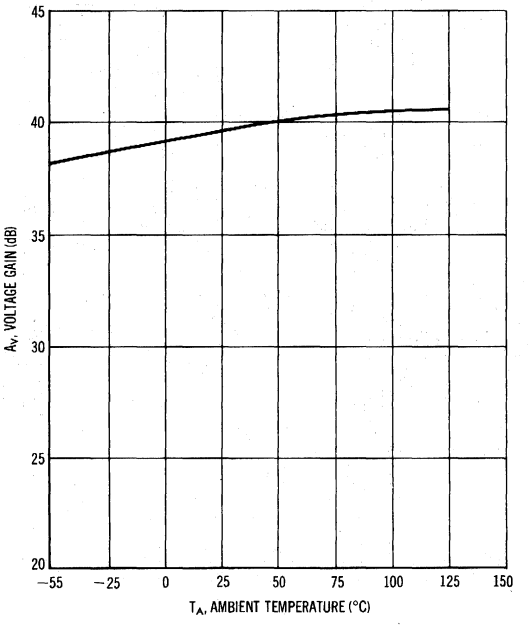


FIGURE 4 — LIMITING CHARACTERISTICS

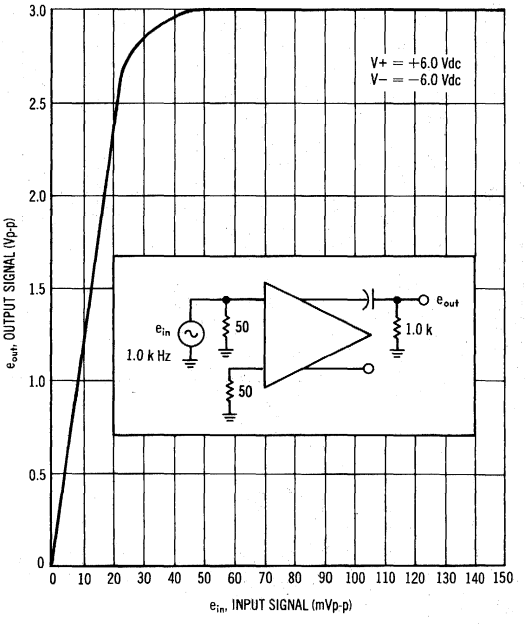


FIGURE 5 — DC OUTPUT VOLTAGE versus TEMPERATURE

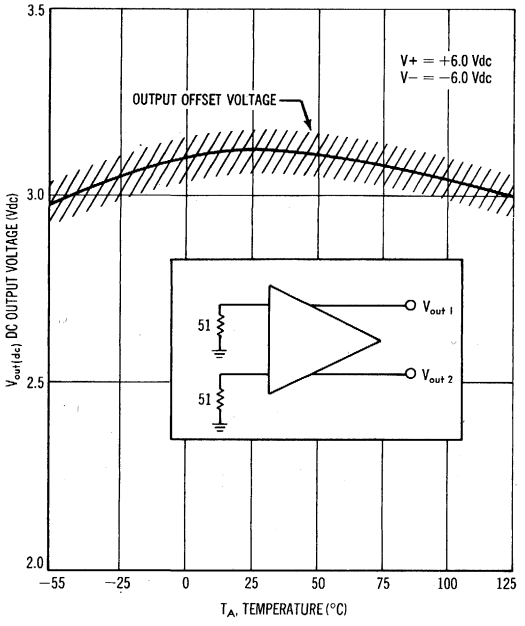


FIGURE 6 — INPUT BIAS CURRENT versus TEMPERATURE

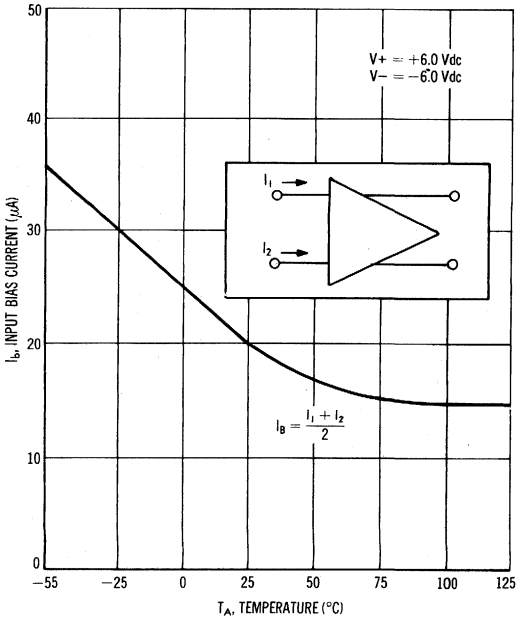


FIGURE 7 — POWER DISSIPATION versus SUPPLY VOLTAGE

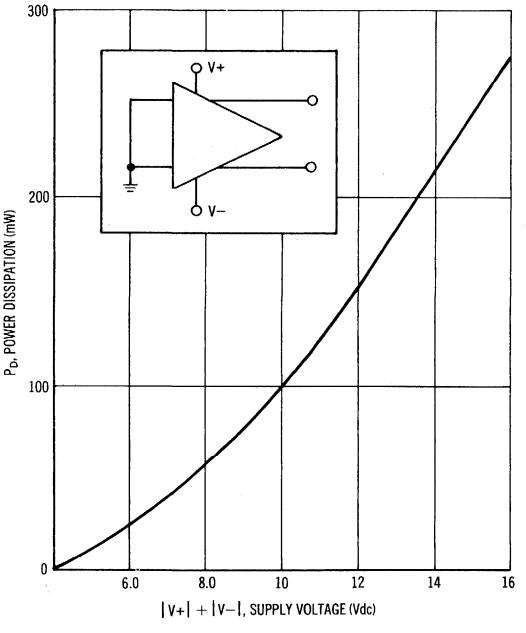
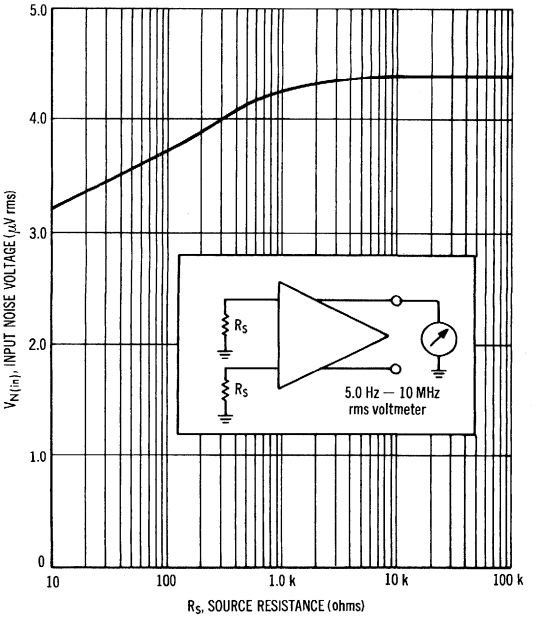


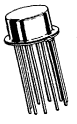
FIGURE 8 — INPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



RF-IF AMPLIFIER

MC1550G

. . . a versatile, common-emitter, common-base cascode circuit for use in communications applications.



Lead 7 connected to case

CASE 71

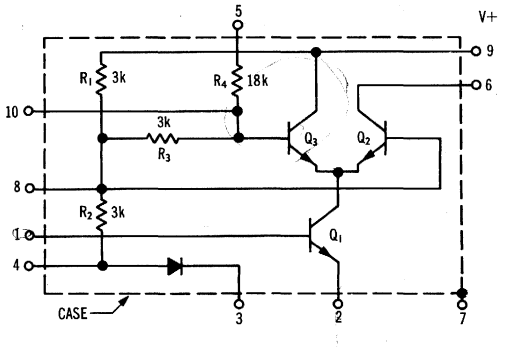
Typical Amplifier Features:

- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} – 0.001 mmho
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5.0 dB @ 60 MHz
- High Voltage-Gain–Bandwidth Product – 2.0 GHz

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V+	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Differential Input Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{in}	±5	V (RMS)
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = 25°C$)

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_{out}	3.80 5.90	— —	4.65 6.00	Vdc
Test Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_8	2.85 3.25	— —	3.40 3.80	Vdc
Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_D	— —	— —	2.2 2.5	mAdc
AGC Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_{AGC}	— —	— —	-0.2 0.18	mAdc
SMALL-SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	—	29	dB
Bandwidth	-3.0 dB	2	BW	22	—	—	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	A_P	— —	25 21	— —	dB

FIGURE 1 — DC CHARACTERISTICS TEST CIRCUIT

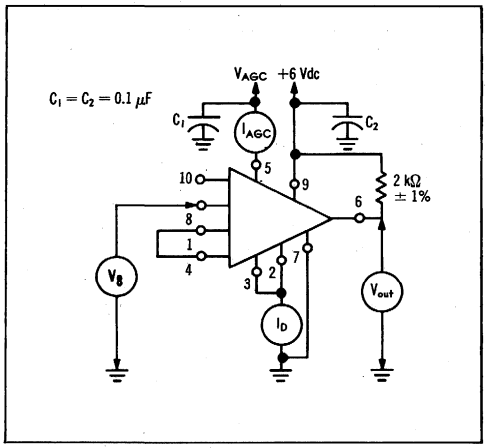


FIGURE 2 — VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

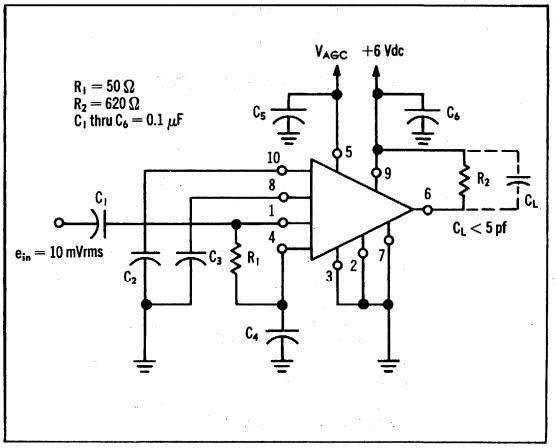


FIGURE 3 — POWER GAIN TEST CIRCUIT @ 60 MHz

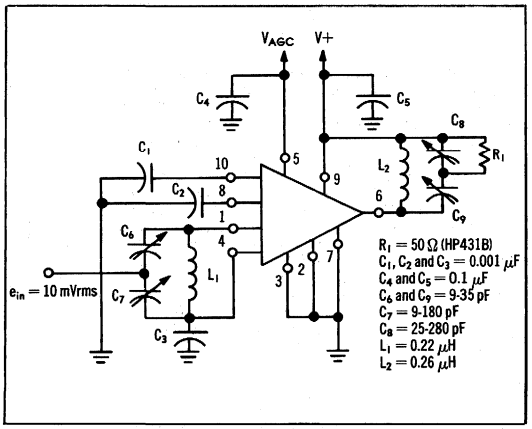


FIGURE 4 — DRAIN CURRENT TEMPERATURE CHARACTERISTICS

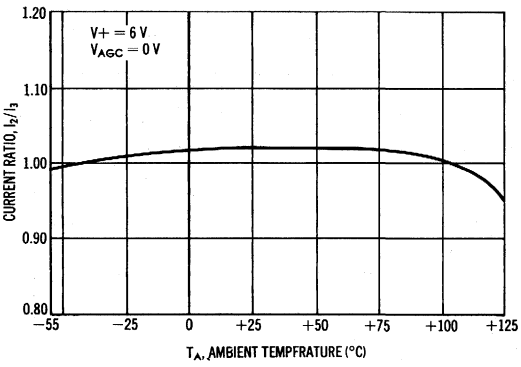


FIGURE 5 — INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

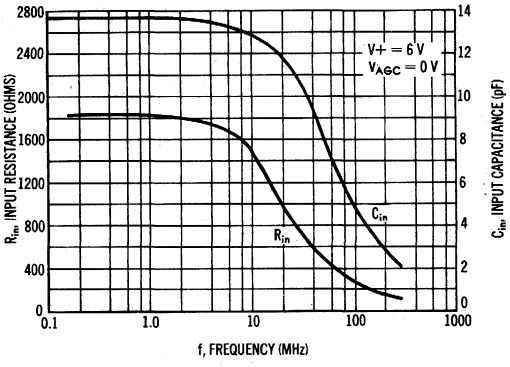


FIGURE 6 — INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

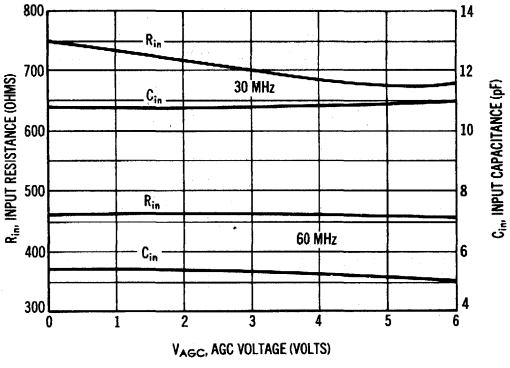


FIGURE 7 — OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

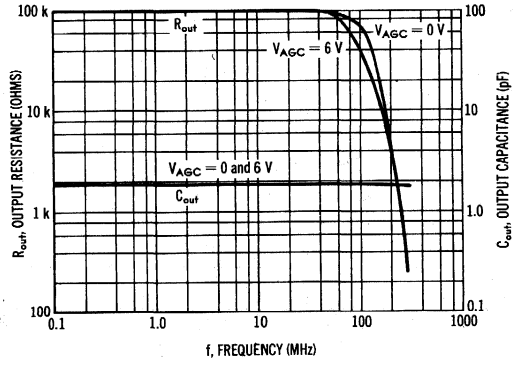


FIGURE 8 — OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

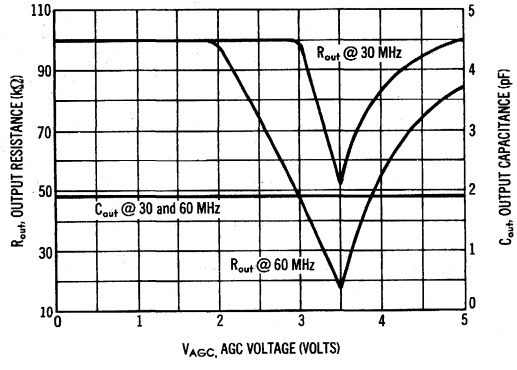


FIGURE 9 — FORWARD TRANSFER ADMITTANCE versus FREQUENCY

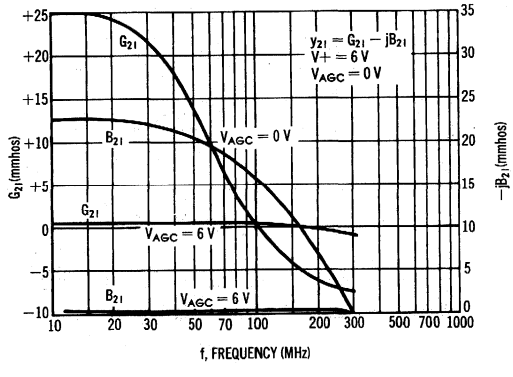


FIGURE 10 — FORWARD TRANSFER ADMITTANCE versus AGC VOLTAGE

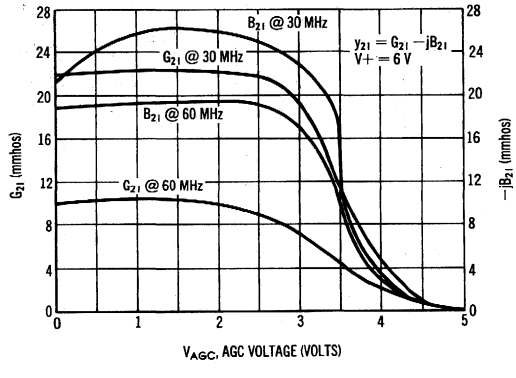


FIGURE 11 — MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

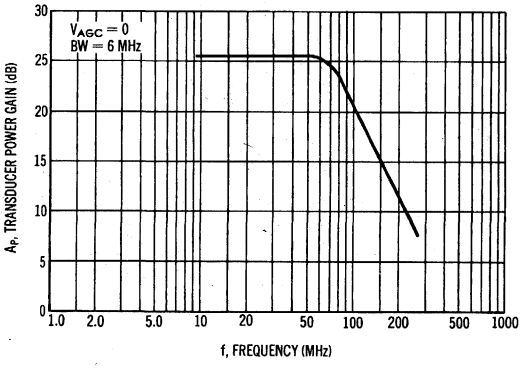


FIGURE 12 — TRANSDUCER POWER GAIN versus TEMPERATURE

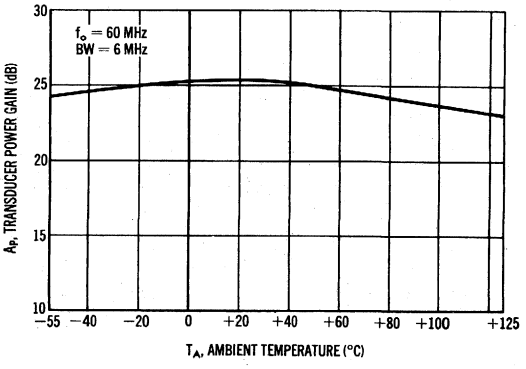


FIGURE 13 — TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

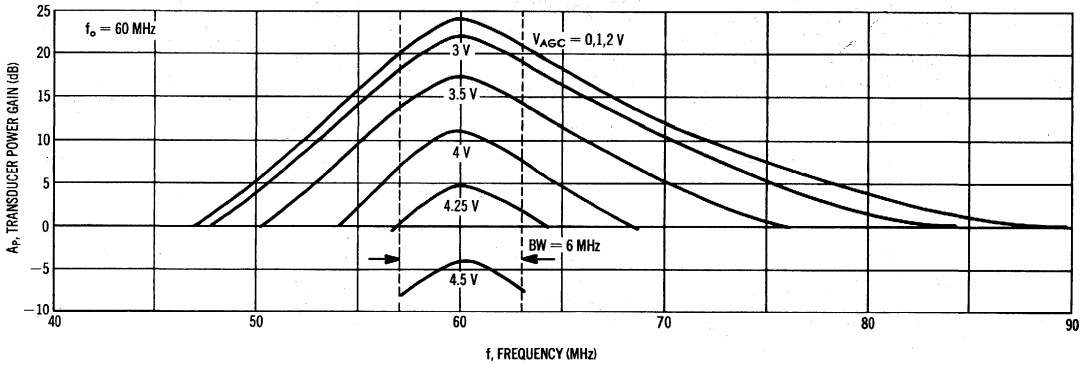


FIGURE 14 — NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

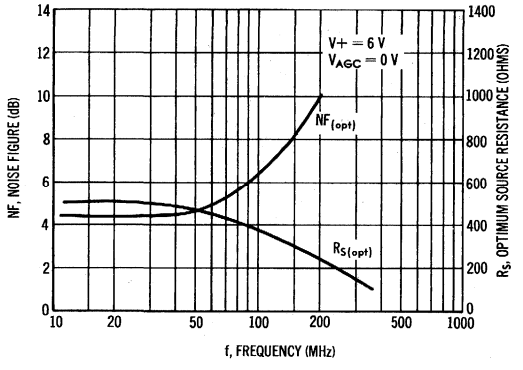
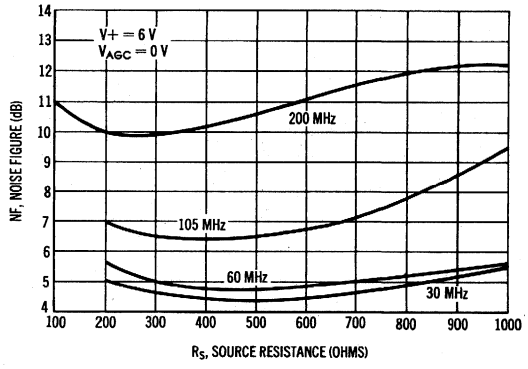
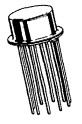


FIGURE 15 — NOISE FIGURE versus SOURCE RESISTANCE



MC1552G
MC1553G

. . . a three-stage, direct-coupled, common-emitter cascade incorporating series-series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. Employs a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output. Intended for use as either a wide-band linear amplifier or as a fast rise pulse amplifier.



Lead 6 connected to case

CASE 71

Typical Amplifier Features:

- High Gain – 34 dB ±1.0 dB (MC1552)
  52 dB ±1.0 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V^+	9	Vdc
Input Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{in}	1.0	V(RMS)
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS

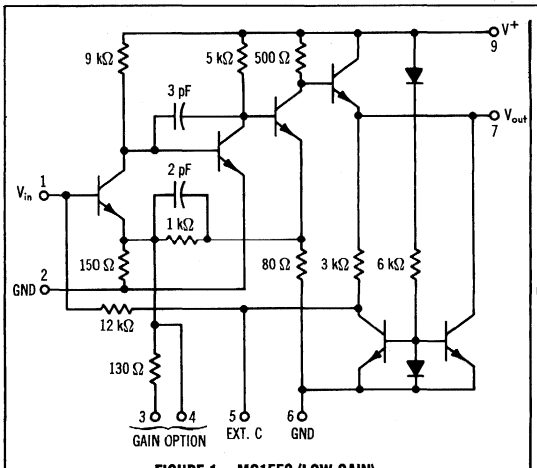


FIGURE 1 – MC1552 (LOW GAIN)

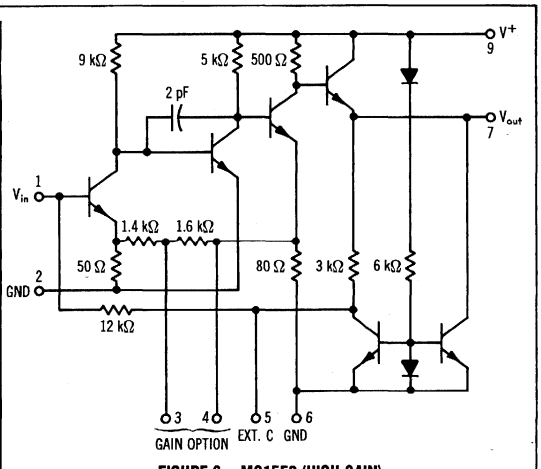


FIGURE 2 – MC1553 (HIGH GAIN)

ELECTRICAL CHARACTERISTICS (V^+ = +6 Vdc, T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Gain * Option	Symbol	Min	Typ	Max	Unit
Voltage Gain	MC1552	3	50	V_{out}/V_{in}	44	50	56	V/V
			100		87	100	113	
	MC1553		200		175	200	225	
			400		350	400	450	
Voltage Gain Variation (T_A = -55°C to +125°C)		3	All	—	—	±0.2	—	dB
Bandwidth	MC1552	3, 6	50	BW	21	40	—	MHz
			100		17	35	—	
	MC1553		200		17	35	—	
			400		7.5	15	—	
Input Impedance (f = 100 kHz, R_L = 1 kΩ)		—	All	$\lvert Z_{in} \rvert$	7	10	—	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		—	All	$\lvert Z_{out} \rvert$	—	16	50	Ω
DC Output Voltage		3	All	V_{out} (dc)	2.5	2.9	3.2	Vdc
DC Output Voltage Variation (T_A = -55°C to +125°C)		3	All	ΔV_{out} (dc)	—	±0.05	—	Vdc
Output Voltage Swing ($Z_L \geq$ 1 kΩ, V_{in} = 100 mV rms)		3	All	V_{out}	3.6	4.2	—	Vp-p
Power Dissipation		—	All	P_D	—	75	120	mW
Delay Time	MC1552	3, 4	50	t_{pd}	—	8	—	ns
			100		—	9	—	
	MC1553		200		—	10	—	
			400		—	25	—	
Rise Time	MC1552	3, 4	50	t_r	—	9	16	ns
			100		—	12	20	
	MC1553		200		—	11	20	
			400		—	30	45	
Overshoot		3, 4	All	$(V_{os}/V_p)100$	—	5	—	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz, BW = 3 MHz)		—	All	NF	—	5	—	dB
Total Harmonic Distortion (V_{out} = 2 Vp-p, f = 200 kHz, R_L = 1 kΩ)		—	All	THD	—	0.2	—	%

*To obtain the voltage-gain characteristic desired, use the following pin connections:

Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

NOTES

1. Ground Pin 6 as close to can as possible to minimize overshoot. Best results by directly grounding can.
2. If large input and output coupling capacitors are used, place shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to bypass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C_1 and C_2 rather than the circuits shown in Figure 5.

Fig. 5b $C_1 = \dfrac{1}{2\pi f_c (1.7 \times 10^4)}$ Farads; $C_2 = 8\,C_1 (V_{out}/V_{in})$ Farads

Fig. 5c $C_1 = \dfrac{V_{out}/V_{in}}{2\pi f_c (1.5 \times 10^4)}$ Farads

Fig. 5d $C_2 = \dfrac{V_{out}/V_{in}}{2\pi f_c (3 \times 10^3)}$ Farads

FIGURE 3—TEST CIRCUIT

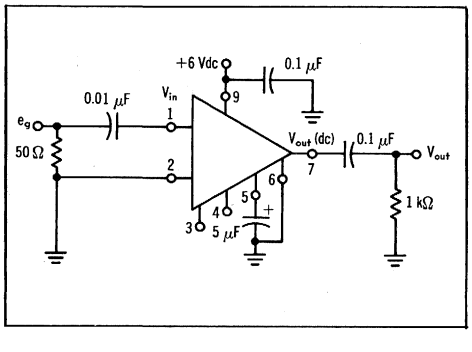
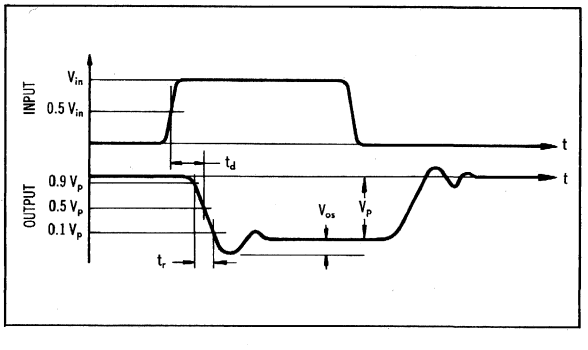


FIGURE 4—PULSE RESPONSE DEFINITIONS



TYPICAL CHARACTERISTICS

$T_A = 25°C$

FIGURE 5a — FREQUENCY RESPONSE

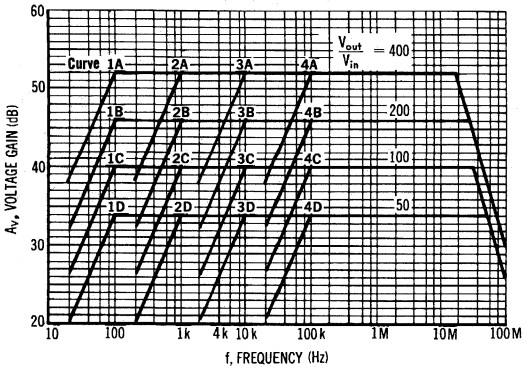
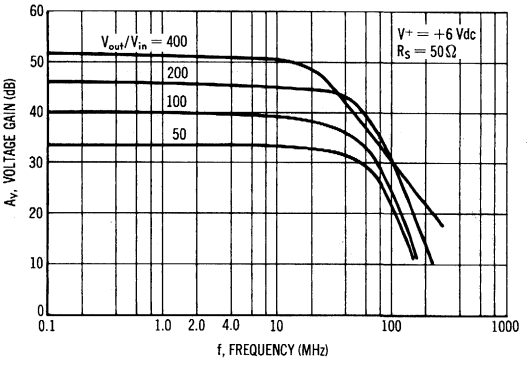
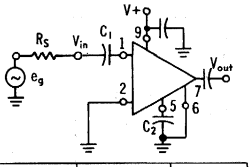


FIGURE 6 — VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

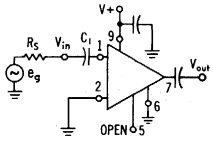
FIGURE 5b — CAPACITIVE COUPLED INPUT ($R_s < 5k\Omega$)



Curve No.	C_1 (μF)	C_2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

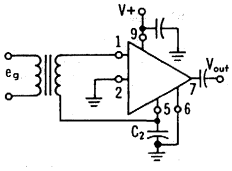
Curve No.	C_1 (μF)	C_2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 5c — CAPACITIVE COUPLED INPUT ($R_s < 500\Omega$)



Curve No.	C_1 (μF)	Curve No.	C_1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 5d — TRANSFORMER COUPLED INPUT



Curve No.	C_2 (μF)	Curve No.	C_2 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

FIGURE 7 — MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

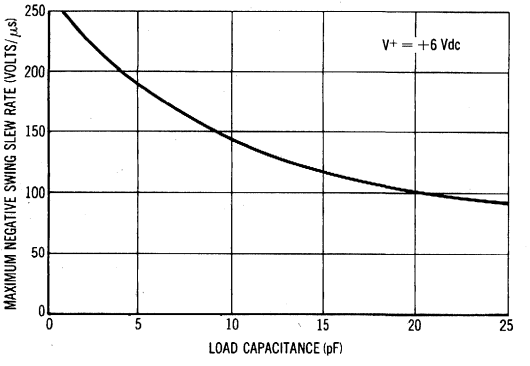
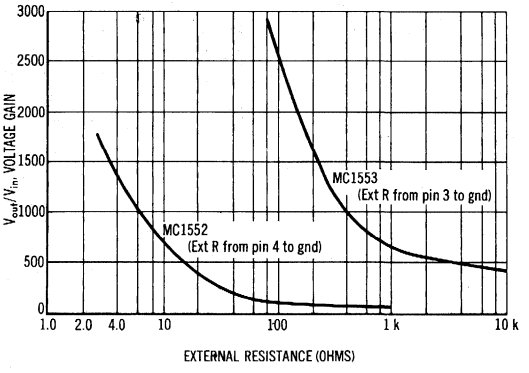


FIGURE 8 — VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR



INPUT ADMITTANCE

$V^+ = 6$ Vdc, $R_L = 1$ kΩ, $T_A = 25°C$

FIGURE 9 – GAIN = 50

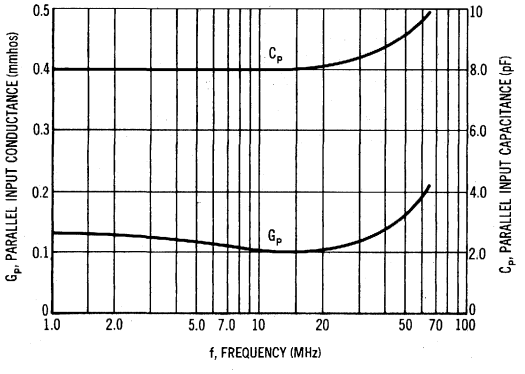


FIGURE 10 – GAIN = 100

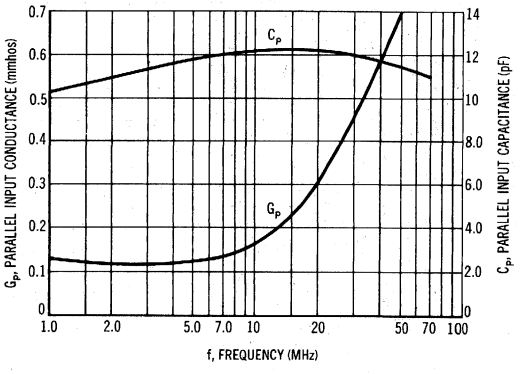


FIGURE 11 – GAIN = 200

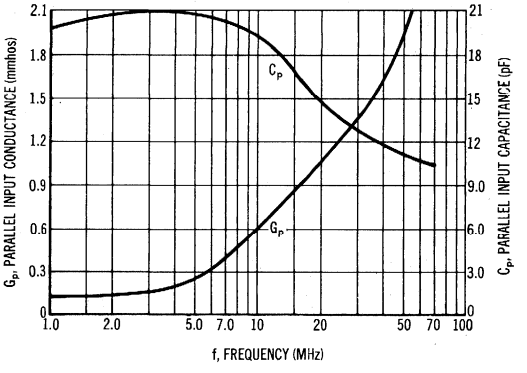


FIGURE 12 – GAIN = 400

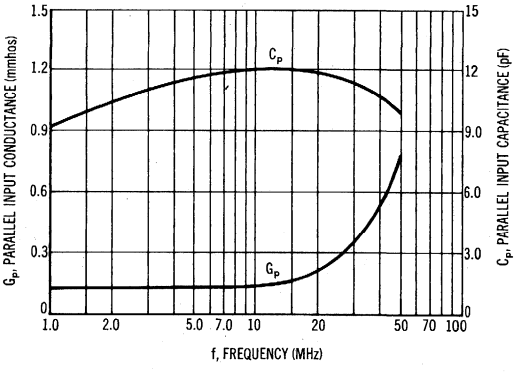


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

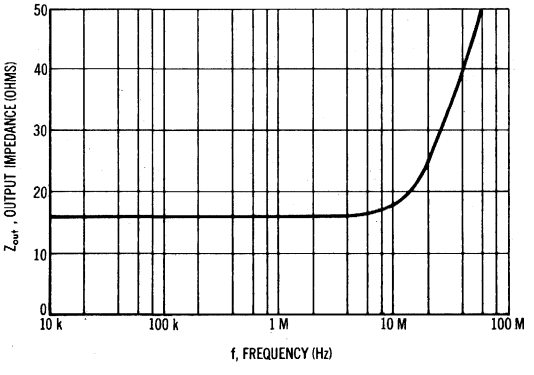
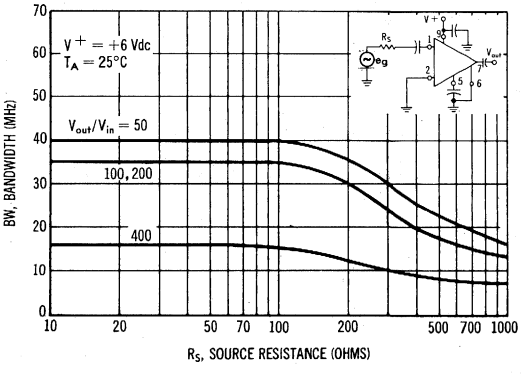


FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE



MC1524

Typical Amplifier Features:

- Low Standby Current Drain – < 4 mA
- Low Total Harmonic Distortion
- 1-Watt Power Output
- Low Output Impedance
- Direct Coupling to Load
- Excellent Gain – Temperature Stability



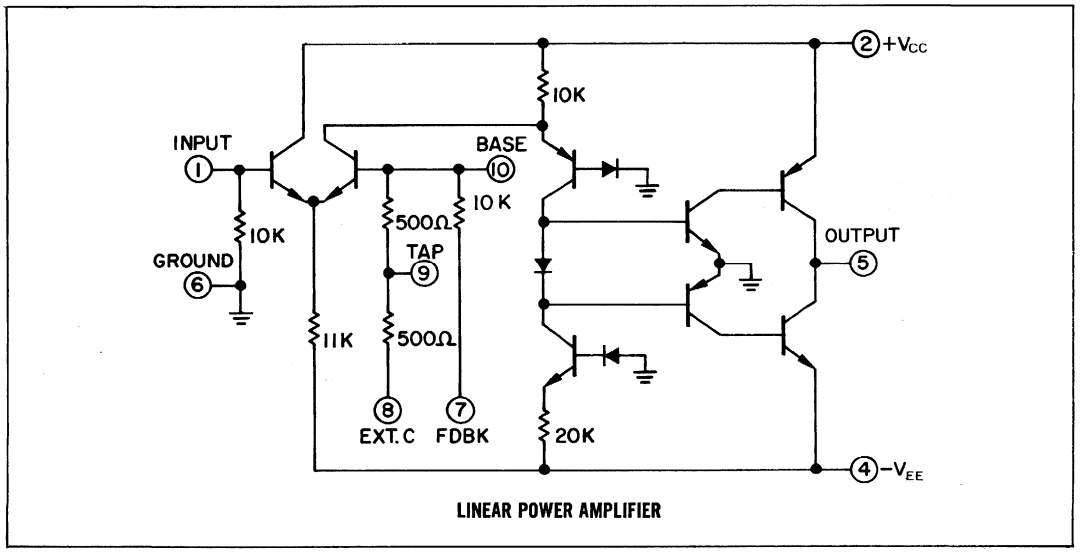
CASE 71

Lead 6 connected to case

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	Vdc
Power Supply Voltage	V_{EE}	-12	Vdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C
Maximum Audio Output Power (T_A = -55°C to +125°C)	$P_{out(max)}$	1.0	Watt

FIGURE 1 – CIRCUIT SCHEMATIC



LINEAR POWER AMPLIFIER

ELECTRICAL CHARACTERISTICS ($V_{CC} = +6\,V, V_{EE} = -6\,V, T_A = 25°C$. See Fig. 1)

Characteristic	Load Impedance ohms	Feedback Tap ohms	Symbol	Min	Typ	Max	Units
Maximum Peak-to-Peak Output Voltage for THD < 3% @ 1 kHz	16	1000	V_{Omax}	9.0	10.0	—	$V_{(P-P)}$
Voltage Gain @ 1 kHz	16	250	A_V	—	37.9	—	—
		500		—	20.0	—	
		1000		10.0	11.5	12.5	
	100	250		—	41.2	—	
		500		—	21.3	—	
		1000		11.0	12.3	13.5	
Input Impedance @ 1 kHz	—	1000	Z_{in}	6.0	8.5	—	kohms
Output Impedance @ 1 kHz	—	1000	Z_{out}	—	0.58	0.80	ohms
Bandwidth	16	250	BW	—	350	—	kHz
		500		—	480	—	
		1000		250	770	—	
	40	250		—	340	—	
		500		—	480	—	
		1000		—	790	—	
	100	250		—	320	—	
		500		—	480	—	
		1000		—	810	—	
Zero Signal Current Drain (Each Supply)	16	1000	I_S	—	1.5	4.0	mA
Low Level Total Harmonic Distortion @ 1 kHz (50 mVrms in)	16	1000	THD	—	0.6	2.0	%

FIGURE 1 — AC COUPLED CIRCUIT

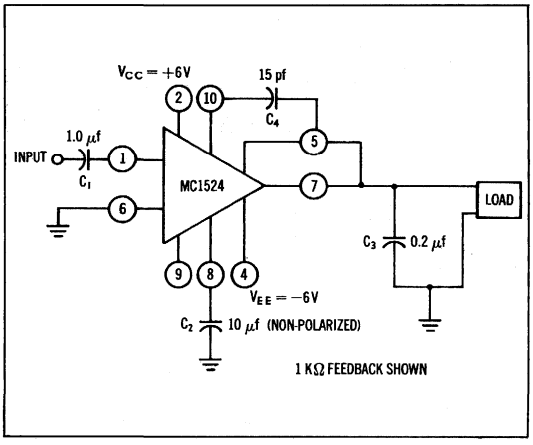
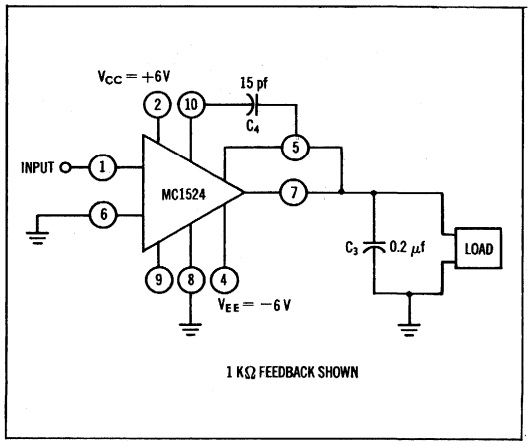


FIGURE 2 — DC COUPLED CIRCUIT



RECOMMENDED OPERATING CONDITIONS

1) DC load resistance (R_L) should be greater than 5 ohms for DC stability.

2) Power supplies should be balanced, have low source impedances, and should be turned on and off simultaneously. (See Fig. 6 for Standby Current vs. Supply Unbalance.)

3) Capacitors C_3 and C_4 provide high-frequency stability. For most loads, at temperatures below 70°C, C_4 may be omitted.

4) Low frequency rolloff of AC coupled circuit is determined by C_1 and C_2. Fig 1 is recommended for loudspeaker loads because of DC stability introduced by C_2.

5) Open loop operation is not recommended. Feedback taps are connected as follows:

Feedback Tap	Pin Connection
1 KΩ	8 to C_2 (AC) or ground (DC)
500Ω	9 to C_2 (AC) or ground (DC)
250Ω	8 to 10; 9 to C_2 (AC) or ground (DC)

FIGURE 3 — MAXIMUM AVAILABLE OUTPUT POWER
(BEFORE CLIPPING — RESISTIVE LOAD)

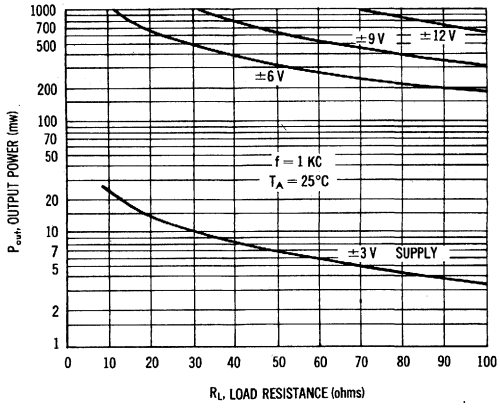


FIGURE 4 — TOTAL HARMONIC DISTORTION

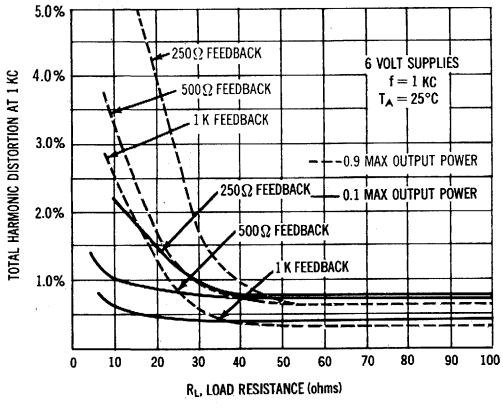


FIGURE 5 — AC COUPLED FREQUENCY RESPONSE

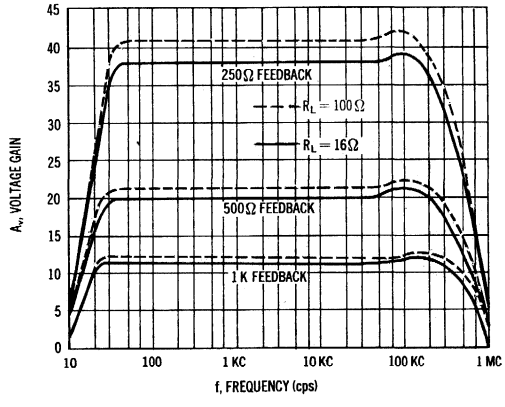


FIGURE 6 — STANDBY CURRENT VARIATION DUE TO SUPPLY UNBALANCE

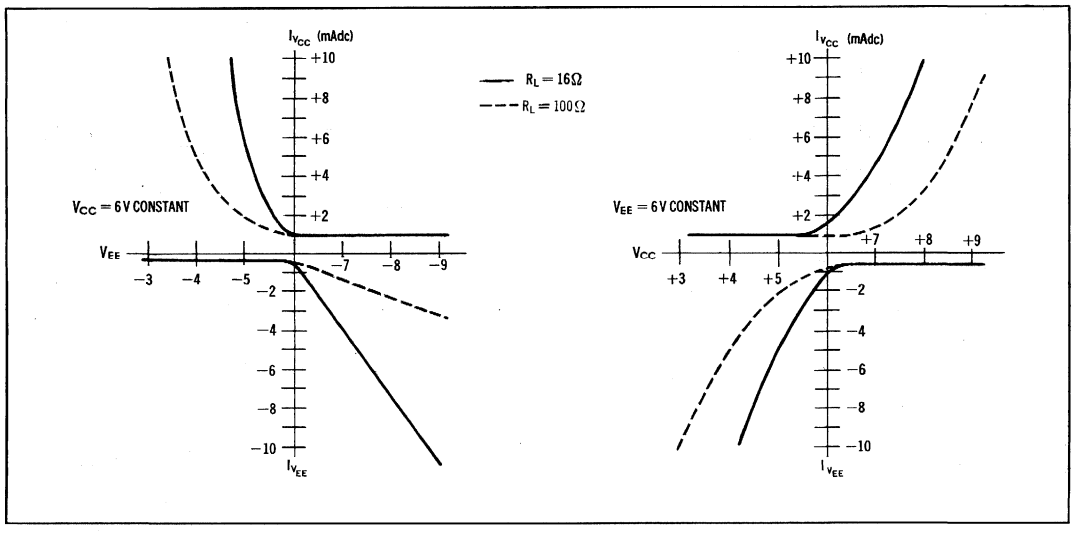
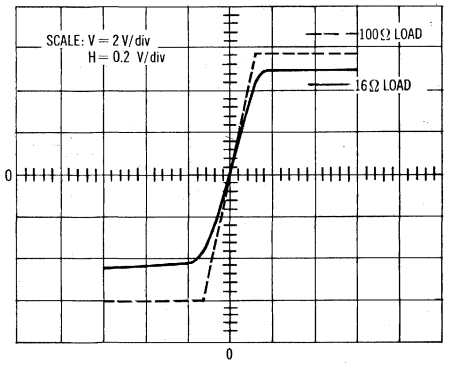
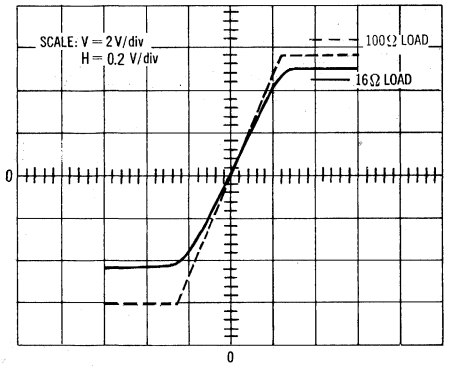


FIGURE 7 – DC TRANSFER CHARACTERISTICS





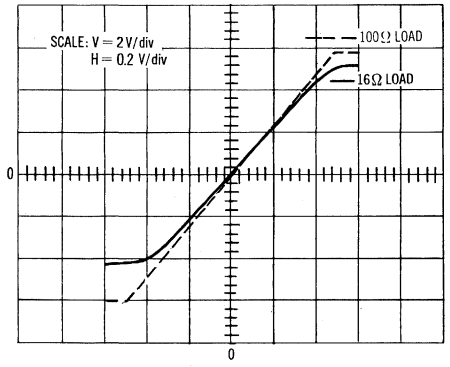
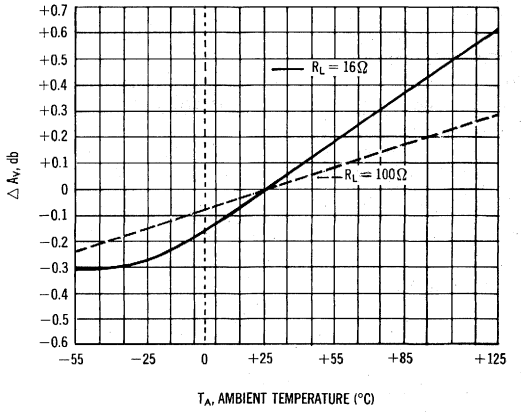
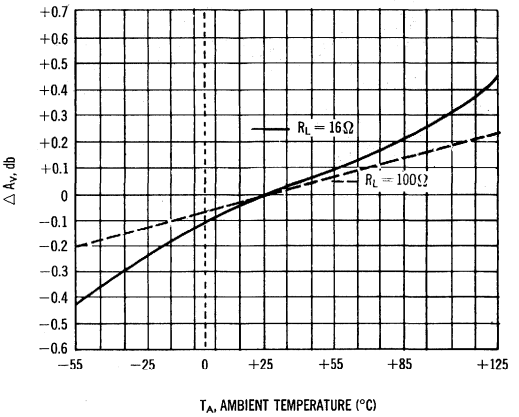


FIGURE 8 – VOLTAGE GAIN versus TEMPERATURE

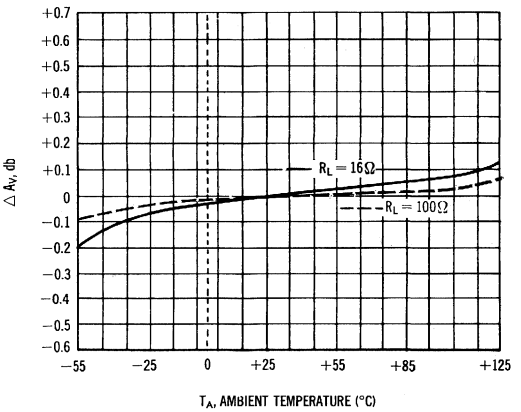
250Ω FEEDBACK TAP



500Ω FEEDBACK TAP



1 KΩ FEEDBACK TAP

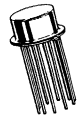


MC1554G

. . . designed to amplify signals to 300 kHz with one watt delivered to a direct or capacitively coupled load.

Typical Amplifier Features:

- Low Total Harmonic Distortion — 0.4% typical at 1.0 Watt
- Low Output Impedance — 0.2 ohm
- Excellent Gain — Temperature Stability



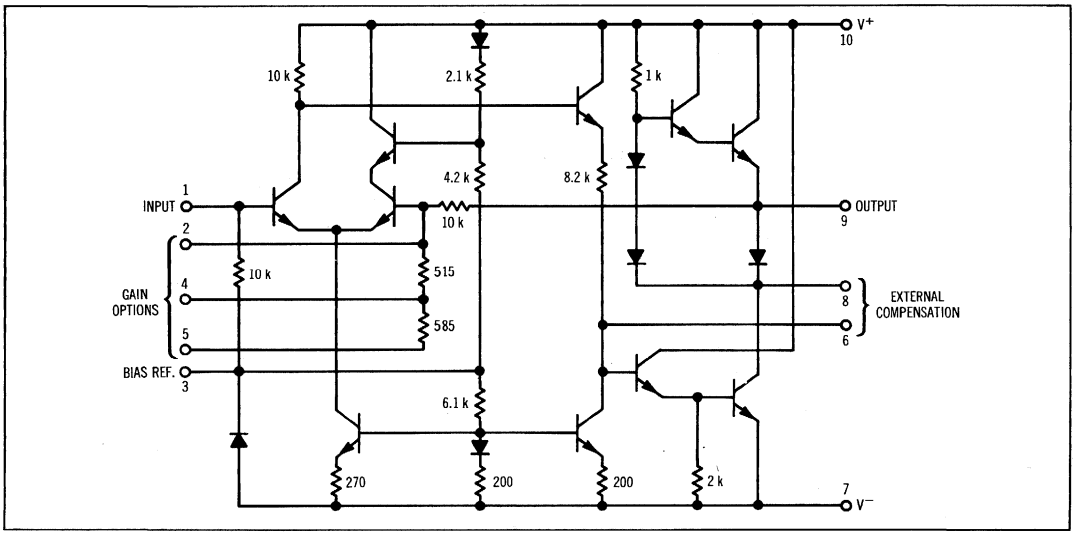
CASE 71

Lead 7 connected to case

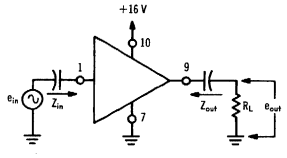
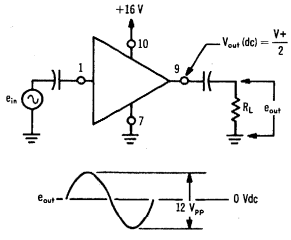
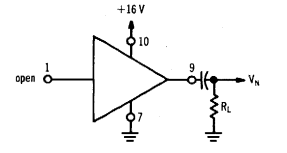
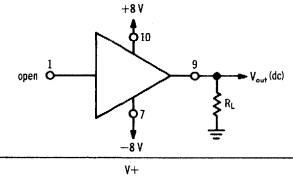
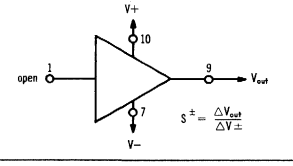
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Total Power Supply Voltage	$\|V^+\| + \|V^-\|$	18	Vdc
Peak Load Current	I_{out}	0.5	Amp
Audio Output Power	P_{out}	1.8	Watt
Power Dissipation (package limitation)	P_D		
T_A = 25°C		600	mW
Derate above 25°C		4.8	mW/°C
T_C = 25°C		1.8	Watts
Derate above 25°C		14.4	mW/°C
Operating Temperature Range	T_C	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)
Frequency compensation shown in Figures 2 and 3.

Characteristic Definitions	Characteristic	R_L (ohms)	Gain Option*	Symbol	Min	Typ	Max	Unit
	Output Power	16	-	P_{out}	1.0	1.1	-	Watt
	Power Dissipation (@ P_{out} = 1.0 W)	16	-	P_D	-	0.9	1.2	Watt
	Voltage Gain	16	10	A_V	8.0	10	12	V/V
		16	18		-	18	-	
		16	36		-	36	-	
	Input Impedance	-	10	Z_{in}	7.0	10	-	kΩ
	Output Impedance	-	10	Z_{out}	-	0.2	-	Ω
	Power Bandwidth (for e_{out} < 5% THD)	16	10		-	270	-	kHz
		16	18		-	250	-	
		16	36		-	210	-	
	Total Harmonic Distortion (for e_{in} < 0.05% THD, f = 20 Hz to 20 kHz)			THD				%
	P_{out} = 1.0 Watt (sinewave)	16	10		-	0.4	-	
	P_{out} = 0.1 Watt (sinewave)	16	10		-	0.5	-	
	Zero Signal Current Drain	∞	-	I_D	-	11	15	mAdc
	Output Noise Voltage	16	10	V_n	-	0.3	-	mV RMS
	Output Quiescent Voltage (Split Supply Operation)	16	-	$V_{out}(dc)$	-	±10	±30	mVdc
	Positive Supply Sensitivity (V^- constant)	∞	-	S^+	-	-40	-	mV/V
	Negative Supply Sensitivity (V^+constant)	∞	-	S^-	-	-40	-	mV/V

* To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

TYPICAL CONNECTIONS

FIGURE 2—SPLIT SUPPLY OPERATION
VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 25 Hz

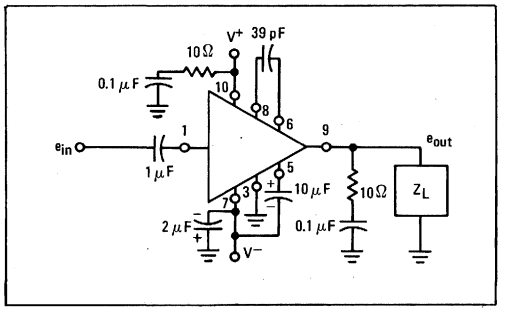
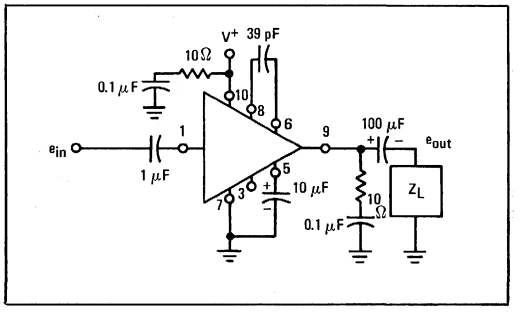


FIGURE 3—SINGLE SUPPLY OPERATION
VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 100 Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 2 and 3, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V+ supply to pin 10 can cause high frequency instability. To prevent this, the V+ by-pass capacitor should be connected with short leads from the V+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 2 and 3.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 4 — MAXIMUM AVAILABLE OUTPUT POWER
(SINE WAVE)

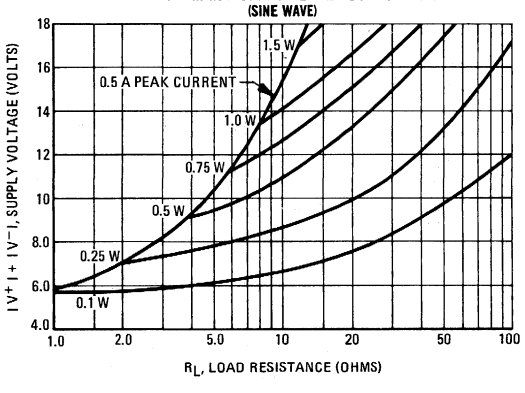


FIGURE 5 — MAXIMUM DEVICE DISSIPATION
(SINE WAVE)

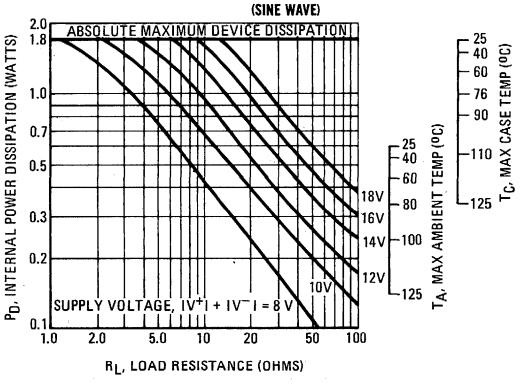


FIGURE 6 — TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

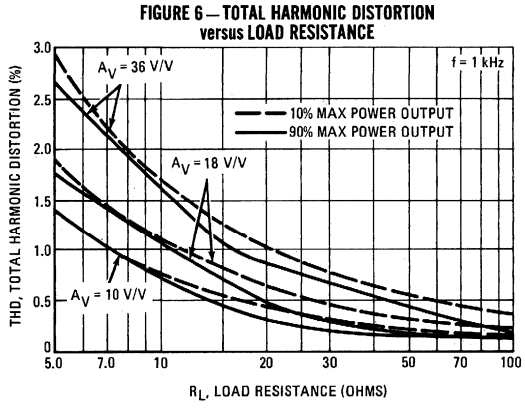
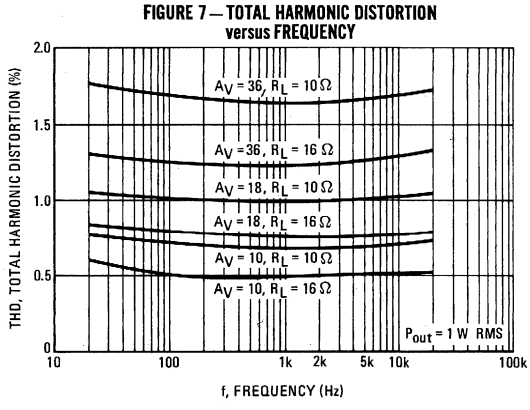


FIGURE 7 — TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS

FIGURE 8 — VOLTAGE GAIN versus TEMPERATURE

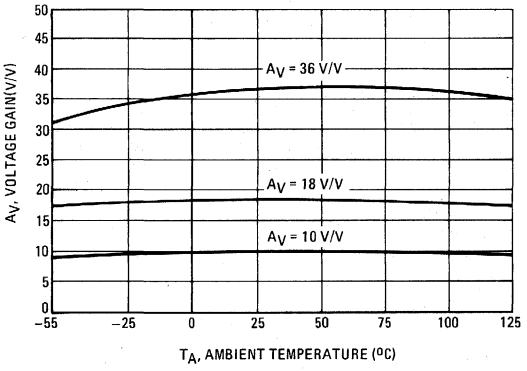


FIGURE 9 — OUTPUT VOLTAGE CHANGE

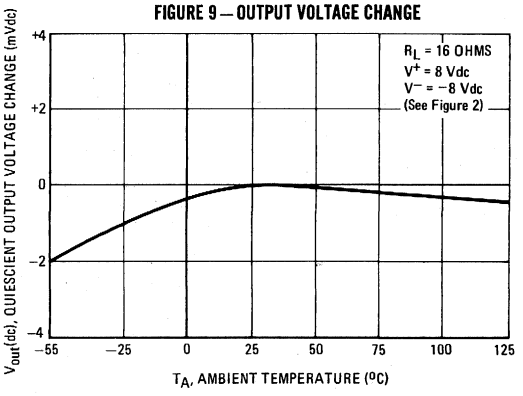


FIGURE 10 — VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)

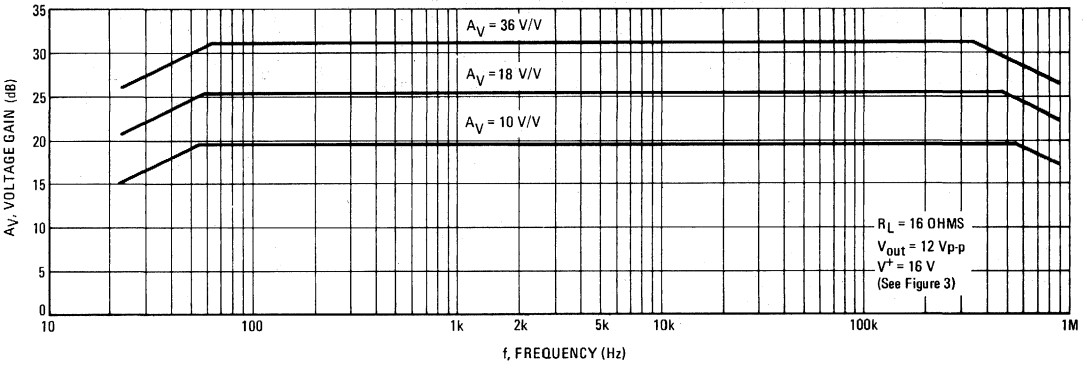
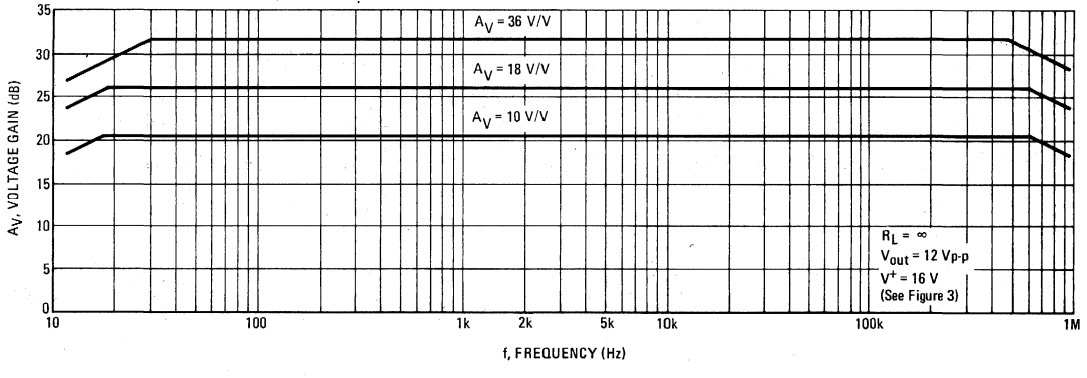


FIGURE 11 — VOLTAGE GAIN versus FREQUENCY (R_L = ∞)



DIFFERENTIAL AMPLIFIER

MC1519

. . . featuring NPN inputs and PNP outputs. Two monolithic compatible* chips are used to provide a versatile and extremely stable amplifier.

*Compatible — a process utilizing thin film resistors deposited on a silicon monolithic integrated circuit.



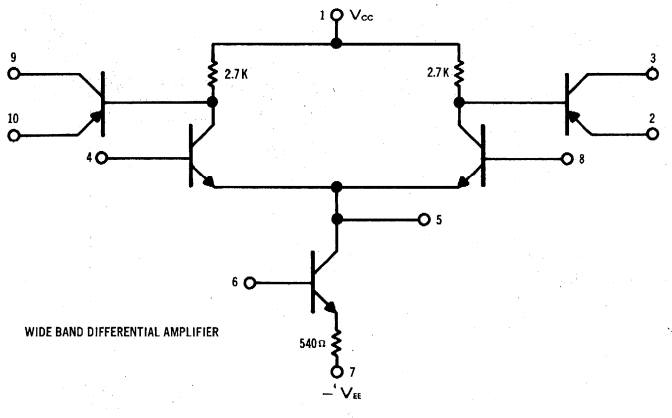
CASE 71

All pins electrically isolated from package

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	Vdc
Power Supply Voltage	V_{EE}	-14	Vdc
Differential Input Signal	V_{in}	±5	Vdc
Total Power Dissipation Derate above 25°C	P_D	300 2.0	mW mW/°C
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

CIRCUIT SCHEMATIC

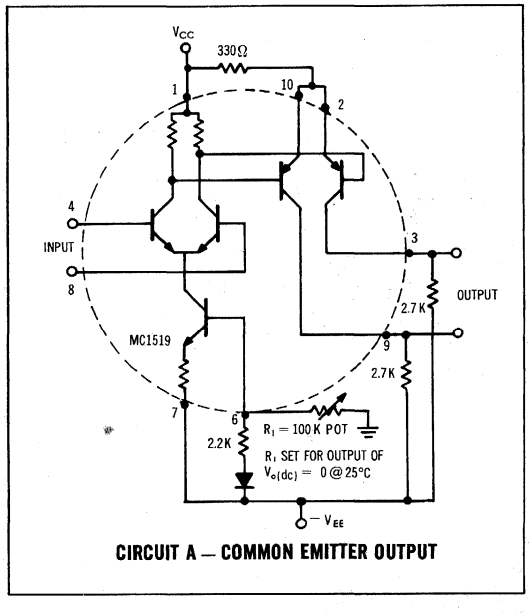


WIDE BAND DIFFERENTIAL AMPLIFIER

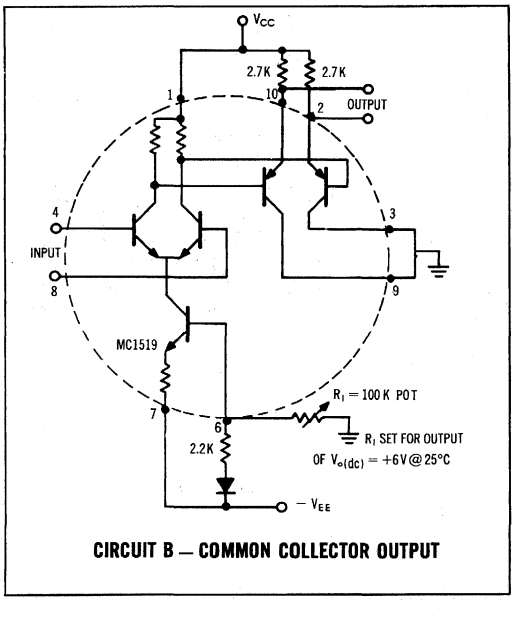
ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc. V_{EE} = −12 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain Circuit A (CE) Circuit B (CC)	3, 8	A_{dd}	 67 40	 73 45	 79 50	db
Single Ended Voltage Gain Circuit A (CE) Circuit B (CC)	3	A_V	 — —	 67 38	 — —	db
Maximum Output Swing Circuit A (CE) Circuit B (CC)	4	V_O	 12.0 8.0	 14.0 10.0	 — —	$V_{(p-p)}$
Input Offset Voltage Circuit A (CE) Circuit B (CC)	5, 9	V_{IO}	 — —	 2.0 2.0	 6.0 6.0	mVdc
Input Offset Voltage Drift Circuit A (CE) Circuit B (CC)	5, 9	V_{IOD}	 — —	 5.0 5.0	 — —	$\mu V/^oC$
Input Offset Current Circuit A (CE) Circuit B (CC)	6, 10	I_{IO}	 — —	 1.0 2.0	 4.0 8.0	μAdc
Input Current Circuit A (CE) Circuit B (CC)	6, 11	I_i	 — —	 40.0 60.0	 70.0 90.0	μAdc
Common Mode Rejection Circuit A (CE) Circuit B (CC)	7	CM_{Rej}	 — —	 89.0 86.0	 — —	db
Bandwidth - 3 db Circuit A (CE) Circuit B (CC)	3, 12	BW	 0.70 5.0	 1.0 8.0	 — —	mc
Differential Input Impedance Circuit A (CE) Circuit B (CC)	2	Z_{in}	 1.8 —	 2.6 1.2	 — —	kohms
Single Ended Output Impedance Circuit A (CE) Circuit B (CC)	2	Z_{out}	 — —	 2.7 0.048	 — 0.120	kohms

FIGURE 1



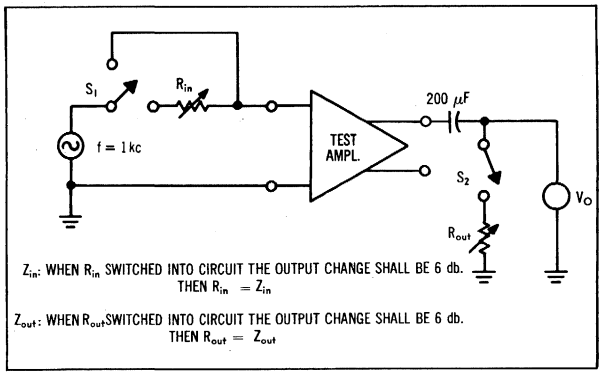
CIRCUIT A — COMMON EMITTER OUTPUT



CIRCUIT B — COMMON COLLECTOR OUTPUT

TEST CIRCUITS

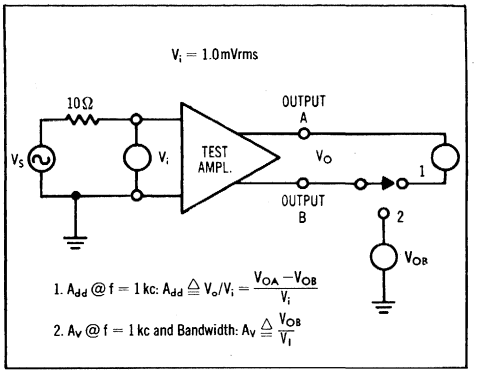
FIGURE 2 — DIFFERENTIAL INPUT IMPEDANCE AND SINGLE-ENDED OUTPUT IMPEDANCE



Z_{in}: WHEN R_{in} SWITCHED INTO CIRCUIT THE OUTPUT CHANGE SHALL BE 6 db. THEN $R_{in} = Z_{in}$

Z_{out}: WHEN R_{out} SWITCHED INTO CIRCUIT THE OUTPUT CHANGE SHALL BE 6 db. THEN $R_{out} = Z_{out}$

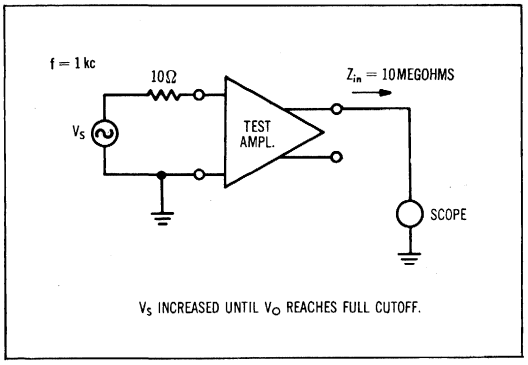
FIGURE 3 — DIFFERENTIAL VOLTAGE GAIN, SINGLE-ENDED VOLTAGE GAIN, and BANDWIDTH



1. A_{dd} @ f = 1 kc: $A_{dd} \triangleq V_o/V_i = \frac{V_{oA} - V_{oB}}{V_i}$

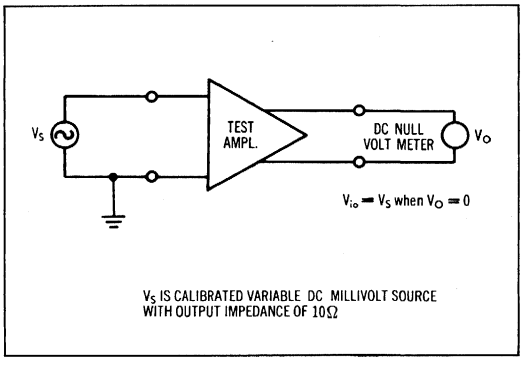
2. A_V @ f = 1 kc and Bandwidth: $A_V \triangleq \frac{V_{oB}}{V_i}$

FIGURE 4 — MAXIMUM OUTPUT SWING



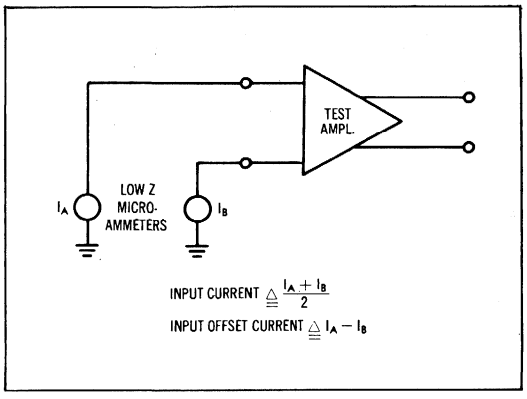
V_S INCREASED UNTIL V_O REACHES FULL CUTOFF.

FIGURE 5 — INPUT OFFSET VOLTAGE



V_S IS CALIBRATED VARIABLE DC MILLIVOLT SOURCE WITH OUTPUT IMPEDANCE OF 10Ω

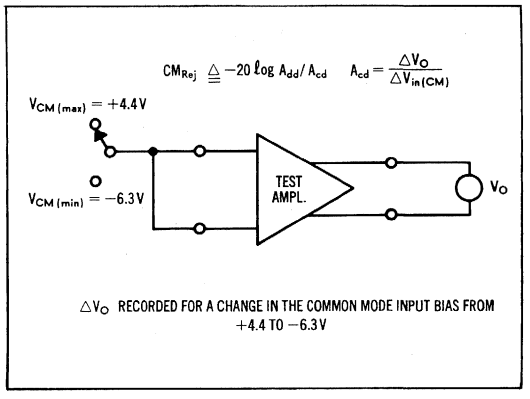
FIGURE 6 — INPUT OFFSET CURRENT and INPUT CURRENT



INPUT CURRENT $\triangleq \frac{I_A + I_B}{2}$

INPUT OFFSET CURRENT $\triangleq I_A - I_B$

FIGURE 7 — COMMON MODE REJECTION



ΔV_O RECORDED FOR A CHANGE IN THE COMMON MODE INPUT BIAS FROM +4.4 TO −6.3 V

EFFECT OF TEMPERATURE ON CIRCUIT B CHARACTERISTICS

R_1 SET FOR $V_{O(CM)} = +6V$ AT $+25°C$

FIGURE 8 — DIFFERENTIAL MODE GAIN

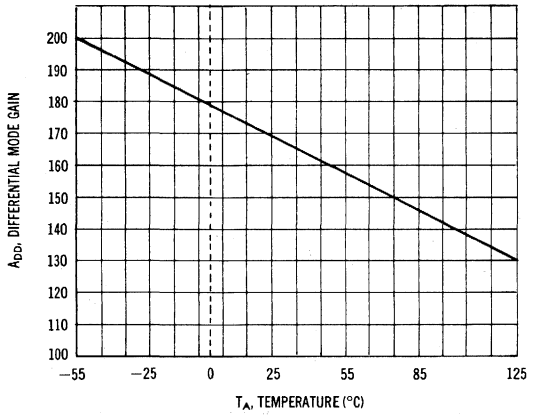


FIGURE 9 — INPUT OFFSET VOLTAGE

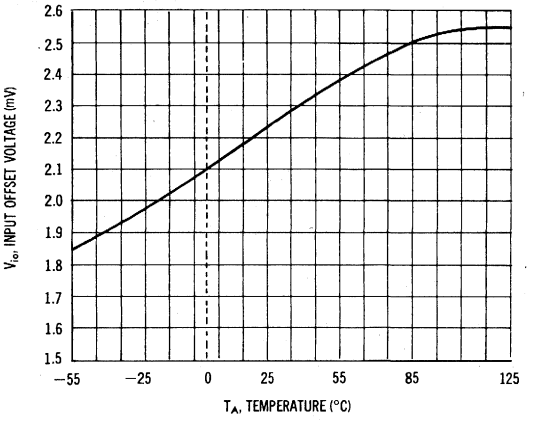


FIGURE 10 — INPUT OFFSET CURRENT

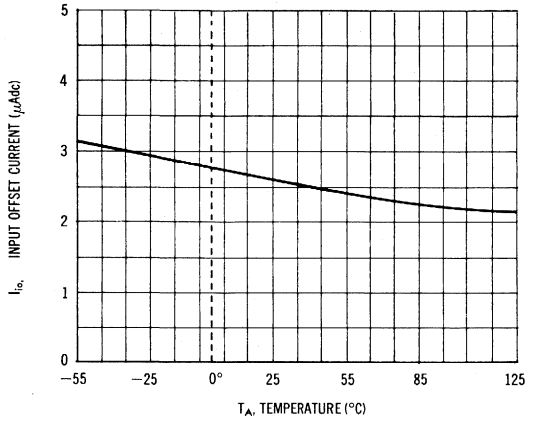


FIGURE 11 — INPUT CURRENT

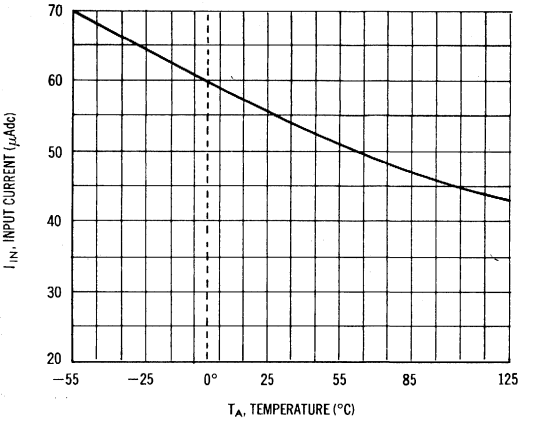


FIGURE 12 — CIRCUIT A BANDWIDTH

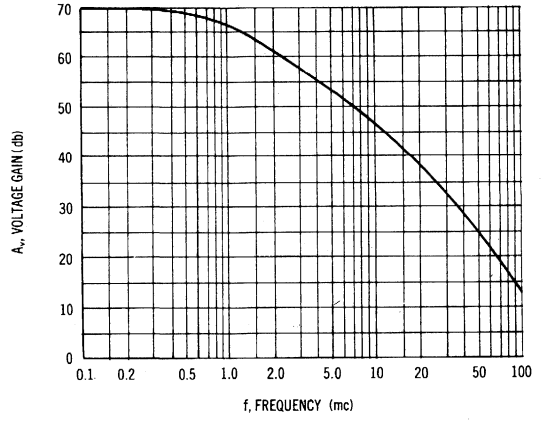
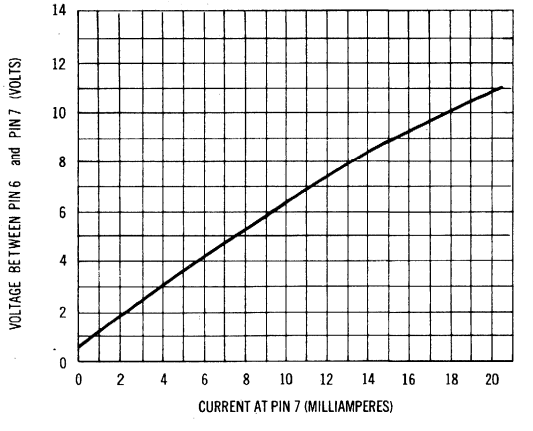


FIGURE 13 — CURRENT SOURCE BIASING



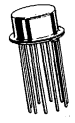
MC1525G
MC1526G

. . . designed for high gain applications. Features built-in temperature compensated current source for excellent temperature stability.

MONOLITHIC

MC1525G DIFFERENTIAL AMPLIFIER

MC1526G DARLINGTON INPUT DIFFERENTIAL AMPLIFIER



CASE 71

Lead 7 connected to case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+14	Vdc
Power Supply Voltage	V-	-14	Vdc
Differential Input Signal	V_{in}	± 5	Vdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	- 65 to +175	°C
Total Power Dissipation, (Package Limitation) Derate above T_A = 25°C	P_D	680 4. 6	mW mW/°C

CIRCUIT SCHEMATICS

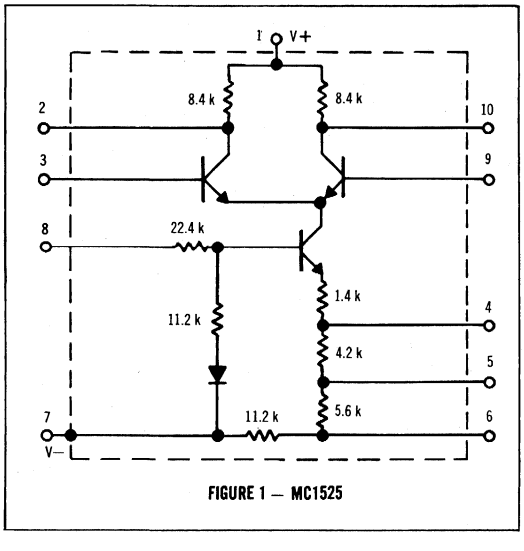


FIGURE 1 – MC1525

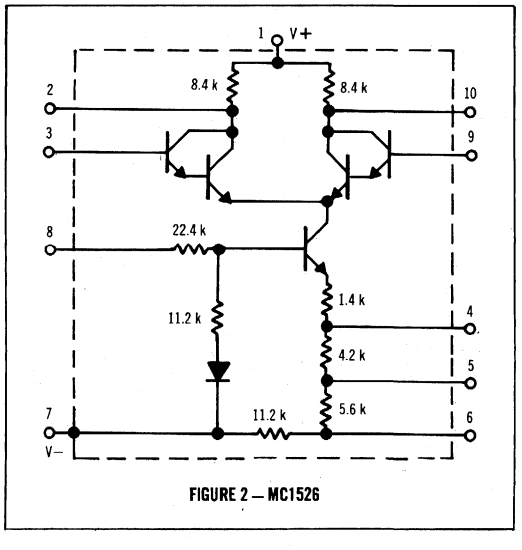


FIGURE 2 – MC1526

ELECTRICAL CHARACTERISTICS ($V+ = +12$ Vdc, $V- = -12$ Vdc, at $T_A = 25°C$ unless otherwise noted)

Characteristic	Fig No	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain MC1525 MC1526	3, 13	A_{dd}	 120 50	 140 65	 160 75	—
Single Ended Voltage Gain MC1525 MC1526	4	A_v	 — —	 75 45	 — —	—
Output Voltage, Common Mode Both Types	5, 14	$V_{o(CM)}$	 6.0	 7.0	 8.0	Vdc
Maximum Output Swing Both Types	6	V_{out}	 7.0	 —	 —	$V_{(p-p)}$
AC Unbalance Both Types	6	U	 —	 —	 300	$mV_{(p-p)}$
Input Offset Voltage MC1525 MC1526	7, 15	V_{io}	 — —	 — —	 5 7	mVdc
Input Offset Current MC1525 MC1526	8, 16	I_{io}	 — —	 — —	 4 2	μAdc
Input Current MC1525 MC1526	8, 18	I_{in}	 — —	 — —	 20 3.5	μAdc
Common Mode Rejection Both Types	9, 17	CM_{Rej}	 80	 —	 —	dB
Bandwidth MC1525 MC1526	10	BW	 1400 500	 — —	 — —	kHz
Differential Input Impedance MC1525 MC1526	11	Z_{in}	 2.0 60	 — —	 — —	kΩ
Single Ended Output Impedance Both Types	12	Z_{out}	 —	 —	 11	kΩ

DC Common Mode Input Voltage Set at: $V_{CM(min)}$ = 5.5 Vdc for MC1526G, $V_{CM(min)}$ = 6.2 Vdc for MC1525G

FIGURE 3 — DIFFERENTIAL VOLTAGE GAIN

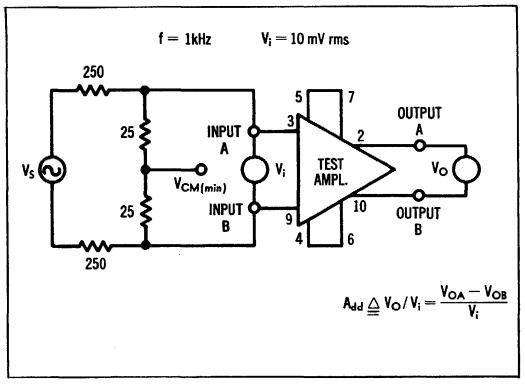


FIGURE 4 — SINGLE-ENDED VOLTAGE GAIN

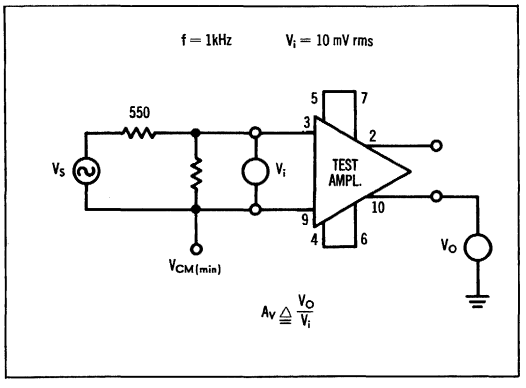


FIGURE 5 — OUTPUT VOLTAGE - COMMON MODE

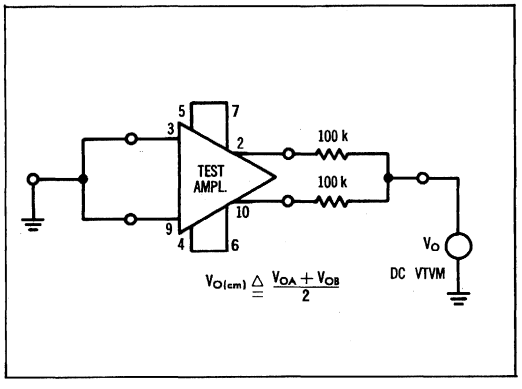


FIGURE 6 — MAXIMUM OUTPUT SWING

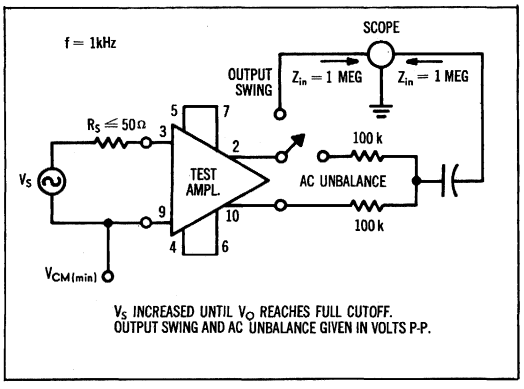


FIGURE 7 — INPUT OFFSET VOLTAGE

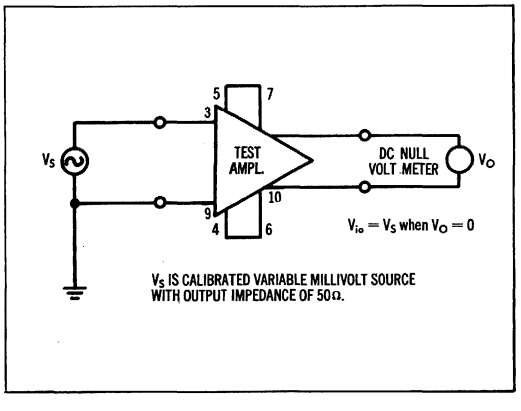
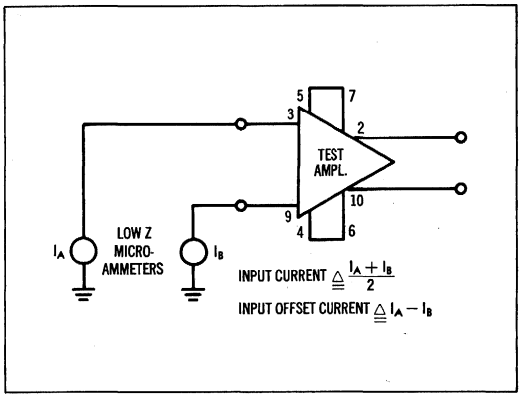
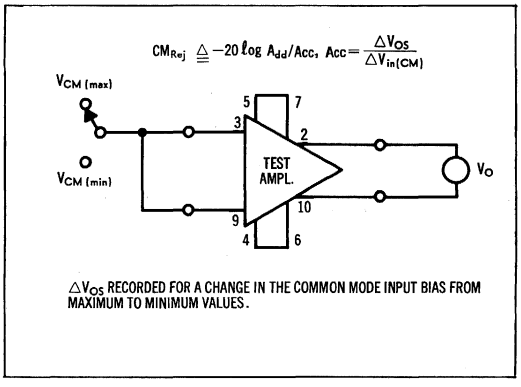


FIGURE 8 — INPUT OFFSET CURRENT and INPUT CURRENT



DC Common Mode Input Voltage Set at: $V_{CM(min)}$ = 5.5 Vdc for MC1526G, $V_{CM(min)}$ = 6.2 Vdc for MC1525G

FIGURE 9 — COMMON MODE REJECTION



ΔV_{OS} RECORDED FOR A CHANGE IN THE COMMON MODE INPUT BIAS FROM MAXIMUM TO MINIMUM VALUES.

FIGURE 10 — BANDWIDTH

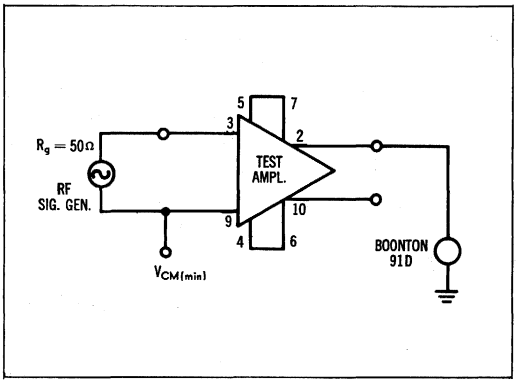
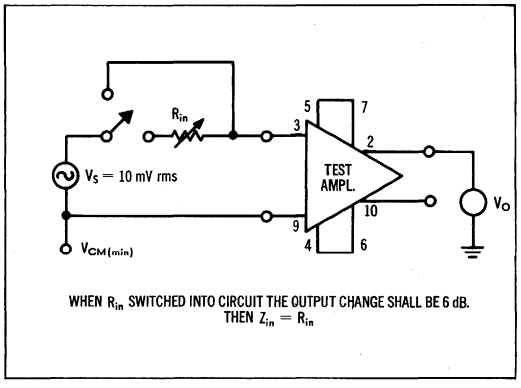
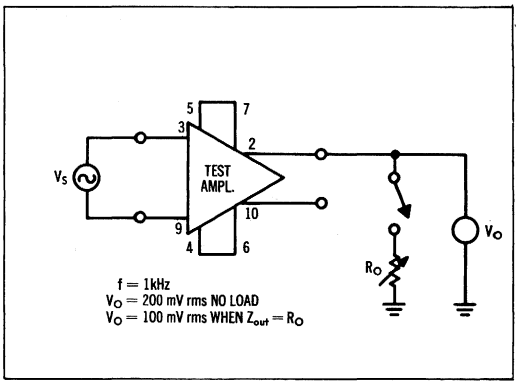


FIGURE 11 — DIFFERENTIAL INPUT IMPEDANCE



WHEN R_{in} SWITCHED INTO CIRCUIT THE OUTPUT CHANGE SHALL BE 6 dB.
THEN $Z_{in} = R_{in}$

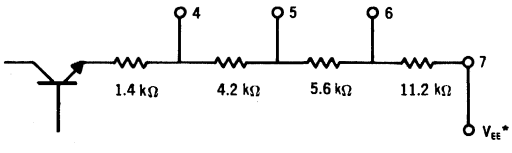
FIGURE 12 — SINGLE-ENDED OUTPUT IMPEDANCE



f = 1kHz
V_O = 200 mV rms NO LOAD
V_O = 100 mV rms WHEN $Z_{out} = R_O$

BIASING ARRANGEMENT

In the emitter of the current source transistor of each of the differential amplifiers, there are four resistors of different values which may be connected in seven ways. The resultant effective resistance in conjunction with a given V_{EE} makes provision for different current levels. For convenience, the seven methods together with their effective resistances are tabulated below.



*Pin 7 is connected to the substrate and must be connected to the V_{EE} supply for proper circuit operation.

METHOD	1	2	3	4	5	6	7
PIN CONNECTIONS	4-7	4-6, 5-7	4-5, 6-7	4-6	4-5	5-6	4,5,6 OPEN
EFFECTIVE RESISTANCE	1.4kΩ	3.37 kΩ	7.0 kΩ	12.6kΩ	18.2 kΩ	16.8kΩ	22.4 kΩ

EFFECT OF TEMPERATURE ON CHARACTERISTICS

FIGURE 13 — DIFFERENTIAL MODE GAIN

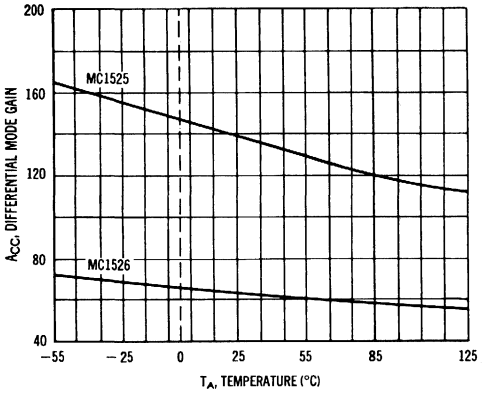


FIGURE 14 — OUTPUT VOLTAGE-COMMON MODE

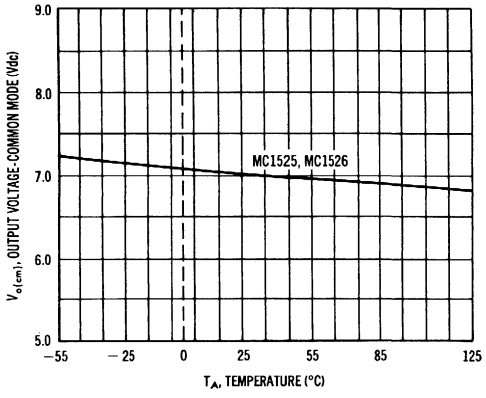


FIGURE 15 — INPUT OFFSET VOLTAGE

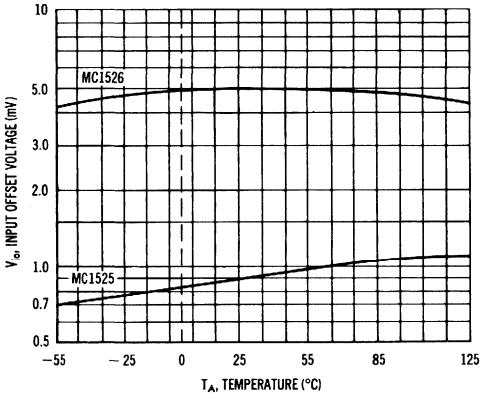


FIGURE 16 — INPUT OFFSET CURRENT

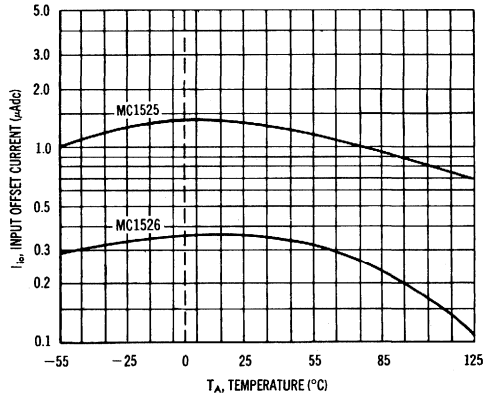


FIGURE 17 — COMMON MODE REJECTION

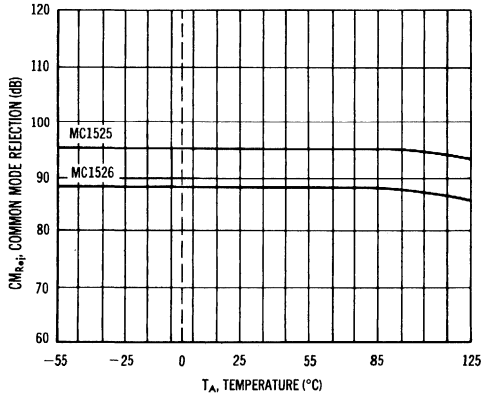
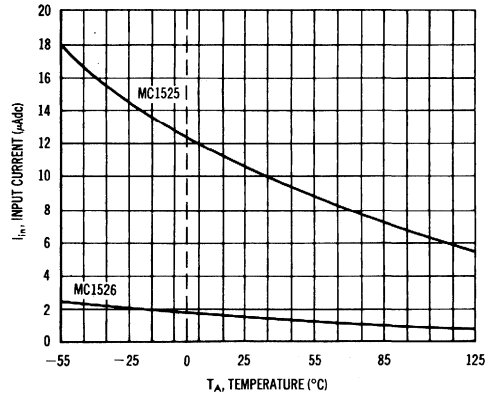


FIGURE 18 — INPUT CURRENT



DIFFERENTIAL AMPLIFIER

MC1529G
MC1429G

. . . designed for high-gain applications. Features built-in temperature compensated current source for excellent temperature stability.



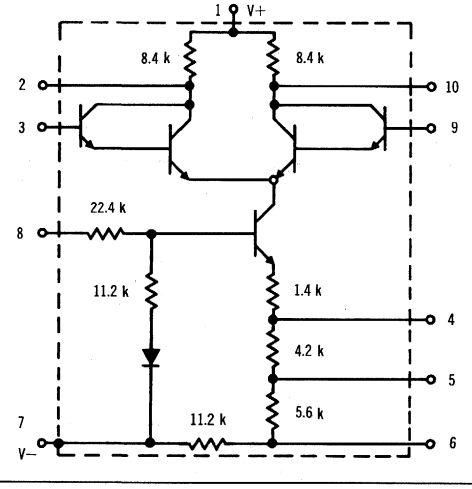
CASE 71

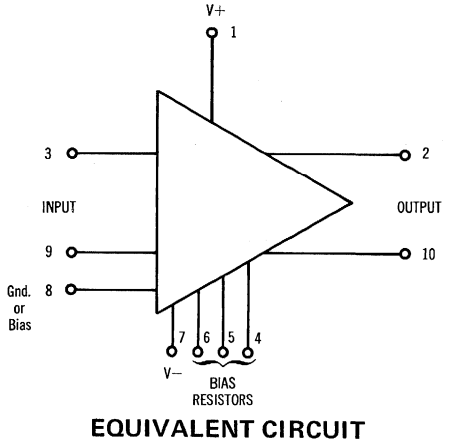
Lead 7 connected to case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V	+14	Vdc
Power Supply Voltage	V	-14	Vdc
Differential Input Signal	V_{in}	± 5	Vdc
Operating Temperature Range MC1529G MC1429G	T_A	 -55 to 125 0 to 75	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Power Dissipation (Package Limitation) Derate above T_A = 25°C)	P_D	680 4.6	mW mW/°C

CIRCUIT SCHEMATICS

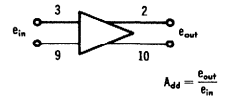
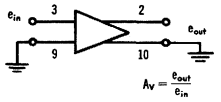
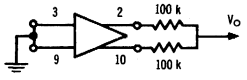
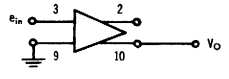
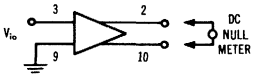
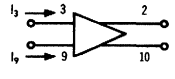
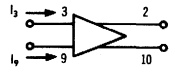
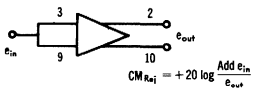
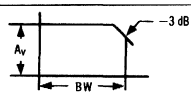
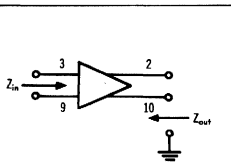




EQUIVALENT CIRCUIT

ELECTRICAL CHARACTERISTICS

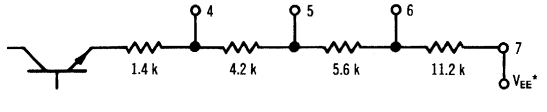
(V+ = +12 Vdc; V− = −12 Vdc; V_8 = 0 Vdc; T_A = 25°C unless otherwise noted)
Connect pin 4 to pin 6 and pin 5 to pin 7 for all tests.

Characteristic Definitions*	Characteristic	Symbol	Min	Typ	Max	Unit
 $A_{dd} = \frac{e_{out}}{e_{in}}$	Differential Voltage Gain MC1529G MC1429G	A_{dd}	50 34 45 33	75 — 75 —	110 41 — —	V/V dB V/V dB
 $A_V = \frac{e_{out}}{e_{in}}$	Single Ended Voltage Gain MC1529G MC1429G	A_V	25 28 22 27	— — — —	55 35 — —	V/V dB V/V dB
	Output Voltage, Common Mode MC1529G MC1429G	$V_{o(CM)}$	6.5 5.5	7.0 7.0	8.5 8.5	Vdc
	Maximum Output Swing Both Types	V_o	5.0	—	—	$V_{(p-p)}$
	Input Offset Voltage MC1529G MC1429G	V_{io}	— —	— —	9.0 12.0	mVdc
 $I_{io} = I_3 - I_9$	Input Offset Current MC1529G MC1429G	I_{io}	— —	— —	2.0 3.0	μAdc
 $I_b = \frac{I_3 + I_9}{2}$	Input Bias Current MC1529G MC1429G	I_{in}	— —	— —	4.0 4.0	μAdc
 $CM_{Rej} = +20 \log \frac{Add\, e_{in}}{e_{out}}$	Common Mode Rejection Both Types	CM_{Rej}	70	—	—	dB
	Bandwidth MC1529G MC1429G	BW	200 150	300 250	— —	kHz
	Differential Input Impedance MC1529G MC1429G Single Ended Output Impedance MC1529G MC1429G	Z_{in} Z_{out}	40 30 — —	— — — —	— — 12 15	kΩ kΩ

*All definitions imply linear operation.

BIASING ARRANGEMENT

In the emitter of the current source transistor of each of the differential amplifiers, there are four resistors of different values which may be connected in seven ways. The resultant effective resistance in conjunction with a given V_{EE} makes provision for different current levels. For convenience, the seven methods together with their effective resistances are tabulated below.



*Pin 7 is connected to the substrate and must be connected to the V_{EE} supply for proper circuit operation.

METHOD	1	2	3	4	5	6	7
PIN CONNECTIONS	4-7	4-6, 5-7	4-5, 6-7	4-6	4-5	5-6	4,5,6 OPEN
EFFECTIVE RESISTANCE	1.4 k	3.37 k	7.0 k	12.6 k	18.2 k	16.8 k	22.4 k

EFFECT OF TEMPERATURE ON CHARACTERISTICS

FIGURE 1 — DIFFERENTIAL MODE GAIN

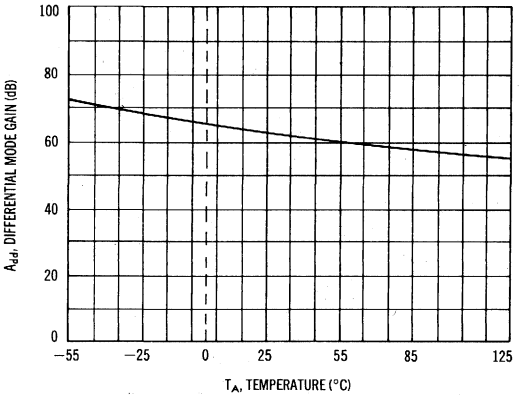


FIGURE 2 — OUTPUT VOLTAGE-COMMON MODE

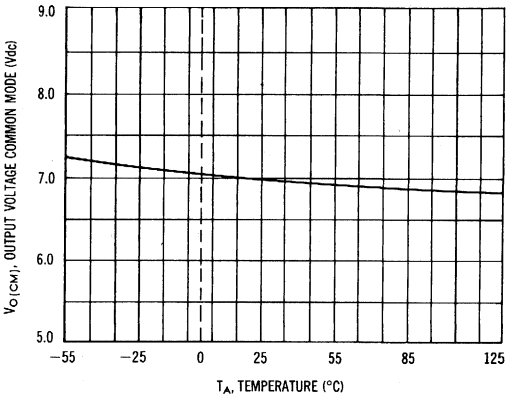


FIGURE 3 — INPUT OFFSET VOLTAGE

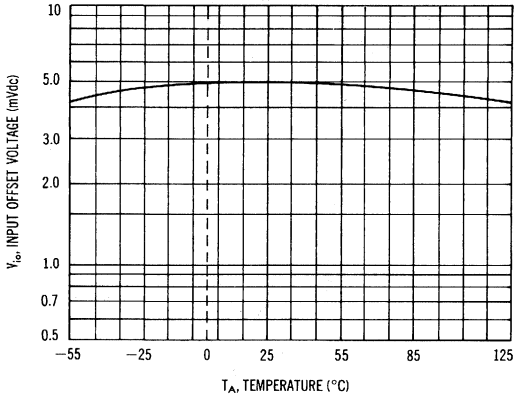


FIGURE 4 — INPUT OFFSET CURRENT

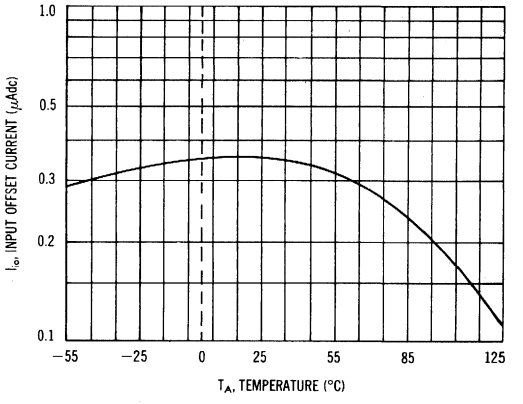


FIGURE 5 — COMMON MODE REJECTION

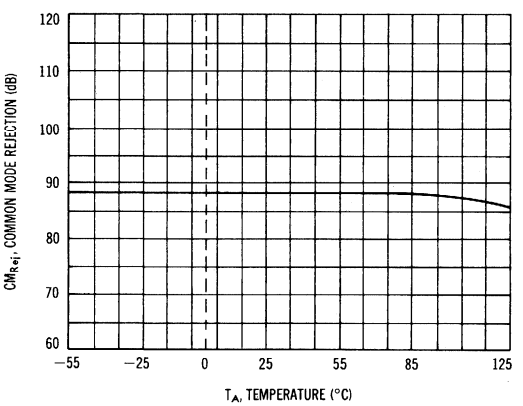
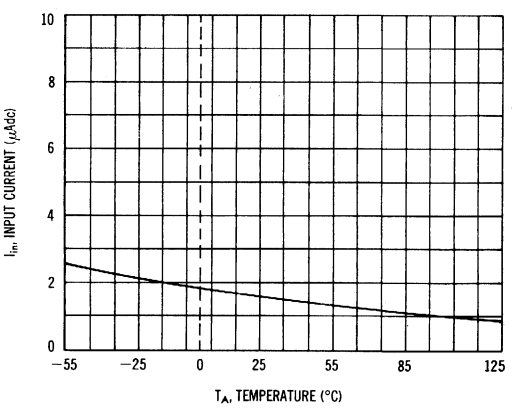


FIGURE 6 — INPUT CURRENT

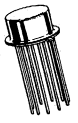


MC1440

. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.

Typical Amplifier Features:

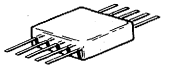
- Differential Threshold Characteristics:
  - Adjustable Threshold — 10-25 mV
  - Nominal Threshold — 17 mV @ V_6 = -6 V
  - Input Offset Voltage — 1.0 mV typical
  - Threshold Drift — -10 μV/°C typical
- Fast Response Time — 20 ns typical
- Short Recovery Time
  - 60 ns max @ e_{in} = 1.8 V Common Mode
  - 90 ns max @ e_{in} = 400 mV Differential Mode

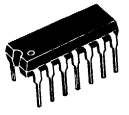


CASE 71
"G" SUFFIX

Lead 5 connected to case

CASE 72
(TO-91)
"F" SUFFIX



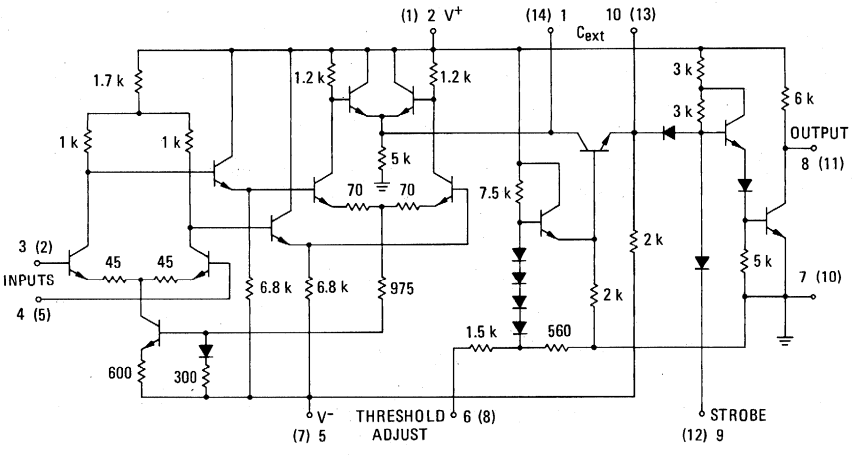


CASE 93
(TO-116)
"P" SUFFIX

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5	Vdc
Common Mode Input Voltage	CMV_{in}	±5	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25° C	P_D	 680 4.6 500 3.3 415 3.3	 mW mW/°C mW mW/°C mW mW/° C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Number at end of terminal represents pin number for devices in flat package and metal can.

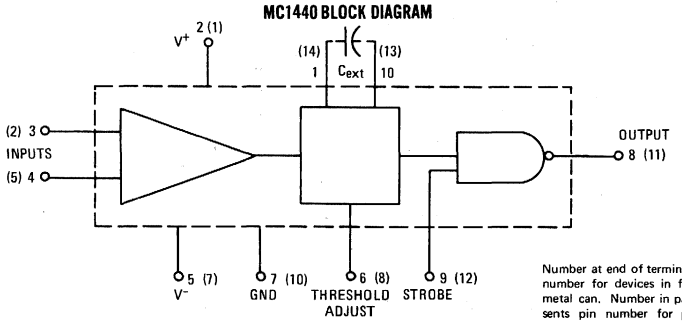
Number in parenthesis represents pin number for plastic package.

ELECTRICAL CHARACTERISTICS

(V^+ = +6 Vdc ±1%, V^- = -6 Vdc ±1%, C_{ext} = 0.01 μF, T_A = 25°C unless otherwise noted)
Pin numbers shown for devices in flat package and metal can. See block diagram for plastic pin numbers.

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage (V_6 = -6 Vdc)	1	V_{th}	12.0	17.0	22.0	mV
Input Offset Voltage	1	V_{io}	-	1.0	6.0	mV
Input Bias Current ($V_3 = V_4 = 0$)	2	I_b	-	7.5	75	μA
Input Offset Current	2	I_{io}	-	2.0	15.0	μA
Output Voltage, High ($V_3 = V_4 = 0$)	3	V_{OH}	5.8	-	-	Vdc
Output Voltage Low ($V_3 = V_4 = 0$, V_{10} = +6 Vdc, I_8 = 6 mAdc)	3	V_{OL}	-	-	400	mVdc
Amplifier Voltage Gain (V_3 = 15 mV peak)	4	A_V	-	85	-	-
Strobe Load Current (V_9 = 0)	-	I_S	-	-	1.5	mAdc
Strobe Reverse Current (V_9 = +5 Vdc)	-	I_R	-	-	5.0	μAdc
Power Dissipation	-	P_D	-	120	250	mW
Propagation Delay						ns
Input to Amplifier Output (V_3 = 25 mV pulse, V_9 = +2 Vdc)	5	t_{3+10+}	-	10	20	
Input to Gate Output (V_3 = 25 mV pulse, V_9 = +2 Vdc)	5	t_{3+8-}	-	20	50	
Strobe to Gate Output ($V_3 = V_4 = 0$, V_9 = +2 V pulse)	6	t_{9+8-}	-	10	30	
Recovery Time						ns
Differential Mode (V_3 = 300 mV pulse)	7	$t_{R(dm)}$	-	20	90	
Common Mode (V_3 = 1.5 V pulse)	7	$t_{R(cm)}$	-	20	60	
TESTS AT 0°C OR +75°C AS NOTED						
Input Threshold Voltage (V_6 = -6.0 V, T_A = 0°C)	1	V_{th}	10.0	17.0	30.0	mV
(V_6 = -6.0 V, T_A = +75°C)			10.0	17.0	30.0	
Input Bias Current ($V_3 = V_4 = 0$, T_A = 0°C)	2	I_b	-	-	100	μA
Output Voltage, Low (V_{10} = +6 Vdc, I_8 = 6 mAdc, T_A = +75°C)	3	V_{OL}	-	-	450	mVdc
Strobe Reverse Current (V_9 = +6 Vdc, T_A = +75°C)	-	I_R	-	-	30	μAdc

MC1440 BLOCK DIAGRAM



Number at end of terminal represents pin number for devices in flat package and metal can. Number in parenthesis represents pin number for plastic package.

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

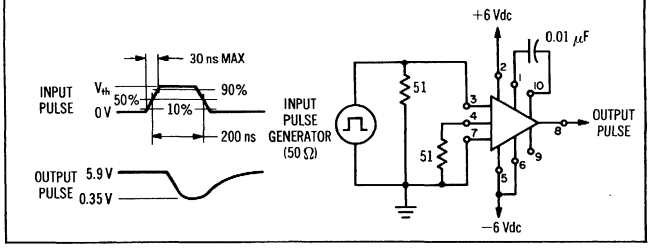


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

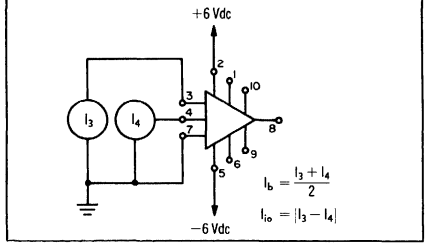


FIGURE 3 — OUTPUT VOLTAGE LEVELS

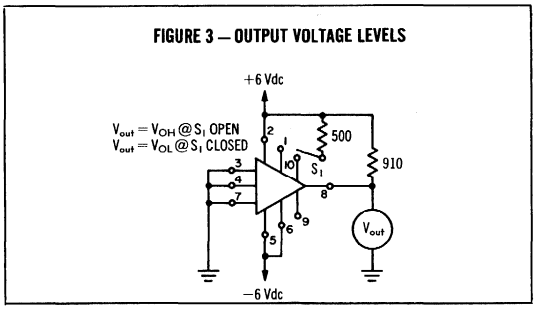


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

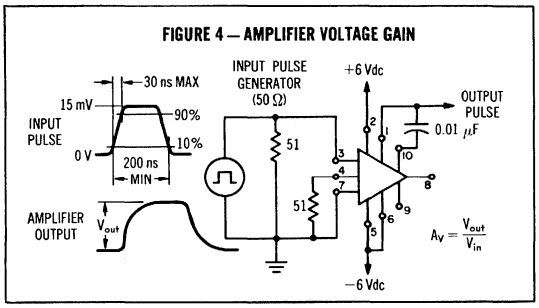


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

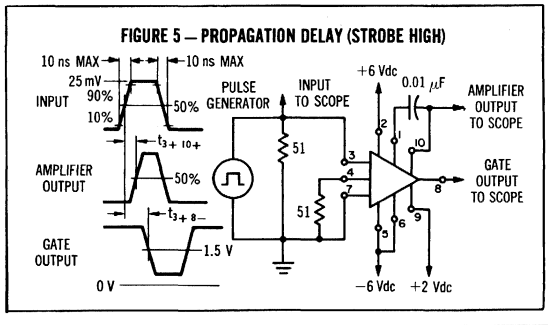


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

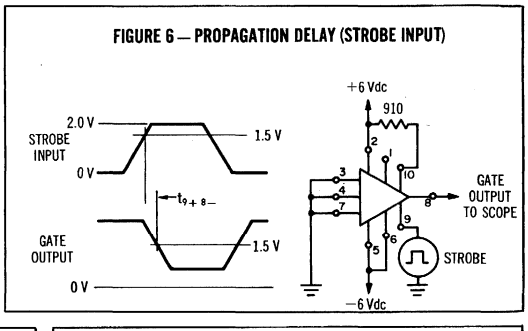


FIGURE 7 — DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

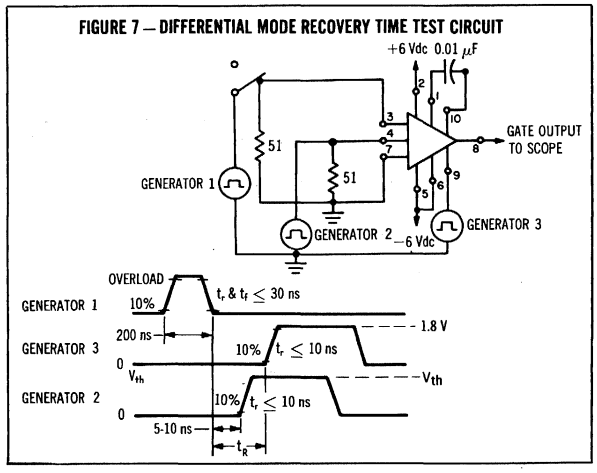
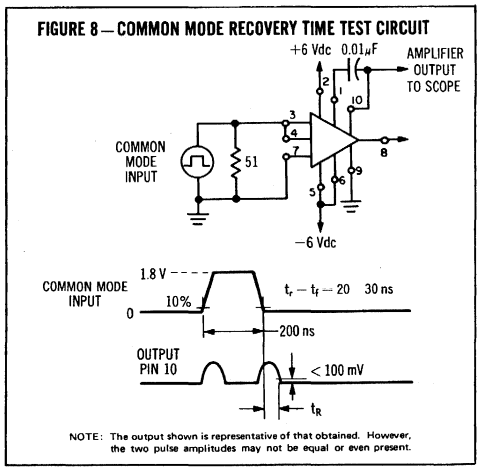


FIGURE 8 — COMMON MODE RECOVERY TIME TEST CIRCUIT



NOTE: The output shown is representative of that obtained. However, the two pulse amplitudes may not be equal or even present.

Pin numbers shown for devices in flat package and metal can. See block diagram for plastic package pin numbers.

FIGURE 9 — TYPICAL TRANSFER CHARACTERISTICS

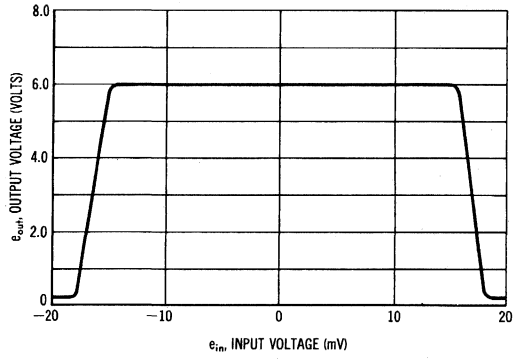


FIGURE 10 — TYPICAL THRESHOLD versus TEMPERATURE

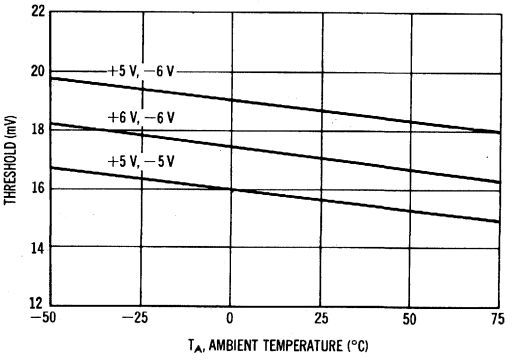


FIGURE 11 — TYPICAL THRESHOLD versus POWER SUPPLIES
$T_A = +25°C$ (Threshold Adjust Attached to V^-)

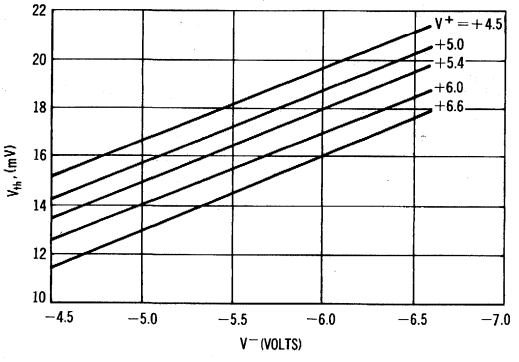
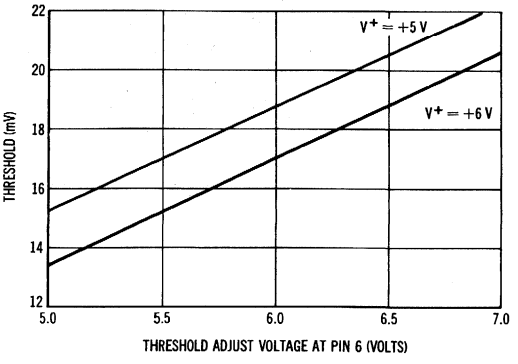


FIGURE 12 — TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR $V^- = -6.0$ V



DEFINITIONS

A_V Amplifier Voltage Gain — The ratio of output voltage at pin 1 to the input voltage at pin 3 or 4.

I_b Input Bias Current — The average input current defined as $(I_3 + I_4)/2$.

I_{io} Input Offset Current — The difference between input current values, $|I_3 - I_4|$.

I_R Strobe Reverse Current — The leakage current when the strobe input is high.

I_S Strobe Load Current — The amount of current drain from the circuit when the strobe pin is grounded.

P_D Power Dissipation — The amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$.

t_R Recovery Time — The time required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold after a differential overload disturbance is within 1.0 mV of the threshold value without the disturbance, or, for common-mode disturbance, when the level at pin 10 is within 100 mV of the quiescent value.

$t_{x\pm y\pm}$ Propagation Delay — The time required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and − denote positive and negative-going pulse transition.)

V_{OH} Output Voltage High — The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low — The low-level output voltage when the output gate is turned on.

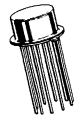
V_{th} Input Threshold — Input pulse amplitude that causes the output to begin saturation.

V_{io} Input Offset Voltage — The difference in V_{th} at each input.

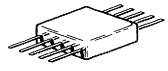
For a more detailed discussion regarding application of sense amplifiers, see Application Note AN-245A, "The MC1540 — An Integrated Core Memory Sense Amplifier."

MC1540

. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.



CASE 71
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

Lead 5 connected to case

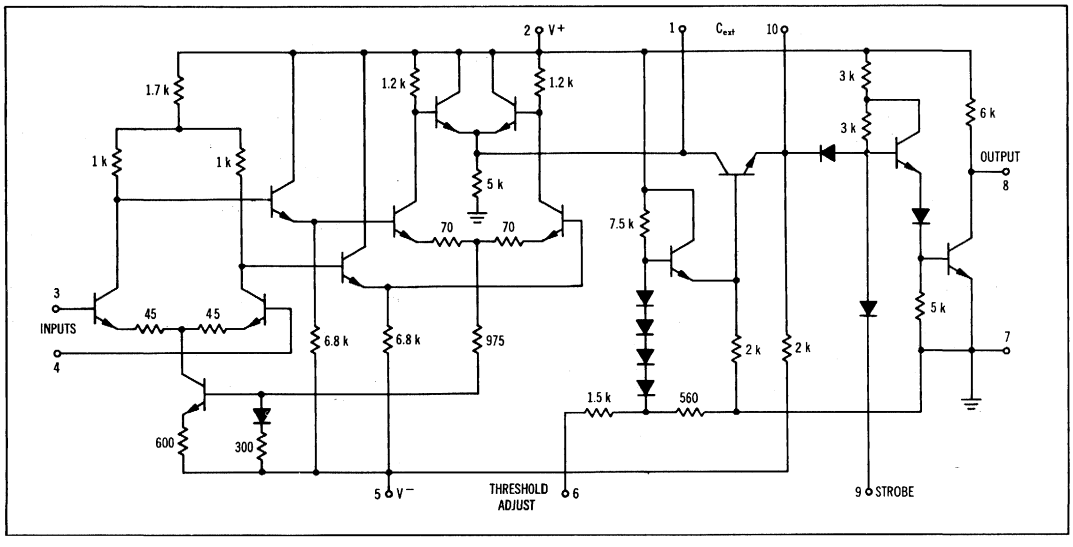
Typical Amplifier Features:

- Differential Threshold Characteristics:
  - Adjustable Threshold — 10-25 mV
  - Nominal Threshold — 17 mV @ V_6 = -6 V
  - Input Offset Voltage — 1.0 mV typical
  - Threshold Drift — -10 μV/°C
- Fast Response Time — 20 ns typical
- Short Recovery Time
  - 50 ns max @ e_{in} = 1.8 V Common Mode
  - 50 ns max @ e_{in} = 400 mV Differential Mode

MAXIMUM RATINGS (T$_A$ = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+10	Vdc
	V^-	-10	Vdc
Differential Input Signal	V_{in}	±5.0	Vdc
Common Mode Input Voltage	CMV_{in}	±5.0	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25°C		4.6	mW/°C
Flat Package		500	mW
Derate above 25°C		3.3	mW/°C
Operating Temperature Range	T_A		°C
Metal Can		-55 to +125	
Flat Package		-55 to +100	
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

($V^+ = +6$ Vdc ±1%, $V^- = -6$ Vdc ±1%, $C_{ext} = 0.01$ μF, $T_A = 25°C$ unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage ($V_6 = -6.0$ V)	1	V_{th}	14.0	17.0	20.0	mV
Input Offset Voltage	1	V_{io}	—	1.0	5.0	mV
Input Bias Current ($V_3 = V_4 = 0$)	2	I_b	—	7.5	50	μA
Input Offset Current	2	I_{io}	—	2.0	10.0	μA
Output Voltage, High ($V_3 = V_4 = 0$)	3	V_{OH}	5.9	—	—	Vdc
Output Voltage, Low ($V_3 = V_4 = 0$, $V_{10} = +6$ Vdc, $I_8 = 6$ mAdc)	3	V_{OL}	—	—	350	mVdc
Amplifier Voltage Gain ($V_3 = 15$ mV)	4	A_V	—	85	—	—
Strobe Load Current ($V_9 = 0$)	—	I_S	—	—	1.2	mAdc
Strobe Reverse Current ($V_9 = +5$ Vdc)	—	I_R	—	—	2.0	μAdc
Power Dissipation	—	P_D	—	120	180	mW
Propagation Delay						ns
Input to Amplifier Output ($V_3 = 25$ mV pulse, $V_9 = +2$ Vdc)	5	t_{3+10+}	—	10	15	
Input to Gate Output ($V_3 = 25$ mV pulse, $V_9 = +2$ Vdc)	5	t_{3+8-}	—	20	30	
Strobe to Gate Output ($V_3 = V_4 = 0$, $V_9 = +2$ V pulse)	6	t_{9+8-}	—	10	15	
Recovery Time						ns
Differential Mode ($V_3 = 400$ mV pulse)	7	$t_{R(dm)}$	—	20	50	
Common Mode ($V_3 = 1.8$ V pulse)	8	$t_{R(cm)}$	—	20	50	
TESTS AT −55°C OR +125°C AS NOTED						
Input Threshold Voltage ($V_6 = -6.0$ V, $T_A = -55°C$)	1	V_{th}	12.0	17.0	24.0	mV
($V_6 = -6.0$ V, $T_A = +125°C$)			12.0	17.0	22.0	
Input Bias Current ($V_3 = V_4 = 0$, $T_A = -55°C$)	2	I_b	—	—	100	μA
Output Voltage, Low ($V_{10} = +6$ Vdc, $I_8 = 6$ mAdc, $T_A = +125°C$)	3	V_{OL}	—	—	400	mVdc
Strobe Reverse Current ($V_9 = +6$ Vdc, $T_A = +125°C$)	—	I_R	—	—	25	μAdc

DEFINITIONS

A_V Amplifier Voltage Gain — The ratio of output voltage at pin 1 to the input voltage at pin 3 or 4.

I_b Input Bias Current — The average input current defined as $(I_3 + I_4)/2$.

I_{io} Input Offset Current — The difference between input current values, $|I_3 - I_4|$.

I_R Strobe Reverse Current — The leakage current when the strobe input is high.

I_S Strobe Load Current — The amount of current drain from the circuit when the strobe pin is grounded.

P_D Power Dissipation — The amount of power dissipated in the unit as defined by $|I_2 \times V^+| + |I_5 \times V^-|$.

t_R Recovery Time — The time required for the device to recover from the specified differential and common-mode overload inputs prior to strobe as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold after a differential overload disturbance is within 1.0 mV of the threshold value without the disturbance, or, for common-mode disturbance, when the level at pin 10 is within 100 mV of the quiescent value.

$t_{x\pm y\pm}$ Propagation Delay — The time required for the output pulse at pin y to achieve 50% of its final value or the 1.5 V level referenced to 50% of the input pulse at pin x. (The + and − denote positive and negative-going pulse transition.)

V_{OH} Output Voltage High — The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low — The low-level output voltage when the output gate is turned on.

V_{th} Input Threshold — Input pulse amplitude that causes the output to begin saturation.

V_{io} Input Offset Voltage — The difference in V_{th} at each input.

FIGURE 1 — INPUT THRESHOLD AT OUTPUT VOLTAGE SWING FROM V_{OL} TO V_{OH}

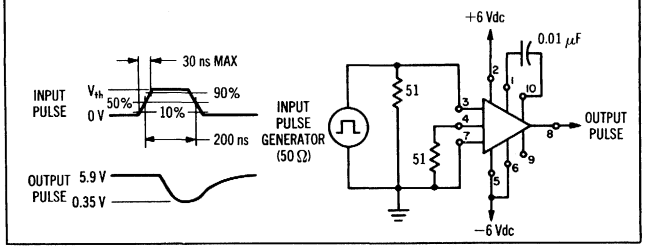


FIGURE 2 — INPUT BIAS CURRENT TEST CIRCUIT

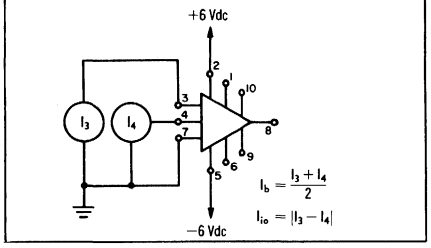


FIGURE 3 — OUTPUT VOLTAGE LEVELS

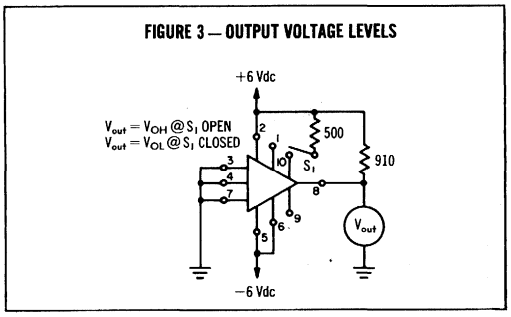


FIGURE 4 — AMPLIFIER VOLTAGE GAIN

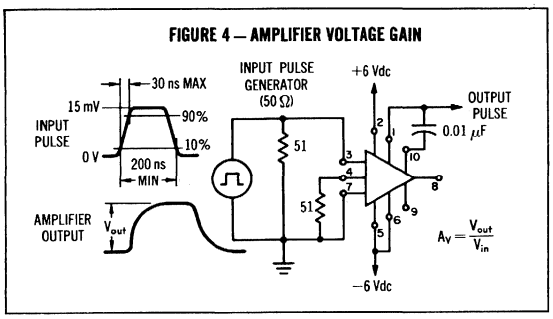


FIGURE 5 — PROPAGATION DELAY (STROBE HIGH)

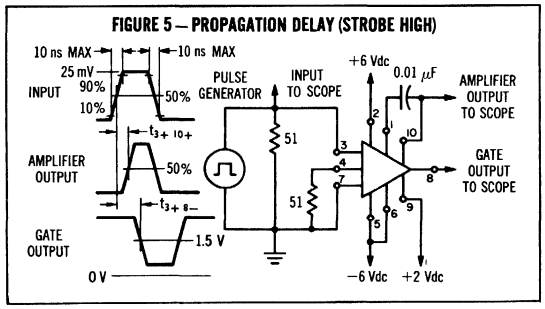


FIGURE 6 — PROPAGATION DELAY (STROBE INPUT)

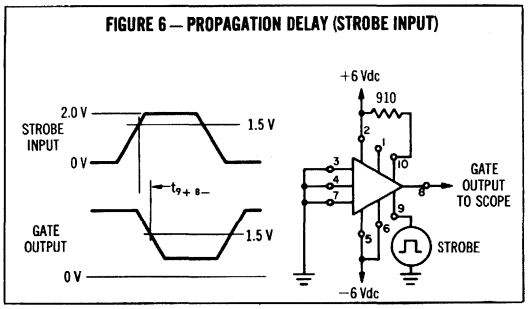


FIGURE 7 — DIFFERENTIAL MODE RECOVERY TIME TEST CIRCUIT

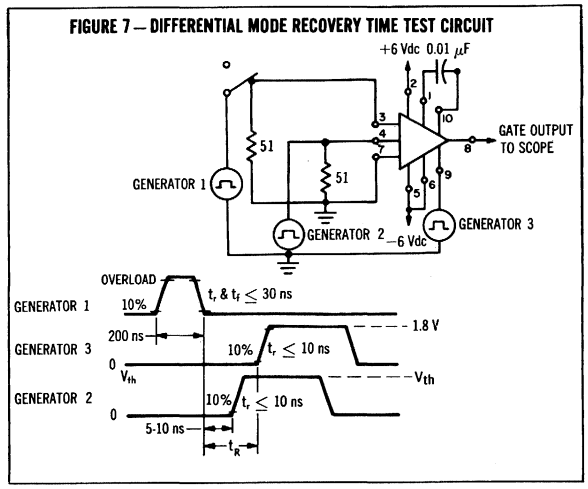
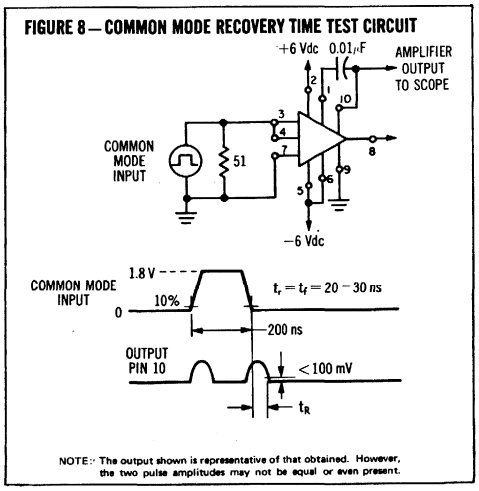


FIGURE 8 — COMMON MODE RECOVERY TIME TEST CIRCUIT



NOTE: The output shown is representative of that obtained. However, the two pulse amplitudes may not be equal or even present.

FIGURE 9 — TYPICAL TRANSFER CHARACTERISTICS

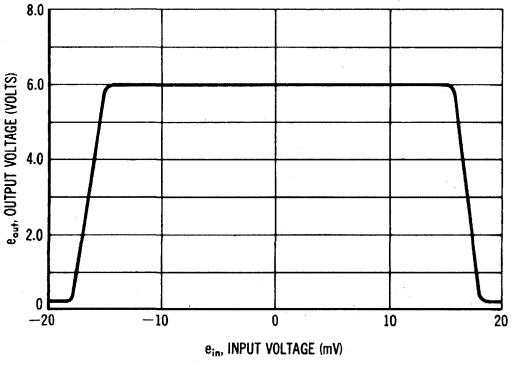


FIGURE 10 — TYPICAL THRESHOLD versus TEMPERATURE

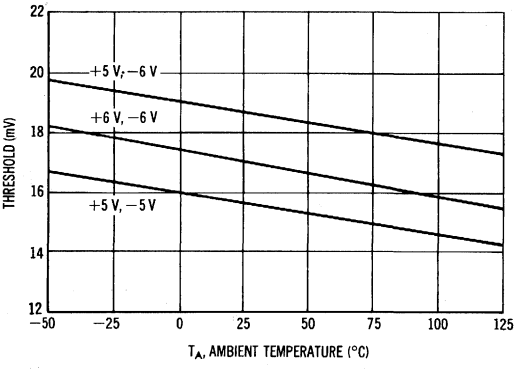


FIGURE 11 — TYPICAL THRESHOLD versus POWER SUPPLIES
T_A = +25°C (Threshold Adjust Attached to V^-)

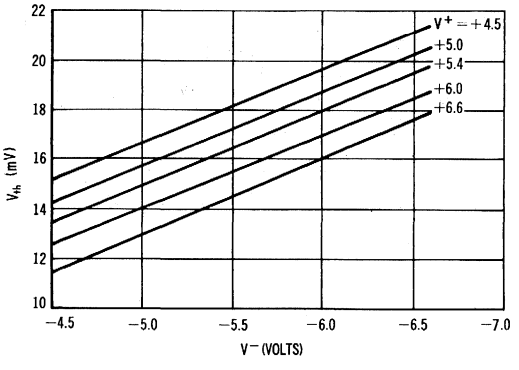


FIGURE 12 — TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST FOR V^- = −6.0 V

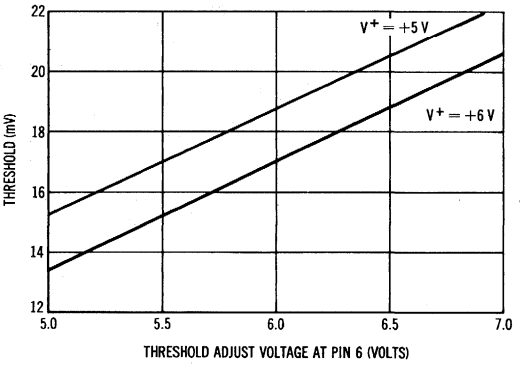
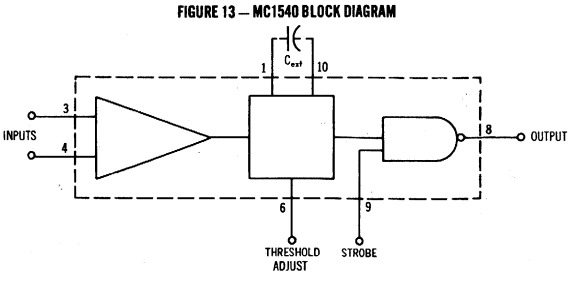


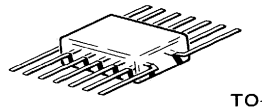
FIGURE 13 — MC1540 BLOCK DIAGRAM



For a more detailed discussion regarding application of sense amplifiers, see Application Note AN-245A, "The MC1540 — An Integrated Core Memory Sense Amplifier."

MC1541F

Dual-channel gated sense amplifier with separate wideband differential input amplifiers. Either input can be gated on from saturated logic levels. The sense amplifier features adjustable threshold, saturated logic output levels, and a strobe input that accommodates saturated logic levels. Designed to detect bipolar signals from either of two sense lines. Operates with core memory cycle times less than 0.5 μs.



TO-86
CASE 83

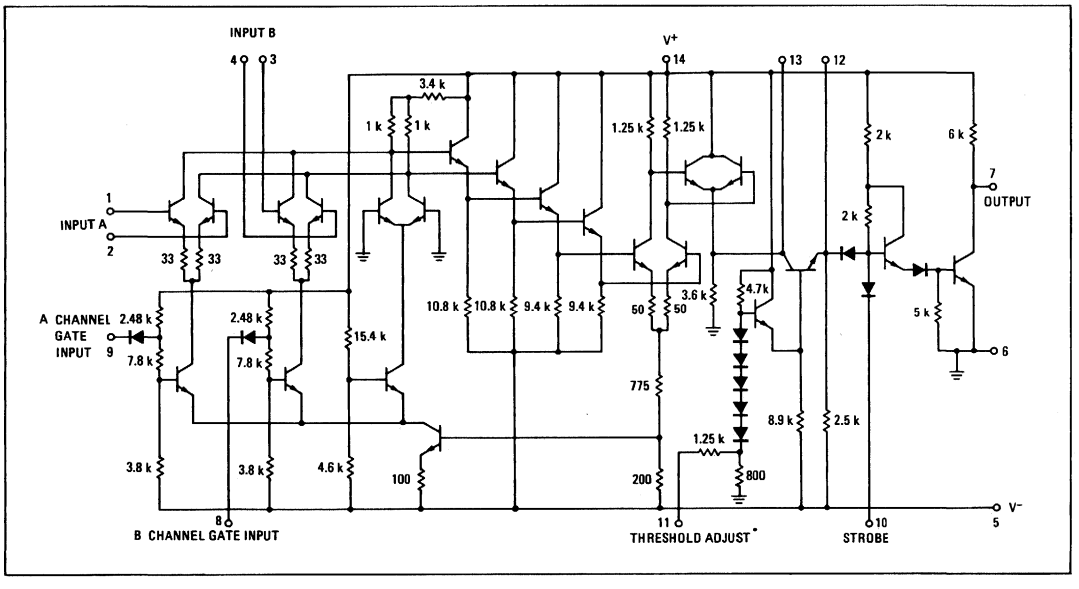
Typical Amplifier Features:

- Nominal Threshold – 17 mV
- Input Offset Voltage – 1.0 mV typical
- Propagation Delay
  - Input to Gate-Output – 20 ns
  - Input to Amplifier-Output – 10 ns
  - Gate Response Time – 15 ns
  - Strobe Response Time – 15 ns
- Common Mode Input Range – 1.5 Volts
- Differential Mode Input Range
  - With Gate On – 600 mV
  - With Gate Off – 1.5 Volts
- Power Dissipation – 140 mW typical

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+ V-	+10 -10	Vdc Vdc
Differential Input Signal	V_{in}	±5	Vdc
Common Mode Input Voltage	CMV_{in}	±5	Vdc
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	500 3.3	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

(V^+ = +5.0 Vdc ± 1%, V^- = -5.0 Vdc ± 1%, $V_{th(pin\ 11)}$ = -5.0 Vdc ± 1%, C_{ext} = 0.01 μF, T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Input Threshold Voltage (T_A = +25°C) (-55°C ≤ T_A ≤ +125°C)	8	V_{th}	 14 12	 17 17	 20 22	mV
Input Offset Voltage	8	V_{io}	-	1.0	6.0	mV
Input Bias Current ($V_1 = V_2 = V_3 = V_4 = 0$) ($V_1 = V_2 = V_3 = V_4 = 0$, T_A = -55°C)	9	I_b	 - -	 5.0 -	 25 50	μA
Input Offset Current	9	I_{io}	-	1.0	2.0	μA
Output Voltage High ($V_1 = V_2 = V_3 = V_4 = 0$)	10	V_{OH}	4.9	-	-	Vdc
Output Voltage Low ($V_1 = V_2 = V_3 = V_4 = 0$, V_{12} = +5.0 Vdc, I_7 = 10 mAdc) (V_{12} = +5.0 Vdc, I_7 = 10 mAdc, T_A = +125°C)	10	V_{OL}	 - -	 - -	 350 400	mVdc
Strobe Load Current (V_{10} = 0)		I_S	-	-	1.2	mAdc
Strobe Reverse Current (V_{10} = +5.0 Vdc) (V_{10} = +5.0 Vdc, T_A = +125°C)		I_{SR}	 - -	 - -	 2.0 25	μAdc
Input Gate Voltage Low ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4$ = 0)	11	V_{GL}	-	0.7	-	Vdc
Input Gate Voltage High ($V_1 = V_3$ = 25 mVdc, $V_2 = V_4$ = 0)	11	V_{GH}	-	1.6	-	Vdc
Input Gate Load Current (V_8 or V_9 = 0)		I_G	-	-	2.5	mAdc
Input Gate Reverse Current (V_8 or V_9 = 5.0 Vdc) (T_A = 25°C) (T_A = +125°C)		I_{GR}	 - -	 - -	 2.0 25	μAdc
Common Mode Range Input Gate High Input Gate Low	13	V_{CM}	 - -	 ±1.5 ±1.5	 - -	Vdc
Differential Mode Range Input Gate High Input Gate Low	14	 V_{DH} V_{DL}	 - -	 ±600 ±1.5	 - -	 mV Vdc
Power Dissipation		P_D	-	140	180	mW

SWITCHING CHARACTERISTICS

Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Amplifier Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IA}	-	10	15	ns
Input to Output (V_1 = 25 mV pulse, V_{10} = +2.0 Vdc)	8	t_{IO}	-	20	30	
Strobe to Output ($V_1 = V_2 = V_3 = V_4 = 0$, V_{10} = +2.0 V pulse)	12	t_{SO}	-	15	20	
Gate Input to Amplifier Input (V_1 = 25 mV pulse, V_9 = 2.0 V pulse)	11	t_{GI}	-	10	15	
Gate Input to Amplifier Output (V_1 = 25 mVdc, V_9 = 2.0 V pulse)	11	t_{GA}	-	30	35	
Recovery Time Differential Mode Input Gate High } V_1 or V_3 = 400 mV pulse Input Gate Low }	14	t_{DR}	 - -	 30 0	 50 -	ns
Common Mode Input Gate High } V_1 or V_3 = 1.5 V pulse Input Gate Low }	13	t_{CMR}	 - -	 15 15	 30 30	

EQUIVALENT CIRCUIT

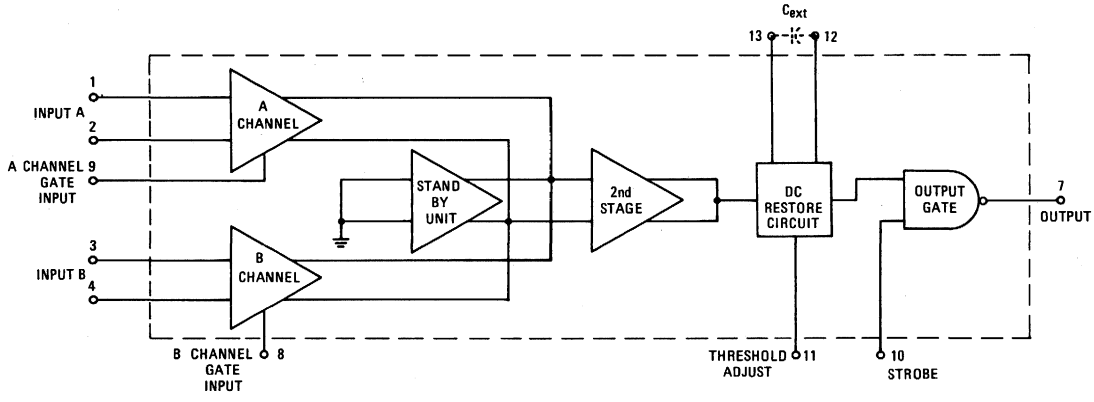


FIGURE 1 – TYPICAL OPERATION

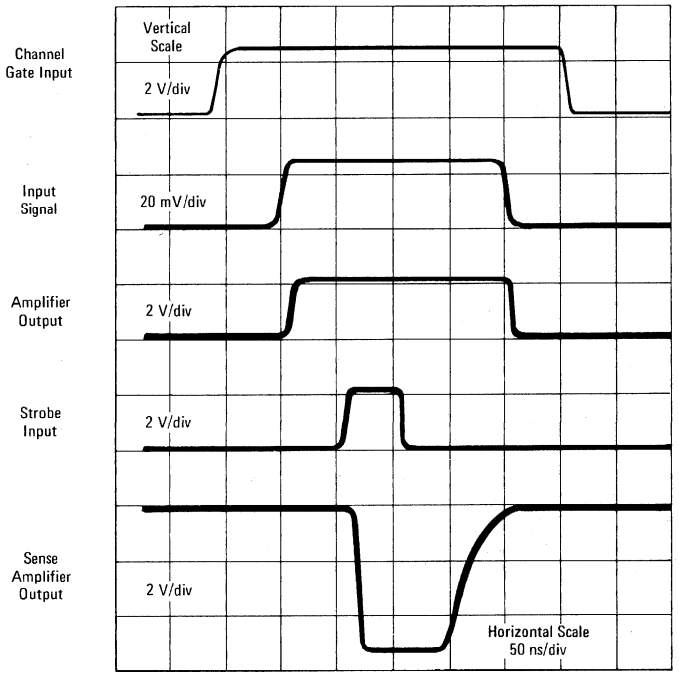


FIGURE 2 – TYPICAL INPUT THRESHOLD versus TEMPERATURE

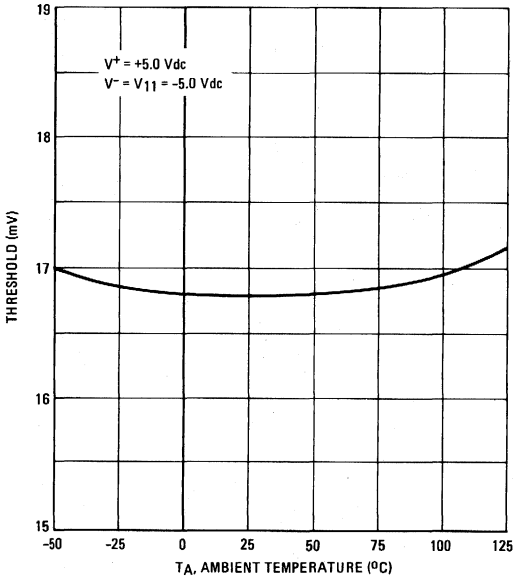


FIGURE 3 – TYPICAL THRESHOLD versus THRESHOLD VOLTAGE ADJUST

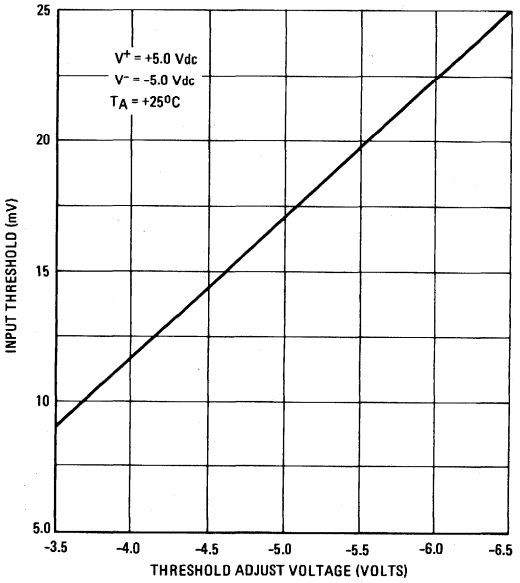


FIGURE 4 – TYPICAL INPUT THRESHOLD versus V⁻

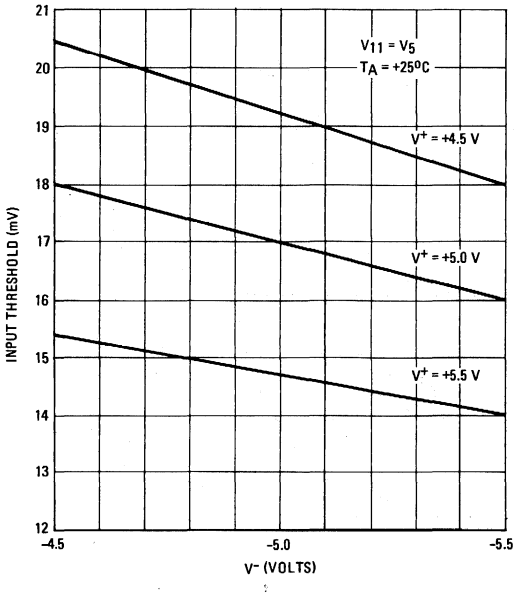


FIGURE 5 – TYPICAL INPUT THRESHOLD versus INPUT PULSE WIDTH

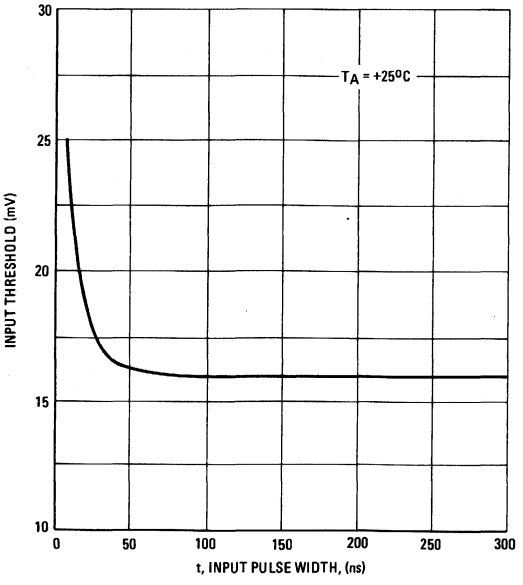


FIGURE 6 – INPUT-OUTPUT TRANSFER CHARACTERISTICS

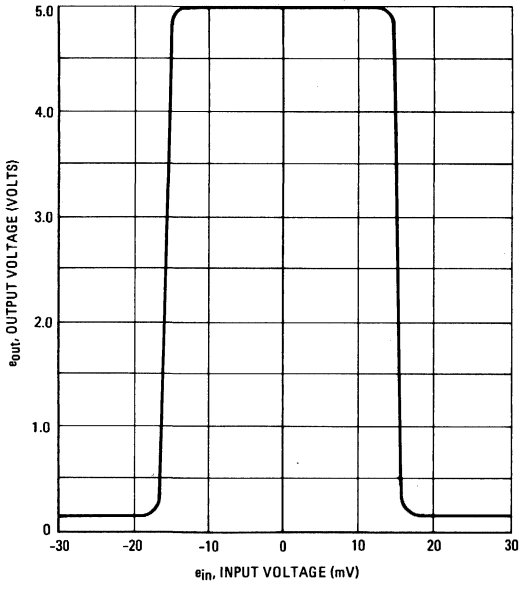


FIGURE 7 – CHANNEL GATE INPUT-AMPLIFIER OUTPUT TRANSFER CHARACTERISTICS

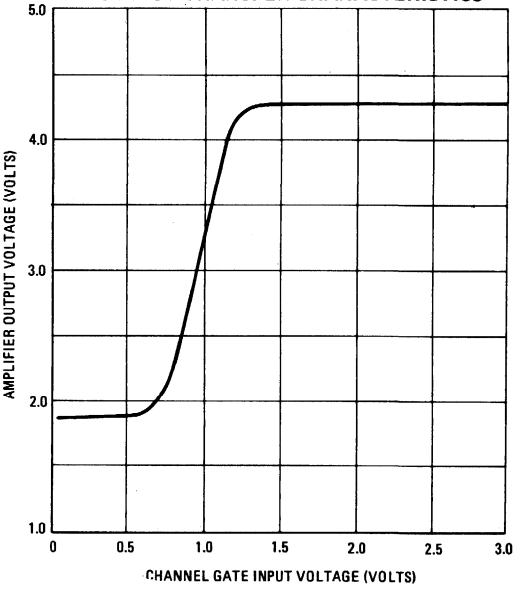


FIGURE 8 – INPUT THRESHOLD FOR OUTPUT VOLTAGE SWING FROM V_{OH} TO V_{OL} PROPAGATION DELAY FROM INPUT TO OUTPUT

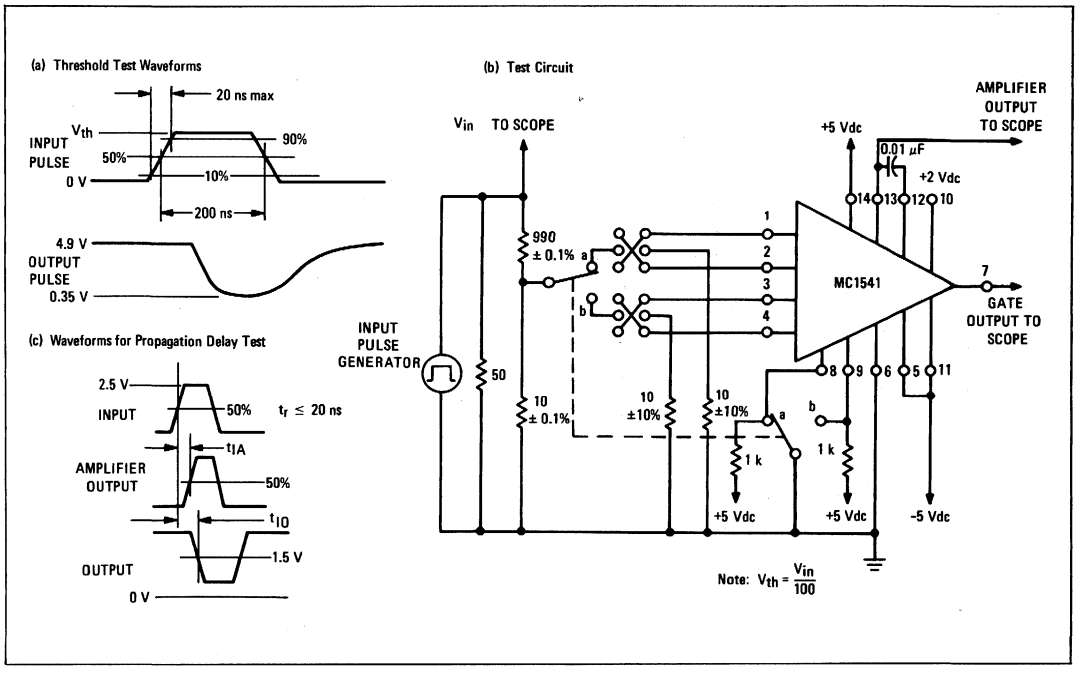
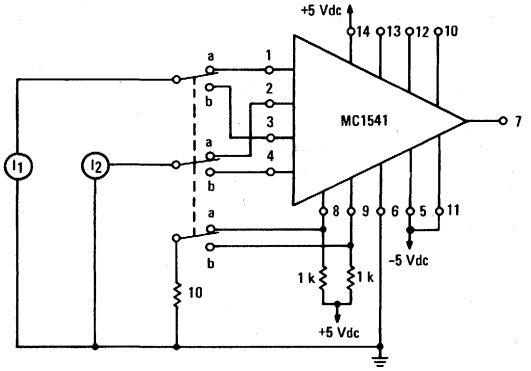


FIGURE 9 – INPUT BIAS CURRENT TEST CIRCUIT



$\frac{I_1 + I_2}{2} = I_b$ for "A" channel when switch is in "a" position

$= I_b$ for "B" channel when switch is in "b" position

$|I_1 - I_2| = I_{io}$

FIGURE 10 – OUTPUT VOLTAGE LEVELS

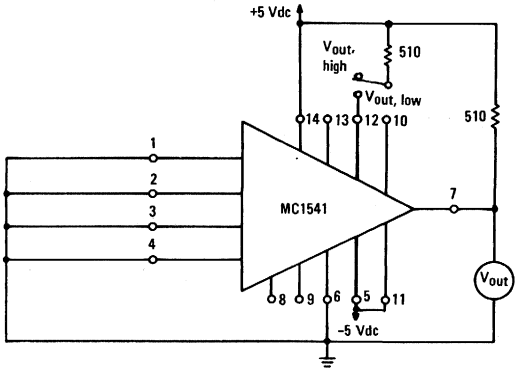


FIGURE 11 – MINIMUM TIME FROM CHANNEL GATE INPUT TO AMPLIFIER INPUT PROPAGATION DELAY FROM CHANNEL GATE INPUT TO AMPLIFIER OUTPUT

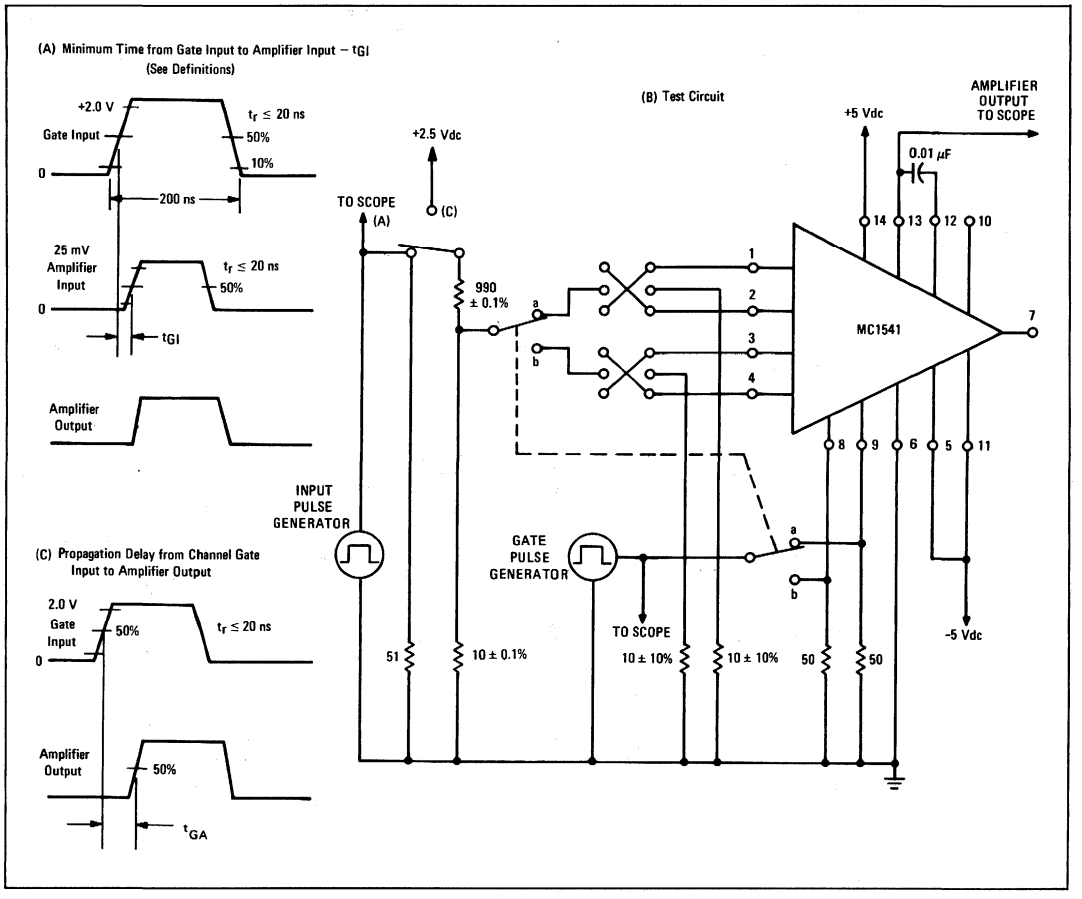


FIGURE 12 – PROPAGATION DELAY FROM STROBE INPUT TO OUTPUT

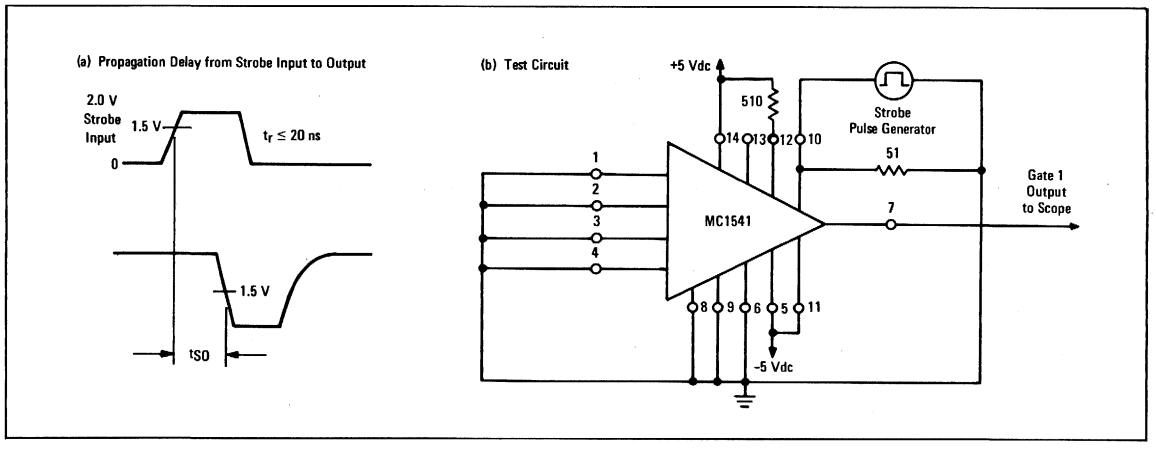


FIGURE 13 – COMMON MODE RECOVERY AND COMMON MODE RANGE

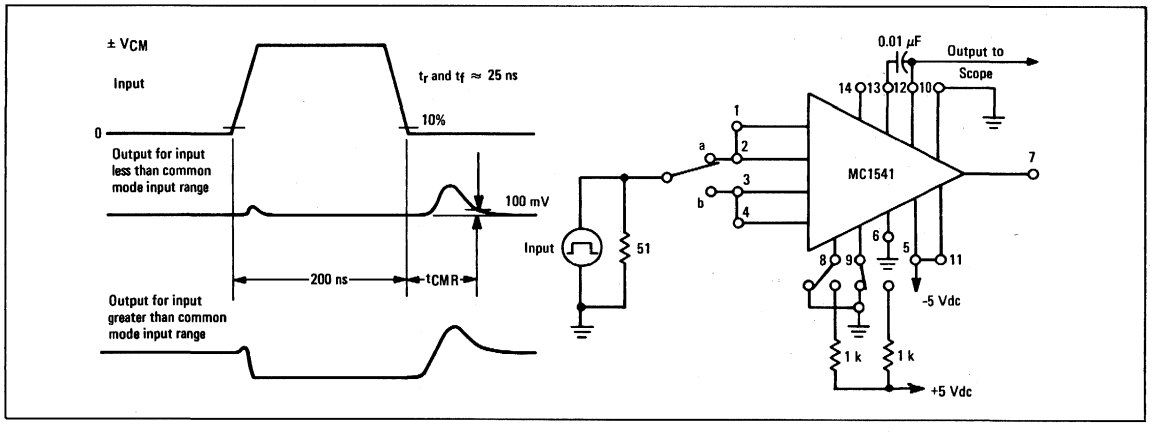
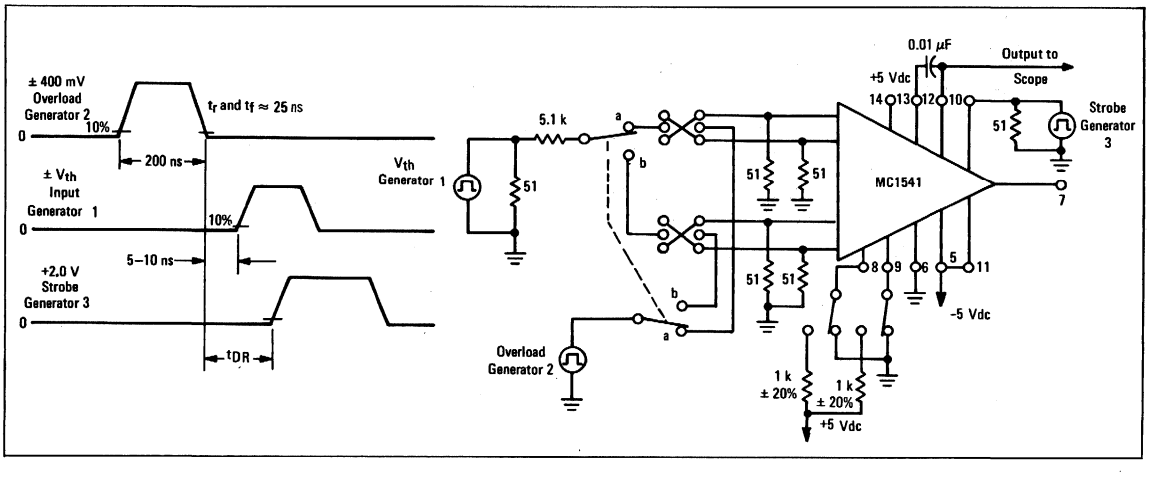


FIGURE 14 – DIFFERENTIAL RECOVERY AND DIFFERENTIAL RANGE



DEFINITIONS

I_B Input Bias Current – The average input current defined as $(I_1 + I_2 + I_3 + I_4)/4$.

I_G Channel Gate Load Current – The amount of current drain from the circuit when the channel gate input (Pin 8 or 9) is grounded.

I_{GR} Channel Gate Reverse Current – The leakage current when the channel gate input (Pin 8 or 9) is high.

I_{io} Input Offset Current – The difference between amplifier input current values $|I_1 - I_2|$ or $|I_3 - I_4|$.

I_S Strobe Load Current – The amount of current drain from the circuit when the strobe pin is grounded.

I_{SR} Strobe Reverse Current – The leakage current when the strobe input is high.

P_D Power Dissipation – The amount of power dissipated in the unit.

t_{CMR} Common Mode Recovery Time – The time required for the voltage at pin 12 to be within 100 mV of the dc value (after overshoot or ringing) as referenced to the 10% point of the trailing edge of a common mode overload signal.

t_{DR} Differential Recovery Time – The time required for the device to recover from the specified differential input prior to strobe enable as referenced to the 10% point of the trailing edge of an input pulse. The device is considered recovered when the threshold with the overload signal applied is within 1.0 mV of the threshold with no overload input.

t_{GI} Minimum Time Between Channel Gate Input and Signal Input – The minimum time between 50% point of channel gate input (Pin 8 or 9) and 50% point of signal input (Pins 1, 2, 3, or 4) that still allows a full width signal at amplifier output.

t_{GA} Propagation Delay, Channel Gate Input to Amplifier Output – The time required for the amplifier output at pin 13 to reach 50% of its final value as referenced to 50% of the input gate pulse at pin 8 or 9 (Amplifier input = 25 mVdc).

t_{IA} Propagation Delay, Input to Amplifier Output – The time required for the amplifier output pulse at pin 13 to achieve 50% of its final value referenced to 50% of the input pulse at pins 1 and 2 or 3 and 4.

t_{IO} Propagation Delay, Input to Output – The time required for the gate output pulse at pin 7 to reach the 1.5 Volt level as referenced to 50% of the input pulse at pins 1 and 2 or 3 or 4.

t_{SO} Strobe Propagation Delay to Output – The time required for the output pulse at pin 7 to reach the 1.5 Volt level as referenced to the 1.5 Volt level of the strobe input at pin 10.

V_{CM} Maximum Common Mode Input Range – The common mode input voltage which causes the output voltage level of the amplifier to decrease by 100 mV. (This is independent of the channel gate input level.)

V_{DH} Maximum Differential Input Range, Gate Input High – The differential input which causes the input stage to begin saturation.

V_{DL} Maximum Differential Input Range, Gate Input Low – The differential input signal which causes the output voltage level of the amplifier to decrease by 100 mV.

V_{GH} Channel Gate Input Voltage High – Gate pulse amplitude that allows the amplifier output pulse to just reach 100% of its final value. (Amplifier input is set at 25 mVdc).

V_{GL} Channel Gate Input Voltage Low – Gate pulse amplitude that allows the amplifier output to just reach a 100 mV level. (Amplifier input is set at 25 mVdc).

V_{io} Input Offset Voltage – The difference in V_{th} between inputs at pins 1 and 2 or 3 and 4.

V_{OH} Output Voltage High – The high-level output voltage when the output gate is turned off.

V_{OL} Output Voltage Low – The low-level output voltage when the output gate is saturated and the output sink current is 10 mA.

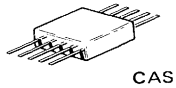
V_{th} Input Threshold – Input pulse amplitude at pins 1, 2, 3 or 4 that causes the output gate to just reach V_{OL}.

MC1710

. . . designed for use in level detection, low-level sensing, and memory applications.

Typical Amplifier Features:

- Differential Input Characteristics:
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 3.0 $\mu V/^{o}C$
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance — 200 ohms



CASE 72
(TO-91)
"F" SUFFIX



CASE 96
(TO-99)
"G" SUFFIX

Lead 4 connected to case

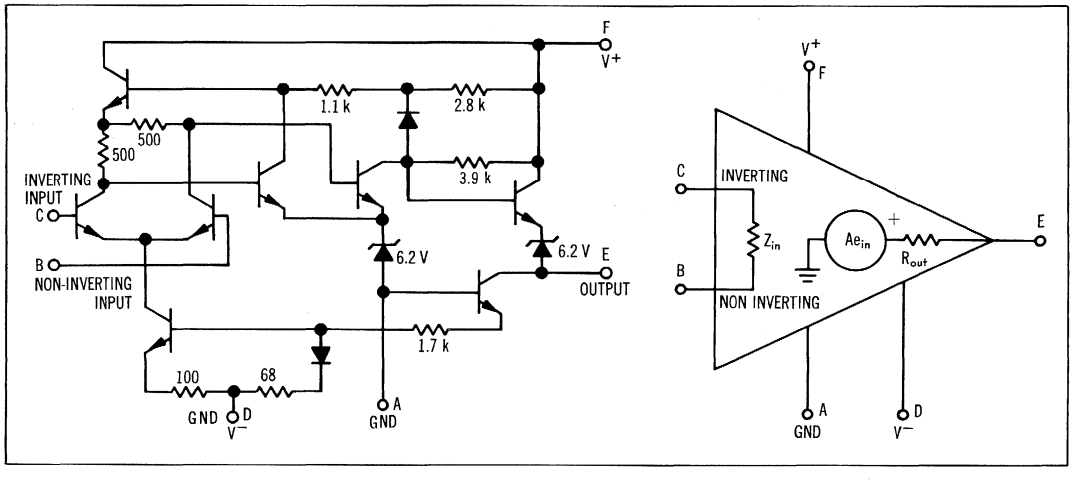
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+ 14 - 7.0	Vdc Vdc
Differential Input Signal	V_{in}	± 5.0	Volts
Common Mode Input Swing	CMV_{in}	± 7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

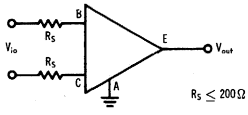
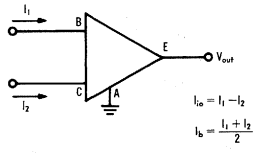
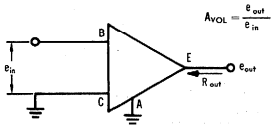
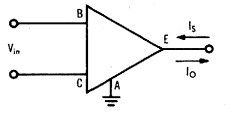
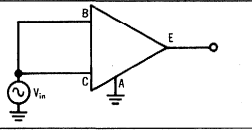
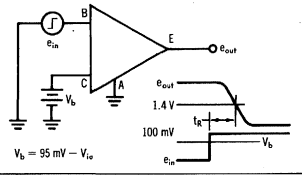
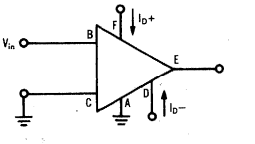
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.8 Vdc, T_A = -55°C V_{out} = 1.0 Vdc, T_A = +125°C	V_{io}	 - - -	 1.0 - -	 2.0 3.0 3.0	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	3.0	-	μV/°C
	Input Offset Current V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.8 Vdc, T_A = -55°C V_{out} = 1.0 Vdc, T_A = +125°C	I_{io}	 - - -	 1.0 - -	 3.0 7.0 3.0	μAdc
	Input Bias Current V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.8 Vdc, T_A = -55°C V_{out} = 1.0 Vdc, T_A = +125°C	I_b	 - - -	 12 - -	 20 45 20	μAdc
	Open Loop Voltage Gain T_A = 25°C T_A = -55 to +125°C	A_{VOL}	 1250 1000	 1700 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq$ 5.0 mV, $0 \leq I_o \leq$ 0.5 mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geq$ -5.0 mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geq$ -5.0 mV, $V_{out} \geq 0$, T_A = 25°C $V_{in} \geq$ -5.0 mV, $V_{out} \geq 0$, T_A = -55°C	I_s	 2.0 1.0	 2.5 2.0	 - -	mAdc
	Input Common Mode Range	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio V^- = -7.0 Vdc, $R_S \leq 200\Omega$	CM_{rej}	80	100	-	dB
	Response Time For Positive and Negative Going Input Pulse	t_R	-	40	-	ns
	Power Supply Current $V_{out} \leq$ 0 Vdc	I_D^+ I_D^-	- -	6.4 5.5	9.0 7.0	mAdc
	Power Consumption TO-99 Metal Can TO-91 Flat Package		 - -	 115 115	 150 150	mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

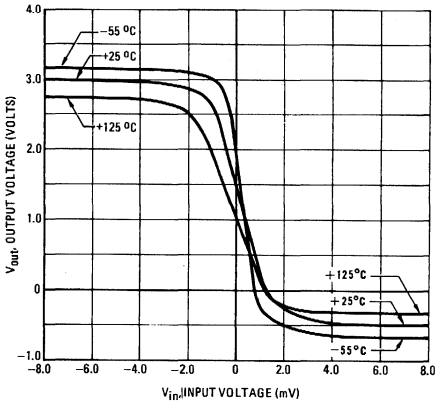


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

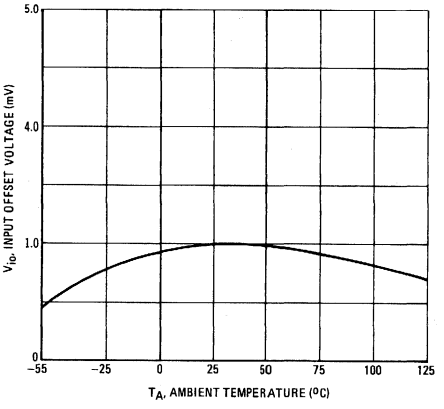


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

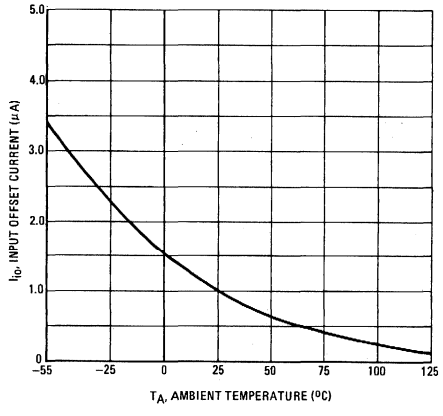


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

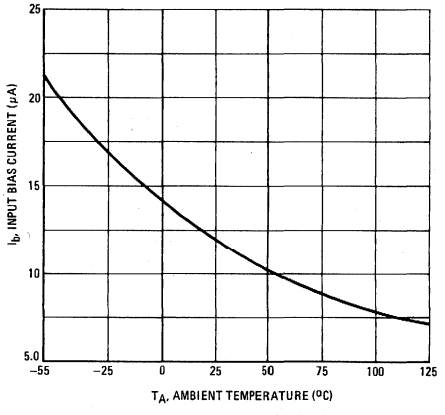


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

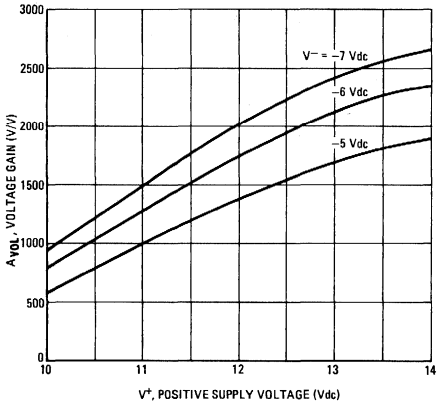


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

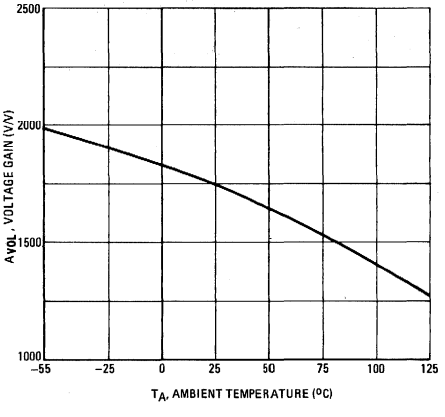


FIGURE 7 – RESPONSE TIME

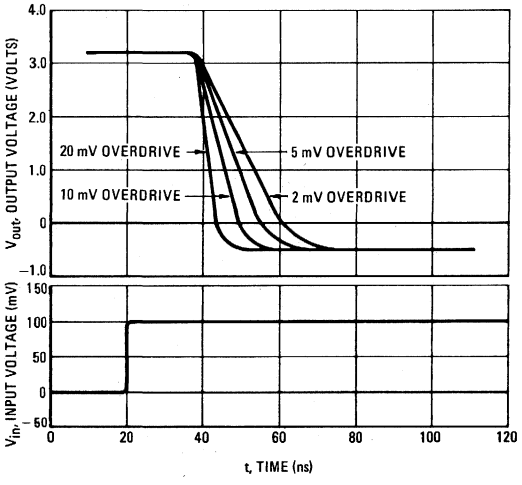


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

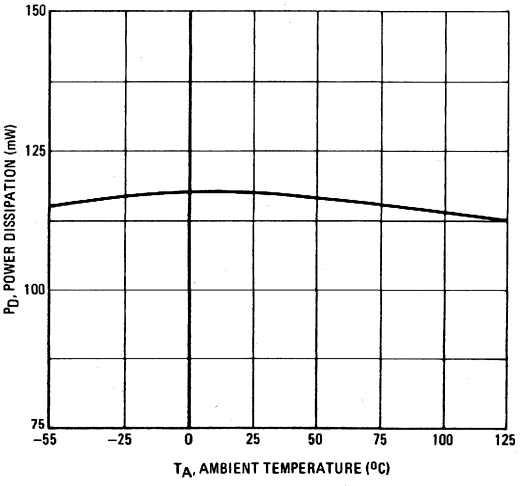


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

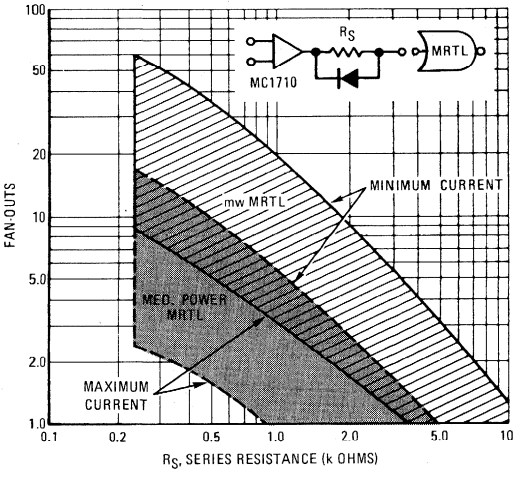
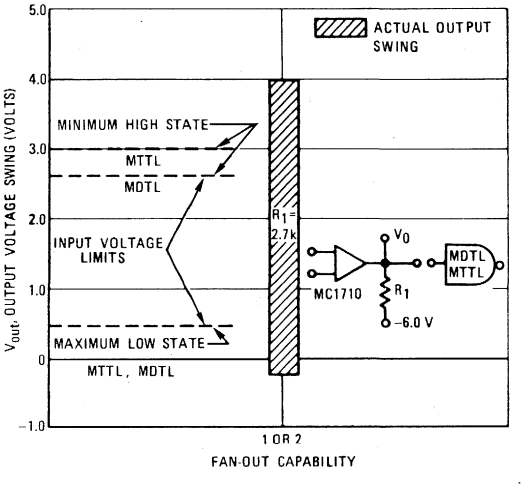


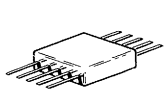
FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



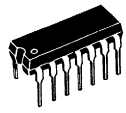
DIFFERENTIAL COMPARATOR

MC1710C

. . . designed for use in level detection, low-level sensing, and memory applications.



CASE 72
(TO-91)
"F" SUFFIX



CASE 93
(TO-116)
"P" SUFFIX

Lead 4 connected to case



CASE 96
(TO-99)
"G" SUFFIX

Typical Amplifier Features:

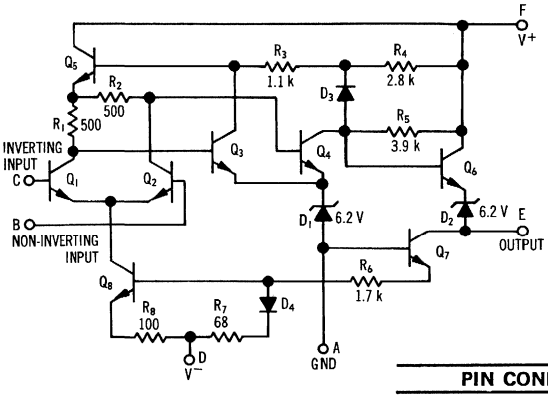
- Differential Input Characteristics:
  Input Offset Voltage = 1.5 mV
  Offset Voltage Drift = 5.0 $\mu V/^{o}C$
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +3.2 V to -0.5 V typical
- Low Output Impedance — 200 ohms

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

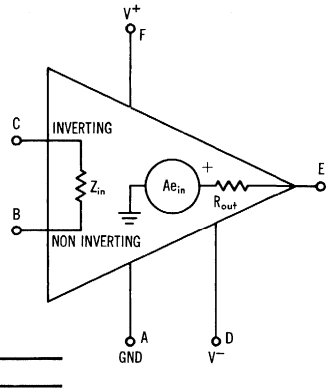
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

*For full temperature range (-55°C to + 125°C) and characteristic curves, see MC1710 data sheet.

CIRCUIT SCHEMATIC



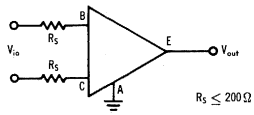
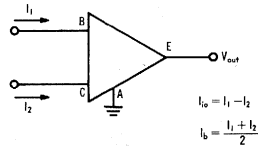
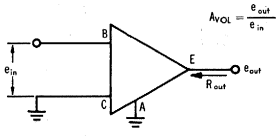
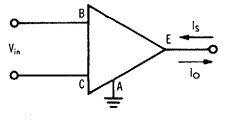
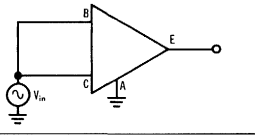
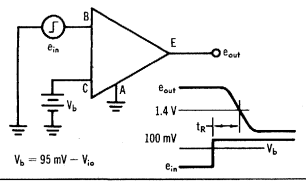
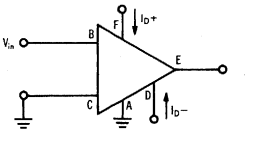
EQUIVALENT CIRCUIT



PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8
"P" Package	2	3	4	6	9	11

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.5 Vdc, T_A = 0°C V_{out} = 1.2 Vdc, T_A = +70°C	V_{io}	- - -	1.5 - -	5.0 6.5 6.5	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	μV/°C
	Input Offset Current V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.5 Vdc, T_A = 0°C V_{out} = 1.2 Vdc, T_A = +70°C	I_{io}	- - -	1.0 - -	5.0 7.5 7.5	μAdc
	Input Bias Current V_{out} = 1.4 Vdc, T_A = 25°C V_{out} = 1.5 Vdc, T_A = 0°C V_{out} = 1.2 Vdc, T_A = +70°C	I_b	- - -	15 25 -	25 40 40	μAdc
	Voltage Gain T_A = 25°C T_A = 0 to +70°C	A_{VOL}	1000 800	1500 -	- -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq$ 5.0 mV, $0 \leq I_O \leq$ 0.5 mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geq$ -5.0 mV	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geq$ -5.0 mV, $V_{out} \geq 0$ T_A = 25°C T_A = 0°C	I_s	 1.6 0.5	 2.5 -	 - -	mAdc
	Input Common Mode Range V^- = -7.0 Vdc	CMV_{in}	±5.0	-	-	Volts
	Common Mode Rejection Ratio $R_S \leq 200\,\Omega$	CM_{rej}	70	100	-	dB
	Propagation Delay Time For Positive and Negative Going Input Pulse	t_{pd}	-	40	-	ns
	Power Supply Current $V_{out} \leq$ 0 Vdc	I_{D^+} I_{D^-}	- -	6.4 5.5	9.0 7.0	mAdc
	Power Consumption		-	110	150	mW

DUAL DIFFERENTIAL COMPARATOR

MC1711

. . . designed for use in level detection, low-level sensing, and memory applications.



Lead 5 connected to case

CASE 71A
"G" SUFFIX



CASE 72
(TO-91)
"F" SUFFIX

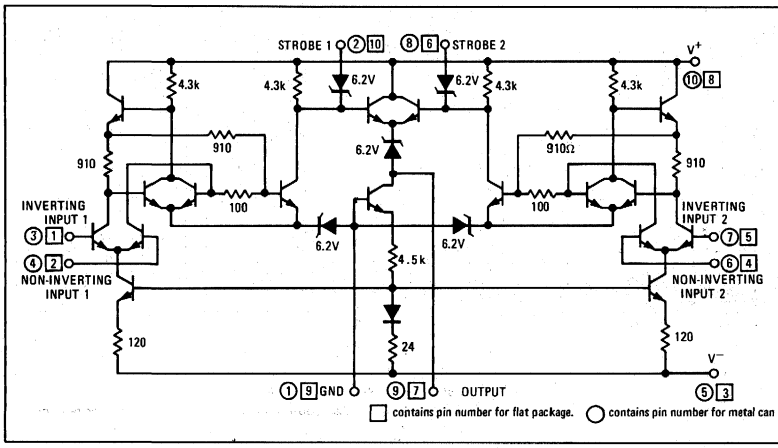
Typical Amplifier Features:

- Differential Input —
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 $\mu V/^{o}C$
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance — 200 ohms

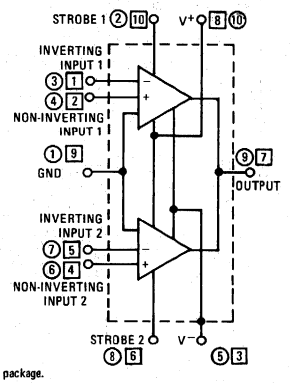
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

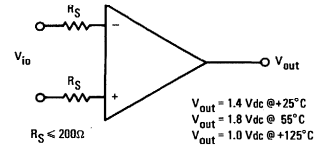
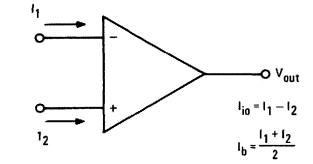
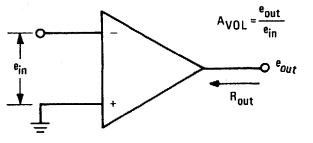
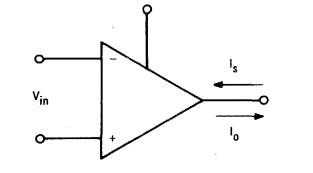
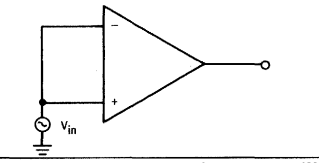
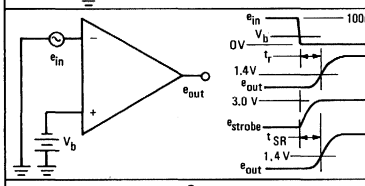
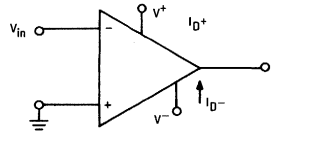
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (each comparator) $V^+ = +12$ Vdc. $V^- = -6.0$ Vdc. $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage CMV_{in} = 0 Vdc, T_A = +25°C T_A = +25°C CMV_{in} = 0 Vdc, T_A = -55 to +125°C T_A = -55 to +125°C	V_{io}	 - - - -	 1.0 1.0 - -	 3.5 5.0 4.5 6.0	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	μV/°C
	Input Offset Current V_{out} = 1.4 Vdc, T_A = +25°C V_{out} = 1.8 Vdc, T_A = -55°C V_{out} = 1.0 Vdc, T_A = +125°C	I_{io}	 - - -	 0.5 - -	 10 20 20	μAdc
	Input Bias Current V_{out} = 1.4 Vdc, T_A = +25°C V_{out} = 1.8 Vdc, T_A = -55°C V_{out} = 1.0 Vdc, T_A = +125°C	I_b	 - - -	 25 - -	 75 150 150	μAdc
	Voltage Gain T_A = +25°C T_A = -55 to +125°C	A_{VOL}	 750 500	 1500 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 10$ mVdc, $0 \leq I_o \leq 0.5$ mA	V_{OH}	2.5	3.2	5.0	Vdc
	Negative Output Voltage $V_{in} \geq -10$ mVdc	V_{OL}	-1.0	-0.5	0	Vdc
	Strobed Output Level $V_{strobe} \leq 0.3$ Vdc	$V_{OL(st)}$	-1.0	-	0	Vdc
	Output Sink Current $V_{in} \geq -10$ mV, $V_{out} \geq 0$	I_S	0.5	0.8	-	mAdc
	Strobe Current V_{strobe} = 100 mVdc	I_{st}	-	1.2	2.5	mAdc
	Input Common Mode Range V^- = -7.0 Vdc	CM_{Vin}	±5.0	-	-	Volts
	Response Time $V_b = 5.0$ mV + V_{io} Strobe Release Time	t_R t_R t_{SR}	- - -	40 40 12	- - -	ns ns ns
	Power Supply Current $V_{out} \leq 0$ Vdc Power Consumption	I_{D^+} I_{D^-} 	- - -	8.6 3.9 130	- - 200	mAdc mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

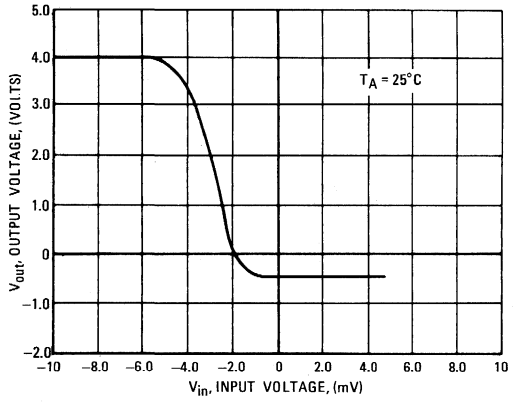


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

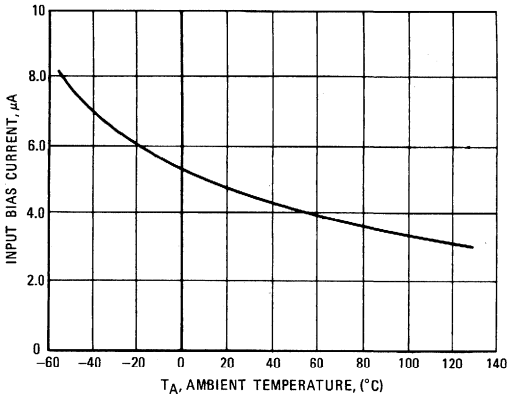


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

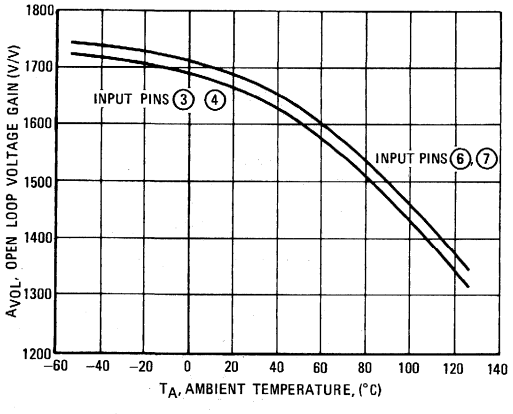


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

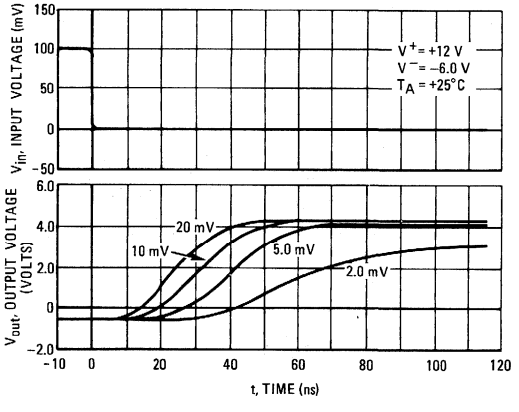


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

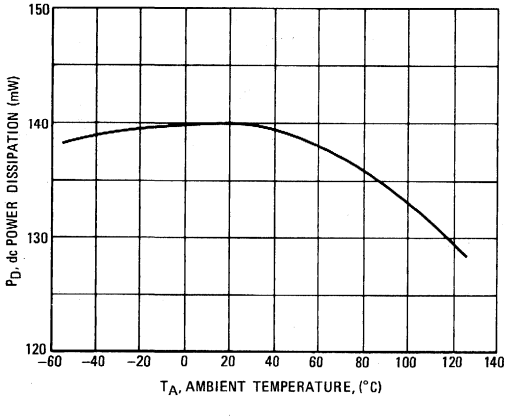


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

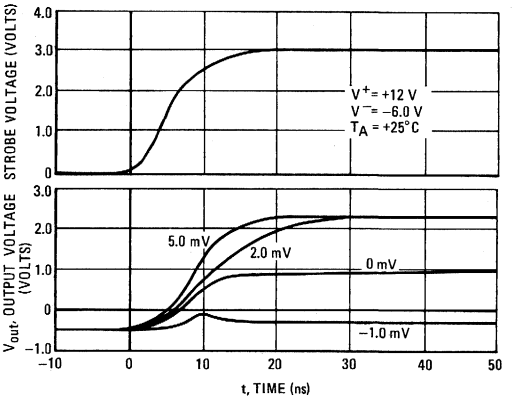


FIGURE 7 – COMMON MODE PULSE RESPONSE

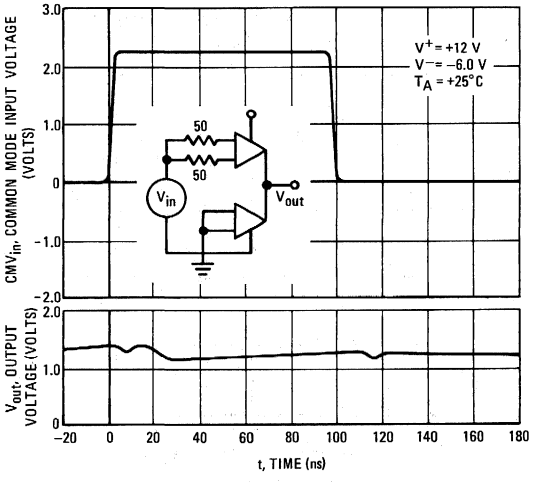


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

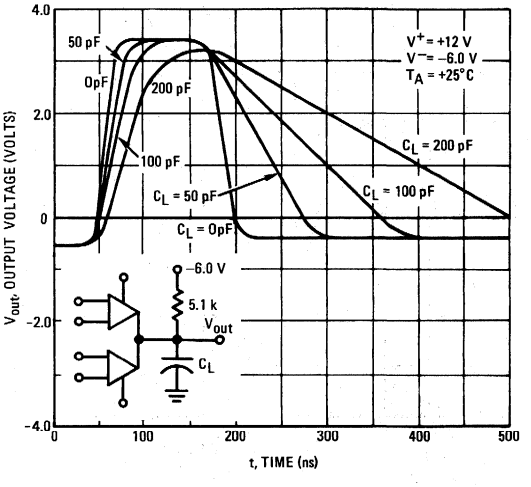


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

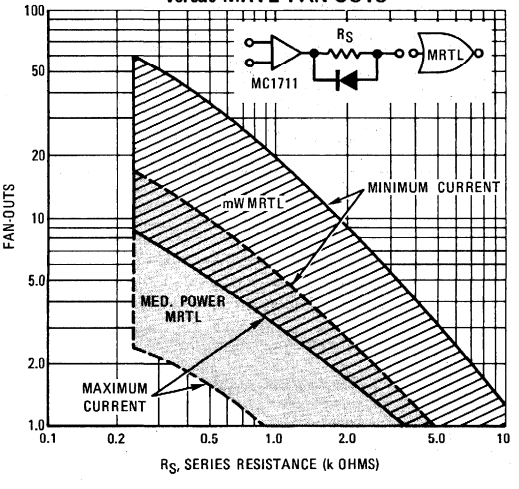
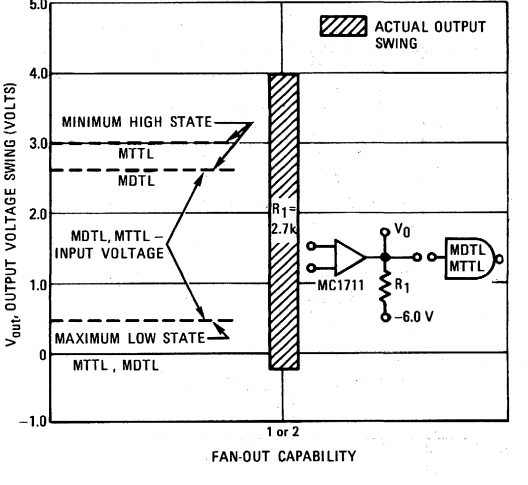


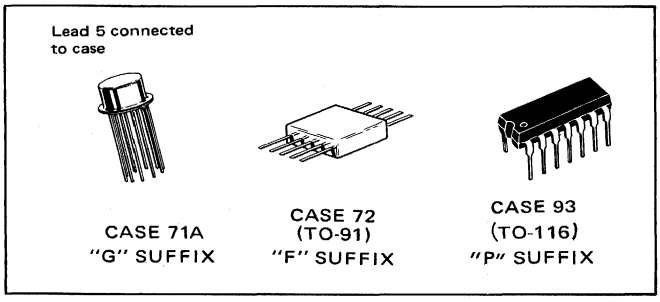
FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



DUAL DIFFERENTIAL COMPARATOR

MC1711C

. . . designed for use in level detection, low level sensing, and memory applications.



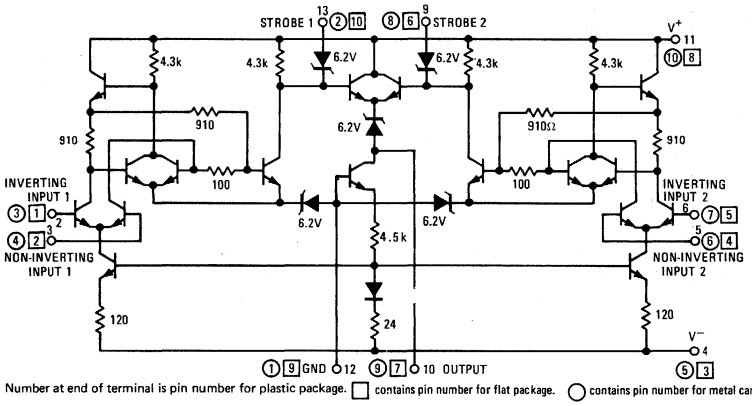
Typical Amplifier Features:

- Differential Input
  Input Offset Voltage = 1.0 mV
  Offset Voltage Drift = 5.0 μV/°C
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance — 200 ohms

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

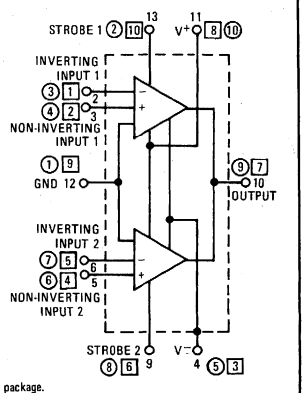
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+14 -7.0	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	±7.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (package limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C Plastic Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C

CIRCUIT SCHEMATIC

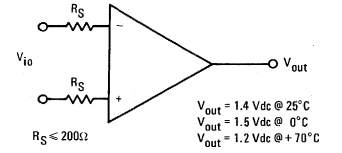
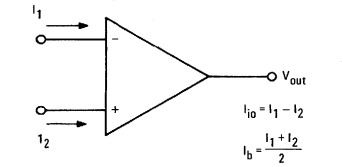
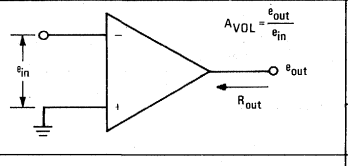
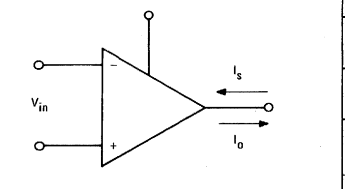
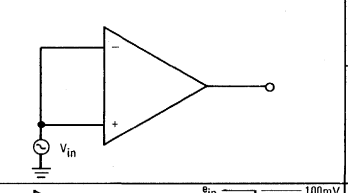
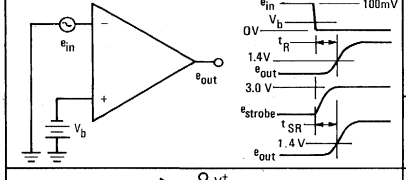
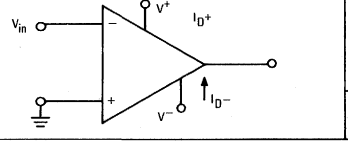


Number at end of terminal is pin number for plastic package. ☐ contains pin number for flat package. ◯ contains pin number for metal can package.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (each comparator) $V^+ = +12$ Vdc, $V^- = -6.0$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage CMV_{in} = 0 Vdc, T_A = +25°C $CMV_{in} \neq 0$ Vdc, T_A = +25°C CMV_{in} = 0 Vdc, T_A = 0 to +70°C $CMV_{in} \neq 0$ Vdc, T_A = 0 to +70°C	V_{io}	 - - - -	 1.0 1.0 - -	 5.0 7.5 6.0 10	mVdc
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	μV/°C
	Input Offset Current V_{out} = 1.4 Vdc, T_A = +25°C V_{out} = 1.5 Vdc, T_A = 0°C V_{out} = 1.2 Vdc, T_A = +70°C	I_{io}	 - - -	 0.5 - -	 15 25 25	μAdc
	Input Bias Current V_{out} = 1.4 Vdc, T_A = +25°C V_{out} = 1.5 Vdc, T_A = 0°C V_{out} = 1.2 Vdc, T_A = +70°C	I_b	 - - -	 25 - -	 100 150 150	μAdc
	Voltage Gain T_A = +25°C T_A = -55 to +125°C	A_{VOL}	 700 500	 1500 -	 - -	V/V
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 10$ mVdc, $0 \leq I_o \leq 0.5$ mA	V_{OH}	2.5	3.2	5.0	Vdc
	Negative Output Voltage $V_{in} \geq -10$ mVdc	V_{OL}	-1.0	-0.5	0	Vdc
	Strobed Output Level $V_{strobe} \leq 0.3$ Vdc	$V_{OL(st)}$	-1.0	-	0	Vdc
	Output Sink Current $V_{in} \geq -10$ mV, $V_{out} \geq 0$	I_S	0.5	0.8	-	mAdc
	Strobe Current V_{strobe} = 100 mVdc	I_{st}	-	1.2	2.5	mAdc
	Input Common Mode Range V^- = -7.0 Vdc	CM_{Vin}	±5.0	-	-	Volts
	Response Time V_b = 5.0 mV + V_{io}	t_R	-	40	-	ns
	Strobe Release Time	t_{SR}	-	12	-	ns
	Power Supply Current $V_{out} \leq 0$ Vdc	I_D^+ I_D^-	- -	8.6 3.9	- -	mAdc
	Power Consumption		-	130	200	mW

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

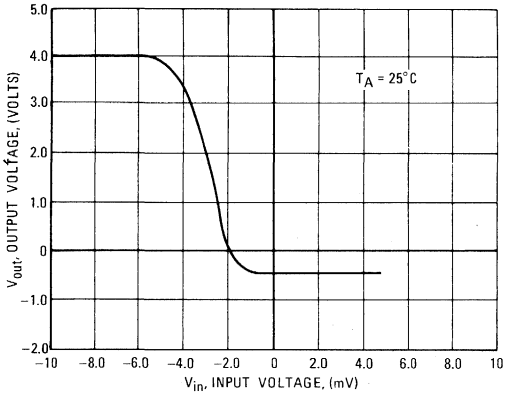


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

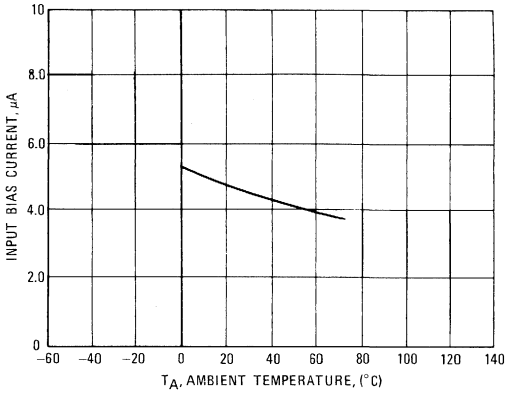


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

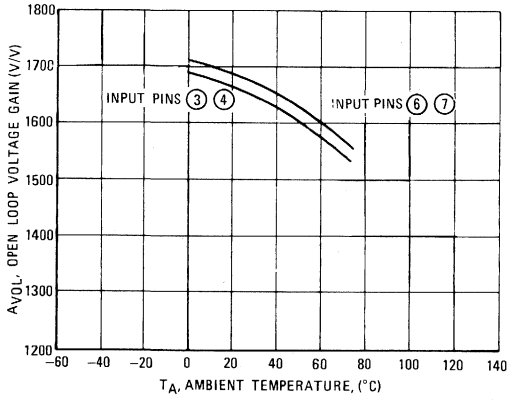


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

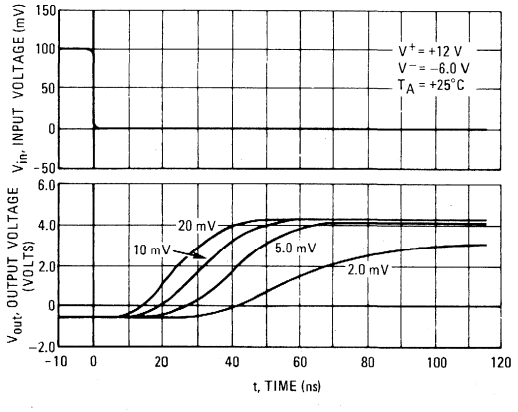


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

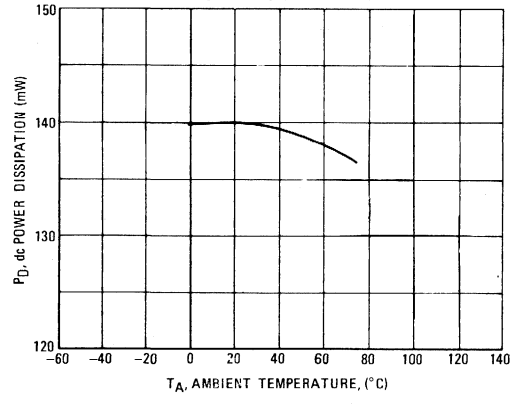


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

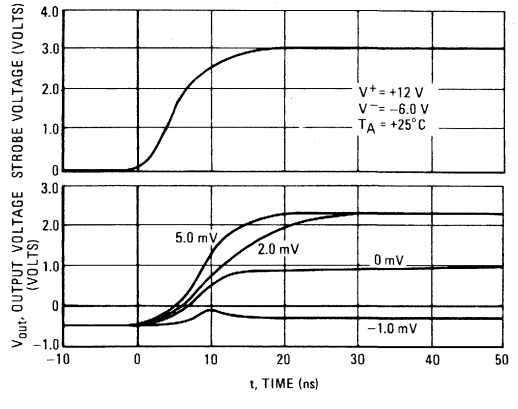


FIGURE 7 – COMMON MODE PULSE RESPONSE

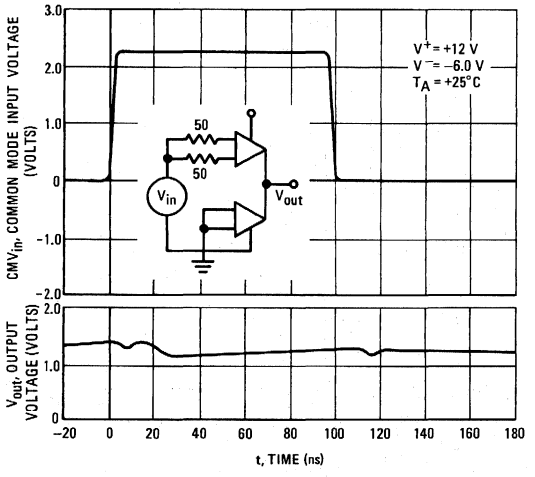


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

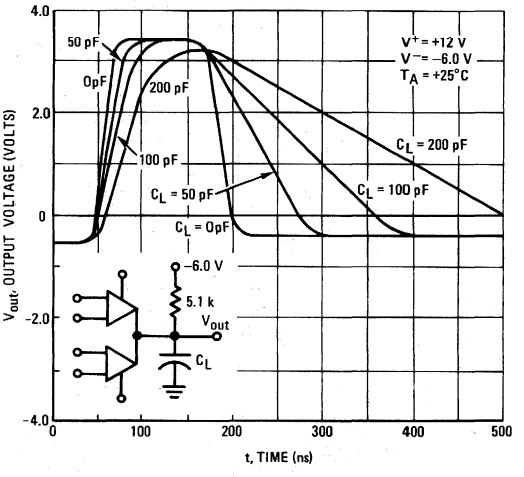


FIGURE 9 – SERIES RESISTANCE versus MRTL FAN-OUTS

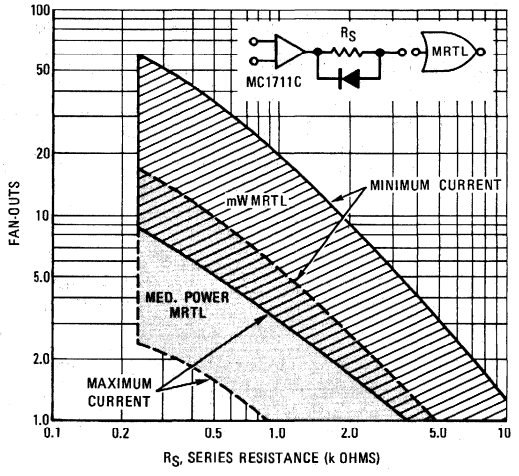
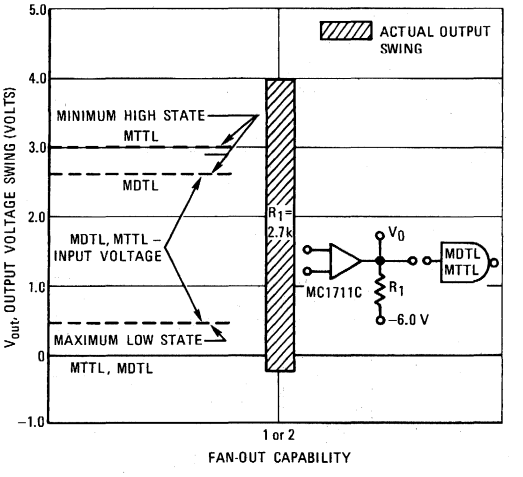


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



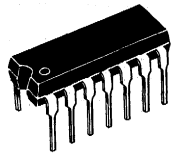
DUAL STEREO PREAMPLIFIER

MC1303P

. . . designed for amplifying low-level stereo audio signals with two preamplifiers built into a single monolithic semiconductor.

Each Preamplifier Features:

- Low Input Noise Voltage — 0.5 μV typical
- Large Output Voltage Swing — 4.5 V rms min
- High Open-Loop Voltage Gain = 8,000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

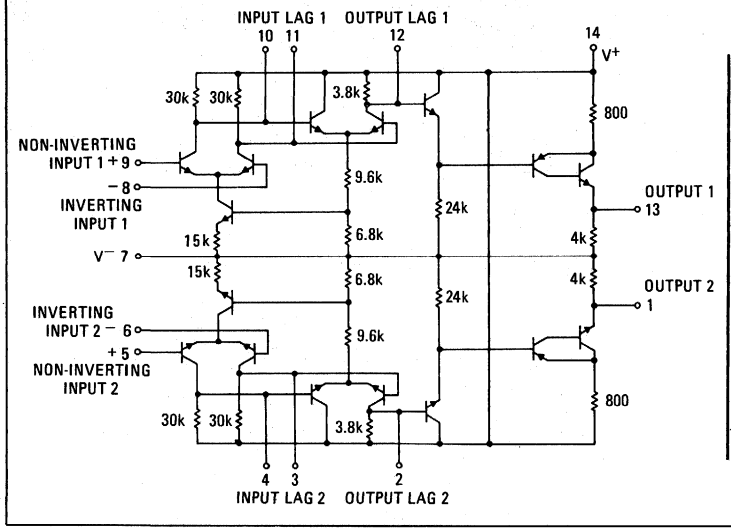


CASE 93
(TO-116)
"P" SUFFIX

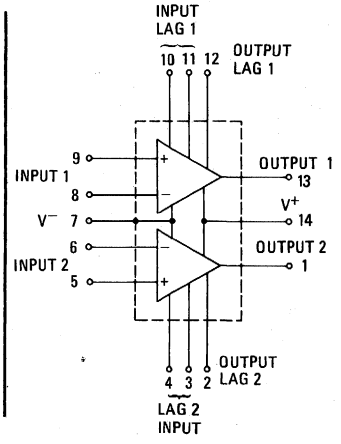
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+15 -15	Vdc Vdc
Power Dissipation (Package Limitation) Derate above 25° C	P_D	415 3.3	mW mW/° C
Operating Temperature Range	T_A	0 to +75	°C

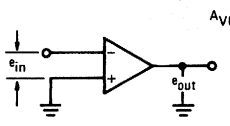
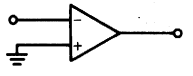
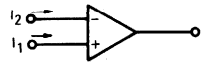
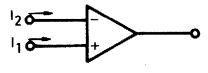
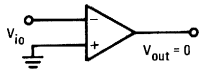
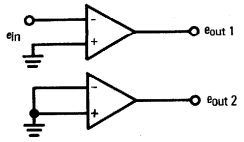
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

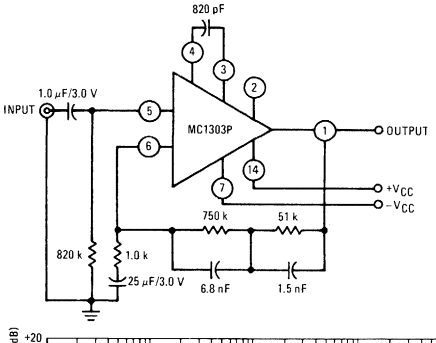


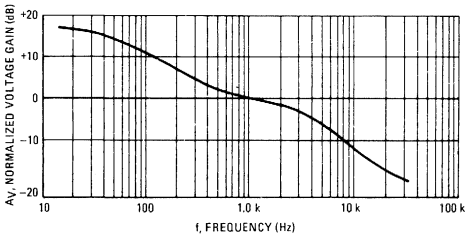
ELECTRICAL CHARACTERISTICS (Each Preamplifier) (V^+ = +13 Vdc, V^- = -13 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions (linear operations)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain	A_{VOL}	8,000	10,000	12,000	V/V
	Output Voltage Swing (R_L = 10 kΩ)	V_{out}	4.5	5.5	-	V rms
	Input Bias Current $I_b = \frac{I_1 + I_2}{2}$	I_b	-	1.0	10	μA
	Input Offset Current ($I_{io} = I_1 - I_2$)	I_{io}	-	0.2	0.4	μA
	Input Offset Voltage	V_{io}	-	1.5	10	mV
	DC Power Dissipation (Power Supply = ±13 V, V_{out} = 0)	P_D	-	-	300	mW
	Channel Separation (f = 10 kHz)	$\frac{e_{out\,1}}{e_{out\,2}}$	60	70	-	dB

TYPICAL PREAMPLIFIER APPLICATIONS

FIGURE 1 – MAGNETIC PHONO PLAYBACK PREAMPLIFIER/RIAA EQUALIZED

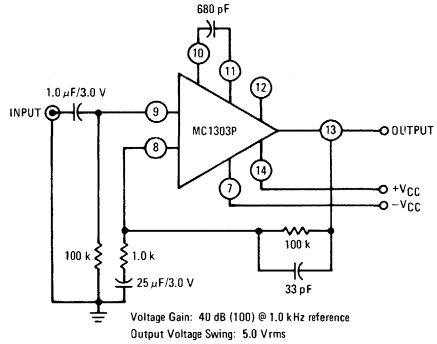




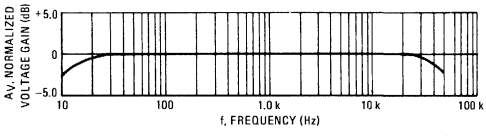
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain	:	34 dB (50) @ 1.0 kHz
Input Overload Point	:	100 mVrms @ 1.0 kHz
Output Voltage Swing	:	5.0 Vrms @ 1.0 kHz @ 0.1% THD.
Output Noise Level	:	Better Than 70 dB Below 10 mV Phono Input (Input Shorted)

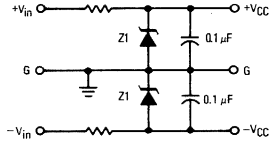
FIGURE 2 – BROADBAND AUDIO AMPLIFIER



Voltage Gain: 40 dB (100) @ 1.0 kHz reference
Output Voltage Swing: 5.0 Vrms

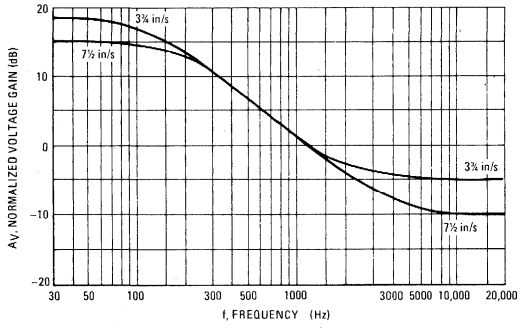


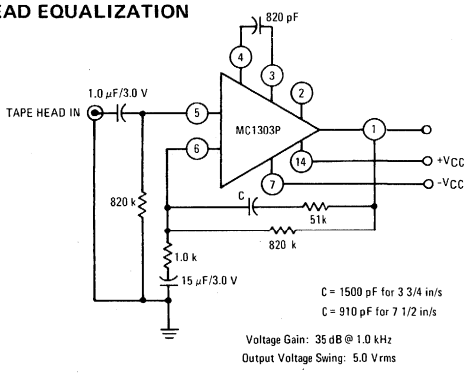
SUGGESTED POWER SUPPLY CIRCUIT



Z1 = MZ-500-19 (13 V nom.)
Select series R by allowing 11 mA for zener, and each dual I/C Preamplifier

FIGURE 3 – NAB TAPE HEAD EQUALIZATION





C = 1500 pF for 3 3/4 in/s
C = 910 pF for 7 1/2 in/s

Voltage Gain: 35 dB @ 1.0 kHz
Output Voltage Swing: 5.0 Vrms

FIGURE 4 – POWER DISSIPATION versus SUPPLY VOLTAGE

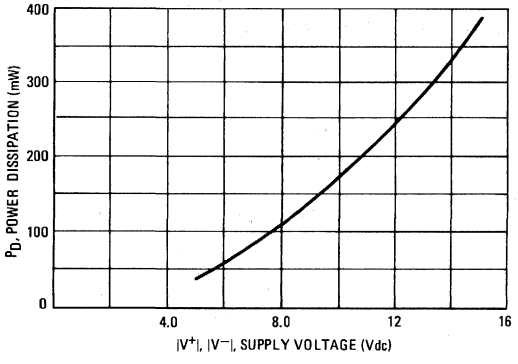


FIGURE 5 – OUTPUT LINEARITY

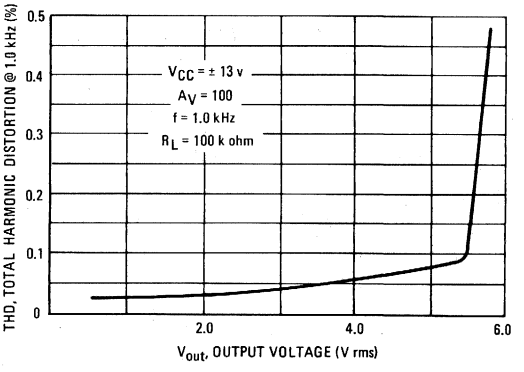
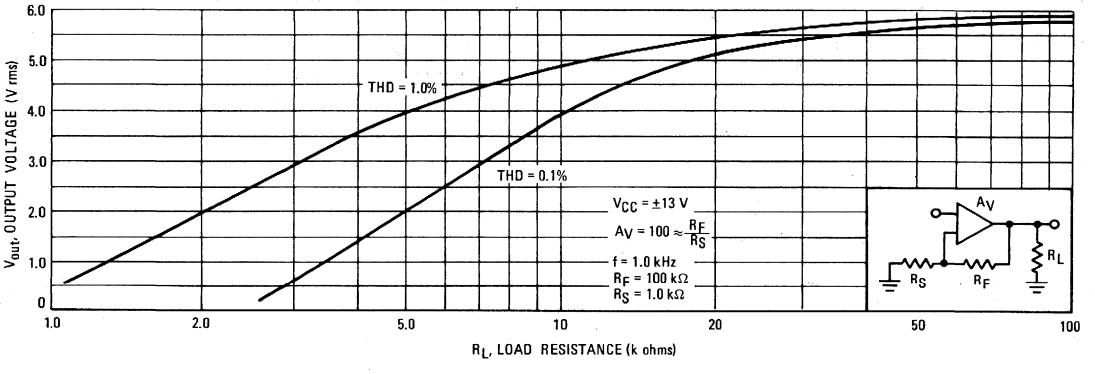


FIGURE 6 – INFLUENCE OF OUTPUT LOADING



NOISE CHARACTERISTICS

FIGURE 7A – INFLUENCE OF SOURCE RESISTANCE & BANDWIDTH

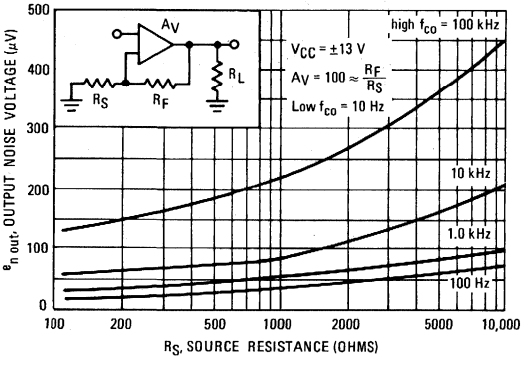
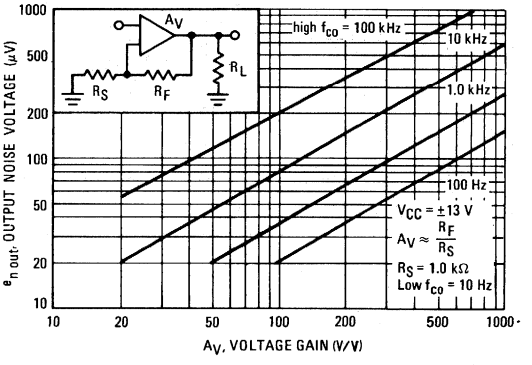


FIGURE 7B – INFLUENCE OF VOLTAGE GAIN & BANDWIDTH



APPLICATION NOTES

The MECL Line of Digital Integrated Circuits	10-3
MECL 70-MHz J-K Flip-Flop	10-27
Using Shift Registers as Pulse Delay Networks	10-33
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INTRODUCTION

The MECL family of monolithic integrated circuits consists of a wide selection of emitter coupled current mode logic circuits. Since MECL employs transistors in the non-saturating mode, it is inherently the fastest type of logic available. MECL is produced in two temperature ranges: the MC300 Series (-55°C to +125°C) and the MC350 Series (0°C to +75°C). Supply voltage is nominally -5.2 V ± 10% which yields a power dissipation between 35 and 40 mW per gate. Delay times range from 5 ns to 10 ns. The noise margin for all possible noise inputs is 200 mV or better over the full temperature range for at least 90% of the devices tested at a fan-out of one. Noise margin at room temperature is typically 300 mV.

The MECL gate employs a differential amplifier input, resulting in high input impedance, and good rejection of power supply variations. The very low output impedance of the emitter followers results in high fan-out and fast risetime for capacitive loads. Resistors and logic levels are chosen to prevent saturation of the input transistors, thus eliminating storage time. The 1.24 k resistor as shown in Figure 1 stabilizes circuit operation for wide variations of transistor β. A logical "1" for MECL is -.75 V which corresponds to one base-emitter voltage drop below ground. Logical "0" is -1.55 V which yields a nominal voltage swing of 800 mV.

Normal circuit operations is as follows: a fixed reference voltage of -1.15 V is applied to the V_{BB} input as shown in Figure 1. This voltage is chosen half way between the "0" and "1" logic levels which establishes the noise margins of the basic circuit. For example with no input to the gate, A_1, A_2 at a zero level or less, transistors A_1 and A_2 will be in a cutoff condition. Point E will now be one V_{B-E} drop below V_{BB} or at -1.90 V. For a logic "0" input A_1 and A_2 are forward biased by only .35 V which is insufficient to cause any current flow. If a logic "1" is now applied to A_1 or A_2, point E is one V_{B-E} drop lower in potential or (-.75 V) -.75 V or -1.50 V. Transistor B is now only forward biased by .35 V which leaves it cutoff. The current that passed through B has now been switched to the input transistor. The current through B was $\frac{-1.90\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} = 2.66$ mA while the current for a "1" input is $\frac{-1.50\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} =$ 2.98 mA which yields a gate that draws almost constant current.

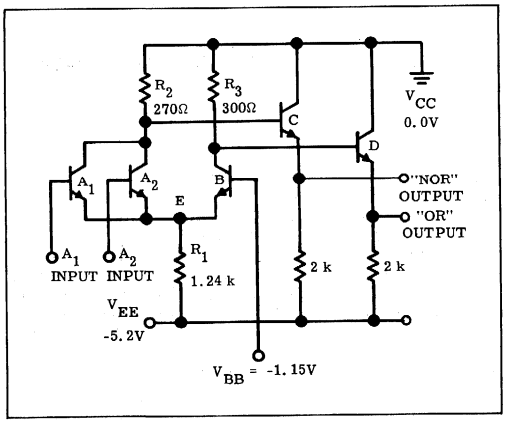


FIGURE 1 — OPERATION OF THE BASIC MECL GATE

The voltage at the collector of B (when conducting) is 0 - (300Ω x 2.66 mA) = -800 mV, while the voltage across the 270Ω resistor for a "1" input is 0 - (270Ω x 2.98 mA) = 800 mV. Transistors C and D are emitter followers; therefore the "NOR" and "OR" output voltage will follow the respective base voltage with a difference of -.75 V. If inputs are all low (logic "0"), the base of C will be at ground potential and the NOR output will be -.75 V (logic "1"). If one or more of the inputs are high, the base of C is at -.800 V and the NOR output drops to a logic "0". Operation of the OR output is similar only with no logic inversion.

The ratios of the collector resistors to the emitter resistor of the differential inputs determine the output "0" levels. Since accurate ratios of resistors are easier to obtain than absolute values of resistance, MECL output levels exhibit good uniformity from device to device. The absolute values of resistance are chosen as a compromise between speed of operation and power dissipation. As the power supply voltage is increased, the "0" level will move more negative while the "1" level remains constant. If V_{BB} is obtained from a Bias Driver connected to the same supply, the reference voltage will track with supply voltage changes or temperature variations, thus keeping V_{BB} in the center of the logic levels. At V_{EE} = -6 V for example, the nominal logic swing is 1.0 V. Not only is the logic swing increased and the noise margin bettered by about 50 mV, but power dissipation is increased as the square of the voltage. It is seen that the choice of V_{EE} = -5.2 V is a compromise between noise immunity and power dissipation. Nominal power dissipation for the basic gate is 37 mW while worst case should be considered as 20% higher.

Since the "1" level output is clamped to one V_{B-E} drop below V_{CC}, any noise appearing on the V_{CC} bus will appear on the output with very little attenuation. While any noise on the V_{EE} line will be attenuated by a factor of 4 to 5 which is primarily due to the ratio of R_1 to R_2 or R_1 to R_3. In most systems the ground plane or bus is the lowest impedance and therefore has the most constant potential and least induced noise. For this reason, the V_{CC} supply for MECL is usually obtained from ground. Another advantage of having V_{CC} at ground potential is that the gate outputs may be shorted to ground without drawing excessive current. If an output is accidently shorted to V_{EE} set at -5.2 V, the gate will draw excessive current (about 200 mA) but permanent damage does not occur until V_{EE} is increased to -8 V or -9 V and the current exceeds 400 mA.

Figure 2 shows the typical input characteristics of a MECL gate (input current vs. input voltage). Figure 3 shows output voltage vs output current over the full temperature range.

The input current is less than .1 mA and the output voltage level does not degrade for a load of 2.5 mA. D.C. fan-out is then 2.5 mA/.1 mA or 25. This is a D.C. fan-out and does not hold for high frequency operation. In fact, a maximum A.C. fan-out of 15 is recommended for high-speed operation. This decrease in fan-out is caused by the input capacitance of a gate, about 5 pF, and the wiring capacitance associated with a practical circuit. For a fan-out of 15, rise time is increased by about 5 ns while fall time will be increased by about 15 ns compared to the nominal values at a fan-out of one. The reason for the increase is that when switching from a zero to a one level, the low output impedance of the emitter follower charges the shunt capacitance, while switching from a one to a zero it is primarily the 2 k resistor that discharges the capacitance to the zero level.

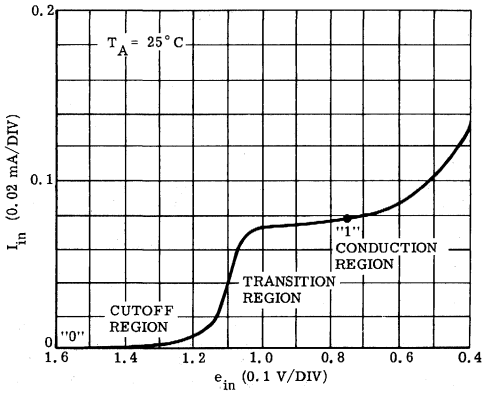


FIGURE 2 — INPUT CHARACTERISTICS OF A MECL GATE

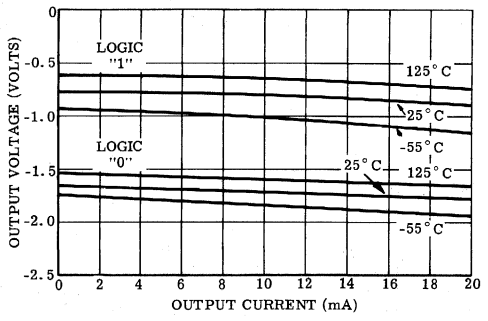


FIGURE 3 — OUTPUT VOLTAGE versus OUTPUT CURRENT

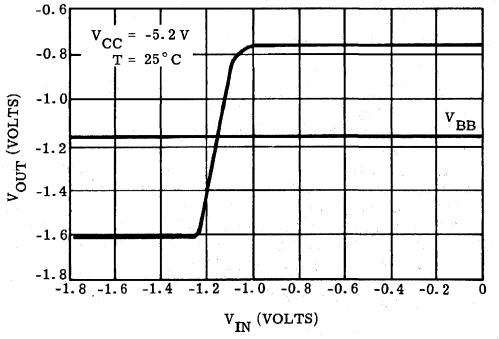


FIGURE 4 — TYPICAL "OR" TRANSFER CHARACTERISTICS

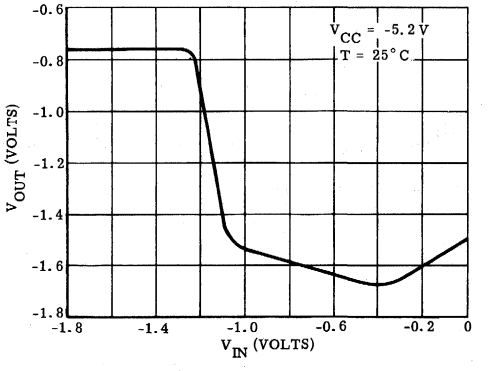


FIGURE 5 — TYPICAL "NOR" TRANSFER CHARACTERISTICS

The output of two gates may be connected in a "wired-OR" configuration, i.e. the gate outputs are wired together and whenever one or the other or both go high, the output goes high. For wired-OR operation, the worst case fan-out is 5 gate loads. Note that the pull down resistor is now effectively 1 k instead of 2 k and the fall time will be corresponding shorter.

Examination of the "OR" characteristic (Figure 4) shows that as the input voltage goes positive from a "0" level, the OR output may start to go positive at about -1.3 volts and will have reached a "1" level by about -1.0 V input. It may be shown that the 10% to 90% transistion width is approximately 115 mV at 25°C regardless of circuit characteristics.* From Figure 1 it can be seen that as the input goes more positive, transistor B remains cut off and the output level remains constant. The "NOR" characteristics show that the width of the active region is about 200 mV. As the input goes more positive than the transition, the output continues to go more negative with a slope of about 1:4. This slope is due to the collector of the particular input transistor going more negative as the input goes more positive (the transistor is approaching saturation). As the input voltage approaches about -.4 volts at 25°C or -.6 V at 125°C, the input transistor reaches saturation. Saturation occurrs with about .45 volts forward bias on the base-collector junction at 25°C and about; .3 V forward bias at +125°C. Under saturation, the collector voltage will start to follow the base input and hence the output will also start to follow the input. The slope is about 0.8:1 since the voltage across the base to collector junction increases with heavier saturation. It should be noted that saturation does not start until an input of -.6 V is reached at 125°C ambient. The worst case "1" level is -.525 V which allows very slight saturation under absolute worst case conditions. The saturation is minimal so that the output rise and fall times are only slightly affected. For high speed operation, input levels should never go more positive than a most positive "1" level.

In consideration of maximum D.C. fan-out at maximum temperature, the input characteristics in Figure 2 show increasing current for -.6 to -.5 volts input, which may occur at worst case at high temperature. Fan-out does not actually decrease since if 25 inputs all drawing high current were connected to a gate with V_{out} = -.525 V, higher than normal current would be drawn from the emitter follower and drop the output level to perhaps -.58 V. The 25 loading gates now have a more negative input and will draw less current. These two effects balance each other and maximum fan-out need not be reduced at high temperature. Worst case fan-out cannot occur at high temperature for a most positive "1" level and actually increased fan-out is available.

The following curves illustrate worst case noise margins of MECL IC'S. The curves include the variations of

*Characterization of Integrated Logic Circuits, J.A. Narud and C.S. Meyer p 1551. Proceedings of the IEEE Special issue on Integrated Electronics, Dec. 1964

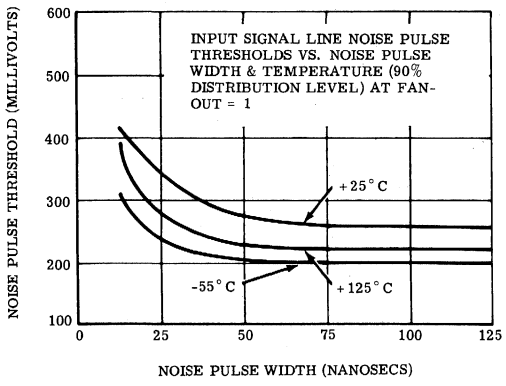


FIGURE 6 — INPUT SIGNAL LINE NOISE PULSE THRESHOLDS versus NOISE PULSE WIDTH AND TEMPERATURE

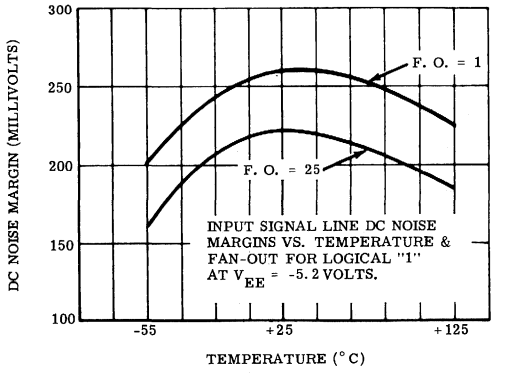


FIGURE 7 — INPUT SIGNAL LINE D.C. NOISE MARGIN versus TEMPERATURE AND FAN-OUT

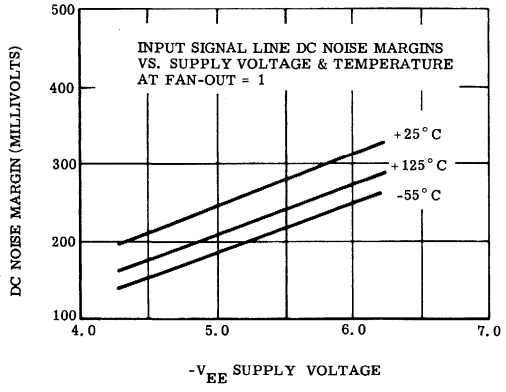


FIGURE 8 — INPUT SIGNAL LINE D.C. NOISE

V_{BB} and assure that 90% of the devices tested will have greater noise immunity than that shown:

Noise margins are slightly better for noise injected on the V_{CC} supply to the MECL gate under test and about four times better for noise injected on the V_{EE} supply.

Since the MECL gate has a differential amplifier input, it is of interest to note the common and differential mode gains. To measure these gains, one input transistor and the reference transistor are biased in the active region, i.e. neither transistor is cut off or saturated. To measure the common mode gain, a gate input such as (A_2) and the (V_{BB}) input are commoned. (Refer to Figure 1.) A nominal input of -1.15 V will center both transistors in the active region. An incremental voltage is now applied to the input while the "NOR" or "OR" output voltage with respect to common is recorded. The "NOR" common mode gain is approximately 1/9 or -19 dB while the "OR" common mode gain is about 1/7.5 or -17.5 dB. The difference arises due to the values of the collector resistors being different (270 and 300 ohms). The differential gain of the input is measured by connecting the V_{BB} input to -1.15 V and applying an incremental voltage centered around -1.15 V to an input transistor such as A_2, the "NOR" or "OR" output voltage is then noted with respect to ground. The differential "NOR" gain is about 5.6 or 14.5 dB while the differential "OR" gain is typically 6.0 application note AN-187. 100 foot twisted pair lines may be driven without problems by using MECL. The "OR" and "NOR" outputs of a gate drive one end of the line while a logic input and the V_{BB} input of a gate act as a differential receiver for the line. The line is terminated at the receiver input with a resistor of about 130Ω.

A better understanding of MECL may also be obtained from the typical curves (Figures 9, 10, and 11) that follow. These curves will answer system questions, concerning power dissipation vs temperature and supply voltage, and change in transfer characteristics with change in supply voltage.

GENERAL DESIGN RULES FOR MECL

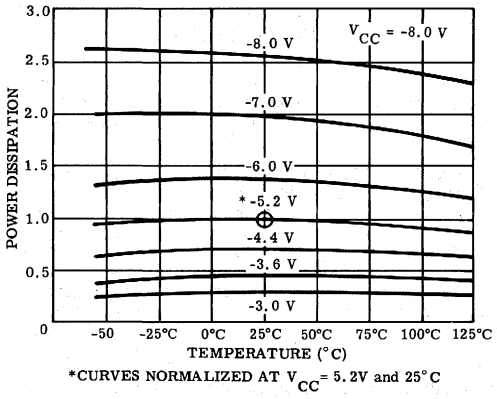
1. The maximum recommended A.C. fan-out for MECL is 15 unit input loads. D.C. fan-out is 25 unit loads. The A.C. fan-out is lower than the D.C. fan-out due to the increase in fall time and rise time with high fan-out. Also, if high fan-outs and long leads are used, overshoot due to lead inductance becomes a problem.

2. The Bias Driver (MC304, MC354) will fan-out to 25 gate loads. A dual gate or Half Adder is equivalent to two gate input loads for the Bias Driver.

3. Each $\overline{J}$ or $\overline{K}$ input to a flip flop is equivalent to one and one-half loads. For example, a $\overline{J}$ and $\overline{K}$ input tied together as a flip flop clock input would be a load of three, allowing a gate to drive five flip flops. All other inputs are a load of unity.

4. The outputs of two gates may be tied together to perform the "wired-OR" function, in which case a maximum fan-out of 5 is allowed. If only one pull down resistor is utilized, each additional common output is equivalent to one gate load. For example, if 6 gates are wired together with only one pull-down resistor connected, the fan-out would be (15) -5 or a fan-out of 10 remaining.

5. All unused inputs must be tied to V_{EE} for reliable operation. As seen from the gate input characteristics, the input impedance of a gate is very high when at a low level voltage. Any leakage to the input and/or wiring capacity of the gate will gradually build up a voltage on the input. This may ef-



*CURVES NORMALIZED AT V_{CC} = 5.2V and 25°C

FIGURE 9 — NORMALIZED POWER DISSIPATION FOR A MECL SYSTEM versus TEMPERATURE AND SUPPLY VOLTAGE

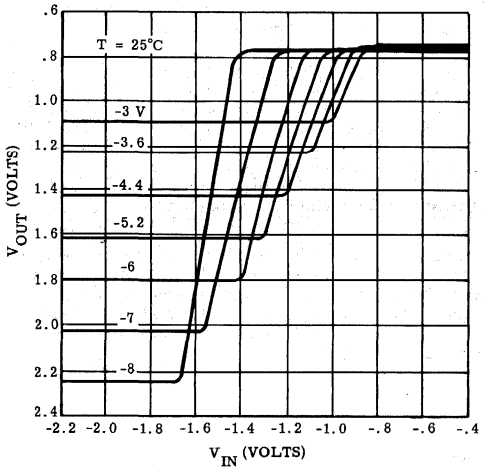


FIGURE 10 — TYPICAL "OR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

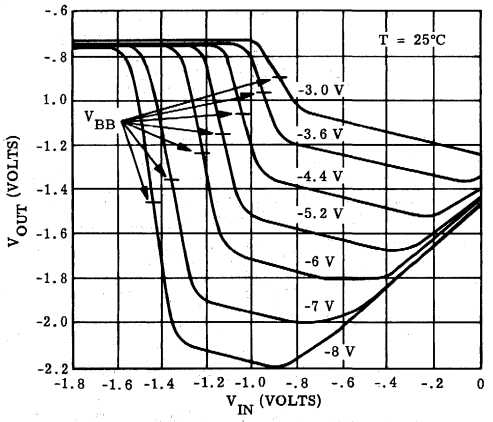


FIGURE 11 — TYPICAL "NOR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

fect noise immunity of the gate or hinder switching characteristics at low repetition rates. Returning the unused inputs to V_{EE} insures no buildup of voltage on the input and a noise immunity dependent only upon the inputs used.

6. A recommended maximum of three input expanders should be used. For example, the MC306/MC307, MC356/MC357 gates would then have a fan-in of 18 available. If more than three input expanders are used, the NOR output rise and fall times suffer noticeably because of the increased capacitance at the collector node of the input transistors. For low frequencies, higher fan-ins may be employed if rise and fall times are of no significance.
7. Each gate package must have external bias supplied (V_{BB}) except for gates with internal reference such as MC312, MC313, MC362A, MC363, MC369, and the flip flops.

MECL IC's -55°C to +125°C

MC301	5-input OR, NOR
MC302	DC R-S Flip Flop, Outputs buffered, Reset input expandable
MC303	Half Adder--Sum, Carry, NOR
MC304	Bias Driver
MC305	5-input Expander
MC306	Expandable 3-input OR, NOR
MC307	Expandable 3-input OR, NOR, No pull-down resistors
MC308	J-K Flip Flop, DC R-S, Buffered outputs
MC309	Dual 2-input NOR, Both pull-down resistors
MC310	Dual 2-input NOR, One pull-down resistor, One optional
MC311	Dual 2-input NOR, One optional pull-down resistor
MC312	Dual 3-input NOR
MC312A	Dual 3-input NOR with Bias Driver
MC313F	Quad 2-input NOR with Bias Driver
MC314	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC315	Line Driver
MC316	Lamp Driver
MC317	Lever Translator MECL to DTL
MC318	Level Translator DTL to MECL

MECL IC's 0° to +75°C

MC351	5-input OR, NOR
MC352	DC R-S Flip Flop, No output buffers, Reset input expandable
MC352A	Same as MC302
MC353	Half Adder--Sum, Carry, NOR
MC354	Bias Driver
MC355	5-input Expander
MC356	Expandable 3-input OR, NOR
MC357	Expandable 3-input OR, NOR, No pull-down resistors
MC358A	J-K Flip Flop, DC R-S, Buffered outputs
MC359	Dual 2-input NOR, Both pull-down resistors
MC360	Dual 2-input NOR, One pull-down resistor, One optional
MC361	Dual 2-input NOR, One optional pull-down resistor
MC362	Dual 3-input NOR
MC362A	Dual 3-input NOR with Bias Driver
*MC363F	Quad 2-input NOR with Bias Driver
MC364	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC365	Line Driver
MC366	Lamp Driver
MC367	Level Translator MECL to DTL
MC368	Level Translator DTL to MECL
*MC369G	Dual-2 OR, NOR Clock Driver and High speed gate
*MC369F	Dual-4 OR, NOR Clock Driver and High speed gate

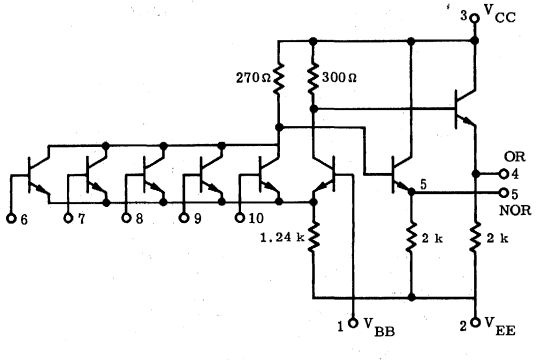
*F indicates a 14 lead flat package
*G indicates a TO-5 type package

TABLE 1 — MECL LOGIC ELEMENTS

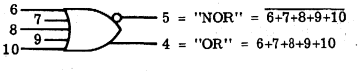
THE MECL FAMILY OF IC LOGIC ELEMENTS

The following section includes a complete explanation of each logic element. Schematics, logic diagrams, logic equations, and truth tables, where applicable, are included along with a detailed description of each circuit.

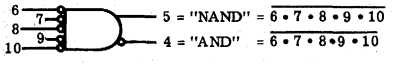
5 INPUT OR, NOR: MC301, MC351



POSITIVE LOGIC
SINGLE GATE

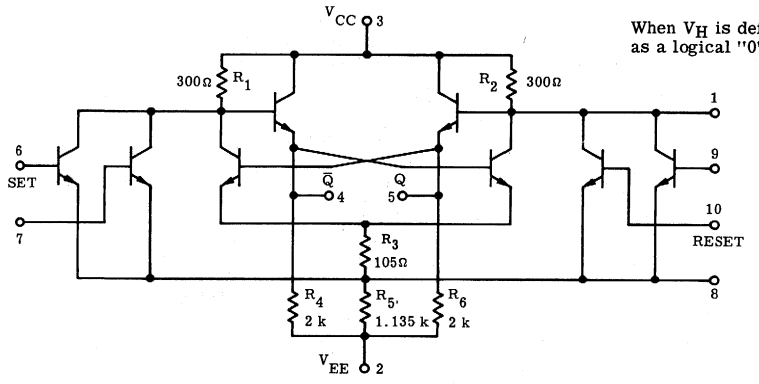


NEGATIVE LOGIC
SINGLE GATE

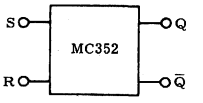


The 5-input gate obtains the maximum number of inputs for a standard TO-5 10-pin can. A pair of the gates may be wire-OR'd to form a 10-input gate. If desired, both NOR's and OR's may be wired together giving a gate that has the properties of a single gate with a fan-out of 5, fast fall time, and 10 inputs. Nominal power dissipation of the gate is 37 mW over the temperature range. Typical propagation delay is 8 ns with rise and fall times of 8 ns. As fan-out increases above 5, the fall time increases more rapidly than the rise time.

DC R-S FLIP-FLOP: MC352



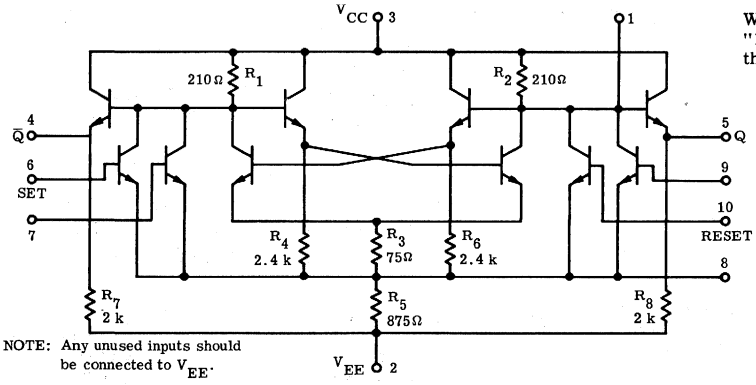
When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

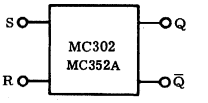
The D.C. R-S flip flop is most useful as a storage element. Dual inputs allow the OR function to be performed at the Set or Reset inputs. As may be noted from the schematic the Reset input is expandable. A maximum of 2 or 3 expanders is recommended for high speed operation since the additional collector node capacitance increases rise and fall times. The Set input may also be expanded by redefining inputs and switching the wiring of Q and $\bar{Q}$. The Set and Reset inputs should be standard MECL levels for optimun operation. Input rise and fall time is unimportant unless high speed operation is desired. Typically, the maximum speed of Set-Reset operation is 65 MHz, propagation delay 6.5 ns, rise and fall times 8 ns, and power dissipation 42 mW. The maximum Set-Reset speed is obtained for inputs with about 6 ns rise and fall times and a pulse widths of about 9 ns.

DC R-S FLIP-FLOP, OUTPUTS BUFFERED, RESET INPUT: MC302, MC352A



NOTE: Any unused inputs should be connected to V_{EE}.

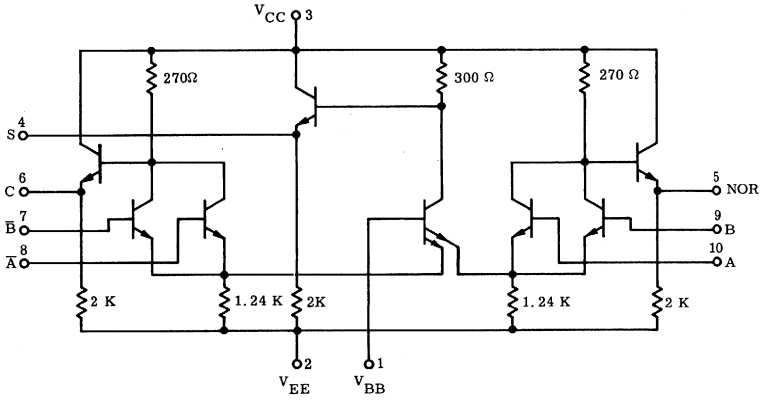
When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:

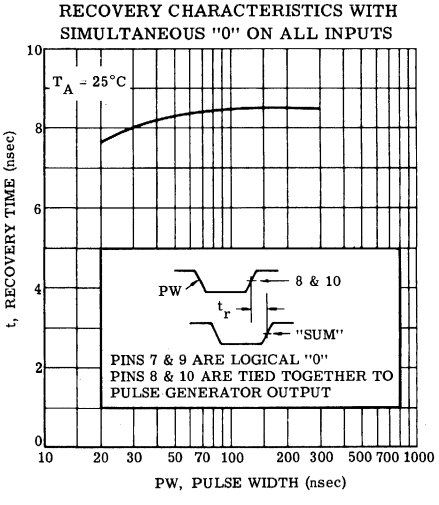


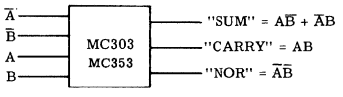
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

This flip flop is essentially the same as the MC352 with the exception that the outputs are isolated. The MC352 is sensitive to noise on the output lines because they feed back directly into the bases of the bistable transistors. The output emitter followers on the MC302, MC352A isolate each output from the respective base of each bistable transistor; giving about 800 mV noise margin for noise coupled into the output.

It should be noted that if both the set and reset inputs are high, both outputs will be low. Bringing both inputs to "0" simultaneously leaves the output in an undefined state, i.e. either a "0" or a "1". Typical parameters: rise time 11.5 ns fall time 12.5 ns, propagation delay time 11 ns, power dissipation 45 mW. The flip flop may be set and reset at a maximum rate of about 50 MHz. Optimum input pulses for 50 MHz operation should have rise and fall times of 6 ns or less with pulse widths of about 14 ns.







HALF ADDER Truth Table

Pin #	A 10	B 9	$\overline{A}$ 8	$\overline{B}$ 7	OUT 4
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

The Half Adder is a very useful element of the MECL family. It can be used as a digitally controlled inverter, a digital comparator, or to provide SUM, CARRY, and NOR, or SUM and $\overline{SUM}$ if desired. Normally two bits and their compliments are applied to the Half Adder so that two of the inputs are always high as shown in the schematic. If all four of the inputs are low, the V_{BB} transistor will be sinking twice the normal current at 25°C and the SUM output will drop to -2.3 V. This does no harm but to saturate the V_{BB} transistor. The graph shown above illustrates the recovery time at 25°C for saturation of the V_{BB} transistor. At higher temperatures it would take longer to recover.

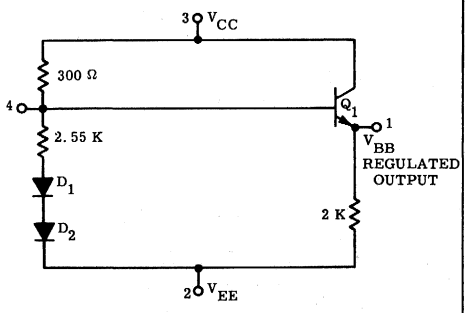
The Half Adder gating functions are the same as the general MECL gate shown in Figure 1 with the exception that the bias transistor performs the AND function, in that when both emitters are high, the SUM output is also high. With reference to the schematic and the letters representing the inputs, it is seen that the collector of the V_{BB} transistor is high when A and $\overline{B}$ are high or $\overline{A}$ and B are high. This represents the exclusive OR function or the sum of A and B. The Carry and NOR outputs may be wired together to form $AB + \overline{A}\overline{B}$ which may be recognized as $\overline{SUM}$. By the rules of Boolean Algebra: $SUM = A\overline{B} + \overline{A}B$ then $\overline{SUM} = A\overline{B} + \overline{A}B = \overline{(A\overline{B})} \cdot \overline{(\overline{A}B)} = (\overline{A}+B)(A+\overline{B}) = \overline{A}\overline{B} + AB$ which is the wired output.

A digitally controlled inverter is one unique application of the MECL Half Adder. The inputs are connected in the same manner as for the SUM function. If A is considered as the digital information input and $\overline{B}$ as the control level (inversion or not inversion), then A appears at the S output if $\overline{B}$ is high and $\overline{A}$ appears at the S output if B is high. Thus A or $\overline{A}$ is obtained on the same wire according to the level of B.

The propagation delay of the circuit is typically 8 ns for the SUM output and 6 ns for the Carry and NOR outputs at room temperature at a fan-out of one gate. Rise times are typically 6.5 ns for all outputs while fall times are 8.5 ns for SUM and 8.0 ns for NOR and CARRY. Typical power dissipation is 65 mW.

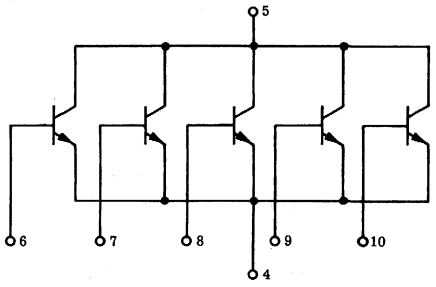
The Half Adder is shown in a digital comparator circuit and a five bit asynchronous adder in the last section of the paper.

BIAS DRIVER: MC304, MC354



The Bias Driver provides a temperature and voltage compensated reference for MECL logic. Any of the three MECL voltages may be grounded, but the common voltage of the Bias Driver must correspond to that of the logic system. The device has a unique application when coupling a signal through a capacitor to pin 4. First the gate acts as a level translator from any voltage to MECL levels. If the input is 800 mV p-p, the standard MECL levels will appear at pin 1. For low level A.C. and R.F. inputs, the output will be centered in the active region of a MECL gate which may then be used as an amplifier. A low quality, high bandwidth differential amplifier may be obtained by using two bias drivers, one connected to a normal gate input and the other connected to the V_{BB} input of a MECL gate. The "OR" and "NOR" outputs then provide a very low impedance differential output. The A.C. input impedance of the Bias Driver is 250Ω in parallel with about 5 pF which will terminate a low impedance line fairly well. If V_{CC} contains excessive noise the output on pin 1 may be filtered by connecting a capacitor between pin 4 and 2. Typical power dissipation is 17 mW. The Bias Driver will fan-out to 25 unit input loads.

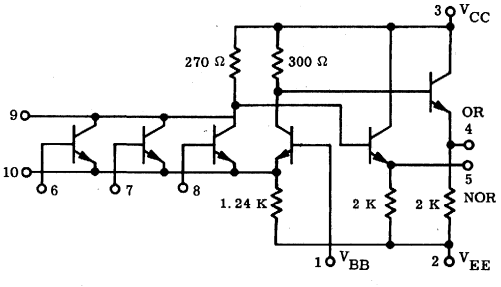
5 INPUT EXPANDER: MC305, MC355



The Gate Expander acts as a 5-input NOR gate when referring to the collectors or as a 5-input OR gate when referring to the emitters. This infers a resistor connected from the collector to a high level voltage while the emitter node is connected to a low voltage through another resistor.

The maximum number of recommended expanders to be used with a gate is three for high speed operation. If more than three expanders are used, the output rise and fall times will become excessive for high speed operation. When used with a MECL gate, power dissipation is negligible.

EXPANDABLE 3 INPUT OR, NOR: MC306, MC356

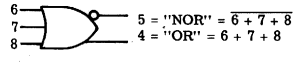


This gate may be expanded to 18 inputs by use of the MC305 or MC355, otherwise operation is the same as the basic MECL gate shown in Figure 1.

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

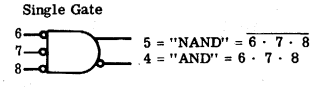
Single Gate



NEGATIVE LOGIC

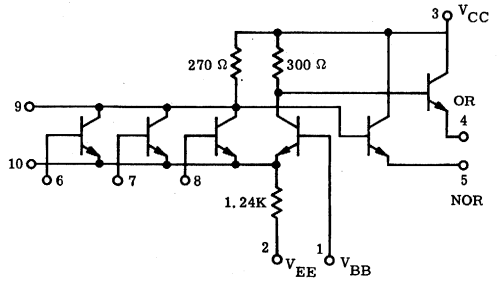
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate



Propagation delay time is typically 6.5 ns with a rise and fall time of 7 ns. Typical power dissipation is 37 mW.

EXPANDABLE 3 INPUT OR, NOR, NO PULL-DOWN RESISTORS: MC307, MC357

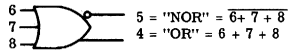


This gate is the same as MC306, MC356 except that the output pull-down resistors have been removed lowering the power dissipation. Propagation delay time is nominally 6.5 ns with rise and fall times of 7 ns with a normal load. The output of this gate may be wire-OR'd with other MC307, MC357 gates and one gate that has a pull-down resistor to -5.2 V. This will result in a large power savings since the gate only dissipates 16 mW at V_{EE} = -5.2 V. The maximum recommended number of gates connected in this manner is: 1 gate with a pull-down resistor, 14 gates with no pull-down resistor and the input of another MECL gate. In other words, the gate with the pull-down resistor, such as the MC301 or MC306, has a recommended maximum fan-out of 15. Each of the other wire-OR'd gates is the equivalent of one load, resulting in a fan-out of 1 to the input of another MECL gate.

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

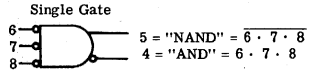
Single Gate



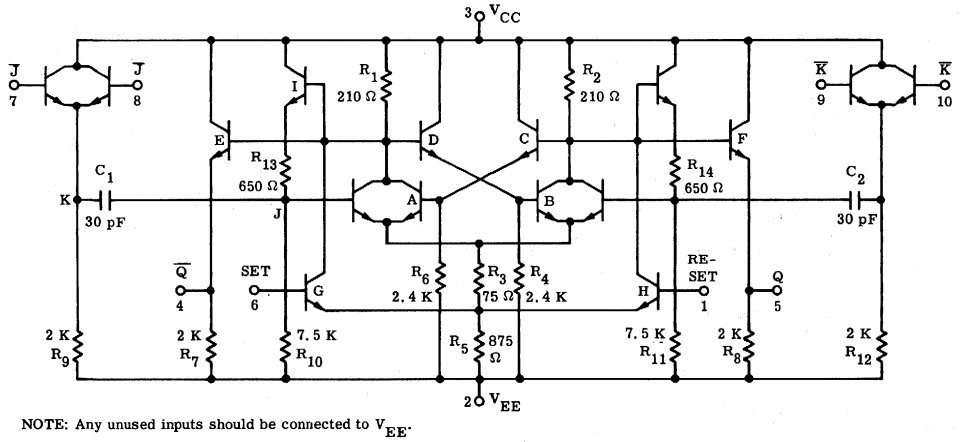
NEGATIVE LOGIC

Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate

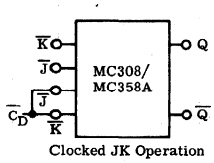


J-K FLIP-FLOP, DC R-S, BUFFERED OUTPUTS: MC308, MC358A



NOTE: Any unused inputs should be connected to V_{EE}.

When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



Clocked JK Operation

State #	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^{n+1}
1	ø	ø	0	Q^n
2	0	0	1	$\overline{Q}^n$
3	0	1	1	1
4	1	0	1	0
5	1	1	1	Q^n

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state.

Set-Reset operation is the same as MC302.

Operation of the MC308, MC358A

Transistors A and B form the "heart" or bistable pair of the flip flop. The collector of B is coupled back to the base of A through C, likewise D couples A back to B forming the bistable element. The output of A is buffered through E to give the $\overline{Q}$ output, while F buffers B to give the Q output. When the Set input (pin 6) goes to a high level (-0.75 V), the collector of G goes low pulling A and D low. The collector of B then goes high which holds the collector of A low through C. The flip flop is now Set to the "1" state, i.e. Q high and $\overline{Q}$ low. Likewise a high level in or a positive pulse on pin 1 resets the flip flop to the "0" state. Since the base of either A or B is at a one level (-0.75 V), the emitters will be one V_{BE} drop lower or at -1.50 V. The potential at the node between R_3 and R_5 is then -1.8 V which corresponds to a

continued

nominal 400 mV noise immunity for a Set or Reset input normally at -1.55 V (logic "0"). The Set, Reset input transistors may be considered to be in the active region at 0.65 V_{BE}.

The emitter of I also follows the collector of A and will yield standard MECL levels. The voltage at point J will then be approximately -1.1 or -1.85 due to the divider action of R_{13} and R_{10}. The $\overline{J}$ inputs on pins 7 and 8 act as emitter followers so that point K will be either -1.5 or -2.3 V. C_1 differentiates the input as it appears at point K. Whenever point K swings negative, nothing will happen, but when point K goes positive, a positive pulse will be coupled to the base of the transistor in parallel with A. If the collectors of the pair were high, they will be brought to a low level as if the flip flop had received a Set pulse. Likewise a positive going level at C_2 will reset the flip flop.

It should be noted that the input rise time must be less than a specified value to transfer enough charge through the capacitor to switch the flip flop. Also the maximum toggle speed of the flip flop is limited by the internal time constants associated with C_1 and C_2. If one of the $\overline{J}$ inputs is high it will inhibit a positive going level on the other $\overline{J}$ input and no pulse will be coupled into the flip flop, unless excessive amplitude, perhaps caused by ringing on the input line, is applied. If differences in the logic levels and ringing both add up to 250 mV for 10 ns or more, it is possible to trigger a flip flop falsely. For worst case design over temperature extremes overshoot should be a maximum of 100 mV. Note the discussion on overshoot for the MC369.

The classical J-K flip flop has its inputs labeled J, K, and C and operates on negative levels. The MECL $\overline{J}$-$\overline{K}$ flip flop is opposite, in that high levels inhibit and positive going clock transitions actually clock the flip flop. The MECL levels generally are preferrable since positive logic is more common than negative logic.

As may be seen from the truth table and the logic diagram for clocked $\overline{J}$-$\overline{K}$ operation, a dynamic "0" or negative going clock does not affect the flip flop when the other $\overline{J}$ and $\overline{K}$ inputs are at a static level. If $\overline{C_D}$ and $\overline{K}$ are low and $\overline{J}$ goes high, the flip flop will be set to a "1" on the Q output. Likewise if $\overline{C_D}$ and $\overline{J}$ are low while $\overline{K}$ goes high, the flip flop will be reset to zero. For normal clocked operation, $\overline{J}$ and $\overline{K}$ are static levels changed only when C_D is high (flip flop inhibited). The symbol in the truth table, ϕ, refers to a static level of either high or low. For state 1 in the truth table, the flip flop output, Q, will be the same level at time t = n + 1 as it was at t = n for a dynamic "0" transition of the clock between t = n and t = n + 1. For state 2 neither $\overline{J}$ or $\overline{K}$ are inhibited, and a dynamic clock will toggle the flip flop, i.e. at t = n + 1 the flip flop will be in the opposite state that it was in at t = n. For state 3, the $\overline{K}$ input is inhibited and a "1" will be shifted into the flip flop. Likewise a "0" will be shifted in for state 4. In state 5, both inputs are inhibited and the flip flop will not change state unless a Set or Reset input is received. Set - Reset inputs take priority over the $\overline{J}$-$\overline{K}$ inputs as may be seen from the schematic. If an uninhibited clock input is received while the Set or Reset level is true (high), a 20 ns pulse of about 400 mV level may appear on the output of the flip flop.

MC308, MC358A Characteristics

As in every $\overline{J}$ $\overline{K}$ flip flop the MC308, MC358A requires a minimum down time of the clock to ensure toggle. Minimum down time of the clock waveform is determined primarily by the discharge time constant of R_9 and C_1 which is nominally 60 ns. After a high level input appears at point K, at least 29 ns under worst case conditions must be allowed for the voltage at point K to decay sufficiently so that the next positive going input will transfer enough charge through C_1 to reliably toggle the flip flop. The maximum guaranteed toggle frequency of the flip flop is 15 MHz with rise and fall times of 9 ns, down time of 29 ns, and 800 mV amplitude. The typical toggle frequency is above 20 MHz when driven from a gate with sharp rise and fall times. Maximum toggle frequency is very dependent upon clock rise time and clock amplitude. This dependence is caused by the variable sensitivity of the flip flop with input rise time changes. Refer to the following section on descriptive curves for MECL flip flops for data showing this relationship.

Typical propagation delay time is 7 ns while nominal rise and fall times are 7 ns and 8 ns respectively. Power dissipation is about 85 mW at V_{EE} = -5.2 V.

DESCRIPTIVE CURVES FOR MECL FLIP-FLOPS

The following data is most helpful to the designer in understanding the characteristics of

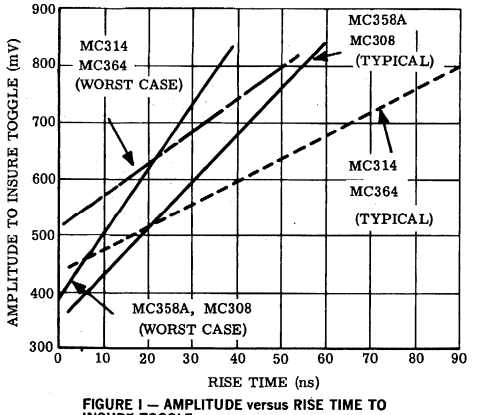


FIGURE I — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

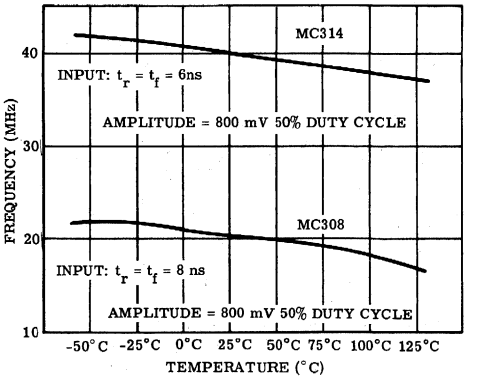
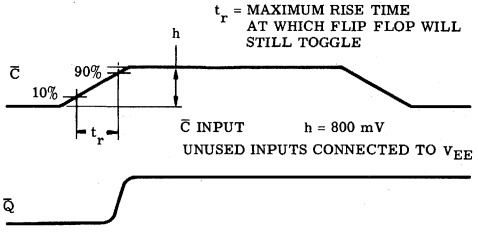


FIGURE II — TYPICAL TOGGLE FREQUENCY versus TEMPERATURE

continued

MECL flip flops. As may be seen from the data, typical characteristics can be much better than those specified for worst case. In fact, typical data usually runs about 30% better than worst case. For example, the distribution of characteristics is wide enough that for fast rise and fall times some of the MC314 flip flops will toggle reliably at 50 MHz. The curves are self-explanatory and include the test conditions for data shown in Figures I, II, III, IV, and V.



90% OF THE DEVICES WILL TOGGLE AT RISE TIMES EQUAL TO OR LESS THAN THAT SHOWN

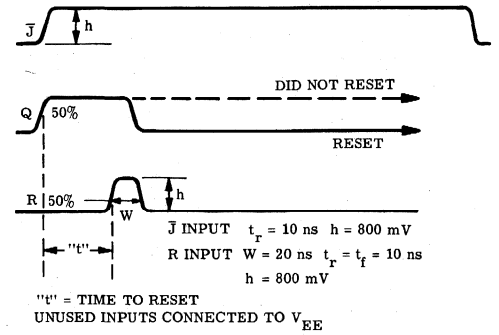
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	60ns		70ns		90ns
MC364		60ns	70ns	85ns	
MC308	40ns		45ns		70ns
MC358A MC358		40ns	45ns	50ns	

NOTE: FOR WORST CASE DESIGN t_r SHOULD BE:

MC314, MC364: $t_r < 50$ns @ 800mV

MC308, MC358A: $t_r < 35$ns @ 800mV

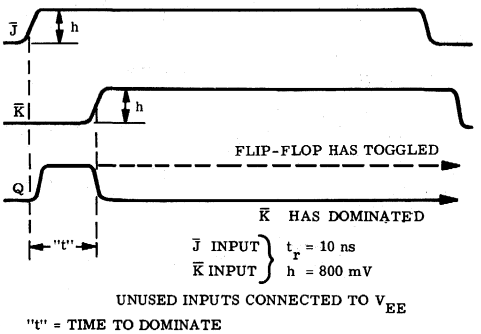
FIGURE III — MAXIMUM RISE TIME TO TOGGLE TEST



THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	2ns		1ns		1ns
MC364		6ns	3ns	7ns	
MC308	22ns		13ns		33ns
MC358A		18ns	9 ns	22ns	

FIGURE IV — MAXIMUM TIME TO RESET TEST

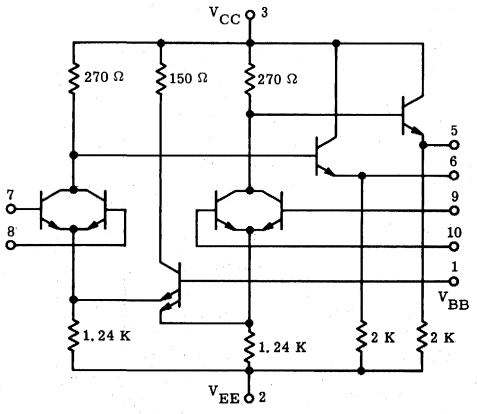


THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

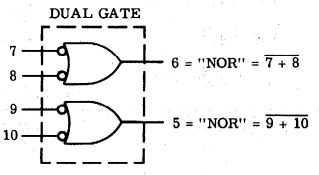
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	20 ns		21 ns		16 ns
MC364		30 ns	32 ns	35 ns	
MC308	30 ns		33 ns		41 ns
MC358A		20 ns	21 ns	26 ns	

FIGURE V — MAXIMUM TIME TO DOMINATE TEST

DUAL 2 INPUT NOR, BOTH PULL-DOWN RESISTORS: MC309, MC359

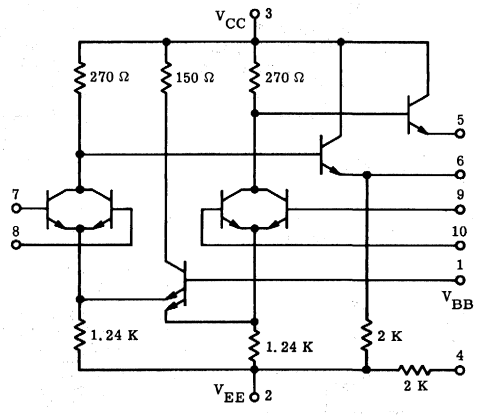


POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:

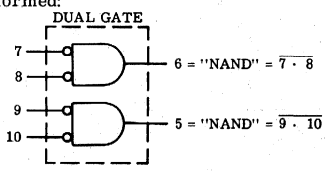


Use of the Dual 2-input NOR gate will usually result in a lower "can count" i.e. the total number of integrated circuits used in a given system. Note that pin 1 the bias driver input is equivalent to two standard loads due to the double emitter output. Typical propagation delay is 7 ns, with a rise time of 6 ns and fall time of 7.5 ns at 25°C. Nominal power dissipation is 55 mW.

DUAL 2 INPUT NOR, ONE PULL-DOWN RESISTOR, ONE OPTIONAL: MC310, MC360

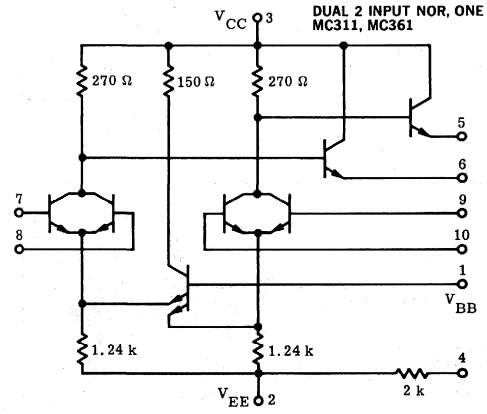


NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:



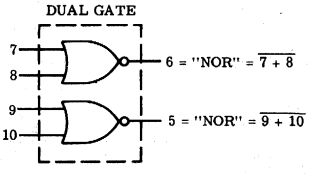
This gate is identical to the MC309, MC359, except that pin 4 allows the option of a pull-down resistor or power savings for the output on pin 5. Typical power dissipation with pin 5 connected to 4 is 55 mW, while it is only 43 mW at V_{EE} = -5.2 V without the pull down resistor. Typical propagation delay is 7 ns. Nominal rise and fall times are 6 ns and 7.5 ns respectively at room temperature.

DUAL 2 INPUT NOR, ONE OPTIONAL PULL-DOWN RESISTOR: MC311, MC361

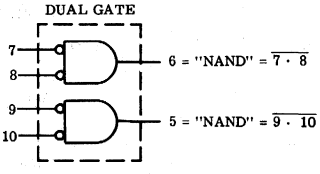


This gate is useful where wire-OR'd outputs are a savings. Both outputs are normally without pull-down resistors which reduces the nominal power dissipation to 31 mW. If the pull-down resistor on pin 4 is used, the nominal dissipation increases to 43 mW. Note the rules governing the wired-OR outputs under General Rules for MECL shown on a previous page. Propagation delay is typically 7 ns with 6 ns rise and 7.5 ns fall times at room temperature.

POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:

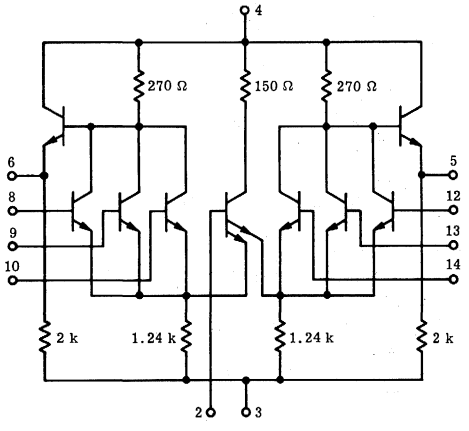


NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:

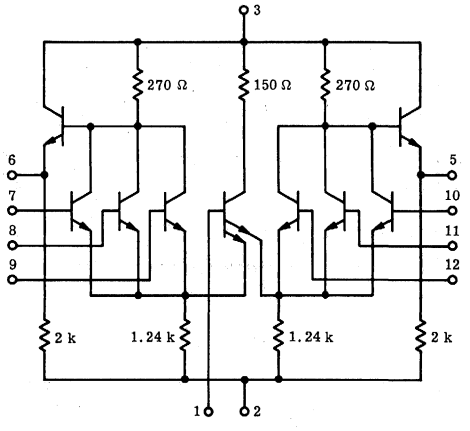


DUAL 3 INPUT NOR: MC312, MC362

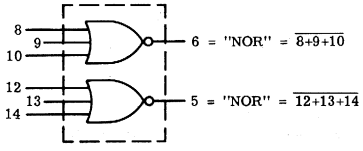
MC312F, MC362F



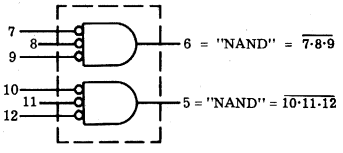
MC312G, MC362G



Positive Logic

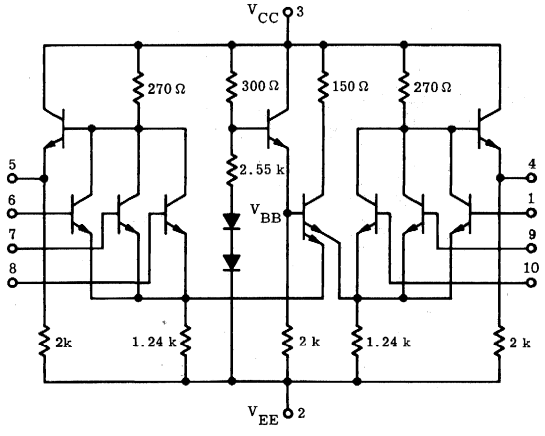


Negative Logic

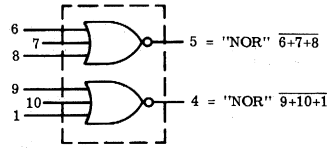


These circuits are preferred wherever three-input gates provide a savings. The F model is available in a 14-pin flat package while the G model number indicates a 12-pin TO-5 package. The typical power dissipation is 55 mW. Nominal delay time is 7 ns with output rise and fall times of about 7 ns.

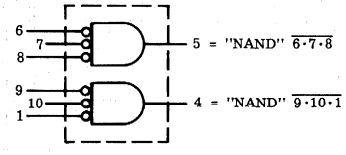
DUAL 3 INPUT NOR WITH BIAS DRIVER: MC312A, MC362A



Positive Logic

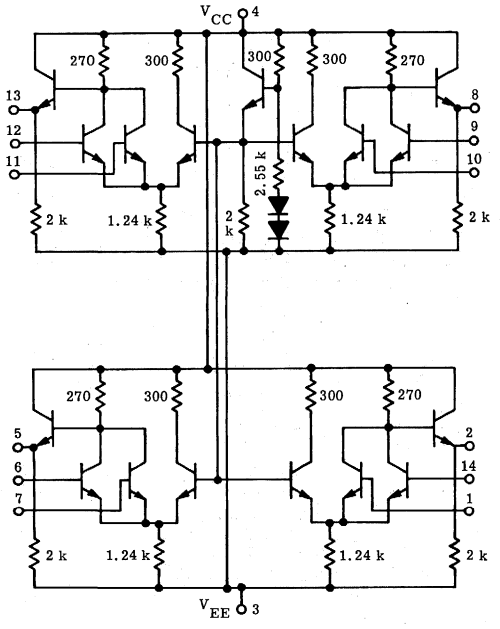


Negative Logic



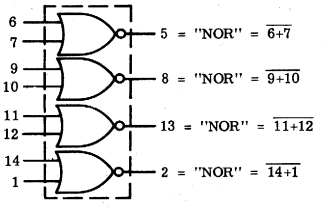
The MC312A, MC362A is essentially the same as the MC312, MC362 except that a bias driver is included on the same monolithic chip, allowing the circuit to be mounted in a 10-pin TO-5 can. Typical characteristics are: power dissipation 72 mW, propagation delay time 8.5 ns and rise and fall times of 9 ns.

QUAD 2 INPUT NOR WITH BIAS DRIVER: MC313F, MC363F



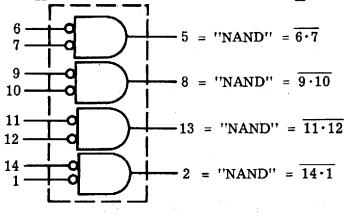
POSITIVE LOGIC

V_H is defined as logical "1", V_L as logical "0"



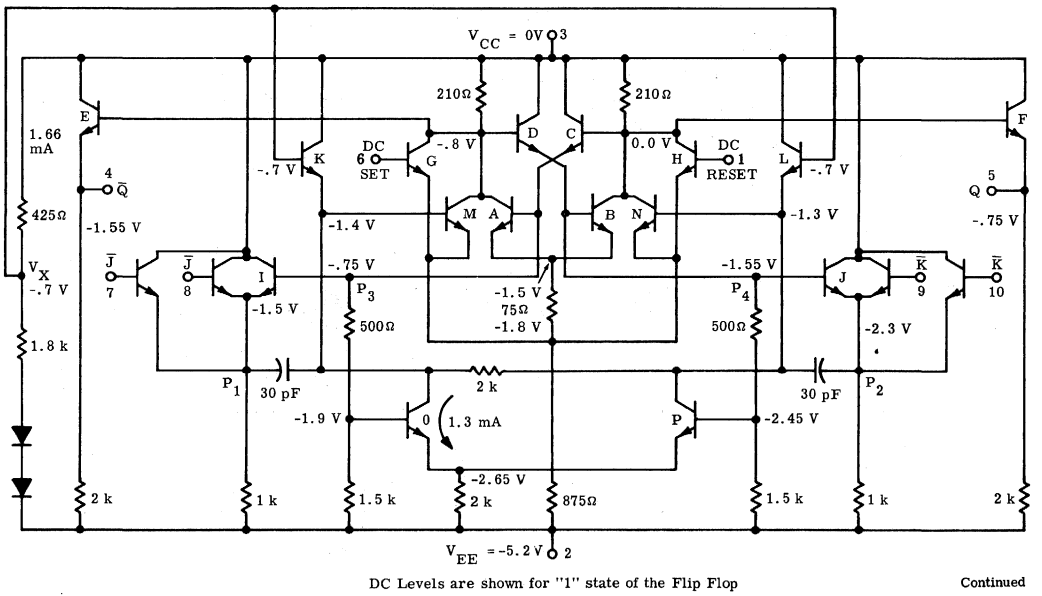
NEGATIVE LOGIC

V_H is defined as logical "0", V_L as logical "1".



The MC313F is available only in the 14-pin flat package due to pin-out limitations of the TO-5 configuration. This multiple function gate may be used to advantage in reducing the can count in a system. Typical power dissipation is 125 mW. Nominal propagation delay time is 7 ns, with a rise time of 6 ns and a fall time of 7.5 ns. The built-in bias driver not only saves a pin but effectively adds to the noise immunity because it sees a fixed load.

J-K FLIP-FLOP, DC R-S; HIGH SPEED, BUFFERED OUTPUTS: MC314, MC364



DC Levels are shown for "1" state of the Flip Flop

Continued

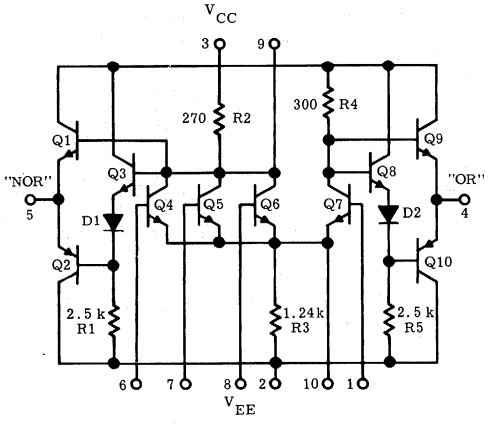
The MC314, MC364 utilizes 20 transistors and two junction capacitors in a high-speed design that guarantees a minimum toggle frequency of 30 MHz at room temperature while typical toggle frequency is 40 MHz at room temperature. Typical characteristics are: power dissipation 115 mW, propagation delay time 12 ns, rise time 13 ns, and fall time 12 ns.

The adjacent schematic shows the nominal D.C. levels for the flip flop in the "1" state, i.e. Q = -0.75 V. Transistors A through H function the same way as in the MC308, MC358A. A and B form the bi-stable element with feedback through D and C. Transistor G sets the flip flop to a "1" while H resets to "0". Transistors E and F buffer the outputs and prevent noise from feeding back into the flip flop from external sources. Transistor I is turned on ensuring that point P_1 is at -1.5 volts. This inhibits a normal MECL $\overline{J}$ input from affecting the state of the flip flop. A high $\overline{J}$ input would have no effect since P_1 is already at -1.5 V.

The K inputs are enabled and a positive going MECL level will couple charge through the 30 pF capacitor and raise the emitter of L to about -0.9 V at which point it is clamped by N which is forward biased and causes the flip flop to change state. As soon as the flip flop changes state, P_4 is raised from -1.55 V to -0.75 V which switches the constant current (1.3 mA) from transistor O to transistor P. This constant current discharges the 30 pF capacitor in about 10 ns. It is seen that the flip flop may be set or reset very soon after a $\overline{J}$ or $\overline{K}$ input has been received due to the rapid discharge of the capacitor. The 30 pF capacitor and the 1 k resistor also form a time constant that requires a minimum down time on a clocking waveform. The 30 ns time constant requires about 8 ns to decay from -1.5 V to -2.3 V with nominal values of R and C. This requires a down time of at least 10 ns at the 10% levels of the clocking waveform. The voltage V_X is internally generated to track with MECL levels over temperature and power supply variations. Transistors K and L are very lightly turned on. One of them, depending upon the state of the flip flop, supplies current for the constant current source employing transistors O and P and the 2 k resistor to V_{EE}. The 2 k resistor between collectors provides a 50 μa pull-down current for either K or L depending upon which is not providing the 1.3 mA discharge current.

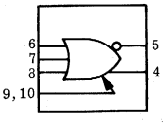
Logically, the MC314, MC364 design is identical with that of the MC308, MC358A. The electrical characteristics have some variations besides maximum toggle frequency. These are illustrated in the section containing MECL flip flop curves.

LINE DRIVER AND CAPACITANCE DRIVER: MC315, MC365



The MC315, MC365 is most useful whenever high speed digital information with little allowed degradation is to be transmitted over long distances without noise pickup. This circuit will drive coax of 50Ω impedance or higher with degradation dependent only upon line losses. Also high values of capacitance may be driven with good rise and fall times.

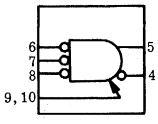
POSITIVE LOGIC - Simultaneous "OR"/"NOR"; V_H is defined as logical "1", V_L as logical "0".



5 = "NOR" = $\overline{6+7+8}$ = $\overline{6}\cdot\overline{7}\cdot\overline{8}$

4 = "OR" = 6+7+8 = $\overline{\overline{6}\cdot\overline{7}\cdot\overline{8}}$

NEGATIVE LOGIC - Simultaneous "AND"/"NAND"; V_H is defined as logical "0", V_L is logical "1".



5 = "NAND" = $\overline{6\cdot7\cdot8}$ = $\overline{6}+\overline{7}+\overline{8}$

4 = "AND" = 6·7·8 = $\overline{\overline{6}+\overline{7}+\overline{8}}$

The gate is a 3-input OR, NOR with bias voltage normally applied to pin 1. Unused inputs must be returned to -5.2 V. The outputs, pins 4 and 5, have active devices to both pull-up and pull-down the load as necessary. For a "1" level output (-0.75 V), the NPN output transistor is turned on giving the low output impedance of an emitter follower to charge any line capacitance. Very low impedance is also provided by the PNP emitter follower to discharge any line capacitance.

Continued

Maximum power dissipation with both outputs loaded to ground with 50Ω is 240 mW, which for maximum reliability requires a case temperature of 125°C maximum rather than 125°C ambient. With only one output loaded, 50Ω to ground, maximum power dissipation is 170 mW. Reducing the single load to 100Ω further decreases dissipation to 110 mW.

For a load of 50Ω and .001μF to ground, the propagation delay is typically 16 ns at room temperature while rise and fall times are about 20 ns. With 50Ω coax terminated in a 50Ω resistor, rise time is typically 15 ns and fall time 20 ns with propagation through the device of about 14 ns.

If the device is used as a capacitance driver, output rise and fall times and propagation delay times depend upon the value of capacitance. Typical curves showing this dependence are drawn below in figures A, B, C, and D. A 10Ω resistor was put in series with the load capacitor to prevent overshoot and ringing on the output waveform. The 10Ω resistor damps the series L-C circuit formed by lead inductance and the lumped capacitance. Without the resistor, overshoot may be about 300 mV depending upon the size of the capacitor. More information on driving lines from MECL outputs may be found in application note AN-187.

Figure E illustrates graphically definitions for rise, fall, and delay times.

For gate loaded 50Ω to ground with variable capacitance in parallel, figures F and G show output rise, fall, and delay times.

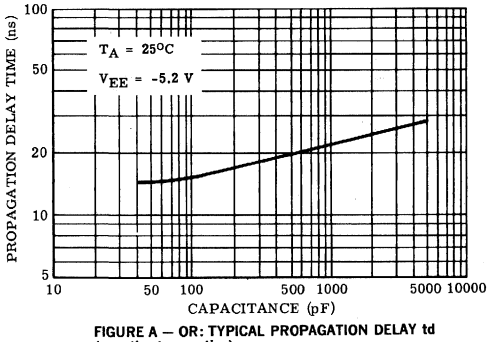


FIGURE A — OR: TYPICAL PROPAGATION DELAY t_d (negative to negative)

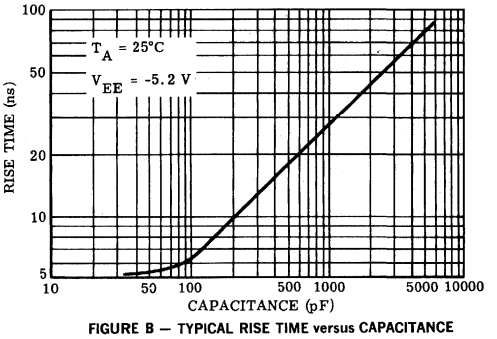


FIGURE B — TYPICAL RISE TIME versus CAPACITANCE

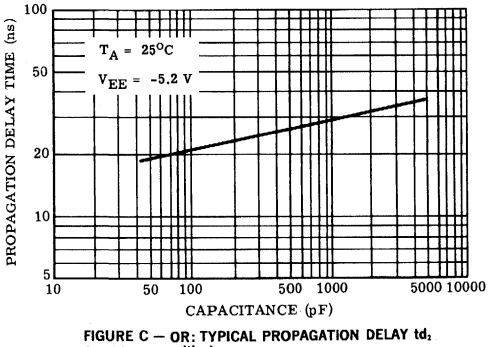


FIGURE C — OR: TYPICAL PROPAGATION DELAY t_{d_2} (positive to positive)

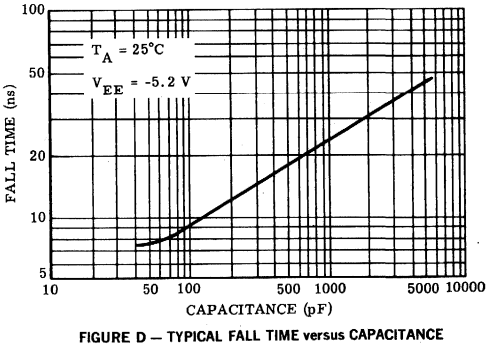


FIGURE D — TYPICAL FALL TIME versus CAPACITANCE

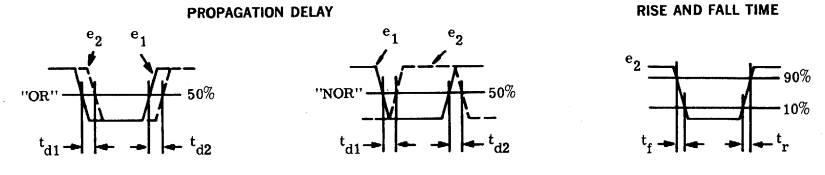


FIGURE E — RISE, FALL AND DELAY INTERVALS

Continued

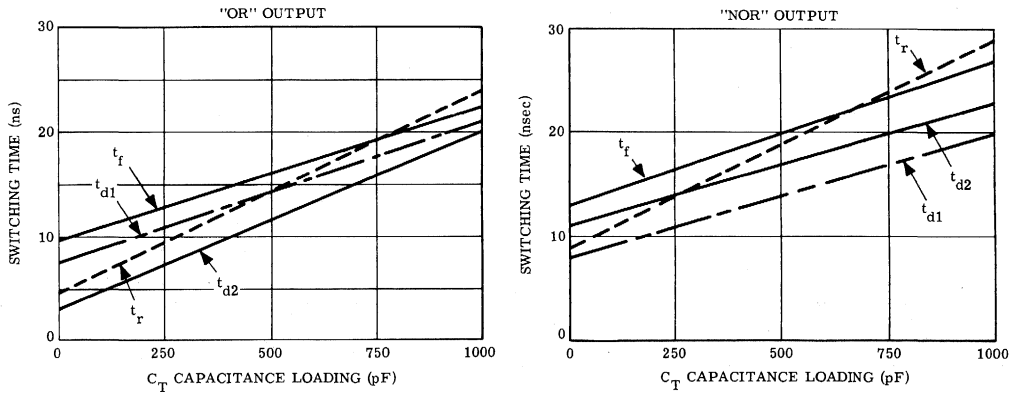


FIGURE F — SWITCHING CHARACTERISTICS OF MC315, MC365

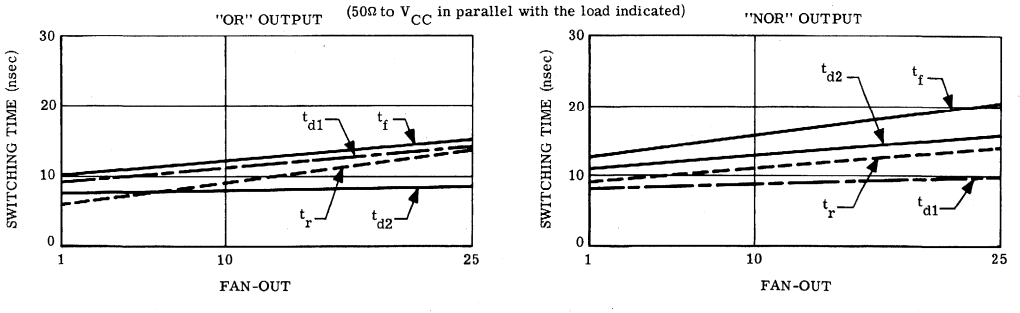
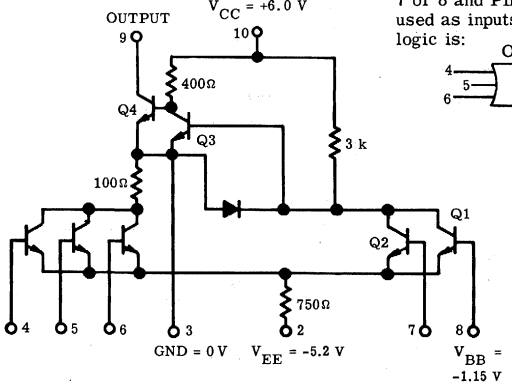
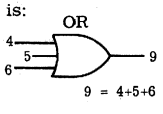


FIGURE G — TYPICAL SWITCHING CHARACTERISTICS OF MC315, MC365

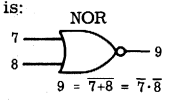
LAMP DRIVER: MC316, MC366



When V_{BB} is applied to PINS 7 or 8 and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



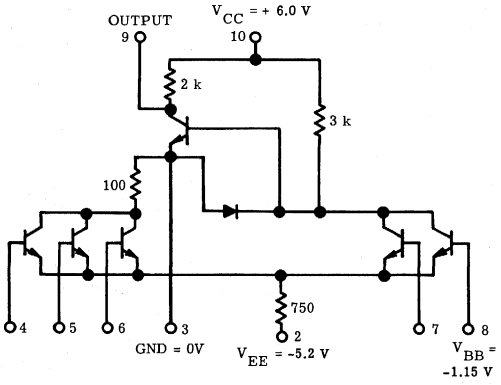
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



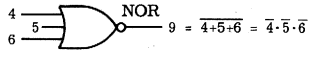
The Lamp Driver operation is the same as that of a regular gate except for the output circuitry which presents saturated logic levels. The current through the 3 k resistor is either switched through the base of Q_3 or transistors Q_1 and Q_2. Q_4, the output transistor, may then be used to turn an indicator light on or off. The diode becomes useful if the gate is to be used as a high speed switch by preventing saturation of Q_1 and Q_2.

Q_4 will sink a maximum of 100 mA at 25°C and 50 mA at 125°C. The maximum V_{sat} is 1.0 V at 100 mA. Typical V_{sat} is 0.75 V at 100 mA with a V_{CC} of 4 V to 6 V. Maximum power dissipation is 235 mW at 6 V and 100 mA sink current.

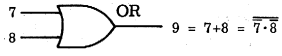
LEVEL TRANSLATOR MECL TO DTL: MC317, MC367



When V_{BB} is applied to PINS 7 or 8, and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



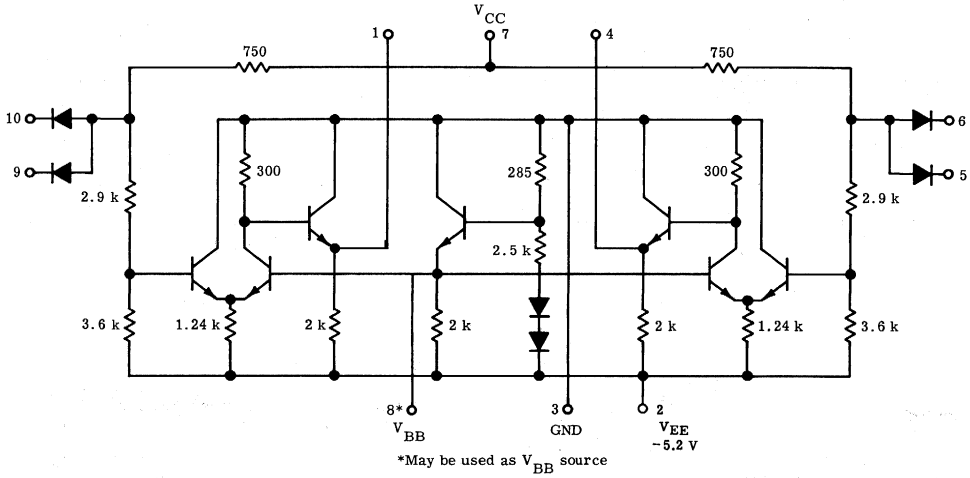
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



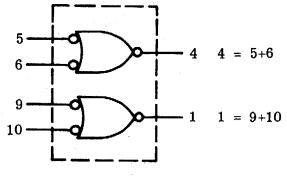
The primary function of this gate is to act as a high speed interface between MECL logic levels and those of saturated logic. Operation is identical to that of the MC316, MC366 Lamp Driver except for the elimination of the output driver transistor.

Maximum saturation voltage of 0.45 V at 25°C is specified for a sink current of 10 mA, while typical V_{sat} is 0.25 V. The output voltage at no load is essentially V_{CC}. Turn on and turn off times are a maximum of 30 ns and 35 ns respectively while worst case power dissipation is 75 mW over the full temperature range.

LEVEL TRANSLATOR DTL TO MECL: MC318, MC368



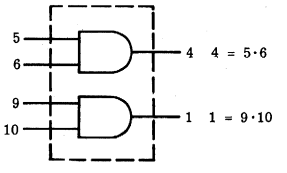
NEGATIVE LOGIC



LOGIC SPECIFICATION

By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at -1.55 V and logical "1" at -0.75 V.

POSITIVE LOGIC

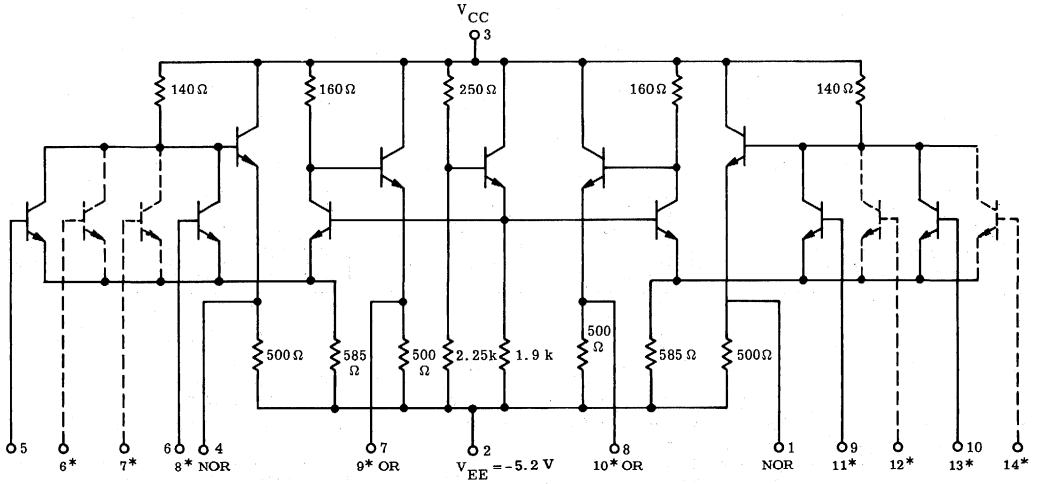


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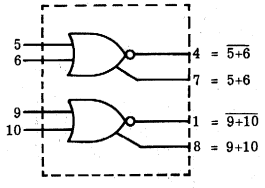
This device is used wherever a high-speed level translator from saturated logic to MECL is required. Turn on and turn off times are about 15 ns with output rise time and fall time nominally 7.5 ns. Maximum power dissipation is 120 mW over the temperature range. The saturated logic input levels should switch from about +0.5 V to + 5.0 or + 6.0 V for the above specifications.

The dual translator operation is as follows: If inputs 5 and 6 are high, the logic input of the respective MECL gate receives a high level through the voltage divider. The OR output of the first MECL gate on pin 4 will then go high. The second translator functions in the same manner for inputs on pins 9 and 10 and an output on pin 1. The device contains a built-in bias driver that compensates for voltage and temperature variations. This reference voltage is available to drive additional gates. A maximum fan-out of 23 is available. Both translators perform the positive AND logic function.

MC369G DUAL-2 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE
MC369F DUAL-4 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE

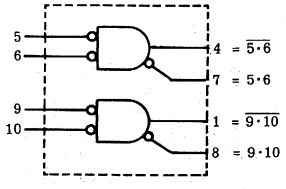


POSITIVE LOGIC
V_H is defined as logical "1", V_L as logical "0".



MD369G

NEGATIVE LOGIC
V_H is defined as logical "0", V_L as logical "1".



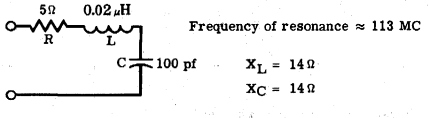
MD369F

The Clock Driver is a very low output impedance device (about 5Ω) and exhibits very fast rise and fall times. Because of its low output impedance and fast rise times, precautions must be taken to reduce ringing in circuits employing the device. The device will fan-out to one or two flip flops ($\overline{J}$ and $\overline{K}$ tied together) with a typical rise time of less than 4 ns. Also, a fan-out to 20 flip flops may be achieved with typical rise times of less than 9 ns.

Operation of the gate is the same as a standard MECL gate with the exception of lower resistance values and higher power dissipation. Typical characteristics at a fan-out of 10 MECL gate loads are: rise time 4.0 ns, fall time 5.0 ns, propagation delay time 5 ns, and power dissipation 240 mW.

Continued

Considering that in a clock driver application, a flip flop may be inhibited with a minimum "1" level and that overshoot may appear on a maximum "1" level clock, worst case allowable overshoot is only 100 mV over the temperature range. For room temperature applications overshoot should be limited to 150 mV. If a lumped capacitance load is added to the clock driver output, overshoot and ringing will be noted. The following is a simplified equivalent circuit for the clock driver output where: R = incremental output impedance of the emitter follower. L = the inductance of 1" of wire. C = the capacitance of 10 flip flop inputs with $\overline{J}$ and $\overline{K}$ tied together.



Frequency of resonance ≈ 113 MC

X_L = 14Ω

X_C = 14Ω

This represents an underdamped series R-L-C circuit and overshoot will be a problem when a step function is applied to the input of the circuit. The following method has been found satisfactory for reducing overshoot to 100 mV or less: (1) Keep the output lead of the device as short as possible, (2) Tap off from the output lead with a resistor of appropriate value to each input being clocked, (3) Keep all devices being clocked as close as possible to the clock driver, (4) If overshoot is still a problem, it may be reduced by 30% to 50% by paralleling two outputs, i.e. two OR's or two NOR's from the same can. This reduces by half the current flowing through an output lead.

The following data in the table are given as a guideline for selecting the proper resistor to be used in series with each flip flop input. Power supplies were bipassed to ground and all loading flip flops were kept within 3 inches of the clock driver.

TABLE OF OVERSHOOT AND RISE-TIME

VS. RESISTANCE AND FAN-OUT

FO = 1 R = 0Ω

S		P	
OS	t_r	OS	t_r
50 mV	3.4 ns	25 mV	3.4 ns

FO = 2 R = 0Ω

S		P	
OS	t_r	OS	t_r
115 mV	3.4 ns	70 mV	3.4 ns

FO = 3 R = 0Ω

S		P	
OS	t_r	OS	t_r
175 mV	3.5 ns	105 mV	3.4 ns

FO = 5 R = 200Ω

S		P	
OS	t_r	OS	t_r
120 mV	5.5 ns	95 mV	5.5 ns

FO = 10 R = 200Ω

S		P	
OS	t_r	OS	t_r
180 mV	5.9 ns	140 mV	5.6 ns

FO = 10 R = 330Ω

S		P	
OS	t_r	OS	t_r
100 mV	7.1 ns	75 mV	6.9 ns

FO = 15 R = 330Ω

S		P	
OS	t_r	OS	t_r
135 mV	7.3 ns	100 mV	7.1 ns

FO = 10 R = 470Ω

S		P	
OS	t_r	OS	t_r
50 mV	8.4 ns	40 mV	8.4 ns

FO = 20 R = 470Ω

S		P	
OS	t_r	OS	t_r
100 mV	8.6 ns	70 mV	8.3 ns

FO = fan-out of clocked flip-flops

S = single gate output

P = paralleled gate outputs (from same can)

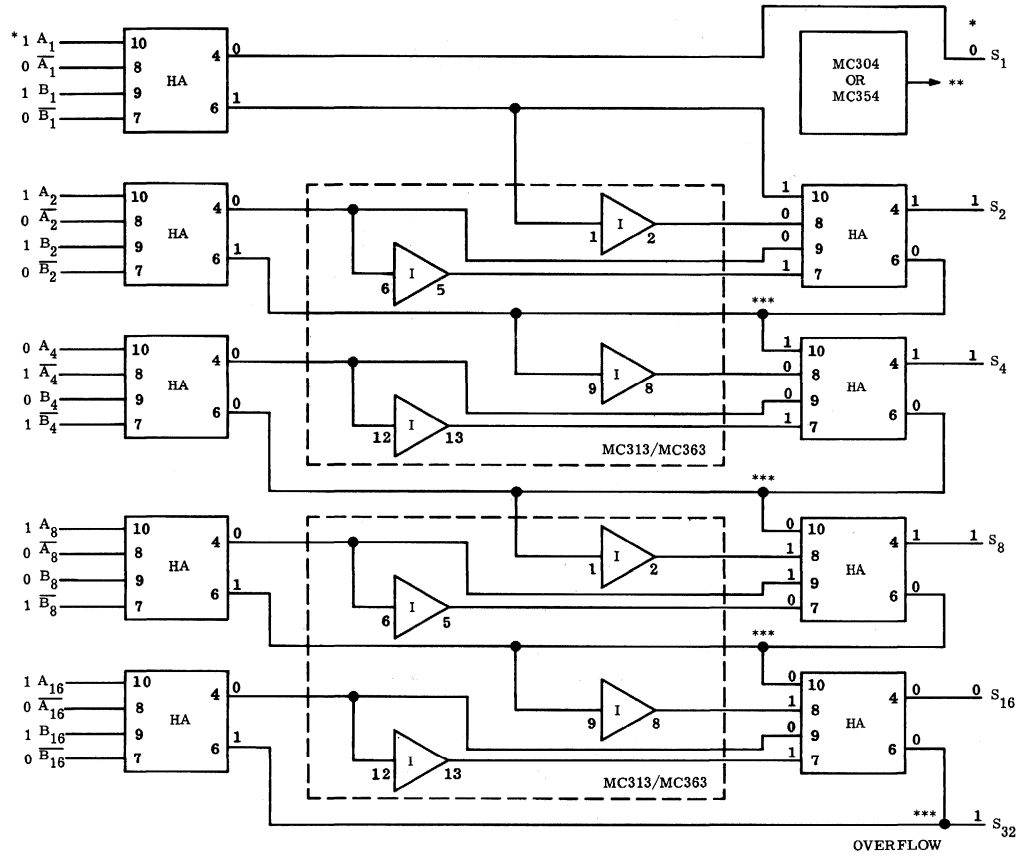
OS = overshoot in millivolts

t_r = rise-time in nanoseconds at input to a flip-flop

MECL SYSTEM APPLICATIONS

This section of sample applications of MECL is included to illustrate the use and versatility of this family. Note the short propagation times obtained. Also additional gates are saved by using the wired-OR feature of MECL.

MECL ASYNCHRONOUS PARALLEL FIVE BIT ADDER



The table illustrates the addition of two 5 bit binary numbers. The subscripts give the decimal equivalent weights of the binary bits. Logic levels for the example are shown in the logic diagram.

TYPICAL EXAMPLE

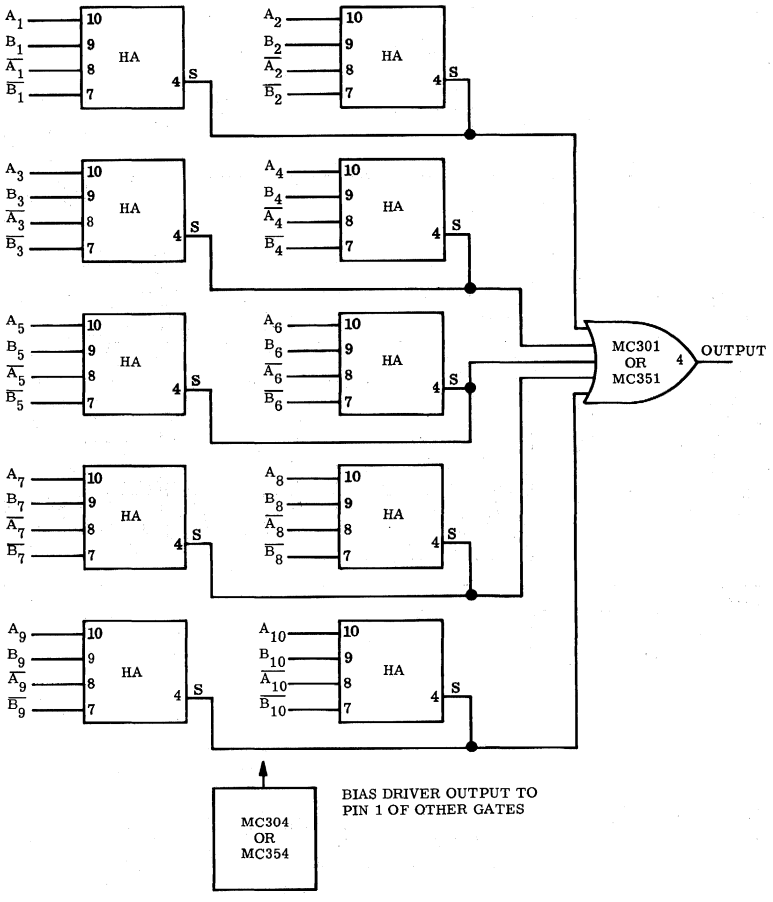
"A" AUGEND		"B" ADDEND		"S" SUM		"C" CARRY	
A_1	1	B_1	1	S_1	0	C_1	1
A_2	1	B_2	1	S_2	1	C_2	1
A_4	0	B_4	0	S_4	1	C_4	0
A_8	1	B_8	0	S_8	1	C_8	0
A_{16}	1	B_{16}	1	S_{16}	0	C_{16}	1

DEFINITIONS:
HA = Half Adder MC303 or MC353. A logical "1" is defined as a relatively high level (-.75 V). A logical "0" is defined as a relatively low level (-1.55 V).

NOTE: The inverters are obtained from 2-quad two-input gates. If desired, 4-dual two-input gates may be used instead of the 14-pin MC313/MC363.
"Can Count" = 9 Half Adders, 2 Quad 2-input gates, 1 Bias Driver = 12 "cans".
The 5-bit adder requires 9 gate delays for a carry to ripple through from the first Half Adder to the overflow output. The total propagation delay time is approximately 60 ns.

*Logic Levels are for the example shown in the table.
**The Bias Driver connects to each gate requiring external bias.
***Outputs are wire OR'd together.

ASYNCHRONOUS 10-BIT MECL COMPARATOR
(Employing the HALF-ADDER as an exclusive OR)



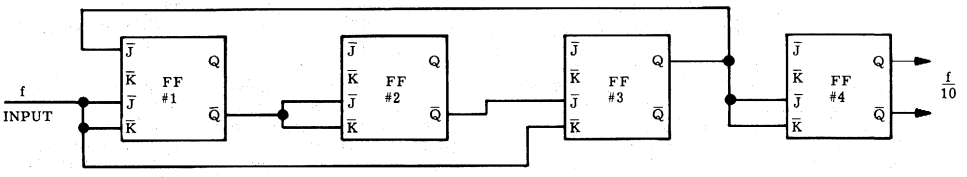
HALF ADDER Truth Table

Pin #	A	B	$\overline{A}$	$\overline{B}$	OUT
	10	9	8	7	4
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

This circuit employing only 12 devices indicates asynchronously whether or not the data from two sources (A and B) agree. If any one of the Half Adder gates (HA) has a pair of input bits that are different, the gate will have a high level output. The Half Adders are wire-OR'd together two at a time resulting in five outputs which drive a 5-input OR gate. The circuit output will be high if any datum from source A disagrees with the corresponding datum from source B.

The circuit has many uses such as enabling the step counting of a register until its output agrees with a given input. Total propagation delay time from input to output is approximately 15 ns. This high speed is an important asset in fast analog to digital conversion. As many bits as desired may be compared with similar propagation delay time by wire OR'ing the output of another 5-input OR with the one shown or by using an expandable gate instead of an MC301 or MC351.

MECL ÷ 10 COUNTER

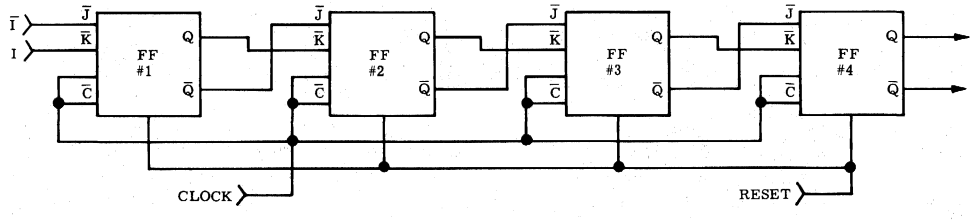


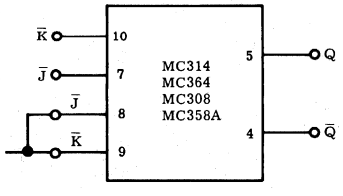
STATE #	FF #1	FF #2	FF #3	FF #4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	1
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	0
10	0	0	0	0

NOTE:
1. A positive going $\overline{J}$, all other inputs to FF low, sets FF to "1".
2. A positive going $\overline{K}$, all other inputs to FF low, sets FF to "0".
3. In going from state 4 to 5, the "1" from FF 3 is fed back to the $\overline{J}$ input of FF 1 while the clock waveform is still high and inhibiting the flip flop. If the up-time of the clock is too short, the $\overline{J}$ input may set FF 1 to the "1" state causing an error.
4. FF 2 and 4 are connected in the toggle mode and simply divide by two.

The main advantage of MECL counters (besides speed), is that any desired count may be obtained without additional gates. The maximum input frequency (f) of the configuration shown is about 15 MHz, without selection of units. If MC314, MC364 flip flops are used and FF 4 is put first in the chain (yielding f/2); inputs of 30 MHz may be employed. The output in the second case is not symmetrical which may be a disadvantage. Further information on counters both clocked and asynchronous may be found in AN-194 and AN-257.

MECL 4-BIT SHIFT REGISTER





CLOCKED JK OPERATION

FLIP FLOP Truth Table

INPUT STATE	$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
	ø	ø	0	Q^n
1	0	0	1	$\overline{Q^n}$
2	0	1	1	1
3	1	0	1	0
4	1	1	1	Q^n

continued

Information received in a shift register will normally be of input state 2 or 3 as shown in the truth table, i.e. inputs of opposite levels. It is seen from the table that the level of the $\overline{K}$ input will be stored in the flip flop, after a dynamic clock, and appear at the Q output. After the first flip flop in the shift register, changes state, the $\overline{J}$ and $\overline{K}$ inputs of the second receive their data. Since the "up time" of a clock waveform is longer than the propagation delay time of a flip flop, a following flip flop is inhibited while the $\overline{J}$ and $\overline{K}$ inputs may be changing levels. Since propagation delay is of no importance, it appears that the maximum shift frequency is the same as the maximum toggle frequency. This is almost true with one exception: If the zero level from the previous flip flop into the $\overline{J}$ or $\overline{K}$ input is more positive than the zero level of the clocking waveform, then a small portion of the clock waveform will be inhibited. This reduces the effective amplitude of the clock. (Note the schematic of one of the flip flops shown previously.) Since maximum toggle frequency depends upon clock amplitude, a reduction in typical operating speed for a given flip flop may be seen. For good clock waveforms and amplitudes, shift frequency is essentially the same as minimum guaranteed toggle frequency.

The Reset input may be used to set every stage to zero if desired, or a combination of Set and Reset inputs may be used to obtain a given count prior to shifting. If the D.C. Set or Reset input is at a high level when the clock also goes high, an undesirable voltage spike will be transmitted to the flip flop output. Therefore, a flip flop should only be Set or Reset at other than clocking time, preferrably when the clock is high.

Another application of the shift register is that of a digital delay. A bit delay of n clock pulses may be obtained between the input and output of a shift register containing n flip flops. Also the output of a shift register may be fed back to the input to form a ring counter. One bit may be inserted in a ring counter and recirculated to form a simple bit time generator for clocking computer decisions.

MECL 70 MHz J-K FLIP-FLOP

INTRODUCTION

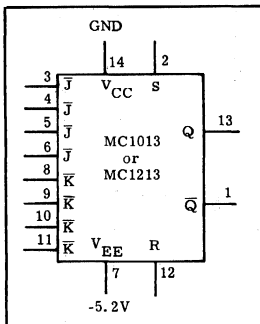
This note presents a thorough characterization of the MC1013/MC1213 $\overline{J}$-$\overline{K}$ flip-flop, which is a member of the new High Speed MECL II family. Both typical and worst case data for system design are given. The flip-flop is versatile in logic designs since four $\overline{J}$ and $\overline{K}$ inputs are provided. The typical operating speed of 85 MHz permits many high speed applications that were only possible with discrete components.

Figure 1 presents the truth tables and pin layouts for the flip-flop. The device is available in the dual in-line 14-pin plastic package (0°C to 75°C) and the 1/4" X 1/4" 14-pin ceramic flat package (-55°C to 125°C). Figure 2 is the device schematic with nominal resistor values. Circuit operation is the same as explained in AN-244 for the MC314/MC364 flip-flop.

The desired input levels are those of a standard MECL gate (see AN-244) i.e., a nominal voltage swing of 800 mV from -.75V to -1.55V at 25°C. Since capacitive coupling is internally employed, the device will accept large variations from the nominal values. In fact, 10 to 20 MHz may be added to the typical toggle frequency at 25°C by "overdriving" the clocked or toggle input with a 1.2V signal between the levels of about -0.4V and -1.6V and keeping the rise and fall times to 2 ns or less.

Figure 3 is the recommended circuit for driving the flip-flop from a pulse generator. For optimum performance, the lead length into and out of the 2N3959 must be kept short to prevent excessive overshoot. The 2N3959 is a 1.8 GHz device and gives good performance down to 1 ns rise and fall times. Output impedance is less than 20 Ω. This circuit closely approximates the output of the MC1023 clock driver which will be available in the first quarter of 1967. The MC1023 exhibits a typical rise time of 2.0 ns and fall time of 3.0 ns at a fanout of 10 (5 $\overline{J}$-$\overline{K}$ pairs) where lead lengths are kept to one inch or less. Each $\overline{J}$-$\overline{K}$ pair should have a separate input lead to the clock driver output if point to point wiring is used.

Other devices in the MECL family will also drive the MC1013/MC1213 satisfactorily at slower risetimes, resulting in slightly lower operating frequencies. The MC369G, MC1050, MC1051, MC1052, all exhibit typical risetimes of 4.0 ns and fall times of 5 ns at a fanout of 5 clocked flip-flops. The flip-flop itself makes a satisfactory driver with a typical output impedance of 15 Ω, risetime of 4 ns, and fall time of 5 ns at a small fanout.



R-S Truth Table

Pin #	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N. D.

ALL $\overline{J}$-$\overline{K}$ INPUTS ARE STATIC

Clocked $\overline{J}$-$\overline{K}$ Truth Table

Pin #	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	Q^n
	-	1	1	1
	1	0	1	0
	1	1	1	Q^n

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

$\overline{J}_D$-$\overline{K}_D$ Truth Table

Pin #	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

NOTES

1. N. D. stands for NOT DEFINED
2. *Any one of the $\overline{J}$ or $\overline{K}$ inputs may be used.
3. **Any $\overline{J}$ and $\overline{K}$ inputs may be tied together to form C_D eg. pins 6 and 8
4. -0.75V nominal is defined as a logic "1" or high level and -1.55V nominal is defined as a logic "0" or low level. $\overline{J}$ and $\overline{K}$ refer to static levels while $\overline{J}_D$, $\overline{K}_D$, C_D refer to dynamic positive-going transitions for a "1".
   A high level on a $\overline{J}$ input inhibits the flip-flop from being set by a $\overline{J}_D$ input. Likewise a "1" level on a $\overline{K}$ inhibits a $\overline{K}_D$ from resetting the flip-flop. The $\overline{J}$ and $\overline{K}$ inputs perform the "OR" function in preventing a $\overline{J}_D$ or $\overline{K}_D$ from setting or resetting the flip-flop.

FIGURE 1 — MECL II J-K FLIP FLOP LOGIC DIAGRAM AND TRUTH TABLES

MC1013/MC1213 CHARACTERISTICS

The following curves are most useful in describing the various parameters of the flip-flop under different operating conditions. The worst case data shown is conservative and may be used for system design purposes. If good system layout techniques are employed, the worst case system data observed will be better than that shown in the graphs. Poor system layout such as long inductive leads, high lumped values of capacitance, and unnecessarily large fanouts can reduce the typical operating speed considerably below 70 MHz.

Figure 4 illustrates the typical and worst case toggle frequency (or divide-by-two parameter) of the flip-flop. The guaranteed minimum toggle frequency of 70 MHz at 25 C is internally guard-banded by the manufacturer to prevent correlation problems with the customer. The toggle test is run with the circuit shown in Figure 3 with 800 mV input amplitude, less than 2.0 ns rise and fall times and a duty cycle of 50%. This test also assures a minimum allowed down and up time of 7.0 ns for the clocking waveform at 25°C (measured at the 50% levels). The worst case down or up time over the full temperature range is 9.0 ns. This corresponds to a worst case toggle frequency of 55 MHz at 125°C. The loading on the flip-flop has a negligible effect upon toggle frequency due to the emitter followers that isolate the flip-flop from the load. With the test input as stated above, a small percentage of the devices will toggle at 100 MHz. Slower rise and fall times will reduce this maximum frequency of operation. It should be noted that

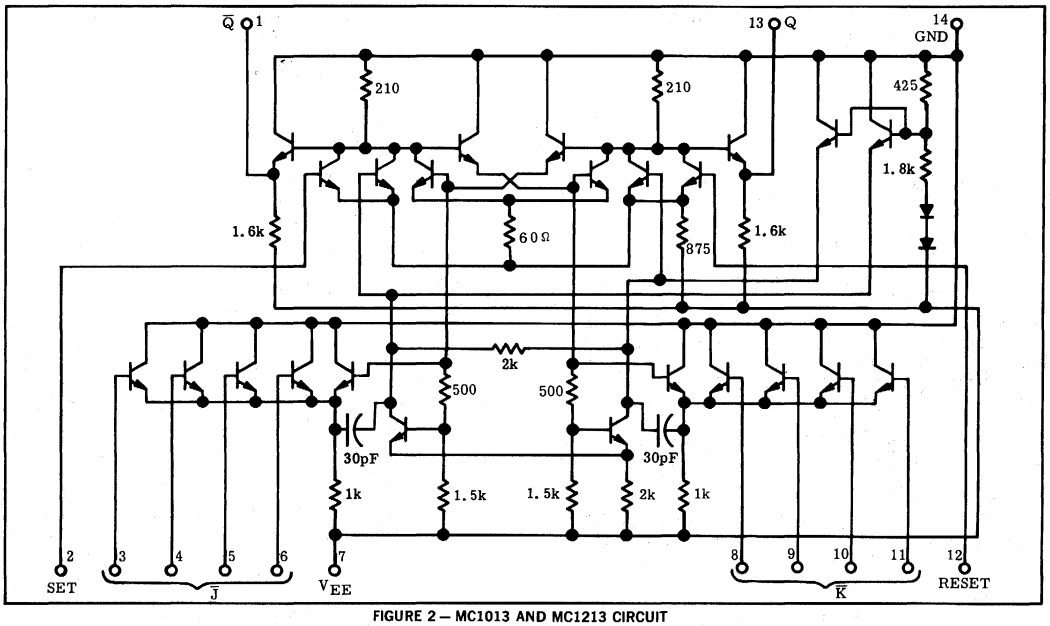


FIGURE 2 — MC1013 AND MC1213 CIRCUIT

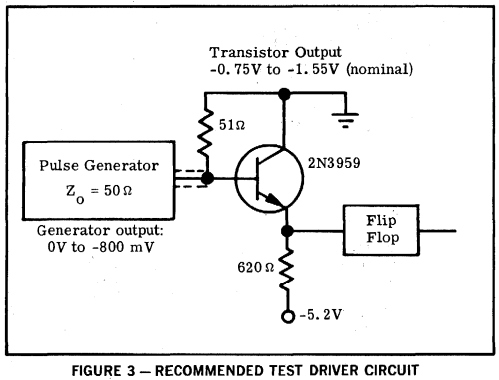


FIGURE 3 — RECOMMENDED TEST DRIVER CIRCUIT

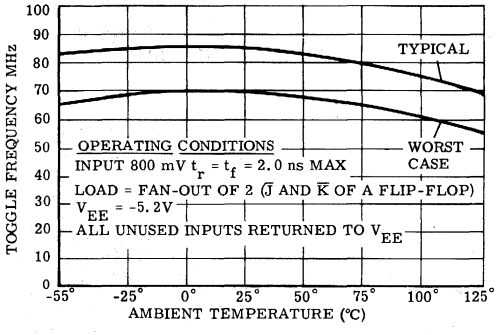


FIGURE 4 — TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

a gate with 4 ns rise and fall times can do no better than a sine wave at 90 MHz.

The typical toggle frequency vs. V_{EE} curve, shown in Figure 5, illustrates the versatility of the MECL design that exhibits common mode rejection of V_{EE} supply variations. Toggle frequency changes very little for ±20% variations in supply voltage. The flip-flop appears as a nominal 215Ω resistive load to the power supply. Therefore, power dissipation is proportional to the square of V_{EE}. At a V_{EE} of -4V, power dissipation drops to a nominal 75 mW. At least 90% of the flip-flops will drive another device with V_{EE} varying from -3.0V to -8V at 25°C.

The minimum input amplitude required to toggle or clock the flip-flop at a given rise time is an important parameter. This measure of sensitivity varies with input rise time as shown in Figure 6. All flip-flops exhibit a slope of about 7.3 mV per ns as is shown for the typical flip-flop. The maximum variation in slope is ±20% which permits worst case design points to be guaranteed by the specification points shown in Figure 6. The worst case limit lines (for least sensitive devices and most sensitive devices) are obtained by changing the slope from that of the nominal flip-flop and leaving a guard-band that insures validity over the full temperature range. (See Figure 13 "Typical Sensitivity Variation VS. Temperature"). The specification points, tested on 100% of the devices, are: the flip-flop must not toggle on 300 mV input at 5.0 ns rise time and the flip-flop must toggle at 600 mV input at 20 ns rise time. These points are guard-banded to prevent any correlation problems. The worst case design points are: An input of 800 mV and greater than 100 ns rise time will not toggle the flip-flop. An input of 800 mV and less than 40 ns rise time will toggle the flip-flop. An input of 250 mV will not toggle the flip-flop, even at 0 ns rise time. These worst case values hold for the full temperature range of -55°C to 125°C.

Figure 7 illustrates typical and worst case propagation delay, rise, and fall times for a fanout of one clocked flip-flop (J and K tied together). The worst case curves are conservative and, therefore, recommended for system design at a fanout of two. t_{pd+-} stands for the propagation delay through the flip-flop from 50% of the positive going clock input to 50% of the negative going output. t_{pd++} is measured from 50% of the positive going clock input to 50% of a positive going output. All clock inputs and outputs are symmetrical and the results are the same regardless of which inputs or outputs are used in the measurements.

The typical and worst case delay, rise, and fall times vs. fanout of MC1000/MC1200 series gates are given in Figure 8. The MECL II gates exhibit less input capacitance than the MC300/MC350 series of MECL. Worst case data for 0°C and -55°C should be taken as the same as that shown for 25°C. Typically these values are slightly better than those shown at 25°C.

The minimum time to toggle after the flip-flop has been set or reset is shown in Figure 9. Worst case data are: width of the set/reset pulse 6 ns minimum, width of the $\overline{K}/\overline{J}$ pulse 8 ns minimum, and the minimum spacing is 8 ns between the falling edge of the set/reset pulse and the rising edge of the $\overline{K}/\overline{J}$ pulse. Times are measured from the 50% portions of all waveforms.

Figure 10 illustrates the minimum required time to reset/set after a $\overline{J}/\overline{K}$ input has been received. This figure indicates the internal time constants of the flip-flop. Under worst case conditions the flip-flop will reset/set with a minimum pulse width of 10 ns, if the pulse is received 11 ns or more after the $\overline{J}/\overline{K}$ input. The worst case times are approximately 1 ns longer than the worst case propagation delay times (Figure 7).

If the $\overline{J}$-$\overline{K}$ inputs to a flip-flop are spaced far enough apart in time, they will act as set-reset inputs (all other inputs at a low level). While if they are brought close enough together, they will act as a toggle input to the flip-flop. Figure 11 illustrates the minimum required time to insure that the $\overline{K}$ input dominates after a $\overline{J}$ input. If the inputs are closer together (time-wise) than that shown for worst case, the flip-flop may toggle. Time to dominate may go as low as 2.0 ns at -55°C for some devices. Therefore, it is recommended that when it is desired to toggle a device, that the particular $\overline{J}$-$\overline{K}$ inputs be wired together rather than be fed through separate gates.

The "Power Dissipation vs. Temperature" curve (Figure 12) is primarily a measure of the device effective resistance over the temperature range. The worst case values are given for a single device, but values for worst case system design may be moved closer to the typical curve if desired. This is due to the averaging effect of multiple devices. Typically power dissipation changes less than 3 mW from D.C. to the maximum operating frequency of a given device. An unloaded flip-flop actually shows a decrease in power dissipation of about 2 mW from D.C. to above 70 MHz.

The sensitivity variation of a flip-flop (minimum input amplitude to toggle) vs. temperature is almost lost in measurement uncertainties. Typically, variations are well within ±10% which is insignificant in a system. Figure 13 illustrates that the typical device is more sensitive at -55°C than at 125°C. The sensitivity tracks very well with typical output amplitude vs. temperature which is shown in Figure 14.

The sensitivity of a flip-flop changes with supply voltage (V_{EE}) as does the output amplitude. Figures 15 and 16 illustrate the tracking capabilities of sensitivity and output amplitude vs. V_{EE}. It is seen that tracking is very good for ±30% variations in V_{EE}. The higher sensitivity at reduced V_{EE} suggests using the device as an RF amplifier, which also divides the input frequency by two. The effective gain through the flip-flop is typically greater than 2.5 at $V_{CC} = -4.0$ V.

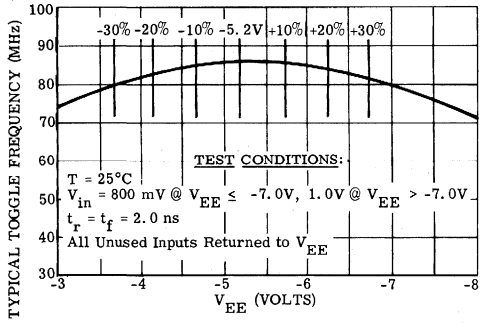


FIGURE 5 — TYPICAL TOGGLE FREQUENCY versus V_{EE}

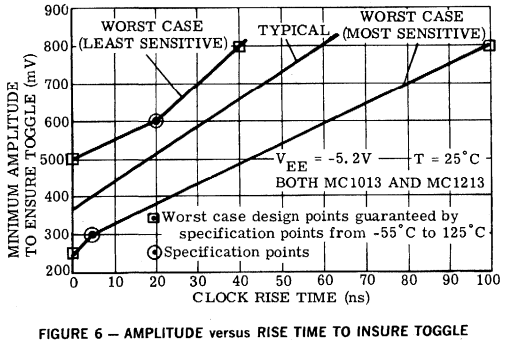
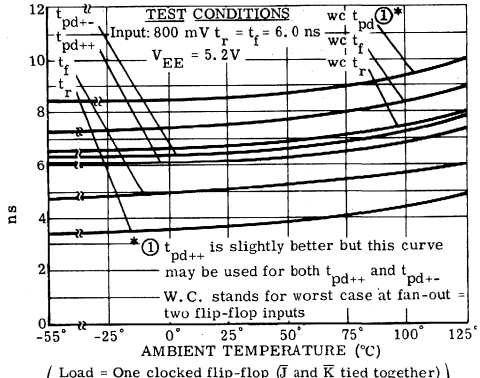


FIGURE 6 — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

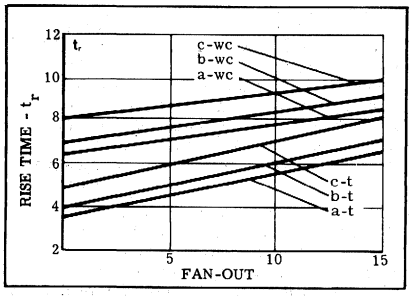
ADDITIONAL FLIP-FLOP CHARACTERISTICS

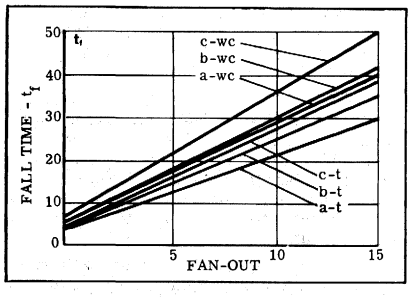
The flip-flop may be set and reset at a rate in excess of 100 MHz. The optimum pulses in this mode of operation are from 4 to 5 ns in width with rise and fall times of less than 2 ns. The MC1013/MC1213 flip-flop exhibits a tighter distribution of parameters than devices in the MC300/MC350 Series. 90% of the devices exhibit less than ±20% variations in propagation delay, rise, and fall times. Also, the maximum toggle frequency varies

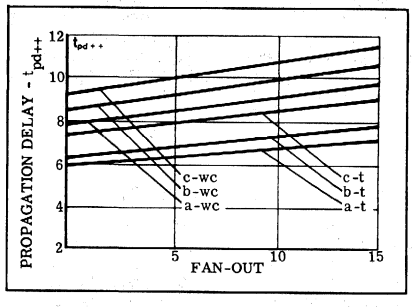


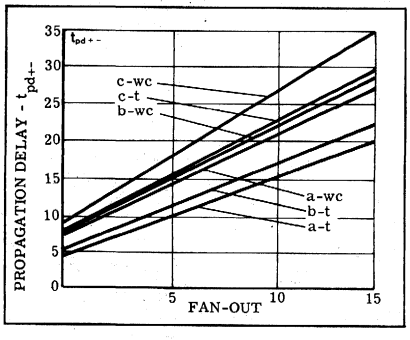
(Load = One clocked flip-flop ($\overline{J}$ and $\overline{K}$ tied together)
All unused inputs are returned to -5.2V)

FIGURE 7 — PROGAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE









INPUT t_r = 5.0 ns — A = 25°C

INPUT AMPLITUDE 800 mV — B = 75°C

V_{EE} = -5.2V — C = 125°C

T = TYPICAL — WC = WORST CASE

FIGURE 8 — PROPAGATION DELAYS, RISE TIME, FALL TIME versus FAN-OUT AND TEMPERATURE

only about ±15% from the nominal value of 85 MHz. Each $\overline{J}$ and $\overline{K}$ input should be considered as a load of one, making a clocked input equivalent to a load of two. The maximum recommended fanout for the flip-flop is 15, above which, fall times become excessive. At low operating frequencies, fanout may be greatly increased if waveform deterioriation is considered in the design. The device has a guaranteed D.C. fanout of 25 which corresponds to a worst case of 2.5 mA load current. The maximum output current that should be drawn from the flip-flop is 10 mA which will decrease the nominal "1" level at no load by about 150 to 200 mV. If the flip-flop is used to drive a gate, the "1" level noise immunity is reduced to about 50 mV under these conditions. At large fanouts, fall time and t_{pd+-} will be decreased if an additional resistor is wired between the output and V_{EE}.

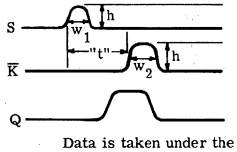
It should be noted that if a DC set or reset input is at a "1" level and the $\overline{J}$-$\overline{K}$ inputs are clocked, that a "glitch" will appear on the outputs. This glitch may be of sufficient amplitude to toggle or clock another flip-flop tied to the Q or $\overline{Q}$ output. This condition is the same as applying both a set and reset input to a current mode R-S flip-flop where both outputs tend to go to a V_{BB} level (half-way between "1" and "0"). This glitch may be minimized by a clock of low amplitude and slow rise time, but good system design eliminates this situation.

The worst case shift frequency depends upon the slowest flip-flop in the shift register. For a shift register without gating, the worst case shift frequency is essentially the same as the worst case toggle frequency of the slowest flip-flop employed in the register. Therefore, the worst case shift frequency is 70 MHz at 25°C and 55 MHz at 125°C.

This flip-flop is most useful in high frequency counters, phase locked loops, frequency synthesizers, special counters, logic designs that require additional $\overline{J}$ and $\overline{K}$ inputs, and high speed registers in the arithmetic portion of digital computers.

SUMMARY

The MC1013/MC1213 flip-flop is a versatile high frequency device that more than doubles the maximum operating frequency of a MECL system. The worst case data given in this note are conservative and, therefore, intended for system design. Due to the high frequencies of operation, performance depends heavily upon system layout. This MECL flip-flop will work best when used with multilayer printed circuit cards where lead lengths have been minimized. This flip-flop is characteristic of MECL II devices which operate in the 5 ns region with typical system loads.



w_1 = 4 ns (optimum)

w_2 = 6 ns (optimum)

h = 800 mV

Data is taken under the following conditions:

S and $\overline{K}$ inputs: $t_r = t_f$ = 1.5 ns

V_{EE} = -5.2V

t = min of 7-10 ns, "t" - w_1 = 3-6 ns min @ 25°C

Worst Case Operation -55°C to 125°C

w_1 = 6 ns min w_2 = 8 ns min "t"-w_1 = 8 ns min

FIGURE 9 — MINIMUM TIME TO TOGGLE AFTER SET OR RESET

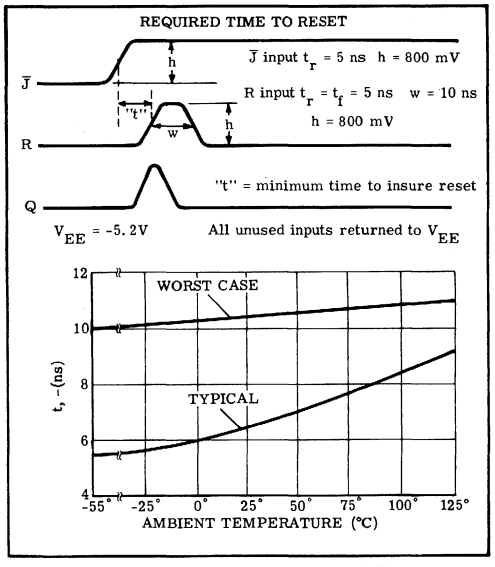


FIGURE 10 — REQUIRED TIME TO RESET

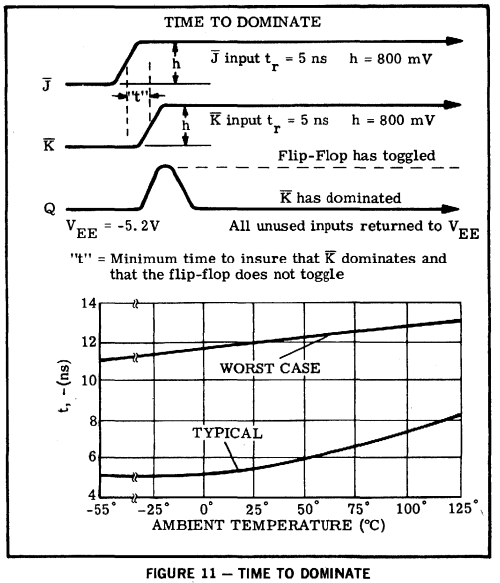


FIGURE 11 — TIME TO DOMINATE

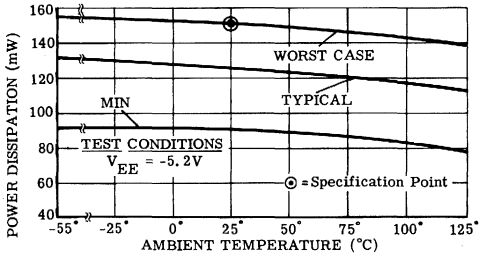


FIGURE 12 — POWER DISSIPATION versus TEMPERATURE

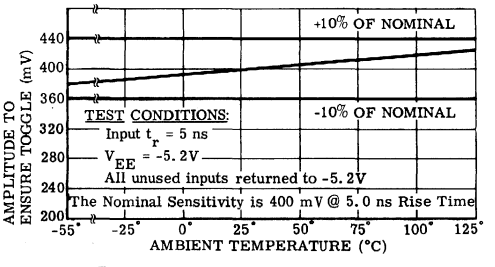


FIGURE 13 — TYPICAL SENSITIVITY VARIATION versus TEMPERATURE

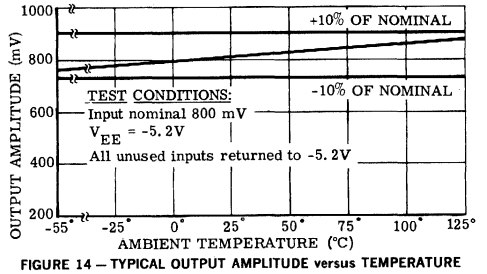


FIGURE 14 — TYPICAL OUTPUT AMPLITUDE versus TEMPERATURE

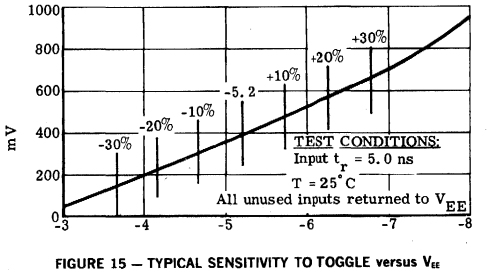


FIGURE 15 — TYPICAL SENSITIVITY TO TOGGLE versus V_{EE}

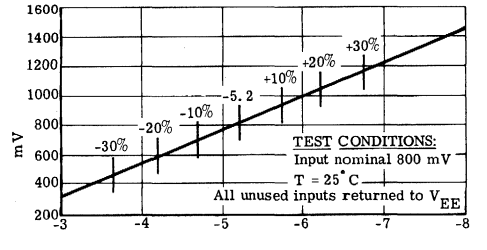


FIGURE 16 — TYPICAL OUTPUT AMPLITUDE versus V_{EE}

USING SHIFT REGISTERS AS PULSE DELAY NETWORKS

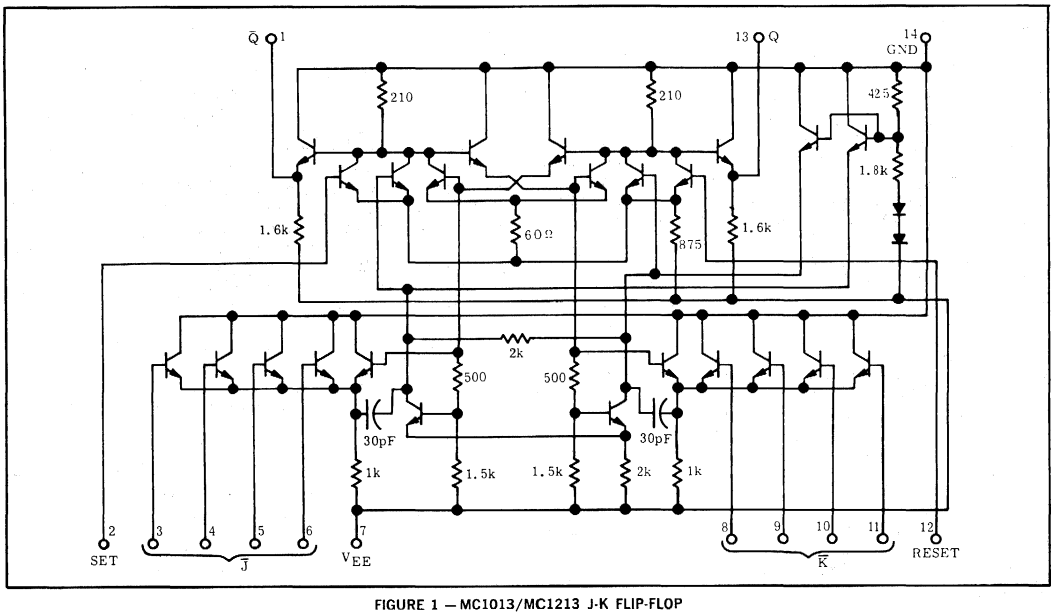
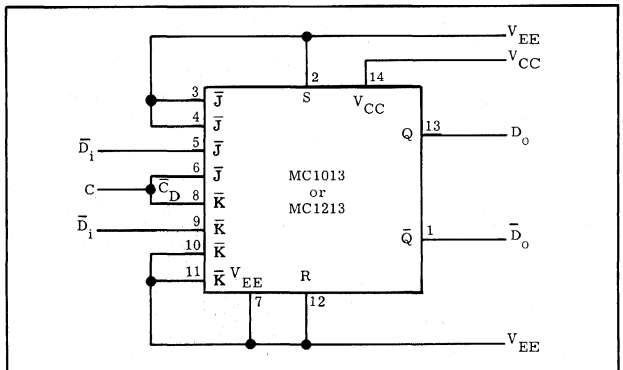


FIGURE 1 — MC1013/MC1213 J-K FLIP-FLOP



V_H = logical "1"
V_L = logical "0"

R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	ND

Q^{n+1} = state of the flip-flop at time = t+1
ND = not defined

J̄	K̄	$\bar{C}_D$	Q^{n+1}
Ø	Ø	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

Note: pin 14 = Gnd = V_{CC}
pin 7 = -5.2V = V_{EE}
all unused inputs are returned to V_{EE}

A relatively high level voltage (-.75V) is defined as a logical "1" while a logical "0" corresponds to (-1.55V). The J̄ and K̄ inputs represent static logic levels while $\bar{C}_D$ refers to a dynamic logic swing. The J̄ or K̄ inputs should be changed to a logic "1" while $\bar{C}_D$ is at a high level; otherwise the J̄ or K̄ signal may clock the flip-flop. Ø = either logic 1 or 0 may be present.

FIGURE 2 — FLIP-FLOP LOGIC BLOCK, J̄-K̄ AND R-S TRUTH TABLES

INTRODUCTION

With the availability of flip-flops that will shift at rates in excess of 70 MHz, high speed shift registers are easily fabricated. These MECL II devices allow a shift register to be employed as a variable digital delay line in many applications. The pulse width degradation and delay errors are shown to amount to uncertainties of a maximum of one clock period for asynchronous inputs. This would amount to 20 ns for a 50 MHz shift register.

The flip-flop used in this application note is the MC1013 (0 to 75°C) or MC1213 (-55 to 125°C). The device is a J̄-K̄ type flip-flop with four J̄ and four K̄ logic inputs, one Reset input, one Set input, and Q-Q̄ outputs. The 70 MHz flip-flop is a member of the MECL II Multifunction family which is available in the dual in-line, 14 pin plastic package (0 to 75°C) and the 14 lead 1/4"×1/4" ceramic flat pack. Flip-flop specifications are: minimum toggle frequency = 70 MHz at 25°C; typical toggle frequency = 85 MHz. Oversensitivity (adequate noise immunity) — the device will not toggle at 5 ns rise time and less than 300 mV input. Adequate sensitivity — the device will toggle at 20 ns rise time and an input greater than 600 mV. The flip-flop will toggle on rise times of 40 ns or less at the nominal input amplitude of 800 mV. Worst case toggle and shift frequency is 55 MHz or better over the full temperature range, -55°to +125°C. Operating voltage is -5.2 V with negligible degradations in characteristics for ±20% variations in supply voltage. Typically rise, fall, and propagation times are from 3.0 to 7.0 ns.

Figure 1 gives the schematic of the MC1013/MC1213 with nominal values of resistance. Circuit operation is the same as explained in AN244 for the MC314/MC364. The only differences are the extra $\overline{J}$ and $\overline{K}$ inputs and improved processing that decreases internal time constants.

Figure 2 illustrates a single flip-flop logic block connected as a single stage of a shift register. The $\overline{J}$-$\overline{K}$ and R-S truth tables are also shown in the figure. For shift register operation, the $\overline{J}$ and $\overline{K}$ inputs are always complements.

DELAY REGISTER OPERATION

Figure 3 is the logical schematic for an "n" bit shift register which includes the necessary logic for electronically controlling the delay of the register in powers of two. The incoming data to be delayed is considered to be asynchronous with the internal clock oscillator and random in nature. The input data (D_I) might appear as shown in Figure 4. The figure illustrates typical waveforms that would result from D_I and a 50 MHz clock.

G_1 is used to split the input into Data (D) and Data Not ($\overline{D}$) since the remaining logic requires complementary data (dual rail logic). The OR and NOR outputs of a gate have essentially the same propagation delay so output skew is no problem. G_2 and G_3 form a logic switch that "switches off" the input data whenever C is low ($\overline{C}$ high). This prevents the undesirable transfer of data into the first $\overline{J}$-$\overline{K}$ flip flop while the clock is at a low level. If the clock input to a $\overline{J}$-$\overline{K}$ flip flop is low, a positive going waveform on $\overline{J}$ would SET the flip flop to the "1" level (Q high) or a positive going waveform on $\overline{K}$ would RESET the flip flop (Q low). This feature is undesirable in this application.

Gates G_4 and G_5 form an R-S flip flop that stores the previous input data while $\overline{C}$ is at a high level. On the positive going transition of C, the data stored in G_4-G_5 is shifted into the first $\overline{J}$-$\overline{K}$ flip flop. The J-K is then inhibited by the high level of the clock. On the positive going edge of C, new data may be started through G_2 and G_3 into G_4-G_5. The input data is delayed through gates G_1 through G_5 and then an additional delay of τ (clock period) as it is shifted through each $\overline{J}$-$\overline{K}$ flip flop.

Figure 4 illustrates several of the possible timing conditions that may occur between D_I and the clock waveforms. For example, D_I is low between time 2.3 and 3.3. This is the longest low level on the input that will not be recognized by the shift register. From the timing diagram, it is seen that if an input is present for longer than the clock period, it will be recognized and shifted through the register. The low level data between 4 and 4.5 is present long enough to be recognized, and is stretched to one clock period in length by the input gating and flip flop #1. Also the positive pulse between time 12 and 12.5 is long enough and in the proper position to be recognized.

The input levels f_0-f_8, shown in the lower portion of Figure 3, allow the selection of the clock frequency $\frac{f}{2^m}$ where m is the number of the flip flops used to divide the basic frequency of the clock oscillator. Inputs f_0-f_8 are negative logic inputs, i.e. only one input should be low at a time. The low input will enable the desired clock frequency. If all inputs go high, the register will store the data that was being shifted in the register.

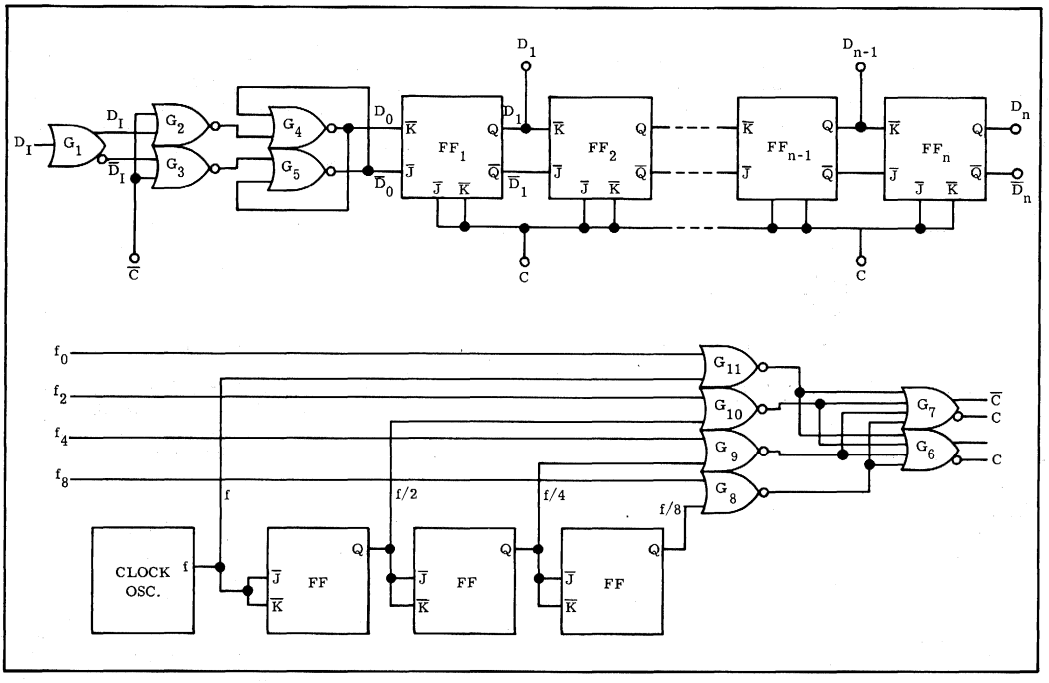


FIGURE 3 — DELAY REGISTER DIAGRAM

The preferred gate for G_1 through G_7 is the MC1023 which is a clock driver and high speed gate. This device exhibits typical propagation delays, rise, and fall times of 2ns. Two clock drivers are shown in Figure 3 where it is assumed that the number of stages in the register is ten or more. The MC1023 is a dual 4-input OR-NOR gate. By using both gates, 10 flip flops may be driven with a typical rise time of 2ns and fall time of 3.0ns. If lead lengths are kept short and low inductance printed circuit wiring employed, the register as shown in Figure 3 will shift at clock rates in excess of 70 MHz at room temperature.

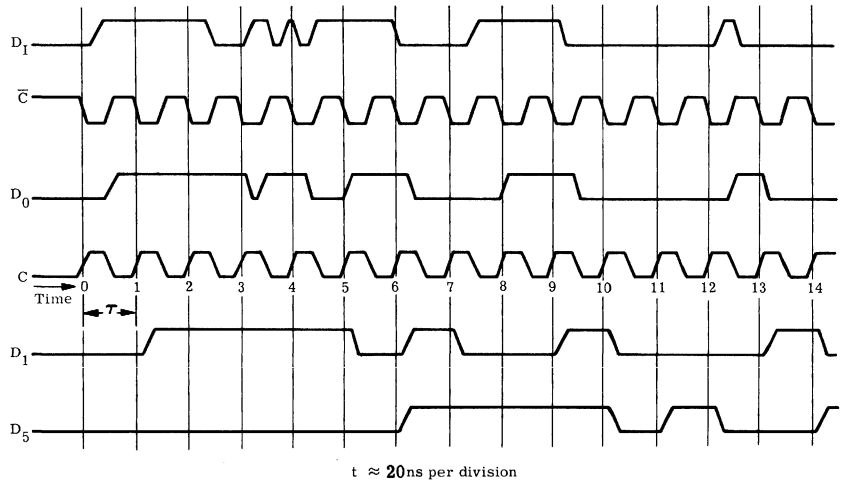
Typically the delay through the input gating using the MC1023 is a minimum of 6ns or a maximum 6ns + $\frac{\tau}{2}$. This amounts to a minimum of 6ns and a maximum of 16ns for a 50 MHz clock, depending upon the relative position of the data and the clock. The delay from D_0 to D_1 is a minimum of $\frac{\tau}{2}$ plus the delay of flip flop 1 or a maximum of τ plus the flip flop delay. For 50 MHz operation, this yields a minimum of 15ns or a maximum of 25ns. The total delay from D_I to D_1 is then a minimum of 21ns or a maximum of 41ns. The incremental delay from flip flop 1 to flip flop 2 is τ and so forth throughout the delay register.

Assuming a 50% duty cycle clock, delay uncertainty of input information is $\pm \frac{\tau}{2}$ and the maximum length of an input datum that may not be recognized is τ. Also an input datum may be lengthened or shortened by as much as τ. The delay of the register shown, using the recommended devices is approximately 11ns + $n\tau \pm \frac{\tau}{2}$, where n is the number of MC1013/MC1213 J-K flip flops between the input and desired output, and τ is the period of the clock waveform.

Further improvement in delay register characteristics may be obtained by using the MC1022 "D" type flip flop. The input is single rail, eliminating the need for G_1. Since the flip flop operates on the master slave principle, gates G_2 through G_5 may also be eliminated. The data input is then brought directly into the flip flop with no additional gating. The delay through a register using the MC1022 is approximately 5ns + $n\tau \pm \frac{\tau}{2}$ where n is the number of "D" flip flops used including the first stage. Typically the "D" type flip flop will operate at greater than 60 MHz allowing values of τ as small as 16.5 ns.

SUMMARY

The MC1013/MC1213 may be used in shift register applications at speeds greater than 50 MHz over the specified temperature range. Incremental delays of 20ns are easily obtained and continuously variable delays are possible with variable clock frequency.



t ≈ 20ns per division

D_1 = Input Data
$\overline{C}$ = Clock to input gating
D_0 = Data into first $\overline{J}$-$\overline{K}$ flip flop
C = Clock to shift register
D_1 = Delayed Data out of first $\overline{J}$-$\overline{K}$ Flip Flop
D_5 = Delayed Data out of fifth $\overline{J}$-$\overline{K}$ Flip Flop

FIGURE 4 — TYPICAL DELAY REGISTER WAVEFORMS FOR A 50 MHz CLOCK FREQUENCY

OVERSHOOT AND RINGING IN HIGH SPEED DIGITAL SYSTEMS

Whenever a switching circuit with low output impedance and fast risetime is used to drive a signal lead that is connected to several gates, overshoot will be present. The term overshoot, as used in this note, is defined as the peak to peak voltage difference between the most positive portion of the rising edge of a waveform and the "1" logic level of the waveform after all transients have decayed. In general, the lower the output impedance of a gate, the faster the risetime, the longer the wiring length, and the larger the fanout, the greater the overshoot caused when switching occurs. This note contains several tables and sets of photographs illustrating the overshoot that can be expected under various worst case configurations and loadings. Methods of overshoot reduction are applied with tabulated results from which general conclusions and guidelines are drawn.

The exact simulation of an integrated circuit load or the loading of several devices is extremely difficult with passive components. This is due to the complex and non-linear input impedance of a MECL device. The input capacitance goes through a peak value of approximately 15pF during a logic transition and averages out to less than 5pF over the entire logic swing. The input resistance will be about 50KΩ (worst case) at a logic "1" level. The input resistance will decrease exponentially if saturation of the MECL input is approached. (A MECL gate may be driven into saturation by sufficient overshoot on the input waveform, especially at high temperatures.) For system design purposes a worst case input capacitance of 5pF per device input and a 50k resistance to V_{EE} may be utilized. If sockets for the gates are used, an additional 1pF should be added per gate input. Wiring capacitance using teflon coated wire is about 1 pF per inch. Inductance per unit length of wire is about 0.02 μH per inch. These values will vary by a large amount depending upon "lead dress" and, therefore, should be considered only as "ball park" figures. When circuit measurements are being made, oscilloscope probe capacitance should be considered. The capacitance of a probe will vary from 1.8pF to about 10pF depending upon the probe design.

Attempts were made to simulate the loading caused by various fan-outs with discrete components. The best simulation was obtained by the following circuit, Figure 1, which will help to explain the parameters affecting overshoot. R_O stands for the output incremental resistance of the gate used as a driver. Values are approximately: MC301--20Ω, MC365--12Ω, MC369--5Ω. L is the series inductance of the signal lead and R_I is the input resistance of the gates used as the load. C is the shunt capacitance caused by the fan-out, wiring capacitance, socket capacitance, and probe capacitance. The value of C is 8-10pF per fan-out. R_D is necessary to damp out excessive overshoot which is caused by the lumped value of C. C is chosen to give rise time equivalent to the measured value for the given fan-out. R_D is on the order of 20Ω with higher values for small fan-out and smaller values for large fan-outs.

This load only simulates overshoot and rise time as can be seen by comparing photographs 2, 8, and 14 with 5, 11, and 17 respectively. The period of oscillation is longer for the simulated load, indicating that the value of C is higher than with the actual load. The effective capacitance of the actual load may be shown to be about 6-7pF per fan-out, i.e. 2-3pF less than in the simulated load. The difference in period of oscillation and damping indicates just how approximate the simulated load is.

How much overshoot can occur under worst case conditions in a MECL system? This question is answered by the data which are shown in the following tables. These data were obtained by using the MC301, MC365, and MC369 gates as drivers. MC356's and MC364's were used as fan-out devices. Lead lengths of 3", 6" and 12" were used with the loads constructed on printed circuit boards and plugged into a single socket which terminated the particular lead. This simulates a worst case situation since fan-out is not usually lumped at the end of a single lead. The devices used as drivers were picked at random and other devices may give somewhat different results due to output impedance and output risetime.

How much overshoot can be tolerated in a MECL system? This question is relatively easy to answer in the case of driving flip-flops, but becomes more difficult when referring to gates. When driving flip-flops, one $\bar{J}$ input may be clocked and the other inhibited at a worst case "1" level. If the level of the clocked J input exceeds the inhibiting level on the other J input by more than the required amplitude to toggle a sensitive flip-flop, then false information may be passed into the flip-flop. For room temperature operation, overshoot should

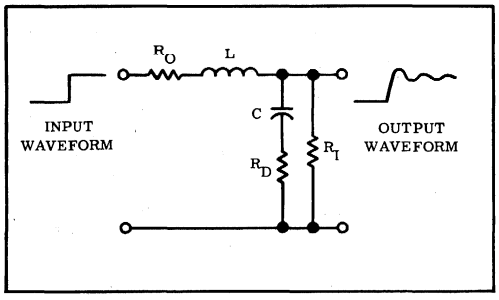


FIGURE 1 — APPROXIMATE EQUIVALENT CIRCUIT

DRIVER GATE	FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	2-MC356	5mV	8.9ns	10mV	7.7ns	50mV	6.8ns
MC301	5-MC356	40mV	9.2ns	60mV	8.5ns	110mV	8.0ns
MC301	10-MC356	90mV	10.9ns	115mV	10.9ns	175mV	11.1ns
MC301	15-MC356	95mV	12.1ns	135mV	12.0ns	200mV	12.3ns
MC365	2-MC356	40mV	6.7ns	70mV	6.2ns	145mV	5.4ns
MC365	5-MC356	80mV	6.9ns	140mV	6.6ns	215mV	6.6ns
MC365	10-MC356	150mV	8.2ns	205mV	8.2ns	270mV	8.4ns
MC365	15-MC356	180mV	9.0ns	220mV	10.0ns	300mV	10.3ns
MC369	2-MC356	80mV	4.2ns	200mV	4.5ns	300mV	4.4ns
MC369	5-MC356	120mV	5.2ns	220mV	5.5ns	330mV	6.3ns
MC369	10-MC356	180mV	7.4ns	220mV	7.7ns	350mV	9.1ns
MC369	15-MC356	200mV	8.9ns	270mV	9.0ns	370mV	9.9ns

TABLE 1 — MEASURED OVERSHOOT AND RISE TIME MC356 AS LOAD

DRIVER GATE	J-K COMMON FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	1-MC364	0mV	7.5ns	0mV	7.8ns	0mV	6.0ns
MC301	2-MC364	45mV	7.5ns	70mV	7.3ns	135mV	7.2ns
MC301	5-MC364	85mV	8.6ns	130mV	8.8ns	200mV	8.8ns
MC301	10-MC364	160mV	12.9ns	190mV	13.0ns	270mV	13.5ns
MC365	1-MC364	0mV	6.7ns	0mV	4.7ns	55mV	4.8ns
MC365	2-MC364	100mV	5.9ns	165mV	5.8ns	250mV	6.0ns
MC365	5-MC364	160mV	6.7ns	210mV	6.9ns	340mV	7.3ns
MC365	10-MC364	180mV	9.9ns	230mV	11.3ns	370mV	11.5ns
MC369	1-MC364	0mV	4.5ns	50mV	4.1ns	280mV	4.1ns
MC369	2-MC364	180mV	4.9ns	280mV	5.0ns	350mV	5.4ns
MC369	5-MC364	250mV	6.0ns	340mV	6.4ns	420mV	6.4ns
MC369	10-MC364	250mV	8.8ns	340mV	9.3ns	440mV	10.1ns

TABLE 2 — MEASURED OVERSHOOT AND RISE TIME MC364 (CLOCKED) AS LOAD

LOADING		MAXIMUM SERIES RESISTANCE (R_S)		
DC FAN-OUT	MAXIMUM EQUIVALENT LOAD CURRENT	STANDARD GATE DRIVER R_O=22	LINE DRIVER MC315/MC365 R_O=15	CLOCK DRIVER MC369 R_O=5
25	2.5mA	0	7	17
15	1.5mA	14	21	31
10	1.0mA	33	40	50
5	0.5mA	88	95	105
3	0.3mA	160	170	180
2	0.2mA	250	260	270
1	0.1mA	530	535	545

NOTE: Worst Case values are calculated from $R_O + R_S = \frac{\Delta V}{\Delta I}$

ΔV = 55mV maximum allowed "1" level voltage change (no load to full load)

ΔI = change in load current (no load to full load) for given fan-out

R_O = incremental output resistance of driver gate

R_S = series resistance added in lead between driver and fan-out

TABLE 3 — MAXIMUM ALLOWED VALUES OF SERIES RESISTANCE VS. FAN-OUT

be less than 150 mV. For worst case design over the full temperature range (-55°C to +125°C), overshoot should be limited to 100 mV or less. Although a regular gate will tolerate far more overshoot than the above-mentioned values, the worst case value of 100 mV should be used in system design. If high overshoot levels occur in a system, problems caused by the cross-coupling of noise from one signal lead to another will be compounded. For example, if 200 mV of overshoot is allowed, a normal transition of 800 mV would be changed to a 1V transition, therefore increasing cross-coupling of noise by 25%.

It is obvious that the worst case values of overshoot shown in Tables 1 and 2 are excessive. How then can overshoot be reduced? It can be seen from the approximate equivalent circuit, Figure 1, that overshoot and the associated ringing is caused primarily by the values of L and C which dominate the other parameters for large fan-outs. Overshoot may be reduced by decreasing L and C and/or adding to the damping by increasing R_O or R_D. The value of L may be decreased by running the lead close to a ground plane or using a flat conductor that has less inductance per unit length. Figures 3, 9, and 15 compared with 4, 10, and 16 respectively, show the striking difference in overshoot for 12" of teflon coated wire driving a fan-out of 15 gates when the wire is touching the ground plane and when it is an average of 3" above the ground plane. The value of C is difficult to reduce. The equivalent capacitance per gate input may be varied by perhaps 2pF depending upon the use of sockets or the direct wiring of the integrated circuits, and the method of wiring used.

The most effective method of reducing overshoot is the reduction of $L\frac{di}{dt}$, the voltage drop across L due to the rate of change of current. One way to accomplish this is by decreasing lead length or running multiple wires between the driver and load. This method is often not practical. The insertion of a resistor in series with the lead, thus increasing the series damping resistance, is the most effective method of overshoot reduction. The time constant of the transmission path is then increased, therefore causing a trade-off with risetime. The addition of a resistor causes a DC voltage drop and large values must be avoided to prevent "1" level degradation. Table 3 gives the maximum value of series resistance that may be inserted for worst case design for a given fan-out and driver.

Since capacitively coupled flip-flops toggle on peak-to-peak amplitude and are relatively unaffected by voltage input levels, higher values of series resistance may be employed. The limit on the values of resistance is determined by the worst case amplitude vs. risetime curves which may be found in AN244. The added resistance, if relatively large in value, forms an R-C integration network which determines the risetime. This may be observed in Table 4.

It is seen from Table 4 that the values of required series resistance become marginal for high fan-outs with 12" signal leads when compared to the allowed values shown in Table 3. Therefore, when driving a high fan-out with fast risetime it may be more desirable to use the following method: A separate signal lead and series resistor from the driver to each fan-out is utilized. This method may be used for a fan-out of 20 clocked flip-flops using the MC369 as a driver. The risetime to each flip-flop or gate is appreciably less for this method than when driving the devices with a single signal lead and resistor.

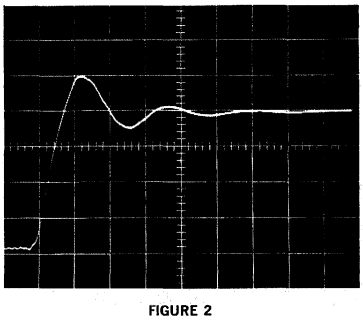
Another method of reducing overshoot is the addition of a ferrite bead around the signal lead between the driver and the load. This is another method of trading overshoot for risetime. Advantages of the ferrite bead are low cost and no shift produced in DC levels. Disadvantages are that it is effective for only small fan-outs, fast risetimes, and long lead lengths. The ferrite bead adds inductance to the signal lead at low frequencies, but this is an inductance of very low Q at high frequencies. Therefore, attenuation is produced for the high frequency components of the risetime, resulting in a slower risetime as seen by the load. Once the risetime is reduced to about 12ns, the addition of further ferrite beads to the signal line will not appreciably reduce overshoot and may actually increase overshoot for slower risetimes.

The following photographs will serve to illustrate the data shown previously. All photographs are taken with the following constants: Horizontal deflection rate 1cm per 20ns, Vertical deflection 1cm per 200mV, and signal lead lengths of 12 inches. The following notation is used for the photographs. OS = overshoot, tr = risetime, and W = 1/8", W = 0", W = 3" which stand for wire 1/8" above ground plane, 0" above ground plane and 3" above ground plane respectively. L stands for load with "A" being the actual integrated load and "S" being the simulated load. R_S is the value of series resistance inserted in the signal lead. The simulated load used in Figures 5, 7, 11, 13 was C = 150pF, R_D = 15Ω, R_I = 3K (refer to Figure 1), while the simulated load in Figures 17, 19 was C = 160pF, R_D = 8 , R_I = 3K.

DRIVER GATE	FAN-OUT	R	3" LEAD LENGTH OVERSHOOT	3" LEAD LENGTH RISETIME	R	6" LEAD LENGTH OVERSHOOT	6" LEAD LENGTH RISETIME	R	12" LEAD LENGTH OVERSHOOT	12" LEAD LENGTH RISETIME
MC301	10-MC356	0	90mV	10.9ns	5	100mV	11.7ns	18	95mV	12.8ns
MC301	15-MC356	0	95mV	12.1ns	12	90mV	14.3ns	12	95mV	14.4ns
MC301	5-MC364	0	85mV	8.6ns	13	90mV	9.9ns	27	100mV	10.2ns
MC301	10-MC364	10	95mV	14.2ns	13	100mV	14.6ns	24	95mV	15.9ns
MC365	10-MC356	10	90mV	9.4ns	15	95mV	9.8ns	25	95mV	10.3ns
MC365	15-MC356	10	100mV	10.3ns	15	100mV	10.9ns	24	95mV	11.8ns
MC365	5-MC364	20	95mV	8.5ns	27	100mV	8.7ns	51	90mV	9.8ns
MC365	10-MC364	13	95mV	11.9ns	18	95mV	12.6ns	27	95mV	13.8ns
MC369	2-MC356	0	80mV	5.1ns	24	90mV	5.4ns	62	100mV	6.0ns
MC369	5-MC356	5	100mV	5.9ns	24	100mV	6.8ns	43	100mV	7.6ns
MC369	10-MC356	10	100mV	8.7ns	24	90mV	10.5ns	33	90mV	11.4ns
MC369	15-MC356	10	95mV	10.2ns	18	95mV	11.4ns	27	95mV	12.7ns
MC369	1-MC364	0	0	4.8ns	0	50mV	3.9ns	68	90mV	4.0ns
MC369	2-MC364	27	100mV	5.9ns	62	95mV	6.7ns	75	100mV	6.8ns
MC369	5-MC364	22	90mV	7.5ns	39	100mV	8.2ns	47	100mV	8.6ns
MC369	10-MC364	15	90mV	10.9ns	22	100mV	11.9ns	33	100mV	13.4ns

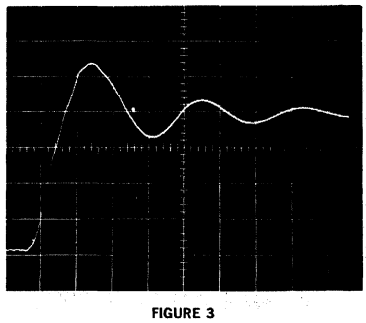
TABLE 4 — REQUIRED SERIES RESISTANCE TO REDUCE OVERSHOOT TO AN ACCEPTABLE LEVEL

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC301
FAN-OUT = 15 MC356'S



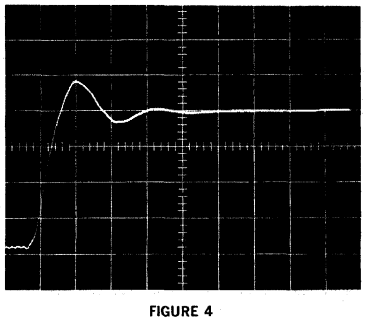
t_r = 12.3ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = A

FIGURE 2



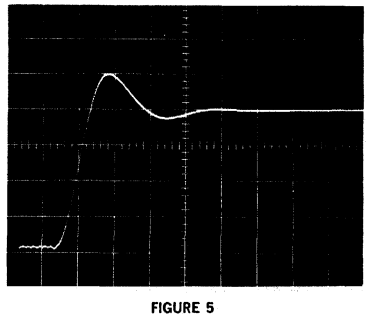
t_r = 14.2ns
w = 3"
R_S = 0Ω
OS = 280mV
L = A

FIGURE 3



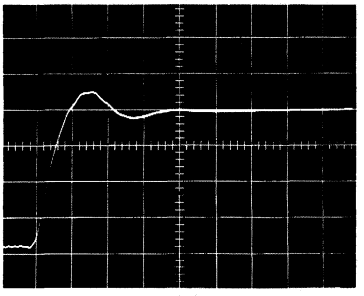
t_r = 12.3ns
w = 0"
R_S = 0Ω
OS = 175mV
L = A

FIGURE 4



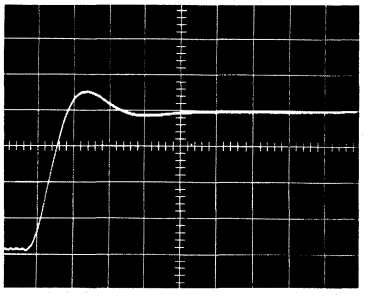
t_r = 12.8ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = S

FIGURE 5



t_r = 14.7ns
w = 1/8"
R_S = 15Ω
OS = 95mV
L = A

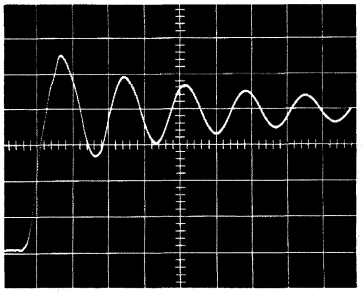
FIGURE 6



t_r = 15.3ns
w = 1/8"
R_S = 15Ω
OS = 100mV
L = S

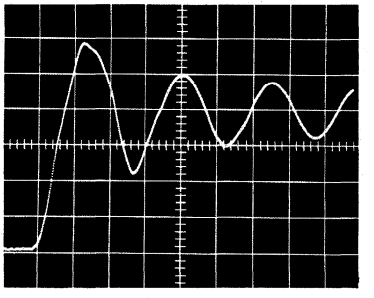
FIGURE 7

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC365
FAN-OUT = 15 MC356'S



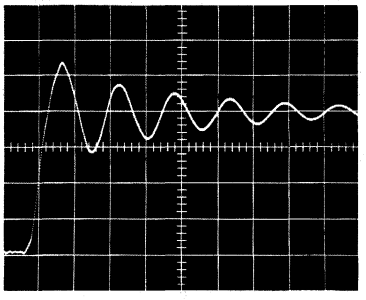
t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = A

FIGURE 8



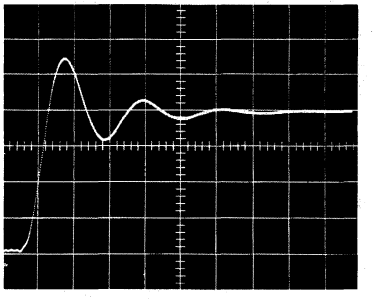
t_r = 12.9ns
w = 3"
R_S = 0
OS = 360mV
L = A

FIGURE 9



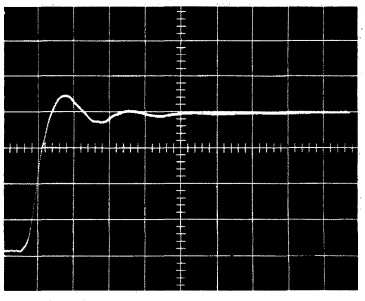
t_r = 9.5ns
w = 0"
R_S = 0
OS = 280mV
L = A

FIGURE 10



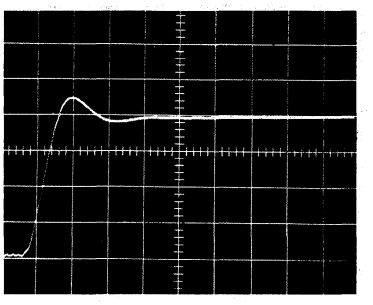
t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = S

FIGURE 11



t_r = 11.8ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = A

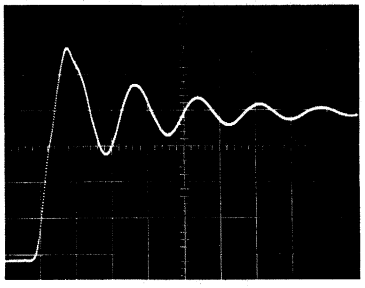
FIGURE 12



t_r = 13.0ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = S

FIGURE 13

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC369
FAN-OUT = 15 MC356'S



t_r = 8.8ns
w = 1/8"
R_S = 0
OS = 370mV
L = A

FIGURE 14

t_r = 12.0ns
w = 3"
R_S = 0
OS = 390mV
L = A

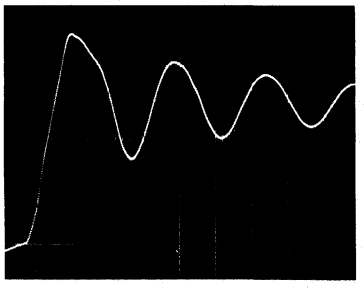
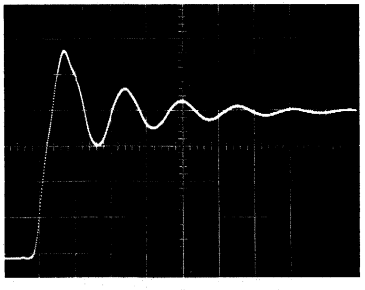


FIGURE 15



t_r = 8.3ns
w = 0"
R_S = 0
OS = 360mV
L = A

FIGURE 16

t_r = 9.2ns
w = 1/8"
R_S = 0
OS = 380mV
L = S

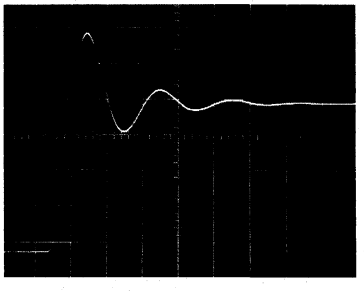
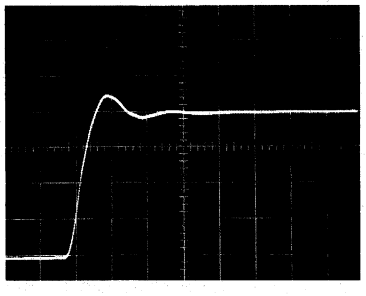


FIGURE 17



t_r = 11.6ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = A

FIGURE 18

t_r = 13.4ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = S

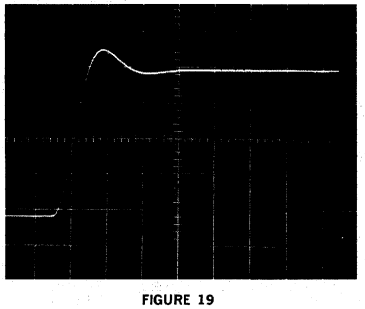


FIGURE 19

CONCLUSIONS

It has been shown that overshoot can be a system problem for long lead lengths and "lumped" fan-outs and that the amount of overshoot is primarily determined by system layout and geometries. Overshoot to typical fan-outs may be reduced to acceptable levels by inserting resistance of the proper value in series with the driver output lead. Higher fan-outs may be driven with fast risetimes by inserting a resistor of appropriate value in series with the input to each integrated circuit load, and running a separate lead from the driver to each resistor. Also, ferrite beads may be used to advantage for certain configurations of long leads and relatively low fan-outs.

As system speeds increase and MECL gates with risetimes of 2ns or less are utilized, these methods will not be useful for reducing overshoot. Strip line techniques utilizing multi-layer printed circuit boards, controlled line impedance, and terminated transmission lines will solve overshoot problems for logic into the sub-nanosecond region.

NOISE IMMUNITY WITH HIGH THRESHOLD LOGIC

INTRODUCTION

The following material discusses general noise considerations and compares the noise immunity of the new high threshold devices with standard saturated logic devices. Some basic illustrations are provided which indicate the flexibility of usage that may be achieved with the MHTL family.

Typical characteristics of the MHTL family are:

Single 15-volt power supply
7.5V switching threshold
6 volt signal line noise margins
13 volt logic swing
30 mW gate power dissipation
85 ns gate propagation delay
4 MHz flip flop toggle frequency
-30^{O} to $+75^{O}$C operating temperature range

NOISE INJECTION

Electrical noise has always been a source of trouble for electronic systems whether they are composed of discrete components or integrated circuits. Origination of electrical noise can be from many sources both external to the electronic system under consideration and self-induced noise by the circuitry itself. Examples of external sources would be switching of inductive circuits, rotating machinery, and various electronic control circuits as depicted in Figure 1.

Internal noise may be caused by the switching of one circuit affecting the state of another circuit (Figure 2). The amount of noise induced into the passive circuit is a function of the voltage swing, current change, and the switching speed of the active circuit and the inductive and capacitive coupling between the two circuits. Coupling may also take place by the use of a common path for the active and passive devices such as a power supply or ground lead. Noise from external sources is induced into the system under similar conditions. Generally, noise is a random combination of many sources and as such is extremely hard to analyze. The net result, however, is that induced positive and negative spikes relative to the quiescent condition of a line may cause erroneous information to be absorbed into the system. This condition must be avoided if proper operation is to be achieved by the unit.

NOISE REDUCTION TECHNIQUES

Several schemes have commonly been employed to reduce the effect of electrical noise on a system composed of integrated circuits. Physical shielding of the integrated circuits and its associated wiring prevents external electromagnetic radiation from inducing noise into the circuitry. Special buffering circuits may be employed between the electronic circuits and signal leads dependent on external sources. These signal leads in many cases require special routing considerations and special shielding. Extra filtering of the power supply leads may be required to reduce the noise introduced by this route. Internal noise generation may require special spacing and routing considerations as well as maintaining short lead lengths. In some cases the power supply may need to be by-passed at several points on a board.

The amount of additional components and equipment necessary to protect integrated circuits from electrical noise can increase to a point where it is economically desirable to seek other methods of operation to obtain the desired results. It would be advantageous to have an integrated circuit family with a high degree of inherent noise immunity for economical construction of an electronic system. This will minimize the amount of special care needed for proper circuit operation in areas with a high electrical noise environment.

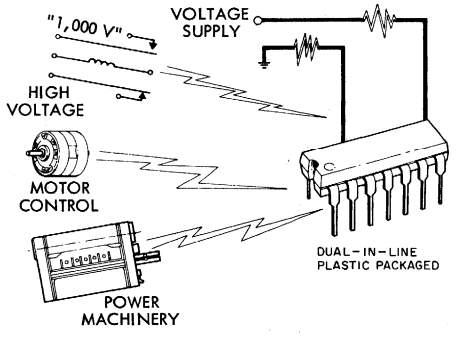


FIGURE 1 - EXTERNAL NOISE GENERATOR

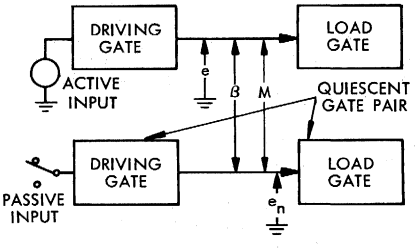


FIGURE 2 - INTERNAL NOISE GENERATOR

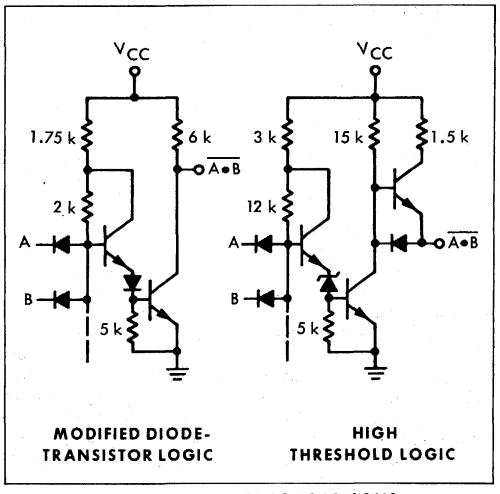


FIGURE 3 - GATE COMPARISONS

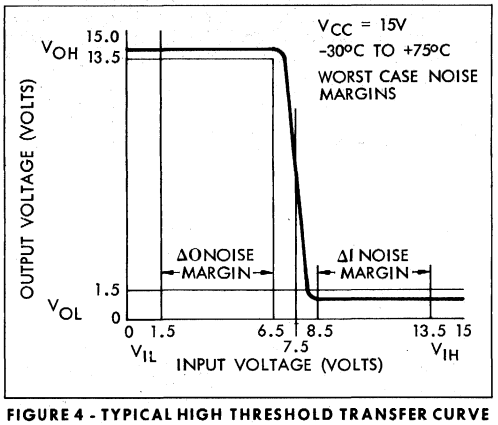


FIGURE 4 - TYPICAL HIGH THRESHOLD TRANSFER CURVE

devices demands a higher power supply and a nominal 15 volts is used. The transfer curve for the basic gate operating with a 15 volt supply is shown in Figure 4. It can be seen that for any input signal up to 6.5 volts, the output will remain in the high state or above 13.5 volts. A 2-volt margin, from 6.5 volts to 8.5 volts, is used for the transition region and guards against variations between manufacturing lots and temperature effects from -30°C to +75°C. At 8.5 volts on the input, the output is in the low state or less than 1.5 volts and remains there for any further increase of the input voltage. This diagram indicates worst case noise margins of 5 volts in both the high and low states for a V_{CC} of 15 volts while typical values are about 6 volts.

LOGIC FAMILY COMPARISONS

BASIC OPERATING CHARACTERISTICS

A comparison of basic operating characteristics for high threshold logic with the standard forms of logic is provided in the table shown in Figure 5. The values given are typical for an ambient temperature of 25°C and indicate relative characteristics between the different families. One difference that should be noted is that the high threshold logic is slower than the other families. This characteristic aids in the rejection of noise and will be illustrated in following figures.

	V_{CC} (VOLTS)	GATE POWER DISSIPATION (mW)	PROPAGATION DELAY (ns)	DC NOISE IMMUNITY (VOLTS)	LOGIC SWING (VOLTS)
RESISTOR TRANSISTOR LOGIC	3.6	12	25	0.5	1.0
MODIFIED DIODE TRANSISTOR LOGIC	5.0	8	30	1.2	4.5
TRANSISTOR – TRANSISTOR LOGIC	5.0	15	10	1.2	3.5
HIGH THRESHOLD LOGIC	15	30	85	6	13

FIGURE 5 - BASIC OPERATING CHARACTERISTICS

A HIGH THRESHOLD LOGIC

The most popular families of integrated circuits in use today exhibit a comparatively high speed of operation and have typical threshold values between 0.7 and 1.5 volts. A new type of logic family, High Threshold Logic (MHTL), has been developed that closely resembles the modified diode-transistor logic family (Figure 3). The basic difference is that the high threshold logic uses a reverse biased base-emitter junction operating in the avalanche breakdown mode as a threshold element. As can be seen in the figure, the logical NAND function is provided by each gate. The inputs of the modified diode-transistor gate must exceed two forward base emitter drops or typically 1.5 volts before base current is applied to the output inverting transistor providing the "0" state. In the high threshold device, however, the inputs must exceed the reverse biased base-emitter breakdown plus one forward V_{BE} drop or typically 7.5 volts before the output inverting transistor turns on. Since the other logic families exhibit a threshold level similar to or less than the modified diode-transistor device, a considerable increase in threshold level has been obtained with the new configuration. The higher threshold incorporated in the

SIGNAL LINE NOISE IMMUNITY

Measurements were made on the different logic families to determine the signal line noise immunity not only from a voltage margin consideration, but also from a pulse width and energy point of view as well. Figure 6-A illustrates a test set-up to measure immunity of the gate to noise on the signal lead. Positive going noise was injected on the signal lead for this set-up with the output of gate #1 in the low state. When sufficient noise was injected, the flip-flop driven by the second gate would begin to toggle indicating the effect of the injected noise. This type of test not only measures the power needed for disturbance, but also the pulse width of noise necessary to propagate through and cause faulty operation of a driven device. A series of values of voltage level and injected current to cause disturbance were taken versus the pulse width at each corresponding point. Current readings were obtained as a voltage drop across the pulse generator resistor. The pulse generator offset voltage was adjusted to eliminate the effect of its quiescent condition on gate levels. Voltage threshold as a function of pulse width is plotted in Figure 6-B. The energy of each logic family is plotted in bar graph form at the knee of each respect-

ive curve in Figure 6-C. For narrower pulse widths, the energy necessary to cause a disturbance increases. The high energy value obtained for MHTL is a result of the high threshold voltage and low gate impedance in this state.

Figure 7-A illustrates a similar test except that gate #1 is in the high state and negative going noise is injected on the signal lead. Similar results are shown in Figure 7-B and C.

GROUND LINE IMMUNITY

Tests were made on the devices to provide information on the immunity to noise injected on the ground terminal. The test configuration is shown in the first part of Figure 8. A plot of voltage threshold versus pulse width is given in Figure 8-B for the worst case condition found for the particular family dependent on the input state. The energy relationships are provided in Figure 8-C.

POWER SUPPLY IMMUNITY

A similar test was made for noise injected on the power supply lead. In this case, the flip flop will only be affected by negative going noise and the results indicate worst case conditions for the particular family dependent on the state of the first gate. The test configuration and results are given in Figure 9.

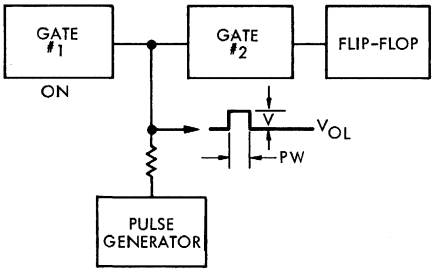


FIGURE 6A

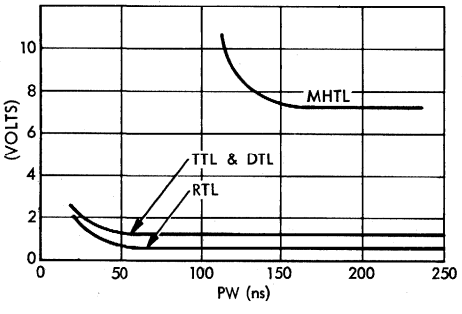


FIGURE 6B

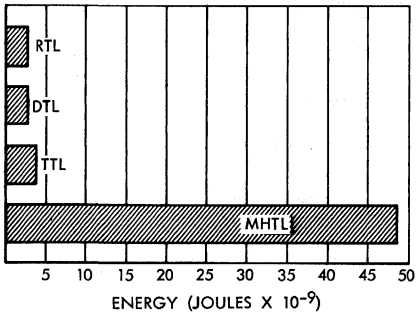


FIGURE 6C

SIGNAL LINE NOISE IMMUNITY

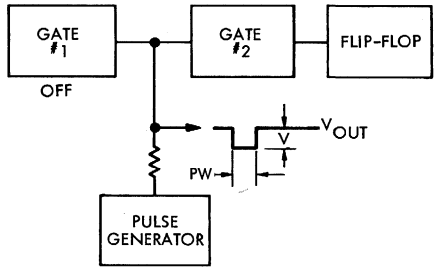


FIGURE 7A

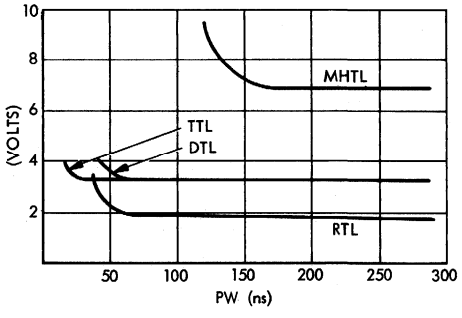


FIGURE 7B

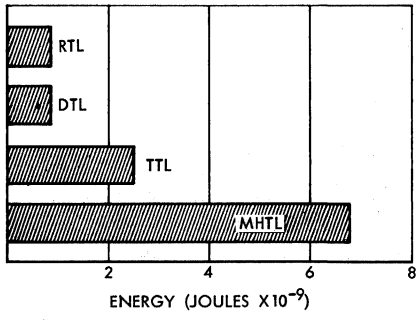


FIGURE 7C

SIGNAL LINE NOISE IMMUNITY

The preceding tests were taken with a fanout of one on the first gate and a fanout of the flip flop only on the second gate. This condition tends to be an advantage for the RTL family and the results are somewhat optimistic in this case.

These comparisons indicate that the high threshold logic has an appreciable inherent advantage over the standard families of integrated circuits. In addition, the higher threshold level present in these devices provides a considerable margin that may be used in conjunction with simplified buffering networks to filter out excessive noise spikes under very extreme conditions.

USAGE

The preceding discussion has generally referred to the basic high threshold gate circuit. Additional components are available, however, which exhibit the same noise immunity characteristics obtained by reverse biased base-emitter breakdown action. The availability of other units such as line drivers, J-K flip flops, R-S flip flops, and monostables will allow the designer to construct a complete logic system with a high degree of noise immunity throughout.

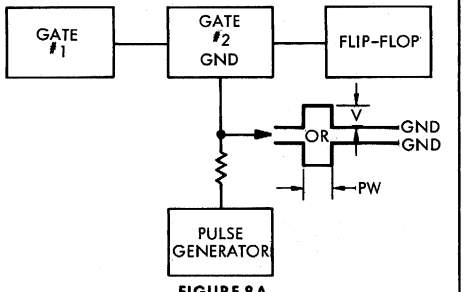


FIGURE 8A

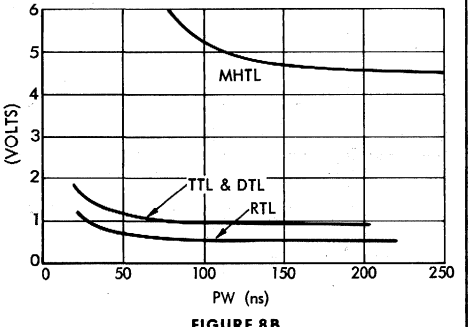


FIGURE 8B

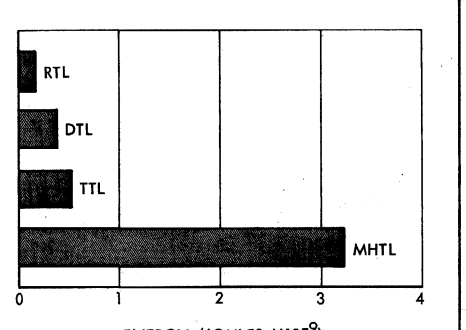


FIGURE 8C

GROUND LINE NOISE IMMUNITY

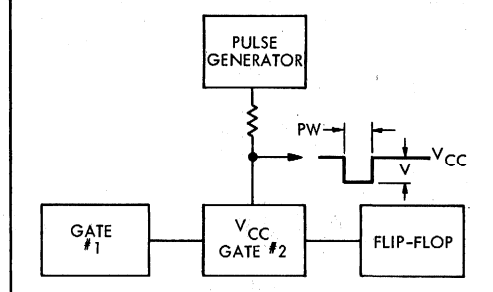


FIGURE 9A

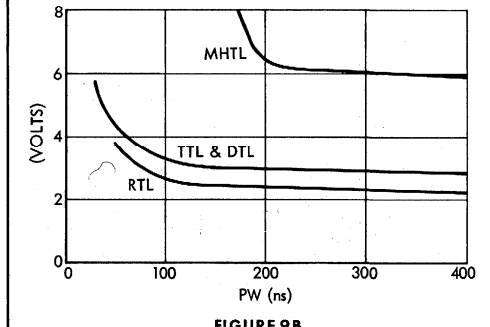


FIGURE 9B

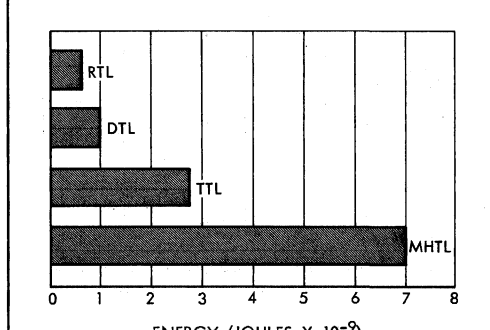


FIGURE 9C

POWER SUPPLY NOISE IMMUNITY

Situations arise where it would be advantageous to work into a system that operates at a higher speed than is obtainable by the high threshold devices. Translation between high threshold logic and standard logic families can be accomplished to allow the usage of high threshold devices as peripheral circuitry to a higher speed logic system. Thus, the high threshold devices may be operated in the noise environments and translation may take place into the lower threshold and higher speed system at the appropriate locations as indicated in Figure 10.

The higher supply voltage used in this logic family provides for the convenient interfacing with many discrete components. For example (Figure 11), the input may be controlled by a photo transistor so that illumination will cause the gate output to be high and darkness will provide a low output state. The output of the gate might feed into a logic system such that after a specific count would operate a relay. If a line driver unit were used as the output element, a 35mA, 15-volt relay could be employed. Other components such as lamps, SCRs, or transistors may also be driven directly at the output. As can be seen, the uses of the high threshold devices are many and varied.

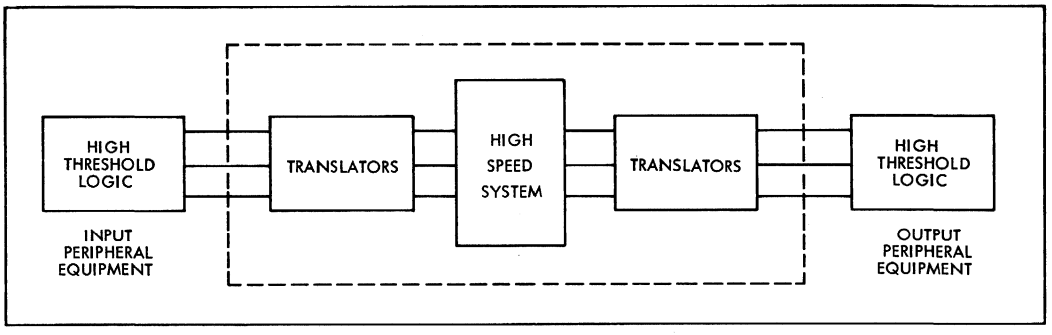


FIGURE 10 - OPERATING AS PERIPHERAL COMPONENTS

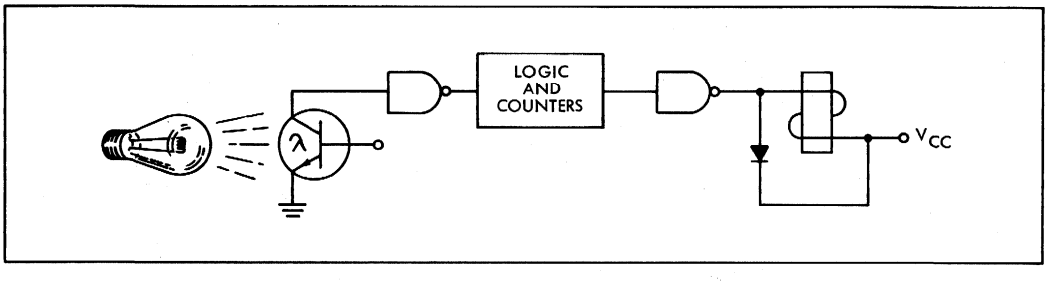


FIGURE 11 - OPERATING WITH DISCRETE COMPONENTS

SUMMARY

The new high threshold logic provides an integrated circuit logic family with a greater inherent immunity to electrical noise than is available with standard logic families. This logic family is ideal for situations where a large degree of electrical noise exists and where it is desirable to minimize the additional precautions necessary to reduce the effects of electrical noise. Input and output compatibility of the units with discrete components opens the door for a wide range of device employment.

OPERATION AND APPLICATION OF MHTL I/C FLIP-FLOPS

INTRODUCTION

The new High Threshold Logic (MHTL) line is designed to satisfy the requirements for systems that will operate in high electrical noise environments. The basic gate circuit of the family is essentially the same as the MDTL gate circuit with the coupling diode replaced by a reverse biased base-emitter junction which operates in the avalanche breakdown mode thus achieving a high input threshold. This family provides a positive logic NAND function or a negative logic NOR function.

Some typical characteristics of the family are:

- Single 15-volt power supply
- 7.5 V switching threshold
- 6-volt signal line noise margins
- 13-volt logic swing
- 30 mW gate power dissipation
- 100 ns gate propagation delay
- -30^{o} to $+75^{o}$C operating temperature range

Two flip-flops are currently available in the MHTL family, a dual J-K, the MC663P and a master-slave R-S, the MC664P. This application note describes the mode of operation of each flip-flop circuit in detail and will illustrate some typical uses of the devices.

MC663P DUAL J-K FLIP-FLOP

The MC663P unit contains two independent J-K flip-flops each with its own clock ($\overline{C}$) and direct reset ($\overline{R_D}$) terminals as shown in the block diagram of Figure 1A. Operation of the flip-flop in the synchronous or clocked mode follows the conditions shown in the Synchronous Truth Table in Figure 1B. The information on the J and K leads is effectively applied to the flip-flop when the clock lead is high and the output corresponds to the (n+1) truth table conditions upon the negative transition of the clock potential with commutation of the flip-flop occuring as the clock potential passes through the transition region (from 8.5 volts to 6.5 volts). The rise and fall times through these levels should not exceed 1 microsecond for proper operation. Clock pulse width at the 8.5 volt level should be greater than 200 nanoseconds, although typical units will operate with a 100 nanosecond pulse width. Operation in the synchronous mode requires that the direct reset inputs be terminated to V_{CC} if they are not used.

The direct reset terminal may be used to place the Q output in the 0 state independent of the steady state conditions on the J, K and $\overline{C}$ inputs. This is accomplished by

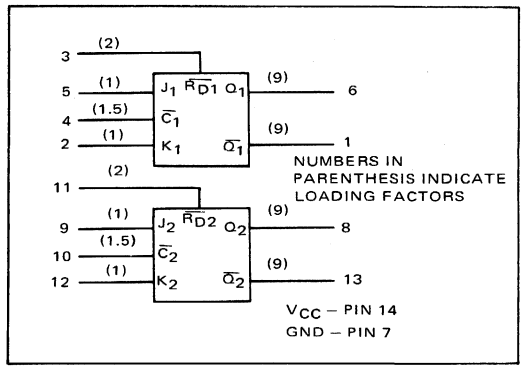


FIGURE 1A – MC663P BLOCK DIAGRAM

SYNCHRONOUS TRUTH TABLE

t_n		t_{n+1}	
J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	0	1
1	1	$\overline{Q_n}$	Q_n

a. Direct input ($\overline{R_D}$) must be high.
b. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
c. 0 denotes low state, 1 denotes high state.
d. Q_n is the state of the Q output in the time period t_n.

DYNAMIC J-K TRUTH TABLE

J_n	K_n	J_{n+1}	K_{n+1}	Q_{n+1}
1	*	0	K_n	1
*	1	J_n	0	0
1	1	0	0	$\overline{Q_n}$
*	*	1	1	Q_n

* – Don't care.
n – Condition before change.
n+1 – Condition after change.
Clock and direct reset must be high.

FIGURE 1B – MC663P TRUTH TABLES

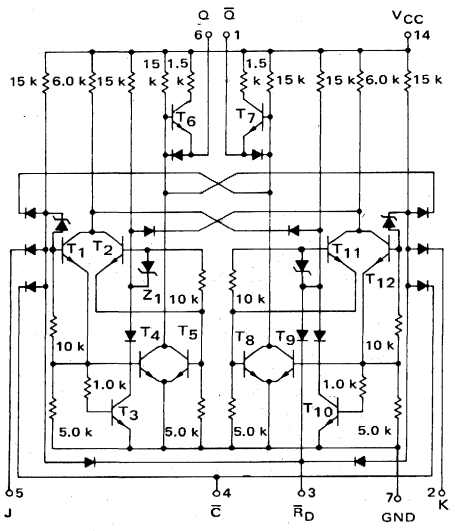


FIGURE 1C – CIRCUIT SCHEMATIC 1/2 MC663P

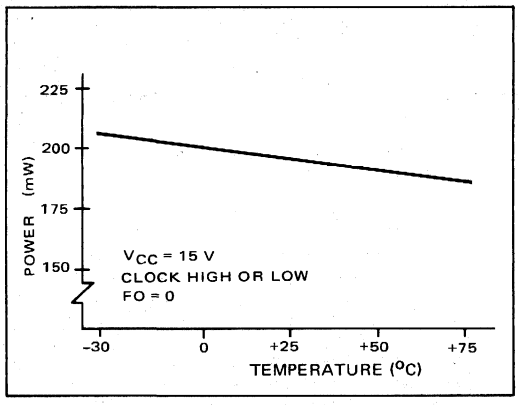


FIGURE 2A – TYPICAL MC663P POWER DISSIPATION versus TEMPERATURE

applying a logic zero to $\overline{R_D}$ for a period not less than 150 nanoseconds.

A third mode of operation may be achieved with these flip-flops as indicated in the Dynamic J-K Truth Table in Figure 1B. Operation in this mode requires the clock input as well as the direct reset input to be in the logic 1 state. Applying a logic 0 to the J and K inputs for a period greater than 150 nanoseconds will give the results indicated in the truth table. The rise time following an independent J or K negative excursion is not critical if the flip-flop remains in the given state; however, it should be less than 1 microsecond if both inputs are connected together when a logic 0 is applied or if the state of the flip-flop is changed by a negative transition on the other input. This characteristic will allow negative going signals to be capacitively coupled into the flip-flop when the J and K inputs are normally held high by external resistors.

Operation of the circuit will be explained using the schematic in Figure 1C. Initially, consider the following conditions: Q output in the low state and correspondingly the $\bar{Q}$ output in the high state, the clock input in the low state, and the direct reset input in the high state. Under these conditions, transistor T_6 will be off, transistor T_7 is on supplying current to any load connected to the $\bar{Q}$ output and T_5 is on, as will be explained later, sinking any load current on the Q output. Transistor T_2 is on with base current supplied through zener Z_1. Transistor T_2 being on supplies base current to T_5. All other transistors are off and this is the quiescent state for these conditions. If the clock input goes high and the J input is high or open, transistor T_1 turns on which also turns on T_3 and T_4. Transistor T_3 turning on will turn off T_2 which correspondingly turns off T_5. It should be noted that the output conditions have not changed due to the logical 1 on the clock input. The flip-flop will remain in this condition as long as the clock and J inputs remain high, but if either input goes low, the flip-flop will change state. If either the J or clock inputs go low, transistor T_1 turns off and its collector potential will rise causing T_{11} to turn on. T_{11} turning on supplies base current to T_8 and the $\bar{Q}$ out-

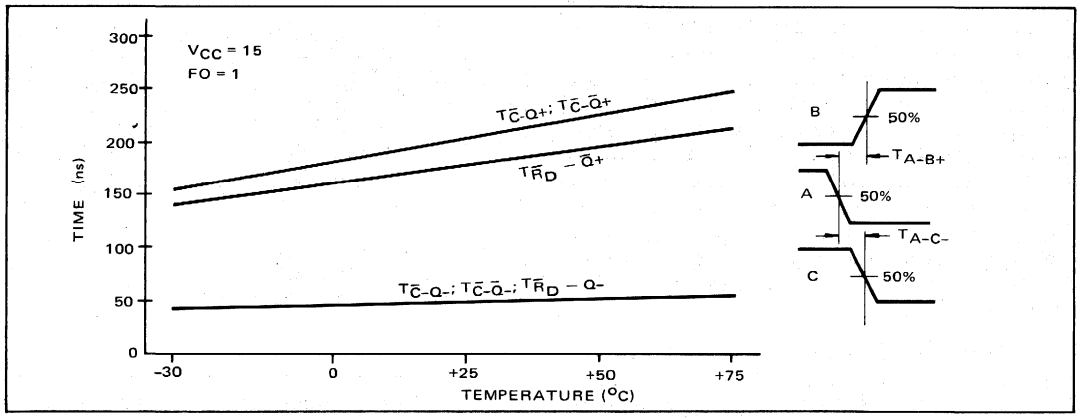


FIGURE 2B – TYPICAL MC663P PROPAGATION DELAY TIMES versus TEMPERATURE

put goes low. Transistors T_3 and T_4 are delayed in turning off after T_1 shuts off due to the charge stored in the base of T_4. Transistor T_3 being on prevents T_2 from turning on and T_2 will be held off once T_{11} turns on. Finally, when T_4 turns off, T_5 is also inhibited and the Q output goes high completing the flip-flop transition. A similar action will occur from this state to cause transition back to the original state if the clock and K input terminals are considered. It can be noted that commutation of the flip-flop may be inhibited by a logic 0 on the J and K inputs. This will prevent transistors T_1 or T_{12} from turning on when the clock is high and thus prevents commutation.

The flip-flop may be set to the Q = 0 state by use of the direct reset terminal $\overline{R_D}$ when the flip-flop is in the Q = 1 state. A logic 0 on $\overline{R_D}$ inhibits the J, K, and $\overline{C}$ inputs and will turn off T_{11} causing T_2 and T_5 to turn on placing the flip-flop in the Q = 0 state. T_{11} turning off removes the base current from T_8 and the $\overline{Q}$ output will go to the logic 1 level.

The load applied to the output terminals must be limited such that the output voltage will not be less than 8.5 volts when in the high state. This is necessary for proper cross-coupling between the two outputs of the flip-flop and the input circuitry.

Typical characteristics of the MC663P over the operating temperature range are provided in Figures 2A and B.

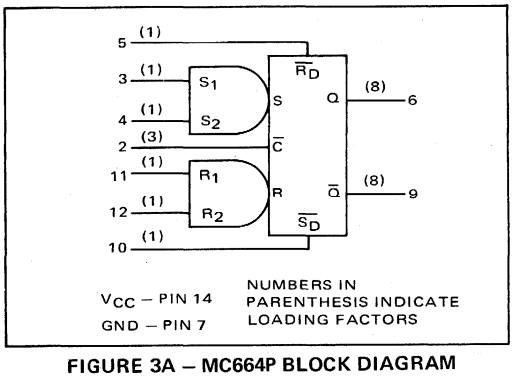


FIGURE 3A – MC664P BLOCK DIAGRAM

MC664P R-S FLIP-FLOP

The MC664P is a dc-coupled R-S flip-flop of the master-slave or two-phase type. Since it is an R-S type, simultaneous high inputs are not allowed because the output cannot be predicted after a negative clock transition. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.

The block diagram shown in Figure 3A indicates the logic function of the flip-flop as well as providing the loading factors for the device. The loading factor of 3 for the clock terminal is tested with the clock input at 1.5 volts. The output loading factors of 8 are reduced from the standard MHTL gate loading factor of 10 because of internal flip-flop cross connections.

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:
Direct inputs ($\overline{R_D}$, $\overline{S_D}$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

DIRECT INPUT OPERATION

$\overline{R_D}$	$\overline{S_D}$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock ($\overline{C}$) input must be low
NC = No change
NA = Not allowed

FIGURE 3B – MC664P TRUTH TABLES

The truth tables for the circuit are provided in Figure 3B for both clocked operation and for the direct input terminals. It should be noted that the $\overline{R_D}$ and $\overline{S_D}$ terminals are high for clocked operation while direct set and reset requires the clock to be low.

The schematic for the MC664P is shown in Figure 3C. Operation of the circuit will be described by making the initial assumptions that the flip-flop is in the Q = 0, $\overline{Q}$ = 1 state, that the clock ($\overline{C}$) is low, and that the direct set and reset ($\overline{S_D}$, $\overline{R_D}$) terminals are high or open. Under these conditions, T_{10} and T_{13} would be off while T_8 and T_{11} would be on. Transistor T_9 is on and supplies base current to T_8 through the zener diode. For this situation to exist T_4 and T_5 would also be on, while the remaining transistors in the circuit are off. This indicates the quiescent condition for the flip-flop under the initial conditions.

To illustrate commutation of the flip-flop, assume that inputs S_1 and S_2 are open or high and that either R_1 and/or R_2 are low. Now, as the clock potential rises to approximately 7 volts, the first change to occur will be the conduction of T_7 which provides a second base current source to T_8 which is already on. A further increase in the clock potential of one forward V_{BE} magnitude will cause T_1 to turn on which turns on T_2. (It is noted that there is a V_{BE}

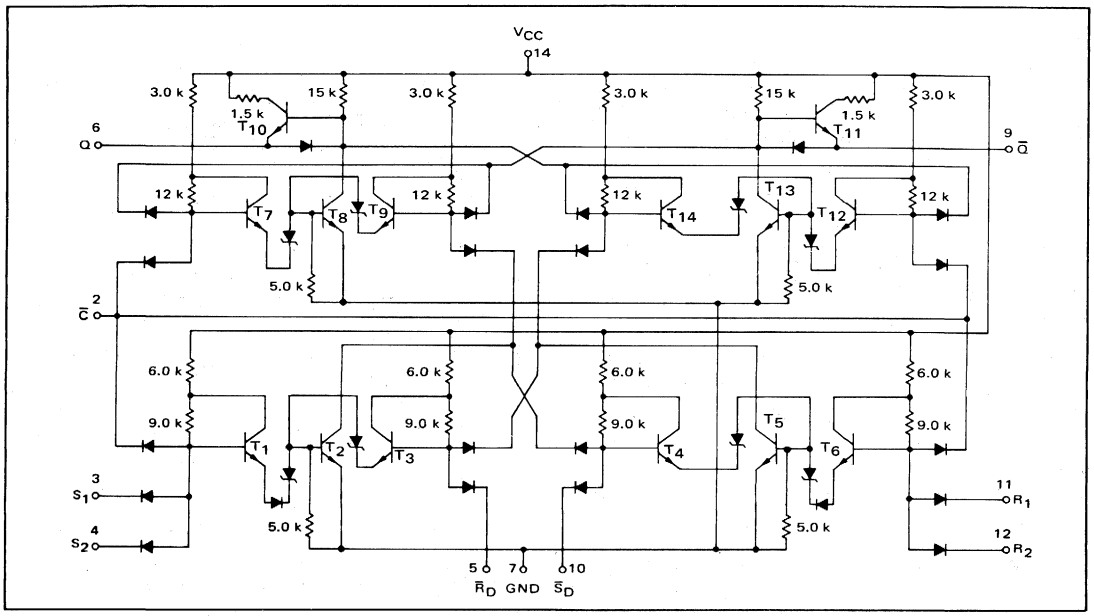


FIGURE 3C – CIRCUIT SCHEMATIC MC664P

diode offset between the master and slave sections of the flip-flop and it is essentially a dc rise time circuit.) Transistor T_2 turning on causes T_9, T_4 and T_5 to turn off. Transistor T_8 remains on, however, due to the second source of base current from T_7. Transistor T_5 being off causes T_3 to turn on and now T_2 is provided with base current from two sources. A continuing increase of the clock input will not cause any further changes in the flip-flop. As the clock potential starts to decrease, T_1 will turn off first although T_2 remains on due to the second base current source. When the clock potential falls an additional V_{BE} drop, T_7 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off turns on T_{14} and T_{13} and the $\overline{Q}$ output goes low generating the changed flip-flop state. The conditions of the flip-flop will now remain the same for any further decrease in the clock potential. A similar action would return the flip-flop to the original state if R_1 and R_2 were high or open with S_1 and/or S_2 at the low level and a clocking waveform applied. Although information may be reliably applied to the flip-flop with essentially dc-risetime clock-waveforms, there is a point where the output rise and fall times are beta dependent on the clock level. This will increase the output transition times when excessively slow clock-waveforms are present.

The flip-flop state may be changed by use of the $\overline{R_D}$ and $\overline{S_D}$ terminals. If the condition is considered where Q = 0, $\overline{Q}$ = 1, $\overline{C}$ is low, and both $\overline{R_D}$ and $\overline{S_D}$ are high as in the preceding example, it can be observed that a momentary low on $\overline{S_D}$ will set the flip-flop to Q = 1, $\overline{Q}$ = 0. In this instance when $\overline{S_D}$ goes low, T_4 and T_5 turn off which causes T_3 and T_2 to turn on. With T_2 on, T_9 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off, turns on T_{14} and T_{13} causing $\overline{Q}$ to go low completing the transition. Similar action results if the flip-flop were in the Q = 1, $\overline{Q}$ = 0 state and a momentary logical zero were placed on the $\overline{R_D}$ terminal.

A toggle mode of operation may be achieved with the flip-flop by connecting the Q output to one of the R inputs and the $\overline{Q}$ output to one of the S inputs. Under this condition, the truth table for synchronous operation of the MC663P would also apply to the MC664P by redefining the S input as the J and the R input as a K.

Power dissipation for this unit is typically 140 mW with V_{CC} = 15 V. Typical characteristics of parameters as a function of temperature are given in Figure 4A and 4B.

APPLICATIONS

Operation of the MC664P master-slave flip-flop is very similar to the MC931/831 flip-flop operation in the MDTL family. This fact, coupled with similar gate operation between the two families, allow construction of MHTL shift registers, counters and decoders in much the manner described in application notes covering the MDTL family (e.g., AN-235, 262, 283 and 284). The MC663P may be employed to take advantage of the dual function in many shift register and counter circuits, but with only the direct reset function available, parallel input operation is not as flexible as with the MC664P. Since the MC663P operates on a stored charge principle and different modes of operation may be obtained, the devices may be easily interconnected to form gateless ripple counters. Figure 5 illustrates several counters that may be constructed with a maximum

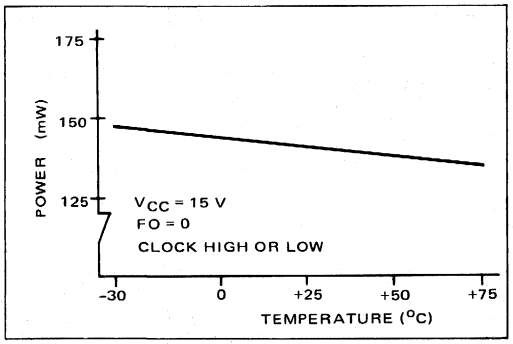


FIGURE 4A – TYPICAL MC664P POWER DISSIPATION versus TEMPERATURE

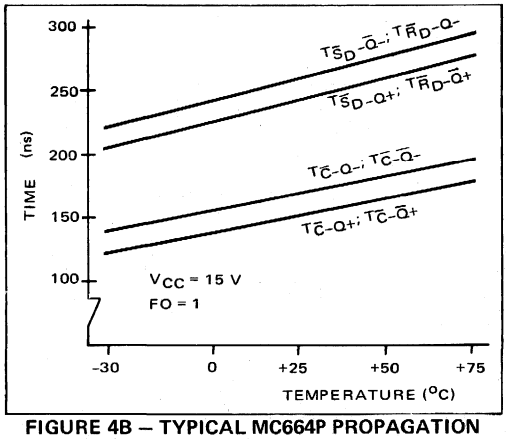
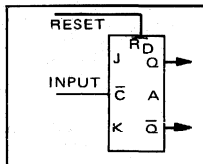


FIGURE 4B – TYPICAL MC664P PROPAGATION DELAY TIMES versus TEMPERATURE

of 2 MC663P Packages. It should be noted that direct resetting of these counters is independent of the clock level, consequently the reset time of any counter equals the reset time of a single flip-flop. The logic sequence and maximum signal ripple for each circuit is also provided in the figure.

In Figure 6, a decade shift counter is constructed using 2 MC663P units and an MC664P for proper input gating. Typical waveshapes are illustrated for this connection and the necessary decoding logic is provided.



MAX RIPPLE–1

÷2

STATE	Q_A
1	0
2	1

MAX RIPPLE–2

÷3

STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1

MAX RIPPLE–2

÷4

STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1
4	1	1

MAX RIPPLE–3

÷5

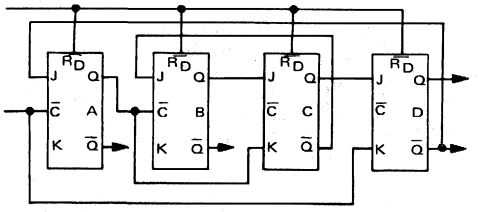
STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1

MAX RIPPLE–3

÷6

STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1

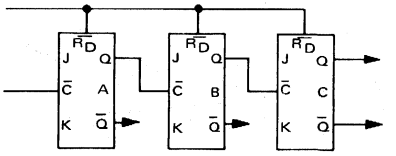
FIGURE 5 – GATELESS RIPPLE COUNTERS FROM MC663P DEVICES



MAX RIPPLE–3

÷7

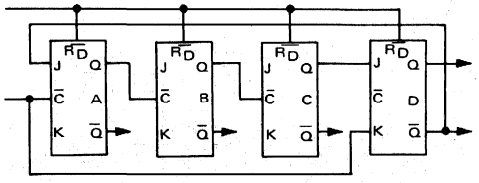
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	0	0	1



MAX RIPPLE–3

÷8

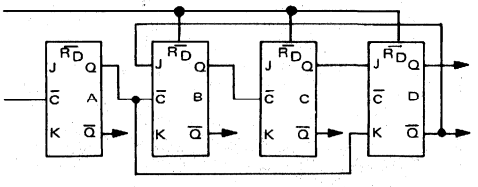
STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1



MAX RIPPLE–4

÷9

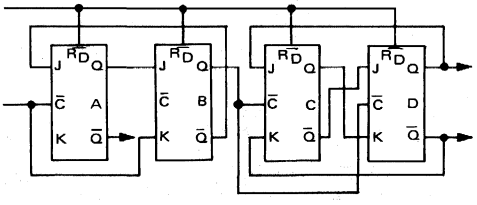
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1



MAX RIPPLE–4

÷10

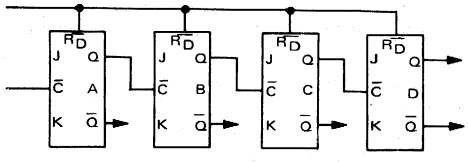
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1



MAX RIPPLE–2

÷12

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	0	0	0	1
5	1	0	0	1
6	0	1	0	1
7	0	0	1	1
8	1	0	1	1
9	0	1	1	1
10	0	0	1	0
11	1	0	1	0
12	0	1	1	0



MAX RIPPLE–4

÷16

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

FIGURE 5 – (continued)

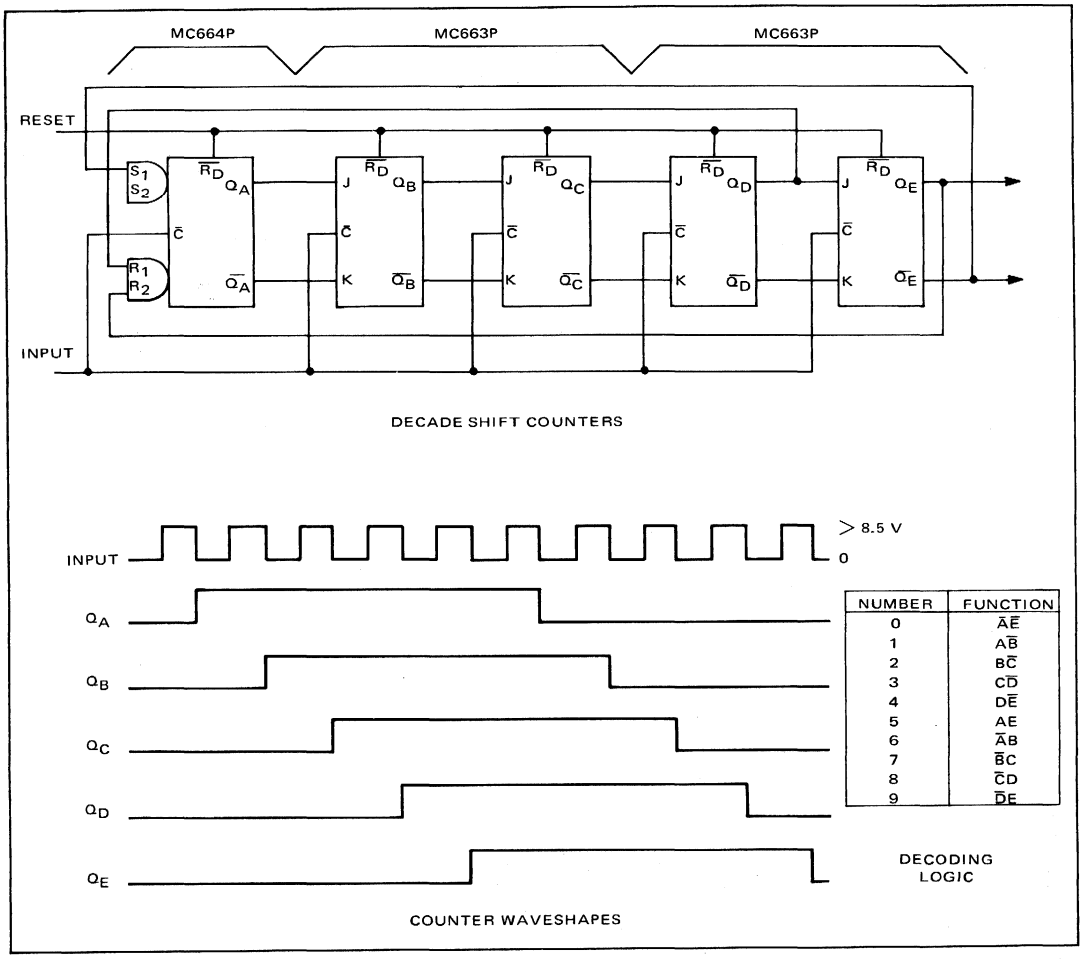


FIGURE 6 – DECADE SHIFT COUNTER AND COUNTER WAVESHAPES

CONCLUSIONS

The initial flip-flops in the MHTL family provide considerable flexibility for the design of digital electronic equipment to operate in environments subject to electrical noise. Some typical applications have been illustrated for usage of these MHTL flip-flops. In addition, a detailed explanation of operation of the devices has been given to help design the units into special applications.

AN INTEGRATED SENSE AMPLIFIER FOR CORE MEMORIES

INTRODUCTION

A definition of a sense amplifier could be "the interface circuitry between the storage elements of a memory and the logic output elements of the memory." By this definition, a sense amplifier can have many different type inputs and outputs. This paper will discuss a sense amplifier for ferrite core memories. Specific sense amplifier requirements were received from computer and core memory manufacturers. From these requirements, design goals were evolved for a sense amplifier that would satisfy the market.

An integrated sense amplifier offers advantages other than such obvious ones as saving weight, space, and assembly wiring; the inherent ability to match active components within the integrated circuit gives the integrated sense amplifier a distinct advantage over the discrete versions. In some cases, it would be very difficult to build a discrete circuit of the same quality as an integrated circuit, or to do so could be quite expensive. Therefore, a well-designed integrated sense amplifier will offer superior performance and be less expensive than its discrete counterpart.

THE CORE MEMORY

Figure 1 is a typical core memory subsystem of a general purpose digital computer. The appropriate x and y lines are selected by the memory address register (MAR). The selection technique depends on the memory organization and will not be discussed in this application note. The most common organizations use one core per bit so the number of cores which must be sensed simultaneously is determined by the "word" length. However, each sense line links one bit for all words in the memory. When a particular word is selected the sense amplifiers detect the presence of "ones" or "zeroes" in all the bits and this information is then placed in the memory data register (MDR). The time required to get the information from the cores to the MDR is called the "access" time. If the memory is of the "destructive readout" type, the information in the MDR must be written back into the memory at the same location. The time required to do this is called the "write" time. The sum of the "read" and "write" times is defined as the cycle time and indicates the speed of the memory.

The various memory organizations use different sense line configurations and current drive techniques. However, in all the configurations the sense winding is routed so as to obtain an optimum signal-to-noise ratio. This generally means the sense winding goes through half the cores in one direction and half in the opposite direction (See Figure 2). The purpose of this wiring technique is to

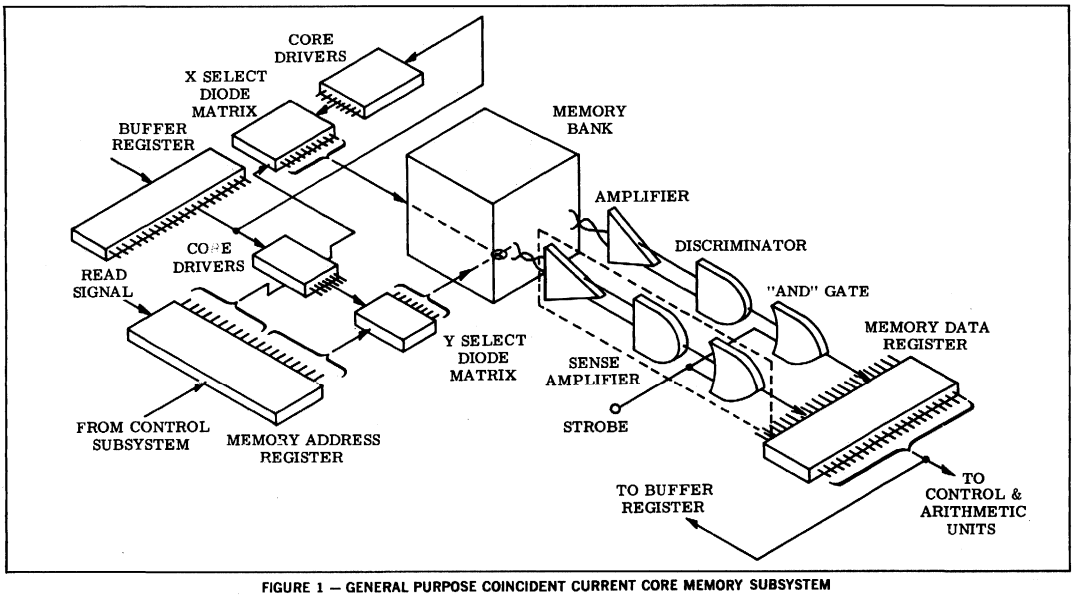


FIGURE 1 — GENERAL PURPOSE COINCIDENT CURRENT CORE MEMORY SUBSYSTEM

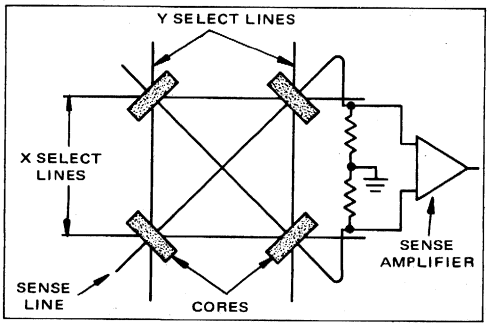


FIGURE 2 – HALF SELECT WIRING

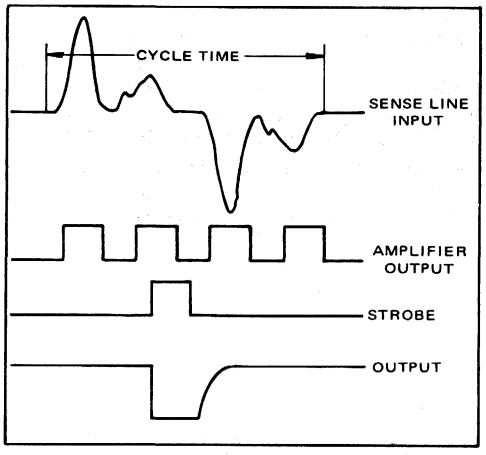


FIGURE 3a – TYPICAL SIGNAL WAVEFORMS

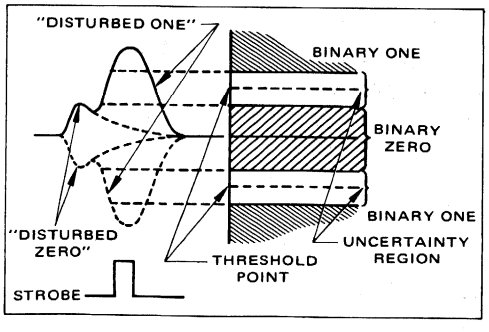


FIGURE 3b – TYPICAL CORE OUTPUT SIGNAL

cause voltages induced in the sense line to cancel. The sense amplifier must detect the difference between the minimum "disturbed one" signal and the maximum "disturbed zero" signal. The "disturbed one" signal can be either positive or negative so the sense amplifier must be bipolar (See Figure 3a).

Typical signal waveforms at the input to the sense amplifier, amplifier output, discriminator output, and strobe are shown in Figure 3a. This is an idealized signal waveform at the input to the sense amplifier. In actuality, there are common and differential mode noise at the input during most of the memory cycle. Figure 3b shows the typical signal as seen at the input to the sense amplifier. The amplitude of the "disturbed one" signal depends on the size of the core and the rise time and amplitude of the select currents from the core drivers. The area between the minimum "disturbed one" signal and the maximum sum of "disturbed zero" signals is called the uncertainty region (See Figure 3b). This area would ideally be as large as possible, since it is very important in the overall performance of the memory subsystem. Normally, the threshold of the sense amplifier will be set in the middle of the uncertainty region.

SENSE AMPLIFIER DESIGN CRITERIA

Many factors must be considered in the design of an integrated core memory sense amplifier. First, the amplifier should be as versatile as possible. The design must meet a wide variety of speed requirements and should be suitable for low cost fabrication. Additional criteria are:

1. The amplifier must be able to detect bipolar signals.
2. The threshold should be adjustable in order to meet the maximum number of requirements with a single amplifier.
3. The threshold should be constant with temperature. This requires the memory manufacturer to compensate the switching currents for the change in core output voltage rather than depend on the sense amplifier to have precisely the correct threshold versus temperature characteristic.
4. The uncertainty region should be as small as possible.
5. The power supplies should be commonly used values and the tolerances on these supplies should be as loose as possible.
6. The sense amplifier requires a strobe to "enable" the amplifier at the optimum point.
7. The bandwidth of the amplifier must be sufficiently high to pass the fastest rise time signals with as little degradation as possible.
8. The amplifier must be able to recover rapidly from large common mode and large differential mode signals.

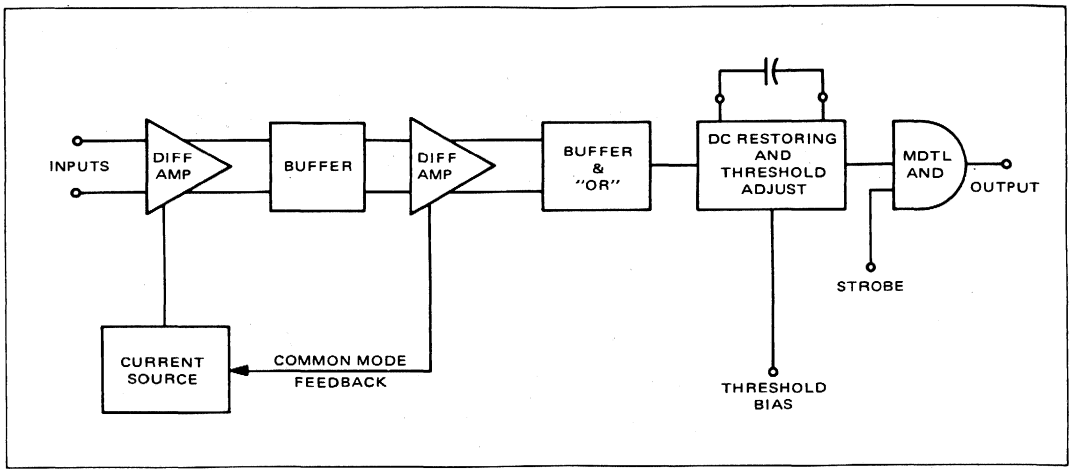


FIGURE 4 – BLOCK DIAGRAM OF MC1540

THE MC1540

Figure 4 is a block diagram of the MC1540. The amplifier portion is a two-stage differential amplifier with emitter degeneration in each stage, buffering between stages, and overall common mode feedback. The schematic of the amplifier section is shown in Figure 5. The low frequency differential voltage gain of the first stage, assuming it is driven from a voltage source, can be closely approximated by:

$$A_{diff} \approx \frac{R_L}{r_e + R_E + \frac{r_b}{\beta + 1}}$$

R_E is the emitter degeneration resistor on each side and r_e approximately $\frac{KT}{qI_E}$. With β relatively high, the last term in the denominator can be neglected and the equation for the gain reduces to the following equation:

$$A_{diff} \approx \frac{R_L}{r_e + R_E} = \frac{R_L}{R_E} \quad \frac{1}{1 + \frac{r}{R_E}}$$

This equation shows that the gain is a function of resistor ratios rather than resistor magnitudes. R_L and R_E are formed during the base diffusion so that the ratio R_L/R_E should be constant from run to run. Also, r_e is directly proportional to a resistor which is formed during the base diffusion and is a function of temperature so that gain variations with temperature change are to be expected. However, the gain variation will be significantly less than for a circuit with no emitter degeneration.

Since the amplifier incorporates differential gain of the first stage and single ended gain of the second stage, the overall gain can be approximated by the following equation:

$$A \approx \left(\frac{R_{L_1}}{r_{e_1} + R_{E_1}}\right) \left[\frac{R_{L_2}}{2(r_{e_2} + R_{E_2})}\right]$$

The buffering between the two stages significantly increases the bandwidth of the amplifier. Without buffering, the predominant pole would be caused by the Miller effect capacitance of the second stage being driven from a high impedance. Buffering reduces this impedance approximately by a factor of β of the transistor.

Some of the data taken on this amplifier in integrated form is shown below.

1. Voltage gain – The voltage gain on all units was between 37.5 dB and 40 dB.

2. Gain versus temperature – The gain changed less than 1.0 dB when the temperature was varied over a -55°C to +125°C range.

3. Bandwidth – The 3.0 dB point on all units was in excess of 50 MHz. The rise time of the amplifier was less than 7.0 ns.

4. Propagation delay – This was found to be between 8.0 and 11.0 ns on all units. The measurement was made between the 50% points of the input and the output waveforms. The rise and fall times of the input were approximately 10 ns and the amplitude was 25 mV.

5. Common mode rejection – The low level common mode rejection defined as the differential mode gain divided by the common mode gain, was found to be 57.0 dB at 10 MHz. Figures 6a and 6b show the amplifier response to a ± 1.0 volt and a ± 2.0 volt common mode input respectively. Figure 6c shows the amplifier response to a 20 mV differential input.

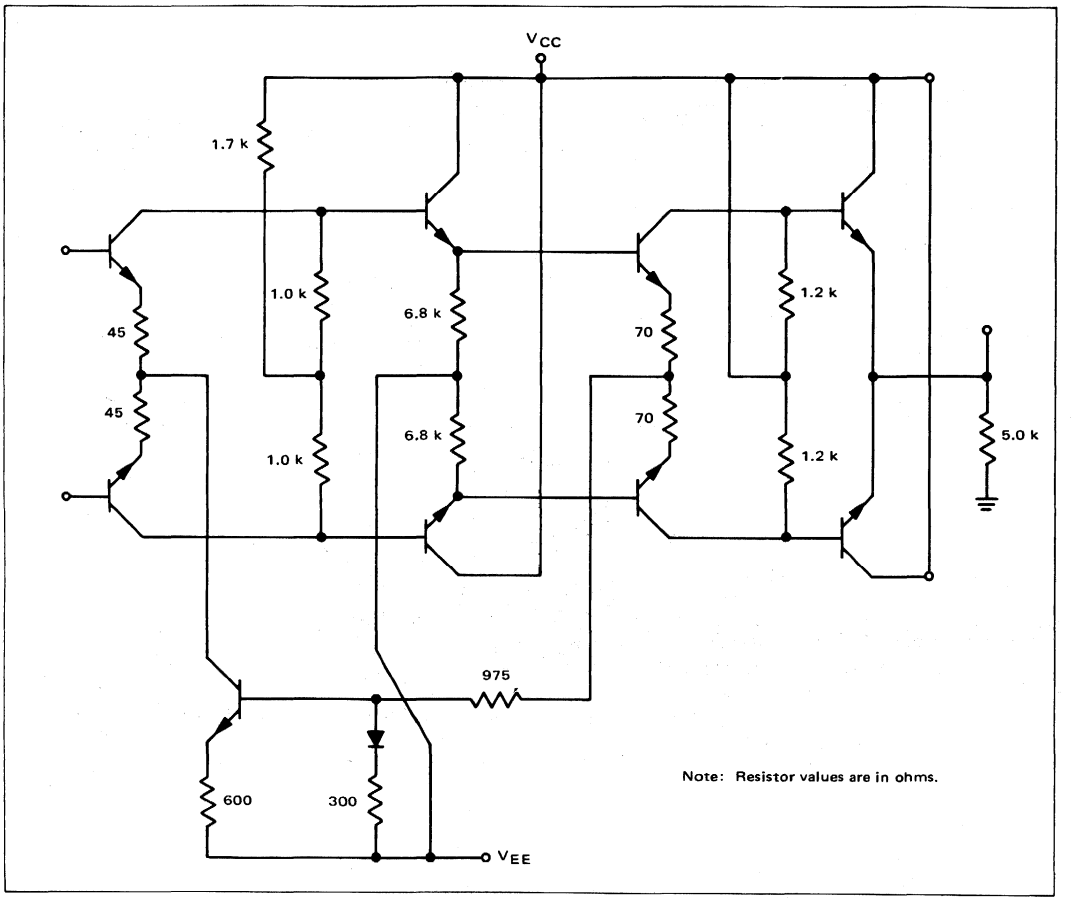


FIGURE 5 – DIFFERENTIAL AMPLIFIER SCHEMATIC

The schematic of the dc restoration circuit, the threshold adjusting circuit, and the output gate is shown in Figure 7. The threshold of the sense amplifier is dependent upon the dc voltage at point A. Since R1 is much larger than R2 or R3, changes in the dc voltage at point C reflects as a dc voltage change at point A; thus, the threshold changes.

The dc restoration action can be explained as follows: The input signal to the collector of Q_1 and the capacitor is positive from a low impedance and the entire signal is coupled through the capacitor. When the leading edge of the signal occurs at point A, both the base-emitter junctions of Q_1 and the gate input diode become reverse biased and the capacitor will start to charge through R4. When the negative going edge of the signal arrives at point A, Q_1 is turned on, and point A becomes a low impedance node because of the emitter follower action. The capacitor will discharge through Q_1 very rapidly. The base of Q_1 is driven by a low impedance source so that the transient base current during the time the capacitor is being discharged produces a negligible voltage change at the base of Q_1. Also Q_1 is designed to supply the maximum transient current required for pulse widths up to 750 ns. Since the dc level at the emitter of Q_1 is restored rapidly, the sense amplifier threshold does not change significantly with a change in duty cycle.

As temperature increases, the threshold of the DTL gate decreases by $2\ \Delta V_{BE}/^{o}C$. The four diodes in the base of Q_2 will decrease the dc level at the base of Q_2 by $4\ \Delta V_{BE}/^{o}C$. The V_{BE} change of Q_1 will cancel one of these, and the V_{BE} change of Q_2 will cancel another; hence the dc level at point A will also decrease by $2\ \Delta V_{BE}/^{o}C$. Therefore, if the amplifier voltage gain does not change with temperature, the sense amplifier threshold will be constant.

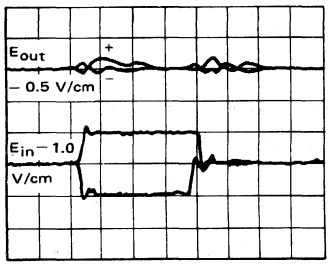


FIGURE 6a – COMMON MODE RECOVERY TIME (E_{in} = ± 1.0 V)

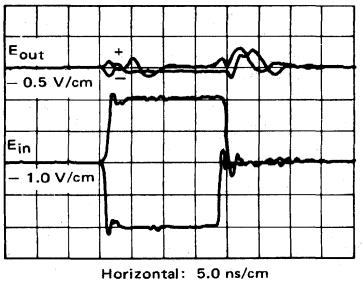


FIGURE 6b – COMMON MODE RECOVERY TIME (E_{in} = ± 2.0 V)

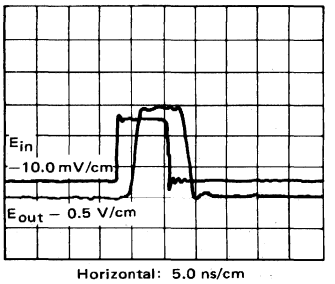


FIGURE 6c – AMPLIFIER RESPONSE TIME

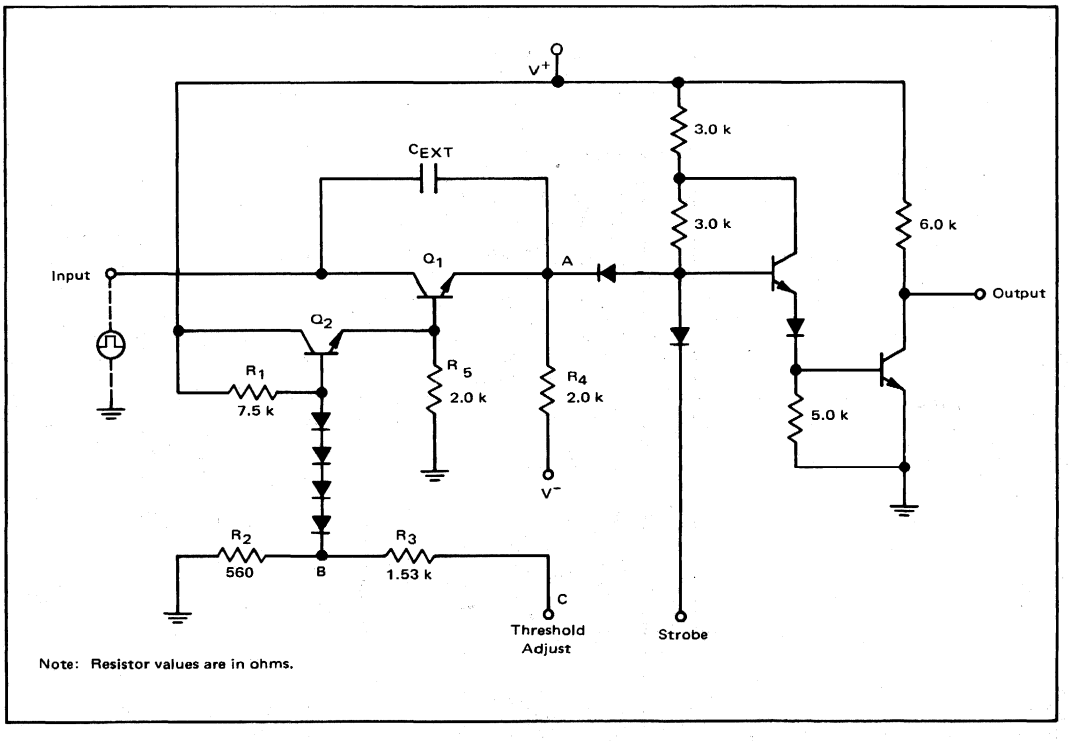


FIGURE 7 – DC RESTORATION CIRCUIT, THRESHOLD ADJUSTING CIRCUIT, AND OUTPUT GATE

The output gate is similar to that of the popular MDTL logic family. Both the amplified signal from the memory and the strobe signal must be above the gate threshold level before the output transistor will saturate. The output transistor is capable of "sinking" 6.0 mA with a saturation voltage less than 400 mV. This guarantees a noise margin equal to that of the MDTL logic family. Many sense amplifiers may be strobed from a common source with no ill effects, as long as the driving unit has sufficient fan-out capability. Also the outputs of several sense amplifiers can be wire-ORed. Figure 8 shows the voltage transfer characteristic of the gate. The width of the transition is approximately 200 mV. This would refer to the input of the sense amplifier as a transition width of 2.0 mV if the voltage gain was 100.

Additional data taken on the sense amplifier are listed below.

1. Threshold – 17 mV nominal for $V^- = -6.0$ V, $V^+ = +6.0$ V, and $V_{th} = -6.0$ V.
2. Threshold temperature coefficient – $-10\ \mu V/^oC$.
3. Threshold range – The nominal threshold varies from 13 mV at -5.0 V threshold bias to 21 mV at -7.0 V threshold bias.
4. Propagation delay from input to output – Typically 20 ns.
5. Propagation delay from strobe input to output – Typically 10 ns.

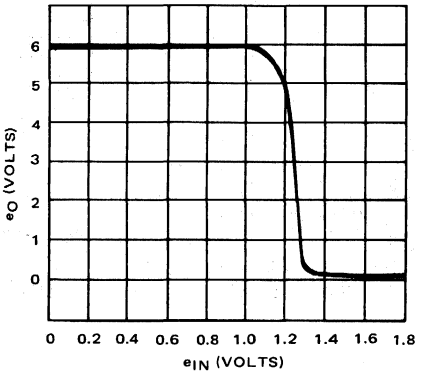


FIGURE 8 – OUTPUT GATE TRANSFER CHARACTERISTICS

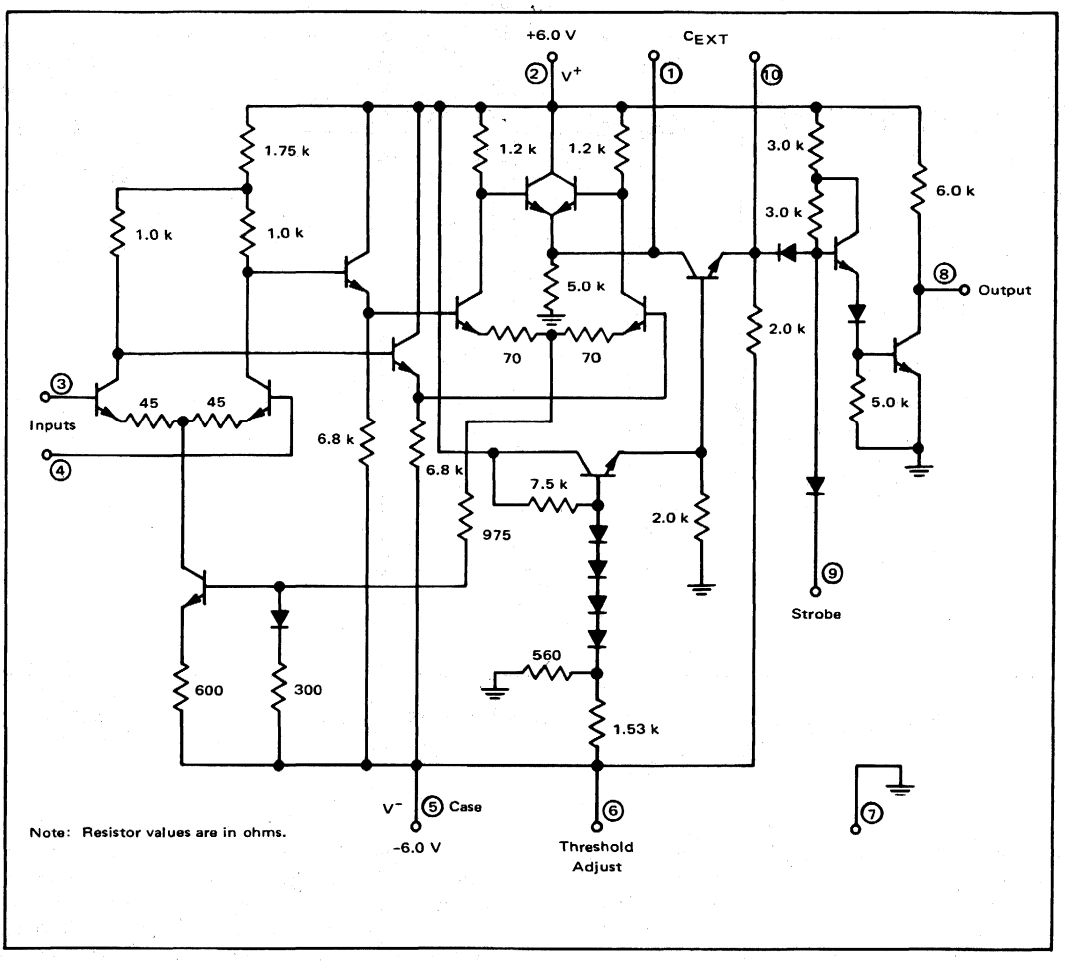


FIGURE 9 – CORE MEMORY SENSE AMPLIFIER

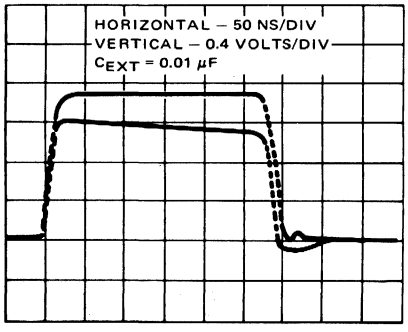


FIGURE 10 – SIGNAL WAVEFORM AT PINS ONE AND TEN

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Threshold	V_{th}	14	17	20	mV
Uncertainty Region			2	6	mV
Amplifier Voltage Gain	Av		80		
Propagation					
Input to Amplifier Output	$t_{3^+10^+}$			15	ns
Input to Gate Output	$t_{3^+8^-}$			30	ns
Strobe to Gate Output	$t_{9^+8^-}$			15	ns
Recovery Time					
e_{in} = ±400 mV (DM)	tr (DM)		20	50	ns
e_{in} = ±2.0 volts (CM)	tr (CM)		40	50	ns

Figure 9 is the schematic of the complete sense amplifier. External components that must be supplied are appropriate resistors for terminating the sense windings and a coupling capacitor. The size of the capacitor is dependent on the width of the disturbed "1" signal from the memory. The capacitor should be of sufficient size to ensure that the "sagging" due to the capacitor charging does not affect the threshold. Also the capacitor must be large enough so that noise, just before the disturbed "1" signal, does not affect the threshold. Figure 10 illustrates the charging and discharging time of a 0.01 μF capacitor. The typical excursion below the base line is approximately 100 mV for an input pulse 300 ns wide.

The rise time of the output can be decreased significantly by connecting an external resistor from the output to the positive power supply. This resistor must be large enough so that the sum of the current through the resistor and the current from an external load does not exceed the rated value of 6.0 mA if a 400 mV V_{sat} at +125°C is a required specification.

The sense amplifier also works fine with +5.0 V and -6.0 V power supplies. If the threshold-adjust pin is also tied to -6.0 V, the nominal threshold increases to approximately 20 mV. However, -5.3 volts on the threshold-adjust pin sets the nominal threshold at 17 mV for +5.0 V and -6.0 V power supply operation. If the threshold-adjust pin is tied to the negative power supply, the nominal threshold is also 17 mV for power supplies of +5.0 V and -5.0 V. Operation is marginal for ±4.5 V power supplies. Therefore it is recommended that ±5% supplies be used if the sense amplifier is operated with ±5.0 V power supplies.

SPECIFICATIONS

Specifications for a sophisticated integrated circuit must be such that the customer is guaranteed a circuit that will meet his requirements. The most important specifications for a sense amplifier are threshold limits (or uncertainty region), propagation delays, and recovery times. Other characteristics must also be limited so that good circuit performance and reliability result.

Some of the important specifications for the MC1540 are listed in the table above. For a complete specification and the manner in which each test is made, refer to the MC1540 data sheet.

SUMMARY

The MC1540 was designed with both customer requirements and integrated circuit production capabilities in mind. The circuit will operate properly with large variations in temperature and power supplies. It requires only three external components to achieve the complete core memory sense amplifier function. It has a saturated logic type output and can be strobed from any saturated logic family. It can be packaged in either the 10 pin TO-5, the 10 pin ceramic flat pack, or the dual in-line plastic package.

TRANSISTOR LOGARITHMIC CONVERSION USING AN INTEGRATED OPERATIONAL AMPLIFIER

INTRODUCTION

Many approaches have been made to the design of logarithmic amplifier circuits, using both active and passive elements. With the proper circuit configuration of diodes or transistors a log amplifier can be constructed using the logarithmic characteristics of these semiconductor devices. All diodes and transistors do not exhibit good logarithmic characteristics, so care must be taken in selecting the proper device. This application note deals with a technique for obtaining logarithmic conversion using operational amplifier-transistor feedback circuits, beginning with an analysis of the logarithmic characteristics of transistors. A brief look at the basic logarithmic amplifier will be given followed by two log function generator applications: direct multiplication of two numbers, and solution of the parabolic equation $Z = X^n$.

TRANSISTOR LOGARITHMIC CHARACTERISTICS

Shockley's first-order theory of a p-n junction

$$I = I_o [e^{(qV/kT)} - 1]$$

considers only diffusion current; however, it is popular because of its simplicity. In other circumstances the series resistance associated with the bulk semiconductor material must be accounted for. Also such mechanisms as surface inversion layers and generation-recombination in the space charge regions are not accounted for in the above expression. Consequently a diode or transistor configuration must be devised which will minimize these adverse effects. The common base transistor configuration discussed in this application note does this very well. By using the transfer conductance and fulfilling certain conditions, the desired logarithmic characteristics can be obtained.

The derivation of the transfer conductance is based around an NPN silicon all-diffused transistor as shown in Figure 1. The detailed derivation is given in the Appendix. The resulting collector current expression is

$$I_c = -\alpha_n I_{es} [e^{qV_E/kT}] \qquad (1)$$

It is important to note that a non-constant base transport factor will cause α_N to vary, consequently, a diffused base transistor such as the 2N2218 is best suited for this application. The base transport factor is within a few tenths of a percent of unity. The upper end range of equation (1) is usually between 1 and 10 mA of collector current depending upon the junction area and contact size of the transistor being used. Measurements elsewhere[1] indicate an 8 to 10 decade range of collector current yielding a logarithmic relation. Simple practical integrated circuit operational amplifiers operating with only a single polarity input are limited to from 3 to 7 decades depending upon the particular amplifier being used and also on the effort expended to reduce external disturbances.

LOGARITHMIC AMPLIFIER TRANSFER FUNCTION

The basic function generator configuration for logarithmically compressing data is shown in Figure 2. In this configuration the requirement that the collector voltage be equal to zero is virtually met. The small amount of collector potential that does exist will be negligible for all practical purposes. Rewriting equation (1) for the direction of collector current shown in Figure 2, we find

$$I_c = +\alpha_n I_{es} [e^{qV_E/kT}] \qquad (2)$$

If $I_b \ll I_c$, which is the condition that governs the lower limit of operation, then

$$I_c = \frac{E_{in}}{R_s} \qquad (3)$$

The polarity of V_E is shown in Figure 2. Combining equations (2) and (3) and the condition of $V_{out} = V_E$ yields

$$\frac{E_{in}}{R_s} = \alpha_n I_{es} [e^{qV_{out}/kT}]$$

or

$$V_{out} = \frac{kT}{q} \ln \frac{E_{in}}{R_s \alpha_n I_{es}}$$

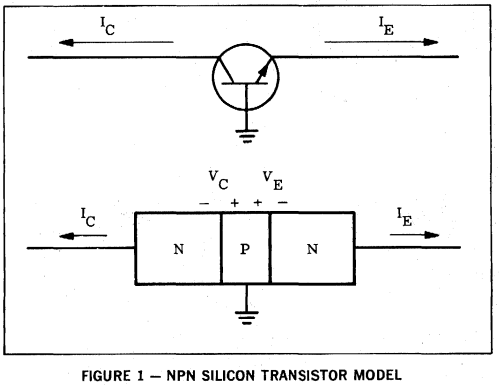


FIGURE 1 — NPN SILICON TRANSISTOR MODEL

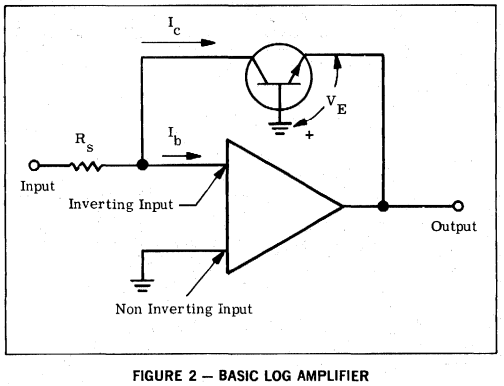


FIGURE 2 — BASIC LOG AMPLIFIER

Converting from $\ln_e$ to $\log_{10}$ gives

$$V_{out} = 2.3 \frac{kT}{q} \log_{10} \left(\frac{E_{in}}{R_s \alpha_n I_{es}}\right)$$

$$V_{out} = 2.3 \frac{kT}{q} \log_{10} (E_{in}) + 2.3 \left(\frac{kT}{q}\right) \log_{10} \left(\frac{1}{R_s \alpha_n I_{es}}\right) \quad (4)$$

at $T = 27°C$ $\quad \frac{kT}{q} = 0.026\,V$

$$V_{out} = 0.06 \log_{10} (E_{in}) + K \quad (5)$$

The empirical results obtained from the log amplifier are plotted in Figure 3a. From Figure 3a the transfer function was found to be

$$E_{out} = 0.062 \log_{10} (E_{in}) + 0.450 \quad (6)$$

where E_{out} and E_{in} are in volts.

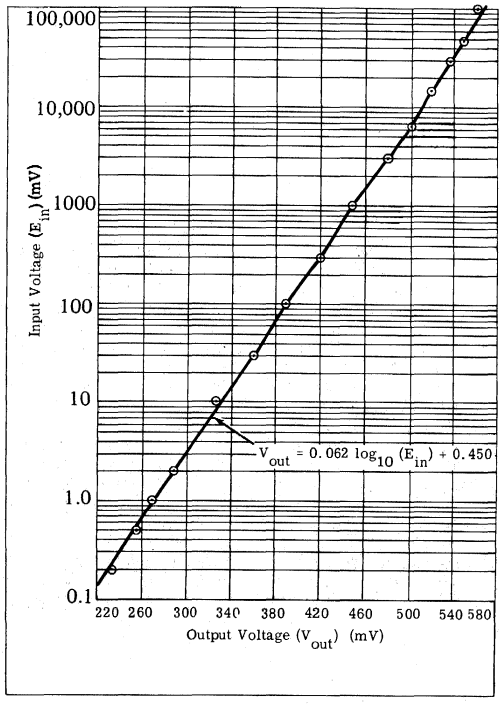


FIGURE 3a — INPUT VS. OUTPUT RESPONSE OF LOGARITHMIC AMPLIFIER OF FIGURE 3b

OPERATIONAL AMPLIFIER LOG AMPLIFIER

The operational amplifier used in the log amplifier is the MC1533. Frequency compensation of the operational amplifier is chosen such that the amplifier will be stable with a closed loop gain of unity. The 0.1 μF capacitor between pins 1 and 5 is necessary to reduce the ac gain of the feedback transistor. It is usually necessary to bypass the power supplies right at the amplifier socket with a 0.01 or 0.1 μF low-inductive capacitor to eliminate any internal high frequency oscillations which might occur because of excessive impedance in the power supplies.

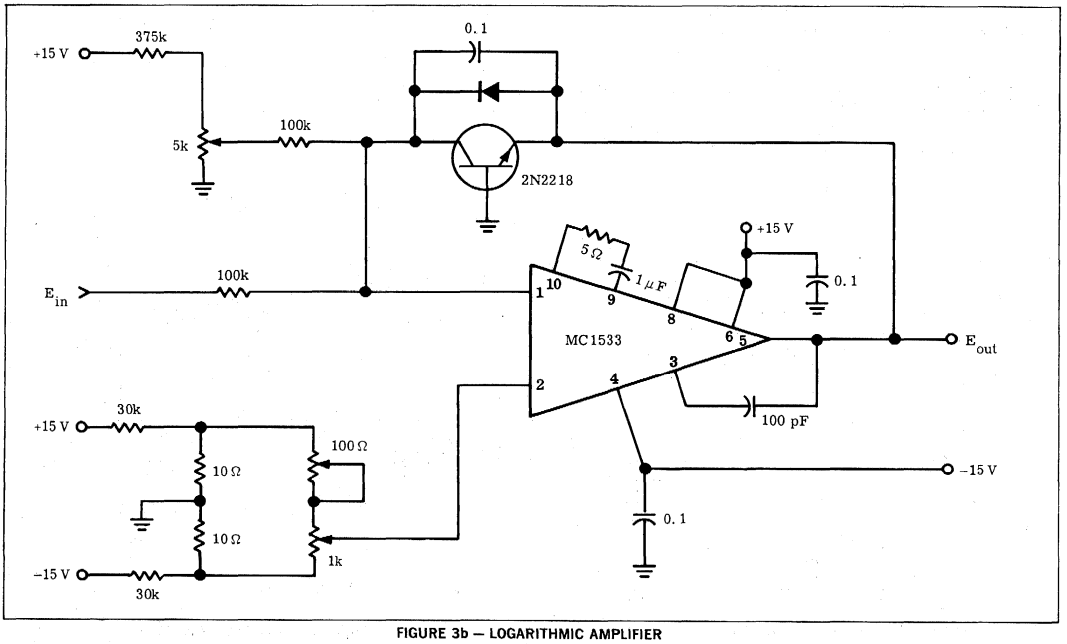


FIGURE 3b — LOGARITHMIC AMPLIFIER

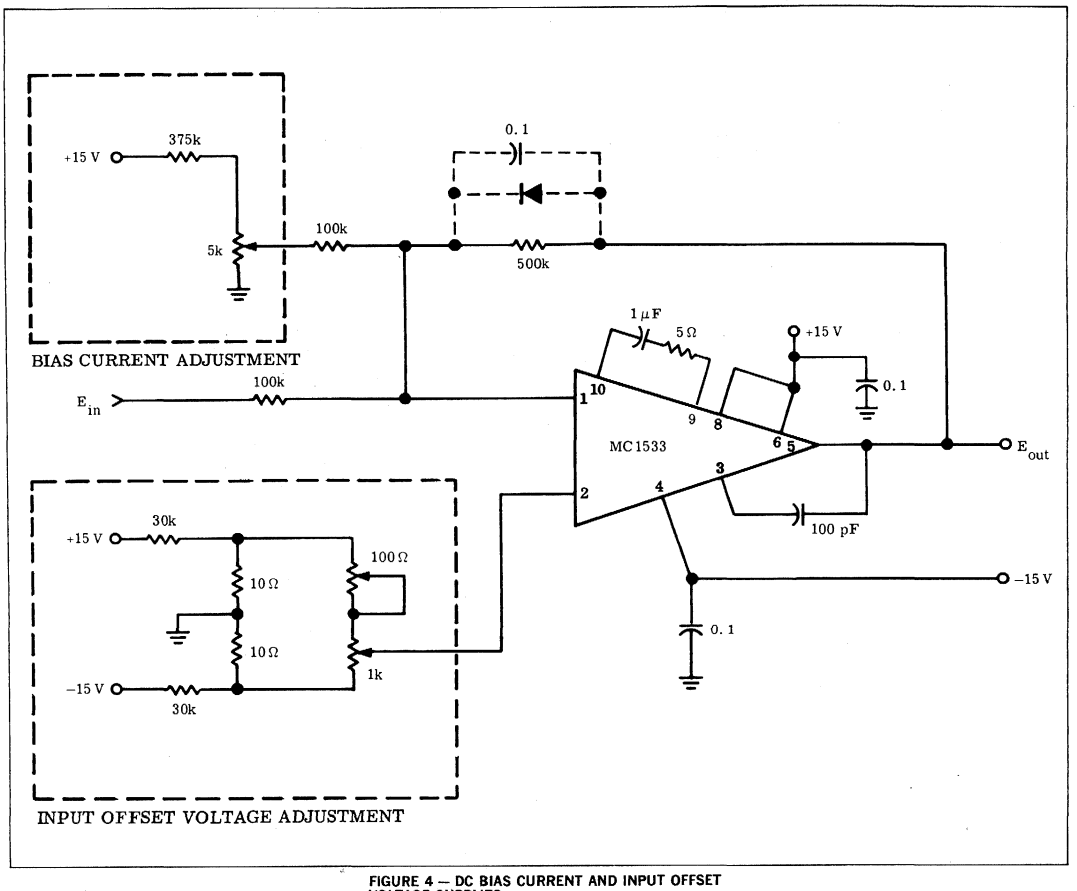


FIGURE 4 — DC BIAS CURRENT AND INPUT OFFSET VOLTAGE SUPPLIES

The extremely wide range of input voltage required makes it necessary that input offset voltage and bias currents be properly compensated for. The typical bias current for the MC 1533 is 0.5 μA. If the amplifier were used without proper bias current compensation, this would require an input voltage of 50 mV above a 100k input resistor just to overcome the bias current requirements. This would immediately swamp out the lower end input of a 4 to 5 decade log amplifier where input voltages are in the 1 to 10 mV range. Input offset voltage, which is reflected to the output by the closed loop gain of the amplifier, will cause an appreciable error, and must be compensated for with an external supply.

The method of dc compensation used is shown in Figure 4. The input offset voltage adjustment is made with pin 1 shorted to ground and E_{out} adjusted to zero. The bias current adjustment is accomplished by placing a 500k feedback resistor in place of the transistor and then monitoring E_{out} and E_{in} and adjusting the bias current pot until E_{out}/E_{in} = 500k/100k = 5 throughout the desired input range. This procedure must be carried out individually for each operational amplifier that is to be used as a log amplifier. After completion of the bias adjustments, the feedback resistor may be replaced by the feedback transistor in the configuration shown in Figure 3b.

The same type of bias current compensation is required in the $\log^{-1}$ amplifier where input voltage levels are in the 300 to 600 mV range. The offset voltage adjustment, however, may be replaced by approximately 100 ohms to ground, since the offset level is insignificant with respect to the input voltage range.

The effect of having an improperly adjusted offset voltage pot or bias current pot is demonstrated in Figure 5. It may be necessary to slightly adjust the bias current pot in order to straighten out the log characteristics, even after the initial adjustment procedure. It is extremely important in applications where log-analog operations are to be performed, that the logarithmic transistors have identical characteristic slopes. Level shifts are not important, since they can be easily adjusted for at the summing point of one of the internal amplifier stages as shown later in the multiplier circuit application.

MULTIPLICATION USING TRANSISTOR LOGARITHMIC CHARACTERISTICS

The following example explains a method of obtaining the product Z = XY. The circuit used is shown in Figure 6. The inputs and output are monitored in millivolts and the scale is selected such that one machine unit equals 10 mV. The circuit can be broken into three por-

tions: the input logarithmic amplifier, the summing point amplifier, and the output $\log^{-1}$ amplifier. The frequency compensation for each amplifier is the same as that shown in Figure 3b.

A. Input Logarithmic Amplifier: Each input in this portion of the product function generator is identical to that shown in Figure 4, with the feedback resistor replaced by the log transistor. Initial adjustments must be carried out in the same manner as discussed previously. The output of amplifier #1 will be of the form

$$E_{out(1)} = -(\text{alog } X + C_1) \quad (7)$$

and amplifier #2 will be identical except for the constant C_1

$$E_{out(2)} = -(\text{alog } Y + C_2) \quad (8)$$

The constants C_1 and C_2 are in the order of 300 mV while a = 62 as determined previously from Figure 3a.

B. Summing Point Amplifier: The output of this amplifier will be

$$E_{out(SPA)} = \text{alog } X + \text{alog } Y + C_1 + C_2 - E_c$$

$$= \text{alog } XY + C_1 + C_2 - E_c \quad (9)$$

The input required for the output $\log^{-1}$ amplifier stage must be of the form alog XY + C_3. With the proper selection of E_c the term $C_1 + C_2 - E_c$ can be made equal to C_3, resulting in the required input of the $\log^{-1}$ amplifier stage.

C. Output Log^{-1} Amplifier: This stage uses a 2N2906 transistor connected in a common base configuration at the input of the operational amplifier to achieve an anti-logarithmic amplifier. This stage must have a base current supply added to avoid having base current drawn from the input voltage. Distortion in the $\log^{-1}$ characteristic would result without this supply. The initial calibration of this stage must be determined by plotting input voltage $E_{in(OLA)}$ versus output voltage on semi-log paper and adjusting the 5 k base current pot until a straight line is obtained over the desired output range.

The results obtained from this circuit configuration are tabulated in Table 1 along with the correct product and percent error. Up to 7.7% error in output voltage was observed over the 3 decades of operation; however, simple calculations indicate that a 0.35% error in $E_{in(OLA)}$ will cause a 10% error in output voltage at the upper end of the output range. A 0.51% error in $I_{in(OLA)}$ will cause a 10% error in output voltage at the lower end of the output range. It becomes apparent why both an input offset voltage adjustment supply and a base current adjustment supply must be provided for where wide ranges of input or output voltages are to occur.

ANALOG SOLUTION OF THE PARABOLIC $= X^n$ EQUATION $Z = X^n$

The circuit shown in Figure 7 was used to generate Z for three different values of "n" (3, 2, and 0.5). The results are shown in Figures 8, 9, and 10, respectively. The value of E_c (summing point amplifier) is positive for $n > 1$ and negative for $n < 1$. As shown in Figure 7, E_c is positive and "n" is equal to 3. It is important here that the ratio of R_f/R_s be selected accurately to avoid additional error in the computation of X^n. The degree of accuracy maintained was 8% for "n" = 3, 9% for "n" = 2, and 5% for "n" = 0.5. As in the output stage of the previous application, a very small percentage error in input will increase more than an order of magnitude at the output.

Temperature variation will cause large deviations in output voltage accuracy since the output voltage of the first stage is directly proportional to temperature in degrees Kelvin.

$$E_{out(1)} = T[2.3(\frac{k}{q})\log_{10}(E_{in}) + 2.3(\frac{k}{q})\log_{10}(\frac{1}{R_s \alpha_n I_{Es}})]$$

The temperature effect will cancel itself if the junction temperatures of the input and output transistors are kept equal. Methods of obtaining the required temperature equalization might be the use of a common heatsink for all the log transistors, use of multiply packaged transistors, or ultimately the use of a monolithic chip containing the logarithmic transistors. A multiply packaged transistor MD 985 (PNP-NPN) was tried in the $Z = X^3$ configuration and resulted in an output error reduction of from 8% maximum to 4% maximum.

CONCLUSION

A diffused base transistor operating in a common base emitter follower configuration, with the collector at zero potential, has a wide range of logarithmic impedance. This configuration can be used to obtain a logarithmic compression of input data over 6 decades of operation with an error of less than 1%. The author feels that additional range could be obtained by the use of a chopper stabilized operational amplifier. Two arithmetic problem solution applications were shown; however, accuracy was limited by temperature variations, interstage inaccuracies, and resistor ratio inaccuracies over the three decades of input and output swing. A monolithic configuration of log transistors is felt to be the best method of compensation for temperature effects.

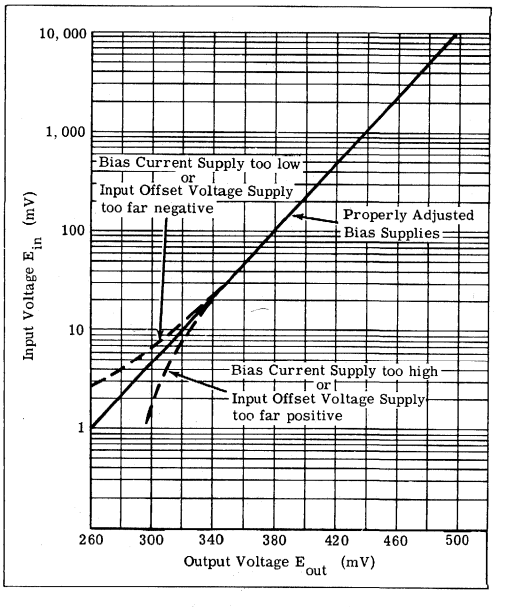


FIGURE 5 — IMPROPER DC COMPENSATION EFFECTS

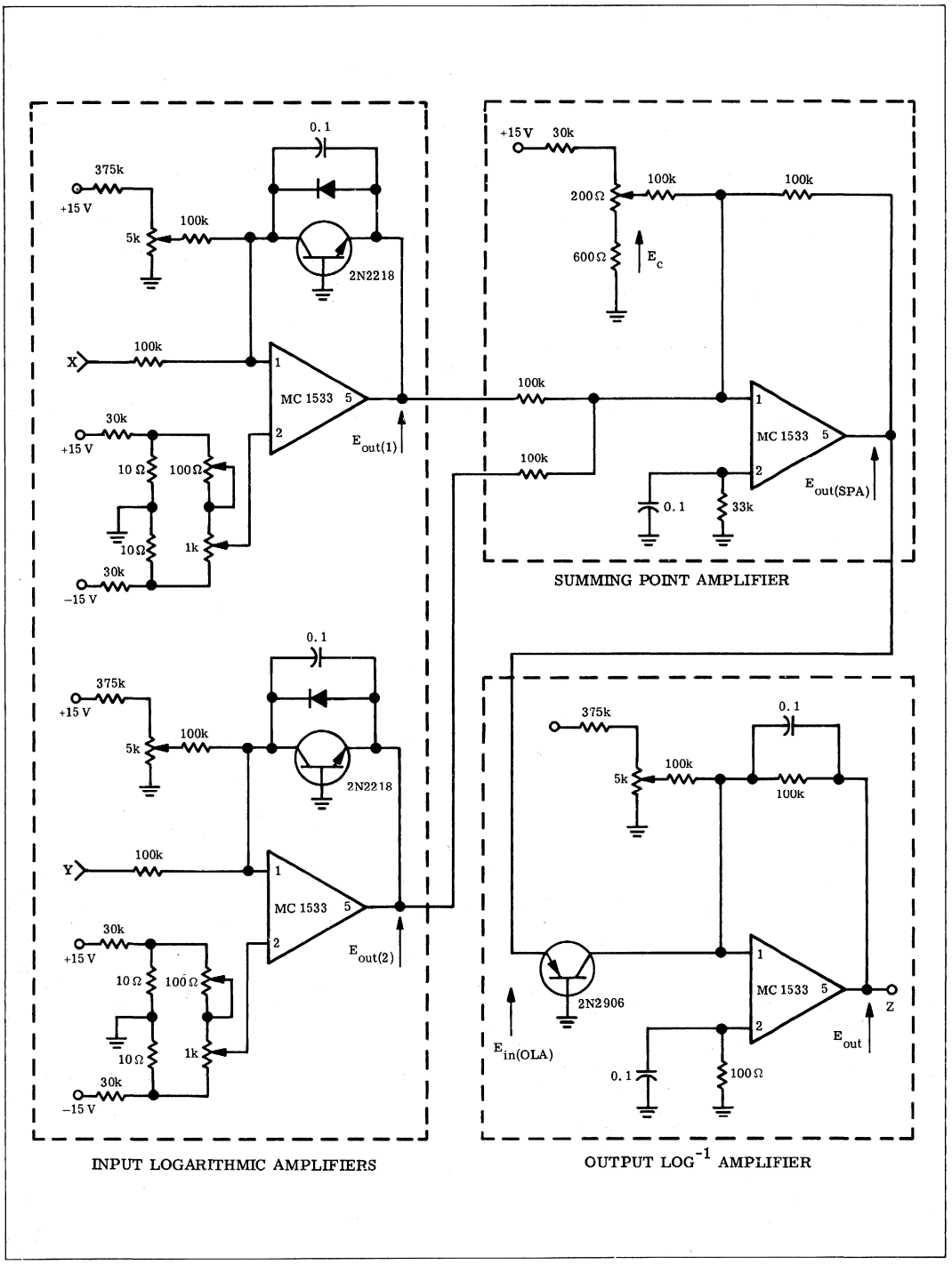


FIGURE 6 — CIRCUIT FOR Z = XY FUNCTION GENERATOR

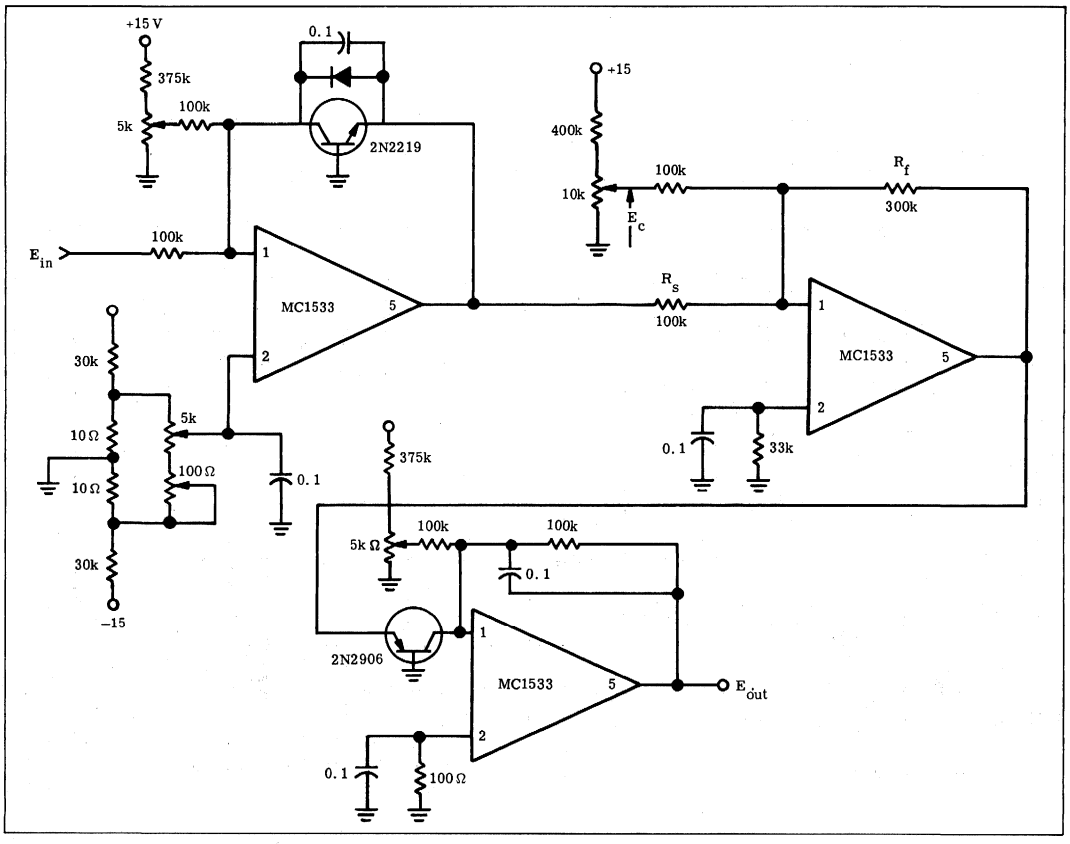


FIGURE 7 — CIRCUIT FOR COMPUTING $Z = X^n$

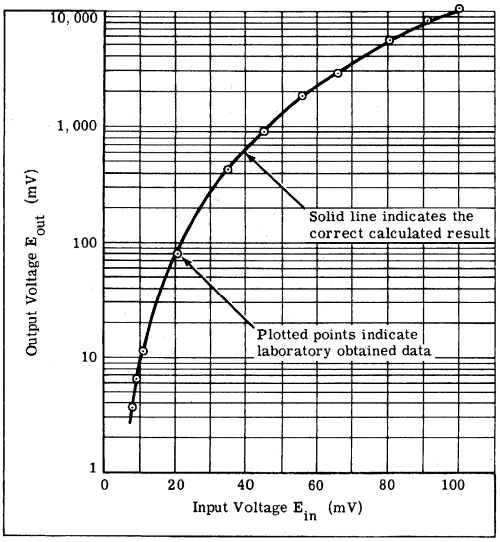


FIGURE 8 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 2

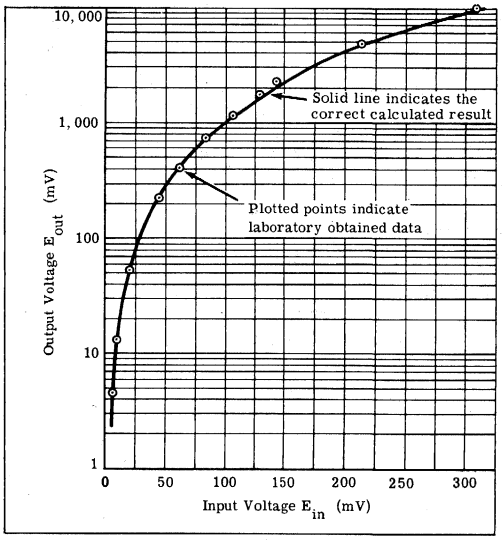


FIGURE 9 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 3

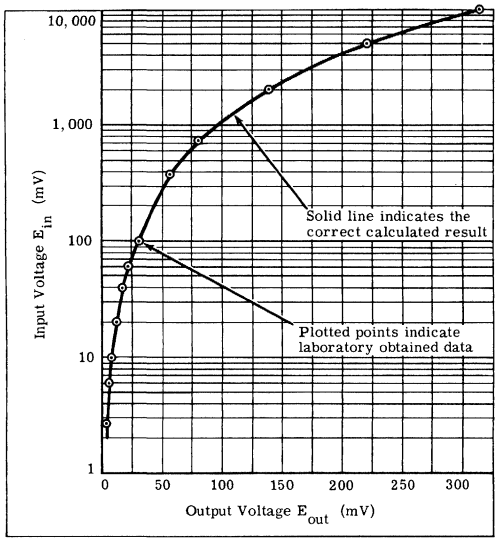


FIGURE 10 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = ½

X Input #1	Y Input #2	Z Output	Calculated Z = XY	Difference	% Error
0.995 mV	13.8 mV	14.0 mV	13.72	0.28	2.04
	81 mV	82.4 mV	80.6	1.8	2.2
	297 mV	308 mV	295.5	12.5	4.2
	605 mV	695 mV	647	48	7.4
	1.042 V	1.110 V	1.038	0.072	6.9
	1.346 V	1.44 V	1.338	0.102	7.7
	2.98 V	2.99 V	2.965	0.025	0.8
	4.99 V	5.04 V	4.97	0.07	1.4
	10.11 V	10.34 V	10.06	0.28	2.8
	12.97 V	12.5 V	12.4	0.1	0.8
4.0 mV	14.44 mV	47.0 mV	57.8	0.8	1.4
	40.9 mV	154.9 mV	163.8	8.9	5.4
	102.3 mV	397 mV	410	13	3.2
	250 mV	1.02 V	1.00	0.02	2.0
	500 mV	2.05 V	2.00	0.05	2.5
	730 mV	3.08 V	2.95	0.13	4.4
	1.003 V	4.28 V	4.02	0.26	6.5
9.8 mV	7.45 mV	72.9 mV	73	0.1	0.14
	14.5 mV	143 mV	142	1	0.7
	40.9 mV	407 mV	401	6	1.5
	85 mV	837 mV	833	4	0.48
	199 mV	2.04 V	1.95	0.09	4.6
	250 mV	2.54 V	2.45	0.09	3.7
50 mV	14 mV	754 mV	700	54	7.7
	50 mV	2.56 V	2.5	0.06	2.4
	102 mV	5.31 V	5.10	0.21	4.1
	155 mV	7.94 V	7.75	0.19	2.5
	207 mV	10.38 V	10.35	0.03	0.29
	250 mV	12.54 V	12.50	0.04	0.32
100.3 mV	5.6 mV	598 mV	562	36	6.4
	14.5 mV	1.44 V	1.455	0.015	1.0
	50 mV	4.91 V	5.02	0.11	2.2
	102 mV	10.2 V	10.23	0.03	0.29
	120 mV	11.87 V	12.04	0.17	1.4
499 mV	5.07 mV	2.48 V	2.53	0.05	2.0
	10.08 mV	5.02 V	5.04	0.02	0.4
	20.15 mV	9.30 V	10.07	0.77	7.7

TABLE I — TABULATED RESULTS FROM MULTIPLIER CIRCUIT Z = XY

APPENDIX

The emitter current of Figure 1 is given by the expression

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] \qquad (10)$$

where I_{ES} = emitter reverse saturation current
I_{CS} = collector reverse saturation current
α_I = inverted common base current gain

The collector current is given by

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (11)$$

where α_n = normal common base current gain.

Equations (1) and (2) must be modified to include those adverse components such as surface leakage currents and space charge generated currents. Since these currents generally behave as majority carriers in the base region, they are consequently not collected and do not appear at the collector junction. These currents may be included in equations (10) and (11) as follows:

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] + \Sigma\, I_{ES_i}[e^{qV_E/kTm_i} - 1] \qquad (12)$$

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] + \Sigma\, I_{CS_j}[e^{qV_C/kTm_j} - 1] \qquad (13)$$

If we now set $V_C = 0$ in equation (13) we find

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (14)$$

For $V_E > 100$ mV, equation (14) reduces to

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT}] \qquad (15)$$

REFERENCES

1. William L. Paterson: Multiplication and Logarithmic Conversion by Operational Amplifier-Transistor Circuits. The Review of Scientific Instruments, Vol. 34, No. 12, Dec. 1963.
2. Leo L. Wisseman: A High Voltage Monolithic Operational Amplifier. Integrated Circuits Application Note, AN-248.

APPLICATIONS OF THE MC1530 -31 INTEGRATED OPERATIONAL AMPLIFIERS

I. INTRODUCTION

The MC1530 and MC1531 operational amplifiers in Figures 1 and 2 are constructed to best utilize the advantages of monolithic integrated circuits. Such advantages as low offset voltage and current, excellent temperature tracking, increased reliability, small size, and reduced cost make the integrated circuits more attractive than many discrete operational amplifiers now in use. On the other hand, many discrete operational amplifiers now in use are of such high quality that their performance cannot presently be equaled by monolithic, high production integrated amplifiers. This condition exists because of the present state-of-the-art of monolithic integrated circuit processing technology. Therefore, a performance cost trade-off must be evaluated when the integrated circuit amplifier is considered for design into any system.

The purpose of this application note is to assist the circuit and system designer in evaluating the performance of the MC1530 and MC1531 amplifiers. This is accomplished by first explaining the detailed A.C. and D.C. operation of each stage in the circuits and some of the constraints on the circuit design that exist because of monolithic fabrication.

After the circuitry and constraints are explained, the amplifiers are applied to four basic operational amplifier applications: a summing amplifier, an integrator, a d.c. comparator, and transfer function simulation. These applications are only representative of the many that could be used, but they indicate that the MC1530 and MC1531 integrated amplifiers are extremely useful low cost tools.

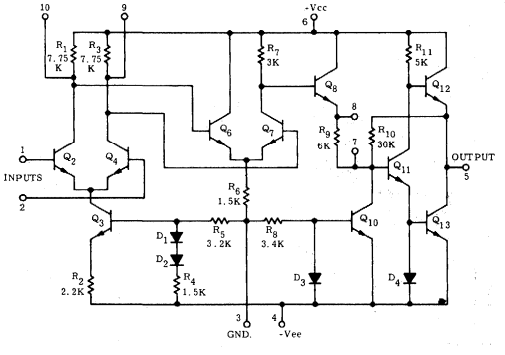


FIGURE 1 — MC1530

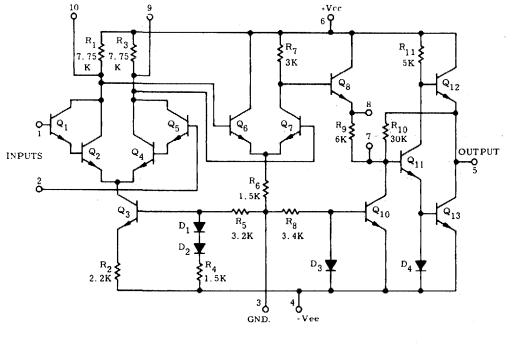


FIGURE 2 — MC1531

II. FABRICATION CONSTRAINTS ON PERFORMANCE

In fabricating an amplifier on a single monolithic chip, the first consideration is the resistivity of the epitaxial layer used for building the components by diffusion processes. Collector-emitter breakdown voltage and collector saturation resistance of transistors are direct functions of the epitaxial resistivity—the higher the resistivity, the higher the breakdown voltage and the higher the collector saturation resistance. High breakdown voltages are desired, while high saturation resistances are undesirable. For the MC1530-31 operational amplifiers, breakdown voltages of 20 volts are achieved while saturation resistances are less than 50 ohms. Therefore, the maximum output voltage swing of 16 volts peak to peak (using ±9 volt supplies) does not approach breakdown in the output devices. At the same time, the collector saturation resistance does not affect the ability to drive loads down to 500 ohms.

In any integrated amplifier, it is very important that critical d.c. levels be a function of resistor ratios and not absolute values. In the MC1530-31, the output d.c. level is a function of only resistor ratios—not of the absolute value of any resistor or of the beta of any device in the circuit. Therefore, the variation of the output voltage with temperature is very small and the major contributor to this variation is any mismatch of the input circuitry. In addition, the open loop gain is very stable: 72 db ± 1.5 db from T = -55°C to T = +125°C.

The ability to match very closely the V_{be} and beta of the input transistors is a strong function of the manner in which these devices are placed on the monolithic chip. By placing these devices very close to each other, the diffusion profiles match each other very closely resulting in very low input offset voltages and currents. In addition, when the devices are very close together thermal gradients across the chip are minimized resulting in excellent tracking with temperature. The MC1530-31 offset voltages of 2 mv and drift of 3.8 $\mu v/^{o}C$ indicates proper layout of the devices on the chip.

Both the MC1530 and MC1531 are fabricated on one monolithic die and the amplifier dies, without wire bonds, are identical. The two circuits, when viewed from their external connections, are distinct from each other because the MC1530 has two internal wire bonds that are not in the MC1531. These two connections convert the Darlington compound circuit used in the MC1531 to a single transistor, resulting in the MC1530 circuit. The two versions offer the circuit designer the option of high gain (5000) and moderate input impedance (10K) or moderate gain (2500) and high input impedance (1 megohm). In addition, the use of two versions with modified input stages requires only two pins for input connections. The biasing, output, and ground leads require four pins, leaving four pins that may be used for internal connections. This allows the popular ten pin TO-5 package to be used and gives the designer a great deal of flexibility in using the four internal points for shaping open loop response, modifying slew rate, noise suppression, etc.

III. CIRCUIT OPERATION

The MC1530 or 31 amplifier can be conveniently considered as a multi-stage amplifier. The MC1530 circuit is redrawn in Figure 3 with dotted lines used to separate the complete circuit into a series of stages. A brief description of the operation and d.c. biasing of each stage in Figure 3 follows:

A. Input Differential Amplifier

Transistors Q_2 and Q_4 differentially amplify the input signal, and Q_3 is a temperature compensated current source used primarily to provide a high common mode rejection.

First considering a.c. operation of the input circuit, the differential voltage gain of the amplifier is given by:

$$A_V \approx \frac{R_L}{r_{e1}} \qquad (1)$$

where R_L = effective load resistance: R_1 or R_3 in parallel with the input impedance of the second stage.

$$r_{e1} \approx \frac{26}{I_e(mA)}$$

(I_e is the emitter current of either Q_2 or Q_4)

For the first stage (as shown later) $I_e \approx 0.5$ mA so that $r_e \approx 52$ ohms. The differential input impedance to the second stage is approximately $2\beta r_{e_2} \approx 5.0$ K ohms; therefore,

$$R_L = \frac{(5K)\ (7.75K)}{12.75\ K} = 3.02 \text{ K ohms.}$$

From (1) the differential voltage gain of the first stage is:

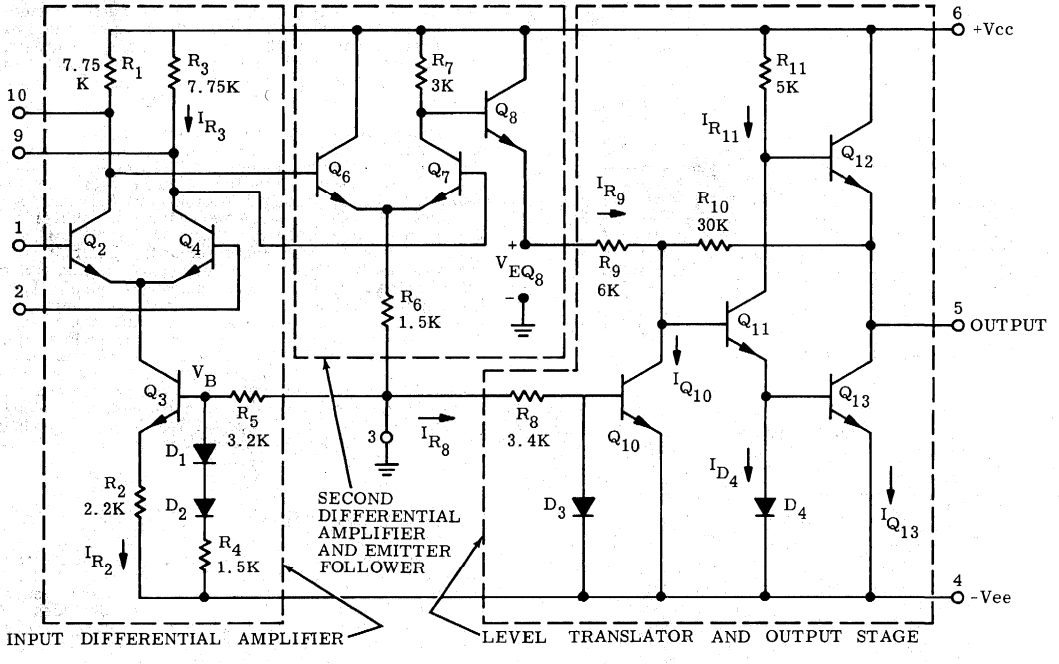
$$A_v \approx \frac{3.02K}{52} \approx 58.5$$

As will be seen later, this is the highest voltage gain stage in the amplifier. A high gain first stage is desirable in order to minimize the effects of V_{be} and β mismatch in the following stages; i.e., any offset in the second differential amplifier is not amplified by the high gain first stage.

The collectors of the first stage are wire bonded to pins 9 and 10 to provide connection points for open loop frequency compensating networks. By using frequency compensation in the first stage of operational amplifiers, the best slew rate* may be obtained. If a single capacitor is used for compensation; it is easily seen that the above statement is true, since voltage variation between the input collectors is smaller at the front than at any other point in the amplifier. Therefore, the time required for the capacitor to reach a fully charged value is minimized. By using this type of compensation a maximum slew rate of 4.5 volts /μ-sec can be obtained from the amplifier when compensated to assure a stable closed loop gain of unity. The MC-1530-31 data sheet shows a curve of slew rate versus the value of capacitance used between pins 9 and 10. Therefore, the circuit designer can first compensate the open loop response to assure closed loop stability and then use the data sheet to determine a typical maximum slew rate.

Before the second stage of the circuit is considered, it is necessary to determine the d.c. voltage from the collectors of the first stage to ground, since these voltages will establish the second stage operating point. In addition, the d.c. voltages from the collector of Q_2 and Q_4 to ground and from the base of Q_3 to ground determine the maximum common mode swing of the amplifier. In all calculations from Figure 3, it is assumed that the base-emitter voltage of transistors and diode forward voltage is approximately 0.7 volts and that base currents are negligible. In addition, the voltages are assumed positive with respect to ground as shown in Figure 3 and the currents in the direction shown.

*Slew rate is defined as the maximum rate of change of output voltage with respect to time: $\frac{\Delta e_o}{\Delta t}$.



NOTES

(1) ALL DIODE FORWARD VOLTAGES AND BASE-EMITTER VOLTAGES ARE APPROXIMATELY 0.7 VOLTS.

(2) ALL BASE CURRENTS ARE NEGLECTED

(3) NOTATION: V_{BQ_3} IS READ AS THE POSITIVE TO NEGATIVE VOLTAGE FROM BASE TO GROUND FOR Q_3; V_{EQ_8} IS FROM THE EMITTER OF Q_8 TO GROUND, ETC.

FIGURE 3

The starting point in biasing the amplifier is the calculation of the current generated by current source Q_3. This may be done by calculating the voltage on the base of Q_3 and using this voltage to determine the current through R_2, which is approximately the value of the current source:

$$V_{BQ_3} \approx \frac{(-Vee + 2(0.7))\, R_5}{(R_4 + R_5)} \qquad (2)$$

$$I_{R_2} \approx \frac{Vee + (V_{BQ_3} - 0.7)}{R_2} \qquad (3)$$

For Vee = 6 volts, $V_{BQ_3} \approx -3.14$ V and $I_{R_2} \approx 1.0$ ma.

If it is assumed by a first approximation that the integrated transistors are perfectly matched, one-half the collector current of Q_3 will flow through Q_4 and one-half through Q_2 so that the current through R_3 or R_4 is:

$$I_{R_3} = I_{R_4} = \frac{1}{2R_2}\left[Vee - 0.7 - \frac{(Vee - 1.4)\, R_5}{(R_4 + R_5)}\right] \qquad (4)$$

Finally, the voltage on the base of Q_6 or Q_7 is:

$$V_{BQ_6} = V_{BQ_7} = Vcc - I_{R_3} R_3$$

$$= Vcc - \frac{R_3}{2R_2}\left[Vee - 0.7 - \frac{(Vee - 1.4)\, R_5}{(R_4 + R_5)}\right] \qquad (5)$$

For Vcc = Vee = 6 volts, $V_{BQ_6} = V_{BQ_7} \approx 2.2$ volts.

(Observe that only the magnitude of the power supply voltages are used in all calculations, the sign is taken into account in the above equations.) The calculated values of V_{BQ_3} and V_{BQ_6} or V_{BQ_7} determine the maximum input common mode voltage range. When using ± 6 volt supplys, this range is ± 2 volts maximum.

B. Second Differential Amplifier

The second differential stage provides additional voltage gain ($A_V \approx 20$) and the output is taken from Q_7 (single-ended), through emitter follower Q_8. Since this amplifier will not have an appreciable input common mode swing, the resistor R_6 is used as a current source, and provides adequate common mode rejection. Before proceeding to the third stage, the D. C. voltage at the emitter of Q_3 must be calculated, since this voltage level is essential to the understanding of the level translator and the output stage. The results of this calculation are shown in equation (6); details are omitted but the method is identical to that used in the first stage calculations.

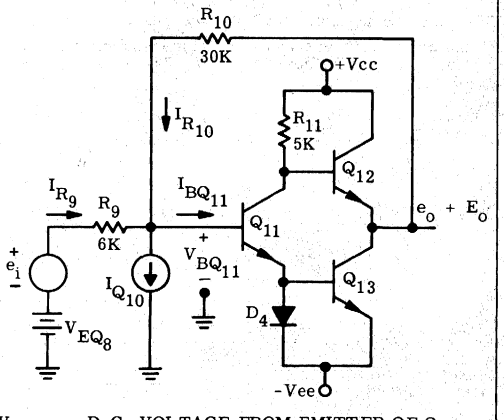
$$V_{EQ_8} = Vcc - \frac{R_7}{2R_6}\left(Vcc - \frac{R_3}{2R_2}\left[Vee - 0.7V - \frac{(Vee - 1.4V)\, R_5}{(R_4 + R_5)}\right] - 0.7\ V\right) - 0.7\ V \qquad (6)$$

For Vee = Vcc = 6 volts, $V_{EQ_8} \approx +3.82$.

C. Level Translator and Output Stage

The problem of level translation arises because of the need for large peak to peak voltage swings at the amplifier output. Since symmetrical a.c. swings are desired the d.c. output voltage should be zero volts; i.e. the amplifier output varies positive and negative about ground. In addition, this voltage should be zero volts so that no current will flow in d. c. coupled loads when the differential input voltage is zero volts. The mismatching of V_{be} and β in the input transistors can cause the d.c. output level to move drastically away from zero volts, and this effect is considered in the next section. However, if the voltage at the emitter of Q_8 (+3.8 volts) is d.c. coupled with gain through the output stage then the output will be between +3.8 volts and the positive supply. Therefore, a d. c. level translation problem exists between the emitter of Q_8 and the output: the +3.8 d. c. voltage must be reduced to zero volts at the output, and the amplifier must be d.c. coupled between the two points.

The circuit of Figure 4 is derived from Figure 3, and will be used to explain the operation of level translation and the output stage. The circuitry in Figure 3 from the emitter of Q_8 to the output may be driven from a voltage source since the impedance seen looking into the emitter of Q_8 is very low. The representation is shown in Figure 4, with e_i representing the a.c. variation at the emitter of Q_8 and V_{EQ_8} the d.c. voltage to ground. In addition, transistor Q_{10} (Figure 3) acts as a d. c. current source and is drawn as such in Figure 4. The value of $I_{Q_{10}}$ may be calculated from Figure 3 as follows:



V_{EQ_8} - D.C. VOLTAGE FROM EMITTER OF Q_8 TO GROUND (+3.8 VOLTS WHEN Vcc = Vee = 6 VOLTS)

e_i - A.C. VOLTAGE GENERATOR

$I_{Q_{10}}$ - D.C. CURRENT SOURCE (COLLECTOR CURRENT OF Q_{10} IN FIGURE 3)

e_o - A.C. OUTPUT VOLTAGE

E_o - D.C. OUTPUT VOLTAGE

$V_{BQ_{11}}$ - D.C. VOLTAGE FROM BASE OF Q_{11} TO GROUND $V_{BQ_{11}} \approx -(Vee - 1.4V)$

FIGURE 4

(1) The current I_{R_8} is given by:

$$I_{R_8} \approx \frac{Vee - 0.7}{R_8}$$

(2) If the diode D_3 matches identically the base emitter junction of Q_{10}, then the emitter current of Q_{10} will be identical to I_{R_8}. Then:

$$I_{Q_{10}} \approx I_{R_8} \approx \frac{Vee - 0.7}{R_8} \quad (7)$$

and $I_{Q_{10}}$ is a constant current.

From Figure 4, the D.C. output voltage may be derived by assuming $e_i = 0$ and $e_o = 0$:

$$I_{R_9} = \frac{V_{EQ_8} - V_{BQ_{11}}}{R_9} = \frac{V_{EQ_8} + Vee - 1.4}{R_9} \quad (8)$$

Observe that I_{R_9} is essentially constant since V_{EQ_8} and Vee are constant. Then, summing currents at the base of Q_{11}:

$$I_{R_9} + I_{R_{10}} = I_{Q_{10}} + I_{BQ_{11}} \quad (9)$$

For purposes of explanation, assume that $I_{BQ_{11}}$ can be neglected. The error caused by neglecting $I_{BQ_{11}}$ will appear in the expression for output voltage. If this error resulted in $e_o = 0.5$ volts D.C. instead of 0 volts, when referred to the input it results in an equivalent input offset voltage of 0.1 mv (for an open loop gain of 5000). This value is insignificant compared to a 0.1 mv V_{be} mismatch on the input transistors since input mismatches are multiplied by the open loop gain. Therefore, (9) reduces to:

$$I_{R_9} + I_{R_{10}} \approx I_{Q_{10}} \quad (10)$$

From Figure 4:

$$E_o = I_{R_{10}} R_{10} + V_{BQ_{11}} \quad (11)$$

and

$$V_{BQ_{11}} \approx -(Vee - 1.4V) \quad (12)$$

Then,

$$E_o \approx (I_{Q_{10}} - I_{R_9}) R_{10} + V_{BQ_{11}} \quad (13)$$

Substituting equations (7) and (8) into (12) and simplifying:

$$E_o \approx Vee\left(\frac{R_{10}}{R_8} - \frac{R_{10}}{R_9} - 1\right) - V_{EQ_8}\left(\frac{R_{10}}{R_9}\right) + 1.4\left(1 + \frac{R_{10}}{R_9} - \frac{R_{10}}{2R_8}\right) \quad (14)$$

Observe that the d.c. output level is a function of resistor ratios and not of the absolute value of any resistor. Substituting Vee = 6 volts, $V_{EQ_8} = 3.82$ volts, and the values of resistors shown in Figure 3, into (14):

$$E_o \approx 0.046 \text{ volts}$$

Therefore, the +3.82 volt d.c. level at the emitter of Q_8 has been translated to essentially 0 volts (within the range of approximation: if $V_{EQ_8} = 3.8292$ volts, then $E_O = 0$ volts) by the use of feedback and current summing into a constant current source at the base of transistor Q_{11}.

If $E_O = 0$ volts, the remaining D.C. biasing currents may be calculated:

$$I_{R_{11}} \approx \frac{Vcc - 0.7}{R_{11}}$$

$$I_{R_{11}} \approx 1.06 \text{ ma for Vcc} = 6 \text{ volts}$$

Since the current through diode D_4 is approximately $I_{R_{11}}$, the current through the output transistors may be found. Previously it was stated that if the diode D_4 matched identically the base-emitter junction of Q_{13}, then $I_{Q_{13}} = 1.06$ ma. For the MC-1530-31, the base-emitter junction of Q_{13} is 3 times larger than the area of D_4 so that:

$$I_{Q_{12}} \approx I_{Q_{13}} \approx 3(I_{D_4}) \approx 3.18 \text{ ma}$$

Therefore, the MC-1530 will drive load resistors as low as 1 K to a maximum peak to peak swing of approximately 11 volts.

Using the equivalent circuit of Figure 4, the a.c. voltage gain of the output stage is:

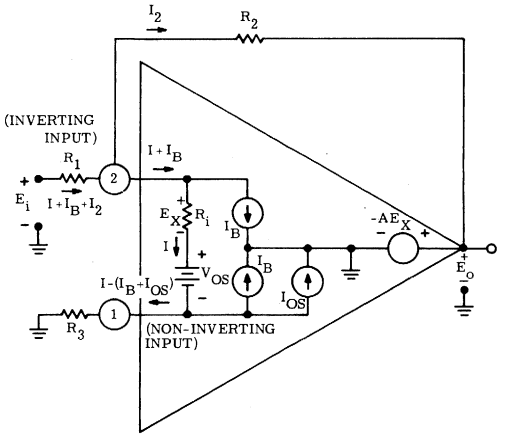
$$A_V \approx \frac{e_o}{e_i} \approx \frac{R_{10}}{R_9} \approx 5$$

(assuming that the input impedance to the base of Q_{11} is very high). Therefore, for an output peak to peak voltage swing of 10 volts (±5), the D.C. levels are adequate throughout the amplifier, and the complete open loop voltage gain is typically 6000.

IV. APPLICATIONS

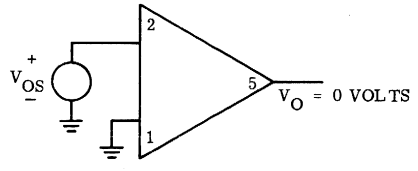
A. D.C. Biasing

In this section, the operational amplifier is considered in terms of the d.c. voltages and currents that can be measured at the input and output terminals. These measurable quantities are shown in an equivalent circuit for the amplifier in Figure 5; and are also defined in the figure. In addition, the general case of resistances, from each input to ground and negative feedback are considered by connecting R_1, R_2, and R_3 as shown.



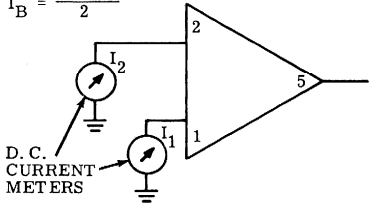
OUTPUT IMPEDANCE $<50\Omega$ AND IS NEGLECTED

V_{OS} = INPUT OFFSET VOLTAGE (VOLTAGE NECESSARY TO CAUSE V_O = 0 AS SHOWN)



I_B = AVERAGE INPUT BIAS CURRENT

$$I_B = \frac{I_1 + I_2}{2}$$



I_{OS} = INPUT OFFSET CURRENT = $I_1 - I_2$

A = OPEN LOOP VOLTAGE GAIN = E_o/E_2

R_i = INPUT RESISTANCE

E_i = D.C. INPUT VOLTAGE

E_o = D.C. OUTPUT VOLTAGE

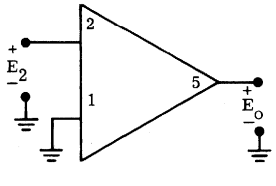


FIGURE 5 — D.C. MODEL FOR OPERATIONAL AMPLIFIER

Using the currents and voltages as shown in Figure 5, the following equations are written:

$$E_i - V_{OS} = (I + I_B + I_2)\,R_1 + IR_i + \left[I - (I_{OS} + I_B)\right]R_3 \tag{15}$$

$$-E_o + V_{OS} = -\left[I - (I_B + I_{OS})\right]R_3 - IR_i + I_2R_2 \tag{16}$$

In addition, from the model:

$$I = \frac{E_X}{R_i} = -\frac{E_o}{AR_i} \tag{17}$$

Solving for I_2 from (16) and substituting the result and equation (17) into (15) the equation for output voltage is:

$$E_o = \frac{-KE_i + V_{OS}(K+1) + KI_BR_1 - (K+1)(I_B + I_{OS})R_3}{1 + \frac{K}{A}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K+1}{K}\right]\right) + \left[\frac{K+1}{K}\right]\right]} \tag{18}$$

where $K = R_2/R_1$.

The K term in (18) represents the closed loop voltage gain if the amplifier was ideal. The term:

$$V_{OS}(K+1) + KI_BR_1 - (K+1)(I_B + I_{OS})R_3 \tag{19}$$

is the d.c. error at the output caused by offset voltages and currents and bias current, while the term:

$$\frac{K}{A}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K+1}{K}\right]\right) + \left[\frac{K+1}{K}\right]\right] \tag{20}$$

is the error caused by $R_i \neq \infty$ and $A \neq \infty$.

The results in equations (18), (19), and (20) can be extended to the a.c. case when e_i = a.c. input voltage and the resistances are replaced by impedances. Care must be taken, however, to prevent <u>both</u> Z_1 and Z_2 from becoming infinite at d.c. (a.c. coupling) since base current I_B will then be blocked to one side of the amplifier. In extending the analysis to a.c. the following equation is obtained:

$$e_o(S) = \frac{-K(S)\,e_i(S)}{1 + \frac{K}{A}(S)\left[\frac{1}{Z_i}\left(Z_1(S) + Z_3(S)\left[\frac{K(S)+1}{K(S)}\right]\right) + \frac{K(S)+1}{K(S)}\right]}$$

$$+ \frac{V_{OS}(K(0)+1) + K(0)I_BZ_1(0) - (K(0)+1)(I_B + I_{OS})Z_3(0)}{\frac{K}{A}(0)\left[\frac{1}{R_i}\left(Z_1(0) + Z_3(0)\left[\frac{K(0)+1}{K(0)}\right]\right) + \frac{K(0)+1}{K(0)}\right]} \tag{21}$$

where $S = \sigma + jw$ (complex frequency) or $S = jw$ for steady state calculations and $K(S) = Z_2(S)/Z_1(S)$ and $K(0) = Z_2(0)/Z_1(0)$.

Equation (21) concisely gives: the a.c. closed loop voltage gain K(S) for the ideal case, the error as a function of frequency in the denominator, and the output offset voltage caused by the d.c. value of the impedances Z_1, Z_2, and Z_3 divided by the d.c. error. The numerator of the latter term is very useful:

$$\text{D.C. output offset} = V_{OS}(K(0)+1) + K(0)I_B Z_1(0) - (K(0)+1)(I_B + I_{OS}) Z_3(0) \qquad (22)$$

and will be used later in this report for several calculations.

B. Open Loop Frequency Compensation

As previously explained, four internal points in the amplifier are wire bonded to external pins 7, 8, 9, and 10 for frequency compensation. The criterion for unconditional stability when resistive negative feedback is used is that the open loop voltage gain must have a 6db/octave slope when passing through 0 db. When using the MC-1530-31, if no external capacitors are connected to pins 7, 8, 9, or 10 the amplifier does not oscillate without feedback. However, as shown by the uncompensated open loop gain slope on the data sheet, it is virtually impossible to close the loop and keep the amplifier stable. Therefore, consider first the use of pins 9 and 10 for open loop frequency compensation.

As previously shown, the differential gain of the first stage with a capacitor C between pins 9 and 10 is:

$$A_{V_1} \approx \frac{Z_L}{r_{e1}} \qquad (23)$$

Figure 6 shows the representation of Z_L when a capacitor is used:

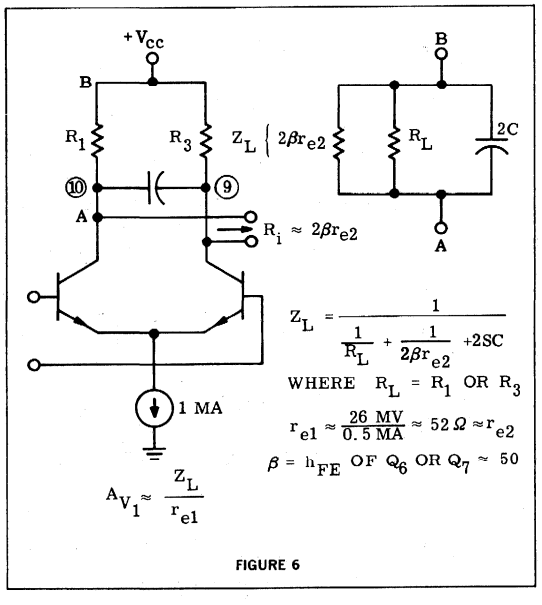


FIGURE 6

$$Z_L = \frac{1}{\frac{1}{R_1} + \frac{1}{2\beta r_{e2}} + 2SC} \qquad (24)$$

Substituting (24) into (23) and simplifying:

$$A_{V_1}(S) \approx \frac{1}{2r_{e1}C}\left[\frac{1}{S + \frac{(R_L + 2\beta r_{e2})}{4\beta R_L r_{e2} C}}\right] \qquad (25)$$

Since the gain equation for the first stage is to determine the frequency response, the complete expression for the open loop gain is:

$$A_{VOL} = A_{V_1}(S)A_{V_2}A_{V_3} \approx 100\, A_{V_1}(S)$$

since

$$A_{V_2} \approx 20 \text{ and } A_{V_3} \approx 5$$

or,

$$A_V(S) \approx \frac{50}{r_{e1}C}\left[\frac{1}{S + \frac{(R_1 + 2\beta r_{e2})}{4\beta R_1 r_{e2} C}}\right] \qquad (26)$$

The d.c. value of the open loop gain is:

$$A_V(0) \approx \frac{100}{r_{e1}}\left[\frac{2\beta R_1 r_{e2}}{R_1 + 2\beta r_{e2}}\right] \approx 6000 \qquad (27)$$

which checks with previous calculations and the typical value on the MC-1530 data sheet. The -3 db value of $A_V(S)$ can be used to find the 3 db frequency using (26) and (27). At $\omega = \omega_{3db}$ $A_V(\omega_{3db}) = 0.707\, A(0)$, so that

$$0.707\left[\frac{100}{r_{e1}}\left[\frac{2\beta R_1 r_{e2}}{R_1 + 2\beta r_{e2}}\right]\right] = \frac{50}{r_{e1}C}\left[\frac{1}{j\omega_{3db} + \left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right]}\right] \qquad (28)$$

Simplifying and solving for ω_{3db}:

$$\omega_{3db} = \sqrt{\frac{1}{(4.24 \times 10^3)C}\left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right] - \left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right]^2} \qquad (29)$$

Using $\beta \approx 50$, $r_{e_2} \approx 50$, $R_1 = 7.75$ K, and Vcc = Vee = 6 volts:

$$\omega_{3db} \approx \frac{1.09 \times 10^{-4}}{C} \qquad (30)$$

One method of using the above equations to compensate the amplifier is to first specify the frequency at which $|A_V(\omega)| = 0$ db. For the MC-1530 amplifier, the uncompensated response shown on the data sheet indicates a pole at 1 mc. This pole could arise because of a collector-substrate parasitic, or from the parasitic capacitance of a diffused resistor. Therefore, the open loop compensated gain can be specified to go through 0 db at 1 mc so that this pole can be avoided. From (26):

$$\left|A_V(\omega)\right| = \frac{50}{\omega r_{e1} C} \qquad (31)$$

when,

$$\omega >> \frac{R_1 + 2\ r_{e2}}{4\ R_1 r_{e2} C}$$

For $\left|A_V(\omega)\right| = 1.0$ at $\omega = 2\pi(1 \times 10^6)$ and $re_1 \approx 50\Omega$,

$$C \approx \frac{50}{50(2\pi)(10^6)} \approx 0.16\ \mu f$$

Using a standard value of capacitance C = 0.1 μf, the gain-crossover point from (28) is:

$$f = \frac{50}{(50)(2\pi)(0.1 \times 10^{-6})} = 1.6 \text{ mcs}$$

The 3 db break frequency may be calculated from (27), with C = 0.1 μf:

$$f_{3db} \approx \frac{1}{2\pi}\left(\frac{1.09 \times 10^{-4}}{1 \times 10^{-7}}\right) \approx 174 \text{ cps}$$

As seen on the MC-1530 data sheet, the 0.1 μf capacitor causes the gain to pass through 0 db at 1.4 mcs with $f_{3db} \approx 230$ cps. Therefore, the above equations can be used as a very good approximation to predict the frequency response.

When the MC-1531 amplifier is used, a good approximation to the open loop compensated gain is simply to divide the MC-1530 gain expression by 2:

$$A_{V_{0L}}(S) = \frac{25}{r_{e1} C}\left[\frac{1}{S + \frac{(R_1 + 2\ r_{e2})}{4\beta R_1 r_{e2} C}}\right] \qquad (32)$$

Therefore, the 3 db frequency expressions previously derived will also be approximately divided by 2 when the same value of C is used in the MC-1531.

As pointed out earlier, the best slew rate may be obtained by compensating the amplifier at pins 9 and 10. However, it sometimes becomes necessary to use a lead network to compensate the open loop gain. The points at pins 7 and 8 are provided for this purpose, as shown in the block diagram of Figure 7. From Figure 7:

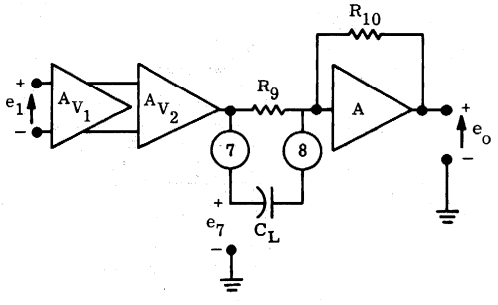


FIGURE 7

$$\frac{e_o}{e_1} = \frac{e_o}{e_7}\frac{e_7}{e_1} \approx A_{V_1} A_{V_2} \frac{e_o}{e_7}$$

where

$$\frac{e_o}{e_7} \approx \frac{R_{10}}{R_9}\ (SR_9C_L + 1)$$

So that the open loop voltage gain can be lead compensated:

$$A_{V_{0L}} \approx A_{V_1} A_{V_2}\left(\frac{R_{10}}{R_9}\left[SR_9C_L + 1\right]\right) \qquad (33)$$

By using all four frequency compensation points, there are many combinations and impedances that may be used to compensate the amplifier. Lead-lag compensation is accomplished by using both of the methods previously discussed at the same time. Another method of compensation that is extremely useful is the use of a capacitor from the output (pin 5) to ground and a capacitor from output to the base of Q_{11} (pin 7). This configuration is used on the MC-1530/31 data sheet primarily for suppression of internally generated broad-band noise voltages. The rms noise voltage at the output can be reduced to 100 uv using this compensating technique, but care must be taken with lead lengths on the external capacitors to avoid oscillations at high frequencies.

C. Specific Applications

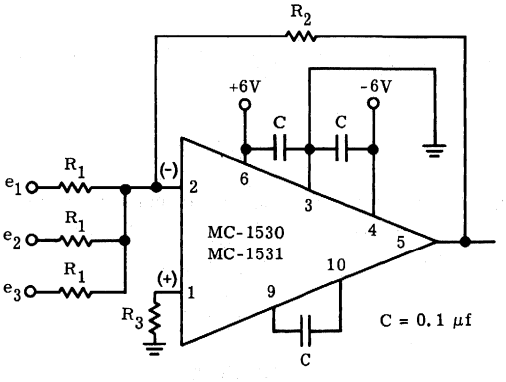


FIGURE 8 – SUMMING AMPLIFIER

1. Summing Amplifier

The MC-1530 or 31 is connected as a summing amplifier as shown in Figure 8. The input resistors used for summing are equal so that the ideal gain is:

$$e_o = \frac{R_2}{R_1}(e_1 + e_2 + e_3) \qquad (34)$$

Using equations (19) and (20), the d.c. summing errors may be calculated, but R_1 must be modified in the following manner. If $E_i = 0$ in Figure 5, the d.c. offset is that shown by equation (19). However, in Figure 8 three resistors are used instead of one so that:

$$R_1 \text{ equivalent} = \frac{R_1}{3}$$

Then the d.c. offset error (V_E) is:

$$V_E = V_{OS}(K' + 1) + I_B\left[R_2 - (K' + 1)R_3\right] - (K' + 1)I_{OS}R_3 \quad (35)$$

where

$$K' = \frac{3R_2}{R_1}$$

Using (35), R_3 may be selected to set the error due to bias current I_b equal to zero:

$$I_B\left[R_2 - (K' + 1)R_3\right] = 0$$

or

$$R_3 = \frac{R_2}{K' + 1} = \frac{R_2R_1}{3R_2 + R_1} \quad (36)$$

then

$$V_E = V_{OS}(K' + 1) - I_{OS}R_2 \quad (37)$$

The error due to $A_{VO} \neq \infty$ and $R_i \neq \infty$ (E) is:

$$E = \frac{K'}{A_{VOL}}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K' + 1}{K'}\right]\right) + \frac{K' + 1}{K'}\right] \quad (38)$$

Proceeding with the design of the summing amplifier, assume that the desired output is:

$$e_o = e_1 + e_2 + e_3$$

If $R_1 = R_2 = 10K$, then the ideal amplifier output voltage would be:

$$e_o = (e_1 + e_2 + e_3)$$

From (36),

$$R_3 = \frac{(10K)(10K)}{(30K) + (10K)} = 2.5K$$

From (37), the calculated d.c. offset voltage using typical MC-1530 data sheet values for V_{OS} and I_{OS} is:

$$V_E = (1 \times 10^{-3}) + -(2 \times 15^{7})(1 \times 10^{4}) = 2 \text{ mv}$$

(V_E = -12mv for the MC-1531 with a typical V_{OS} = -3mv).

The calculated error due to imperfections is less than 1% and is neglected. Measured data on the MC-1530 and MC-1531 is shown in Table I, and compares very favorably with the calculated values.

Using the compensating scheme of Figure 8, the summing amplifier may be used to accurately sum a.c. voltages up to the closed loop band width of approximately 1 mc. A maximum output swing of 10 volts peak to peak may be obtained up to 1 KC (see data sheet for output swing vs frequency).

TABLE I.

$R_1 = R_2 = 10K$ (±1%) $R_3 = 2.5K$ (±1%)

	MC-1530	MC-1531
Offset Voltage ($e_1 = e_2 = e_3 = 0$)	+2 MV	-15 MV
$e_o(e_1 = e_2 = 1V; e_2 = e_3 = 0V)$	-0.9985 V	-1.015 V
$e_o(e_1 = e_2 = 1V; e_3 = 0V)$	-1.9990 V	-2.0163 V
$e_o(e_1 = e_2 = e_3 = 1V)$	-2.9983 V	-3.014 V

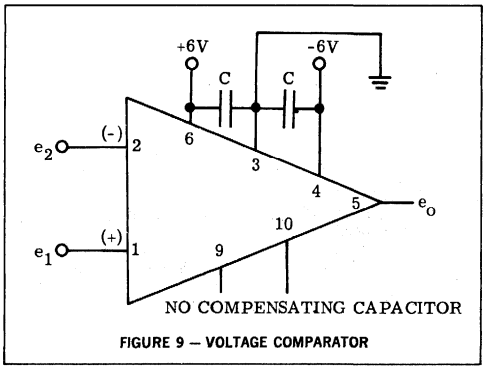


FIGURE 9 — VOLTAGE COMPARATOR

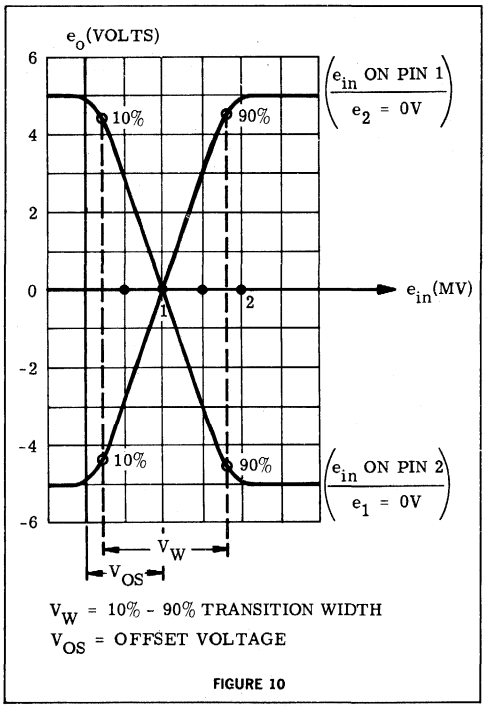


FIGURE 10

2. Voltage Comparator

The MC-1530-31 may be used as a voltage comparator as shown in Figure 9. The input output transfer characteristics of the device is shown in Figure 10, and the voltages of interest are defined for the case where either pin 1 or pin 2 is grounded and the input voltage is applied to the other pin. Observe from Figure 9 that the MC-1530 or 31 can be used without rolloff capacitors; i.e., the amplifier is open loop stable without compensation. The circuit of Figure 9 compares the input voltage with zero volts, but could be used to compare an input voltage e_i with a reference voltage other than ground. However, the reference voltage cannot exceed ±2 volts (the maximum common mode range of the amplifier). Typical values for the offset and transition voltages are:

$$V_{OS} = 1 \text{ mv}$$

$$V_W = 1.8 \text{ mv}$$

Since voltage comparators are usually used to sense the difference between a pulse waveform and a reference voltage, switching times become important. The circuit of Figure 11 was used to measure the switching characteristics of the MC-1530 with a 10-1 overdrive at the input. The storage time is essentially caused by saturation occurring in the latter stages of the amplifier, while the fall time is essentially controlled by the parasitic capacitance in the input stages.

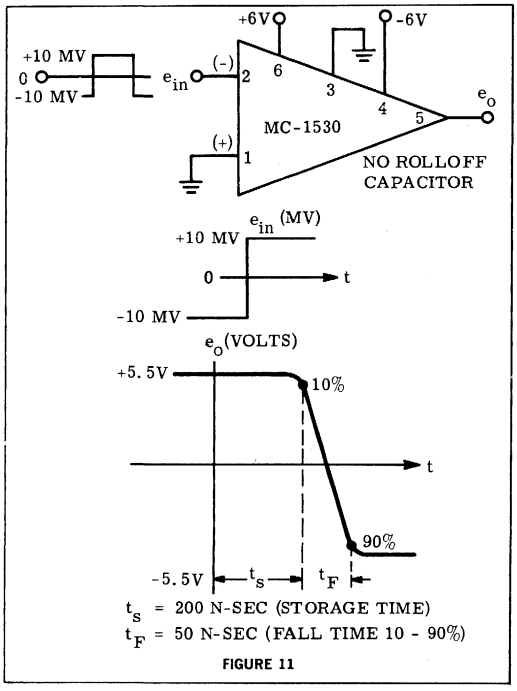


FIGURE 11

Another application for comparators that is often needed in servomechanism work, analog simulation, or as a Schmidtt trigger is shown in Figure 12. The transfer characteristic of the amplifier (Figure 12) shows the hysteresis that results from using R_1 and R_2 in a positive feedback connection. Due to the positive feedback, the transition width, V_W, approaches zero; i.e., the transition width is not a function of the time required for the transition. This time is limited by the maximum slew rate of the amplifier (4.5 V/μ-sec for Figure 12). The threshold voltage (V_T) can be computed from the model of Figure 5, but if $I_B << I_1$ in Figure 12, then:

$$V_T \approx |E_o| \max\left(\frac{R_1}{R_1 + R_2}\right) + V_{OS} \qquad (39)$$

The performance of the circuit in Figure 12 is summarized in Table II.

TABLE II.

	MC-1530	MC-1531
R_1	10 ohms	10 ohms
R_2	10 K	10 K
Transition Width	0	0
Threshold Voltage	+3.8 mv -4.95 mv	-7.0 mv -0.5 mv

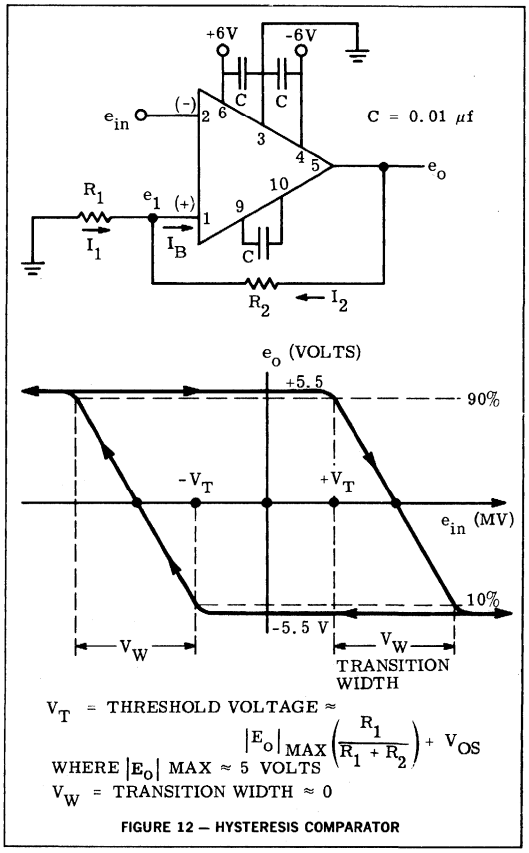


FIGURE 12 — HYSTERESIS COMPARATOR

3. Integration With The MC-1530/31

The MC-1530-31 is connected as an integrator in Figure 13. The biasing network used for this application is designed to minimize the offset voltage drift since this is an error in the integration. Calculating the a.c. closed loop voltage gain of Figure 13:

$$A_V \approx -\frac{Z_f}{Z_1} \qquad (40)$$

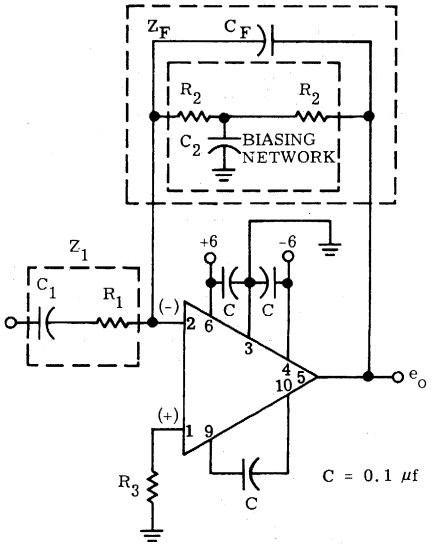


FIGURE 13 — INTEGRATOR CIRCUIT

The exact expressions for Z_f and Z_1 must first be examined to assure that the gain function is of the form:

$$(A_V) = -\frac{1}{SRC}$$

Considering Z_1 first:

$$Z_1 = \frac{SR_1C_1 + 1}{SC_1} \tag{41}$$

Then, for

$$SR_1C_1 >> 1$$

$$Z_1(S) = R_1 \tag{42}$$

which restricts the range of frequencies to

$$\omega >> \frac{1}{R_1C_1} \tag{43}$$

The feedback admittance $1/Z_f$ is given by:

$$\frac{1}{Z_F} = SC_F + \frac{1}{R_2}\left(\frac{S + \frac{1}{R_2C_2}}{S + \frac{2}{R_2C_2}}\right) \tag{44}$$

If

$$S >> \frac{2}{R_2C_2} >> \frac{1}{R_2C_2}$$

Then (44) reduces to

$$\frac{1}{Z_F} = SC_F + \frac{1}{R_2} \tag{45}$$

for

$$\omega >> \frac{2}{R_2C_2}$$

Consider now the d.c. conditions on the integrator. Since the amplifier is a.c. coupled at the input, $Z_1(0) \rightarrow \infty$. Using this fact and equation (22), the output offset voltage is given by:

$$V_{ODC} = V_{OS} + I_B\left[Z_2(0) - Z_3(0)\right] - I_{OS}R_3 \tag{46}$$

Since $Z_2(0) = 2R_2$, and $Z_3(0) = R_3$, and letting $R_3 = 2R_2$, equation (46) reduces to:

$$V_{ODC} = V_{OS} - 2I_{OS}R_2 \tag{47}$$

Equation (47) reveals two advantages in using a.c. coupling at the input:

(1) The input offset voltage V_{OS} appears directly at the output, i.e., it is not multiplied by the closed loop gain of the amplifier. Therefore, this output contribution is typically 3 mv for the MC-1531 and 1 mv for the MC-1530.

(2) The input offset current is so low (25 ma maximum for the MC-1531) that high impedance levels may be used in the feedback loop with low d.c. offset. If R_2 = 100K, then $2I_{OS}R_2$ = 5 mv.

Therefore, use of a.c. coupling and equal d.c. resistances in the feedback loop and from the non-inverting base to ground will degrade the maximum linear output swing of the MC-1531 by only 8 mv. In addition, the use of a high value for R_2 reduces equation (45) to

$$\frac{1}{Z_f} = SC_f \tag{48}$$

for

$$\omega >> \frac{1}{R_2C_f}$$

Substituting equations (48) and (42) into (40)

$$A_V(S) = -\frac{1}{SR_1C_F} \tag{49}$$

or

$$e_o(t) = -\frac{1}{R_1C_F}\int_0^t e_i(t)\,dt \tag{50}$$

Using the previously developed equations, the frequency range of the integrator must be restricted. First choosing a low frequency for the R_2C_2 time constant; if C_2 = 200 μf, then,

$$\omega_1 >> \frac{2}{(1 \times 10^5)(2 \times 10^{-4})} >> 0.5 \text{ rps}$$

from the restriction on equation (45). If the magnitude of $A_V(\omega)$ is specified at a given frequency, the constant of integration may be found:

Let

$$\left|A_V(\omega)\right| = 10 \text{ (20 db)}$$

at

$$\omega = 2\pi(5\text{KC})$$

Then, from (49):

$$\frac{1}{\omega R_1 C_F} = 10$$

or

$$\frac{1}{R_1 C_F} = 10(2\pi)(5 \times 10^3) \qquad (51)$$

Equation (43) indicates that R_1 should be kept reasonably high so that the frequency range will not be too restricted. Therefore, let R_1 = 10K and from (51) C_f = 318 pf. Choosing a practical value:

$$C_f = 300 \text{ pf.}$$

To complete the design, the input R_1C_1 time constant is chosen for

$$\omega >> 2\pi(400 \text{ cps}) >> \frac{1}{R_1 C_1}$$

and C_1 is calculated:

$$C_1 = 100\ \mu\text{f}$$

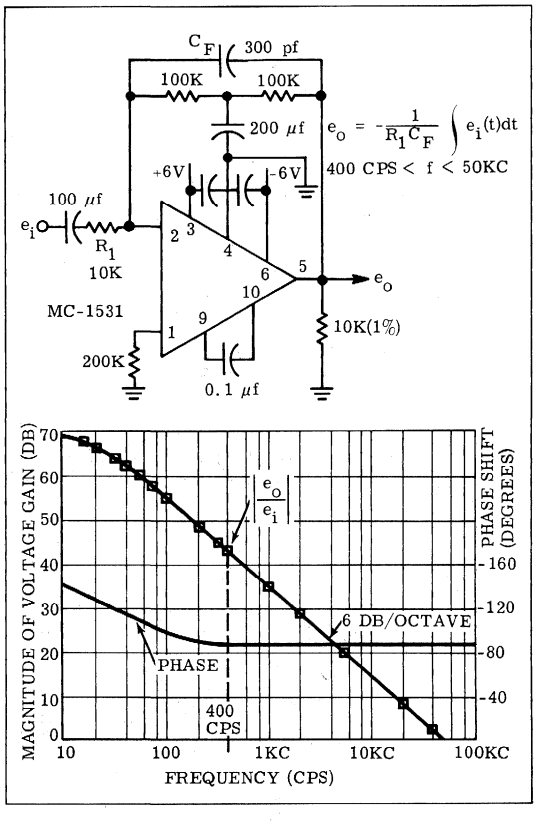


FIGURE 14 — MC1531 INTEGRATOR

The measured response of the integrator constructed with calculated values is shown in Figure 14, and performs as predicted between 400 cps and 50 KC.

4. Simulation of Transfer Functions

The MC-1531 amplifier may be very effectively used in both R-C filters and in transfer function simulation. Using the closed loop gain expression from Figure 13

$$A_{C_L} \approx -\frac{Z_F}{Z_1} \qquad (52)$$

a large number of transfer functions may be generated. As a representative example, the amplifier will be used to simulate equation (53)

$$A_{C_L} = \frac{SRC\,(ST_3 + 1)}{(ST_1 + 1)(ST_2 + 1)^2} \qquad (53)$$

where

$$T_1 = \frac{1}{2\pi(8\text{KC})} = 1.99 \times 10^{-5}$$

$$T_2 = \frac{1}{2\pi(12\text{KC})} = 1.38 \times 10^{-5}$$

$$T_3 = \frac{1}{2\pi(40\text{KC})} = 0.3981 \times 10^{-5}$$

and

$$A_{C_L} = 0 \text{ db at } 10\text{KC}$$

The closed loop expression of equation (53) must first be examined at S = 0 (at d.c.). The MC-1531 should have a very small d.c. offset voltage at the output to obtain the maximum undistorted a.c. output voltage variation. From equation (53), the d.c. closed loop gain is zero. This means that the d.c. value of Z_1 approaches infinity or the d.c. value of Z_f = 0. The Z_f = 0 case requires an undesirable inductor in the feedback loop; so to avoid this case, a.c. coupling may be used at the input which makes $Z_1(0) \rightarrow$ infinity. Then the output offset voltage is the same as that discussed in the integrator:

$$V_{ODC} = V_{OS} + I_B(R_2 - R_3) - I_{OS}R_3$$

If $R_2 = R_3$, then:

$$V_{ODC} = V_{OS} - I_{OS}R_3$$

and the same advantages as those discussed with the integrator apply.

The next step is to synthesize equation (53), then the known value of R_3 may be used to check the output level to make sure that an adequate linear output swing may be obtained from the amplifier. Using equation (52) and tables of R-C transfer impedances found in reference one, equation (53) may be generated. Let $Z_1(S)$ be represented as in Figure 15

$$Z_1(S) = \frac{(ST_1 + 1)(ST_2 + 1)}{SC_2} \qquad (54)$$

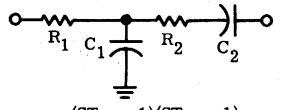
$$T_1 \neq T_2$$

The design equations for the circuit in Figure 15 are:

$$R_1 = \frac{(\sqrt{T_1} - \sqrt{T_2})^2}{C_2} \qquad (55)$$

$$R_2 = \frac{\sqrt{T_1 T_2}}{C_2} \qquad (56)$$

$$C_1 = \frac{\sqrt{T_1 T_2}}{(\sqrt{T_1} - \sqrt{T_2})^2} C_2 \qquad (57)$$

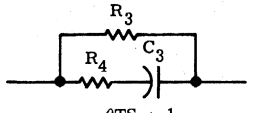


$$Z_1(S) = \frac{(ST_1 + 1)(ST_2 + 1)}{SC} \qquad T_1 \neq T_2$$

FIGURE 15

Next, let Z_f be represented as shown in Figure 16:

$$Z_F(S) = R_3 \left(\frac{\theta T_S + 1}{T_S + 1} \right) \qquad \theta < 1$$



$$Z_F(S) = R_3 \frac{\theta TS + 1}{TS + 1} \qquad \theta < 1$$

FIGURE 16

The design equations for the circuit of Figure 16 are:

$$T = (R_3 + R_4) C_3 \qquad (58)$$

$$\theta = \frac{R_4}{R_3 + R_4} \qquad (59)$$

If $T = T_2$ and $\theta T_2 = T_3$, then the closed loop gain expression for Figure 17 is given by:

$$A_{C_L} = \frac{e_o}{e_i} \quad -\frac{Z_F}{Z_1}(S) = -\frac{SR_3C_2(T_3S + 1)}{(ST_1 + 1)(ST_2 + 1)^2} \qquad (60)$$

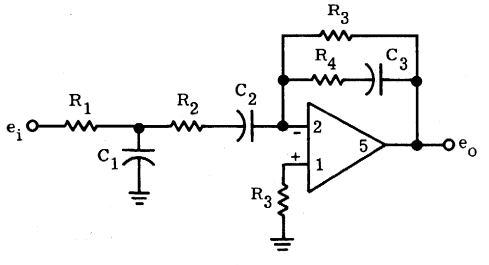


FIGURE 17

Using the time constants T_2 and T_3, θ may be found:

$$\theta = \frac{T_3}{T_2} = \frac{2\pi(12KC)}{2\pi(40KC)} = 0.3$$

There are many ways in which the design equations (55) through (59) may be used to find the R-C values in Figure 17. However, since it is usually required to drive the amplifier from a voltage source, the impedance levels should be high. With this in mind, the design can begin with an arbitrary specification of R_1. Most audio signal generators have 600 ohm internal impedance so that if an arrangement as shown in Figure 18 is used, R_1 should be approximately 10 times larger than R_S (Figure 18) to avoid loading the source. In addition, R_1 should be large enough so that another operational amplifier can drive the circuit of Figure 17 without loading the driving amplifier, thus reducing its output swing. Therefore, let R_1 = 2K; then from equation (55):

$$R_1C_2 = (\sqrt{T_1} - \sqrt{T_2})^2 = 6.73 \times 10^{-7}$$

or

$$C_2 = \frac{6.73 \times 10^{-7}}{2 \times 10^3} = 336 \text{ pf}$$

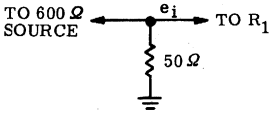


FIGURE 18

Using the value of C_2 and equations (56) and (57), R_2 and C_1 may be calculated, completing the design of Z_1:

$$R_2 = \frac{\sqrt{T_1 T_2}}{C^2} = \frac{1.625 \times 10^{-5}}{3.36 \times 10^{-10}} = 48.4 \text{ K ohms}$$

$$C_1 = \frac{\sqrt{T_1 T_2}}{(\sqrt{T_1} - \sqrt{T_2})^2} C_2$$

$$C_1 = \frac{(3.36 \times 10^{-10})(1.625 \times 10^{-5})}{6.73 \times 10^{-7}} = 0.0081 \ \mu f$$

To design the feedback impedance Z_f, the closed loop gain expression in equation (60) and the specification that A_{CL} = 0 db at 10 KC are used to calculate R_3. When R_3 is known, equations (58) and (59) may be used to calculate R_4 and C_3.

$$A_{C_L} = \frac{j\omega R_3 C_2 \left[1 + j\omega(0.398 \times 10^{-5})\right]}{\left[1 + j\omega(1.99 \times 10^{-5})\right] \left[1 + j\omega(1.38 \times 10^{-5})\right]^2}$$

$$\left|A_{C_L}\right| = 1.0 \text{ and } \omega = 2\pi(1 \times 10^4)$$

then

$$R_3C_2 = 4.16 \times 10^{-5}$$

$$R_3 = \frac{4.16 \times 10^{-5}}{3.36 \times 10^{-10}} = 123.8 \text{ K ohms}$$

from (59)

$$R_4 = \frac{\theta}{(1 - \theta)} R_3$$

$$R_4 = \frac{0.3}{0.7} (123 \text{ K}) = 53 \text{ K}$$

from (58)

$$(R_3 + R_4) C_3 = T = T_2 = 1.38 \times 10^{-5}$$

or

$$C_3 = \frac{1.38 \times 10^{-5}}{1.768 \times 10^{5}} = 75 \text{ pf}$$

The circuit simulating equation (53) is shown in Figure 19 with curves of measured data and data calculated from equation (60).

In using the MC-1530 series to design R-C filters, the same procedure outlined above may be used. However, in the design of filters to meet specified gain, bandwidth, and skirt selectivity, an additional problem arises in approximating the desired frequency response by a transfer function in the S-plane. Several methods are available for solving the approximation problem (one of the best is found in chapter 6 of reference two), but they are beyond the scope of this report.

V. SUMMARY AND CONCLUSIONS

Several circuit design constraints on integrated operational amplifiers caused by monolithic fabrication have been considered. Although all the problems associated with this topic have not been discussed, the major ones of importance are included:

(1) effects of epitaxial resistivity,

(2) importance of resistor ratios, and

(3) importance of transistor and diode matching.

The operation of each stage in the MC-1530-31 is explained and analyzed at d.c. and low frequencies. This clarifies the circuit design and points out the contribution of each stage to the overall amplifier.

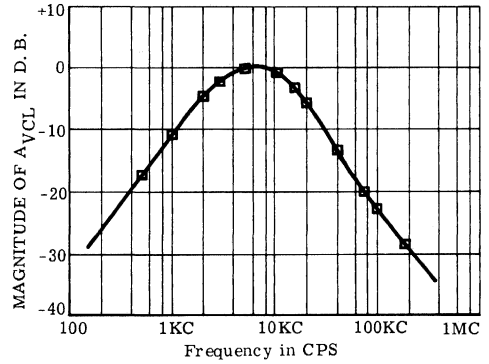
In the final section, as a prelude to practical applications, the details of d.c. biasing and methods of frequency compensation are explained. The note is closed with the design of four practical circuits using the amplifier: a summing amplifier, a voltage compensator, an integrator, and transfer function simulation.

By comparing the measured data with calculated data in the applications section, it is obvious that the MC-1530-31 amplifiers are predictable and useful tools. Since these amplifiers are fabricated by the high volume monolithic process resulting in a low cost, most users should consider them for a wide variety of applications.

VI. REFERENCES

(1) H. Chestnut and R. Mayer "Servomechanisms and Regulating System Design", John Wiley and Sons, Inc., New York, New York, pp 560-571, 1961.

(2) J.G. Truxal "Control System Synthesis", Mc Graw Hill Book Co., Inc., New York, New York, Chapter 6, 1955.



— CALCULATED FROM $A_{VCL} = \frac{SR_3C_2 (ST_3 + 1)}{(ST_1 + 1)(ST_2 + 1)^2}$

□ MEASURED POINTS

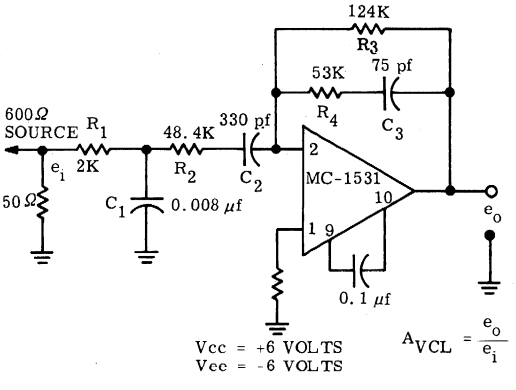


FIGURE 19

AN INTEGRATED CIRCUIT RF-IF AMPLIFIER

INTRODUCTION

A versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback, and wide AGC range. The circuit is a common-emitter, common-base pair (the cascode connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF wideband amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

I. EXPLANATION OF OPERATION

The simplified schematic shown in Figure 1 will be used to quantitatively explain the A.C. and D.C. operation of the MC1550. Considering D.C. operation first, the voltage V_S and resistor R_S establish the current I_{D_1} in diode D_1. Since this diode is on the same silicon die as transistor Q_1 and they are laid out very close to each other, the emitter current of Q_1 will be within 5% of the diode current.* This biasing technique takes advantage of the matching characteristics that are available with integrated circuits and illustrates a method which would be difficult to accomplish with discrete components but with ease using I/C's. The current established in the emitter of Q_1 will be shared in some manner between Q_2 and Q_3 depending on the relationship between V_{AGC} and V_R in the same manner as a current mode switch or differential amplifier. For the case where V_{AGC} is at least 114 mV greater than V_R, Q_3 is turned off and all the collector current of Q_2 is transferred to Q_1. Since Q_3 is off, the A.C. gain will be at its minimum point. If, on the other hand, V_{AGC} is less than V_R by 114 mV or more, all the collector current present in Q_1 will flow through Q_3. This, then, is the operating point for maximum A.C. gain. Considering now the A.C. operation, the input is

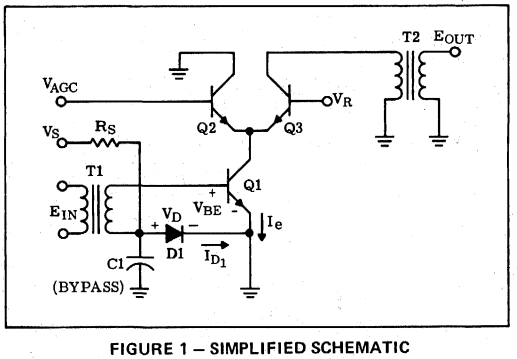


FIGURE 1 – SIMPLIFIED SCHEMATIC

applied to the base of Q_1 and the output taken from the collector of Q_3. Thus, the combination of Q_1 - Q_3 acts as a common-emitter common-base pair. This pair offers the distinct performance advantage of reducing internal feedback (Y_{12}) two orders of magnitude when compared to a single transistor. Using the General Radio 1607-A Immittance bridge, Y_{12} was unmeasurable up to frequencies of 300 MHz. This indicates that the magnitude of Y_{12} is less than 0.001 m-mhos over the useful frequencies of operation of the MC1550, and can, for all practical purposes, be neglected. The ability to vary the gain of this circuit can also be a performance advantage when compared to a single transistor. The following reasoning makes this apparent: As will be shown in the next section, changing the AGC voltage has a very minor effect on the operating point of Q_1; therefore, the input impedance of Q_1 remains constant. Thus, there is no detuning of the tuned input circuitry as performance curves of practical circuits shown in following sections will verify.

A schematic of the MC1550 amplifier including biasing resistors is shown in Figure 2. The circuit is constructed on a 30 x 32 mil die using 200 ohm/square sheet resistance material and 1 x 0.5 mil emitters in the box geometry transistors. Resistors R_1 and R_2 bias the diode D_1 and also establish a base voltage for transistor Q_3. Resistors R_3 and R_4 serve to widen the AGC voltage range from 114 mV to about 0.86 volts. This is necessary so that the AGC line will be less susceptible to external noise.

II. D. C. CALCULATIONS AND BIASING

A D.C. analysis which closely approximates the actual operation is as follows. Using Figure 3 and writing node equations for nodes 8 and 10, we have

for node 8,

$$\frac{V_8 - V_{CC}}{R_1} + \frac{V_8 - V_{10}}{R_3} + \frac{V_8 - V_{D_1}}{R_2} + I_{B_3} = 0$$

for node 10,

$$\frac{V_{10} - V_{AGC}}{R_4} + \frac{V_{10} - V_8}{R_3} + I_{B_2} = 0$$

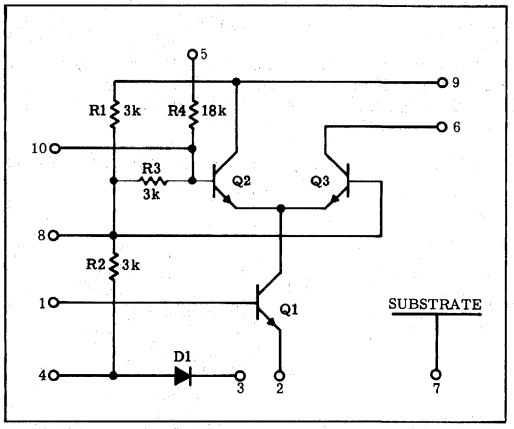


FIGURE 2 – MC1550 SCHEMATIC

*See Appendix A for derivation

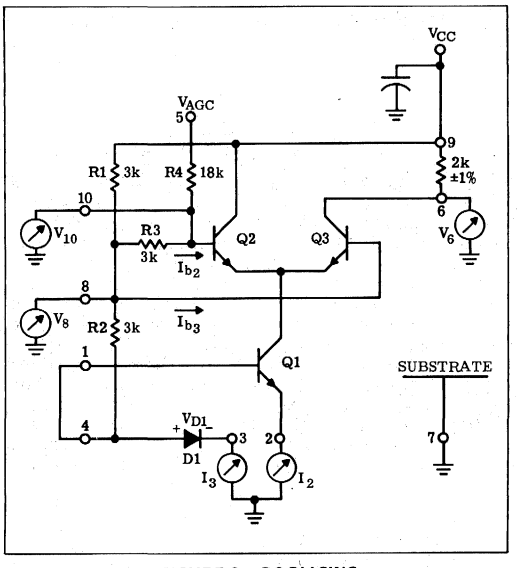


FIGURE 3 – DC BIASING

Neglecting I_{b_2} and I_{b_3} and solving for V_8 and V_{10}, we have

$$V_8 = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right]\left[1 + \frac{R_4}{R_3}\right] + V_{AGC}\left[\frac{R_1}{R_3}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (1)$$

$$V_{10} = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right]\left[\frac{R_4}{R_3}\right] + V_{AGC}\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (2)$$

From equations (1) and (2), observe that the D. C. voltages are dependent upon resistor ratios rather than absolute values. Present integrated circuit technology enables these tolerances to be held within 5% quite easily, thus achieving very good D. C. stability.

The manner in which transistors Q_2 and Q_3 share the current which passes through transistor Q_1 is determined by the difference of the base voltages, $V_8 - V_{10}$ (See Appendix B).

Define $V_0 = V_8 - V_{10}$, and subtracting (2) from (1):

$$V_0 = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right] - V_{AGC}\left[1 + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (3)$$

The change in equation (3) with AGC voltage may be calculated by differentiating,

$$\frac{\partial V_0}{\partial V_{AGC}} = \frac{-\left[1 + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]}$$

For the nominal case of $R_1 = R_2 = R_3 = R$ equation (3) simplifies to

$$\frac{\partial V_0}{\partial V_{AGC}} = \frac{-2}{3 + 2\left(\frac{R_4}{R}\right)} \quad (4)$$

which is, again, a function of a resistor ratio. Using nominal values of R = 3k ohms and R_4 = 18k ohms

$$\frac{\partial V_0}{\partial V_{AGC}} = -0.133\ \frac{\text{Volts}}{\text{Volt}} \quad (5)$$

Using (5), for a change in V_0 of 114 mV, the AGC voltage must change 0.86 volts at room temperature, which corresponds to measured values.

To determine the effect of the AGC voltage on the operating point of Q_1, the emitter current of Q_1 is calculated as a function of AGC voltage using Figure 4. Writing a node equation for the node at the base of Q_1:

$$\frac{V_8 - V_{D_1}}{R_2} = I_{D_1} + I_{B_1} \quad (6)$$

Assuming a close match of p-n junctions for diode D_1 and the base to emitter junction of Q_1,

$$I_{D_1} = I_{E_1} = (h_{FE} + 1)\, I_{B_1}$$

Substituting the above into (6):

$$V_8 - V_{D_1} = R_2\left(\frac{h_{FE} + 2}{h_{FE} + 1}\right) I_{E_1} \quad (7)$$

For $h_{FE} \gg 1$

$$I_{E_1} \approx \frac{V_8 - V_{D_1}}{R_2}$$

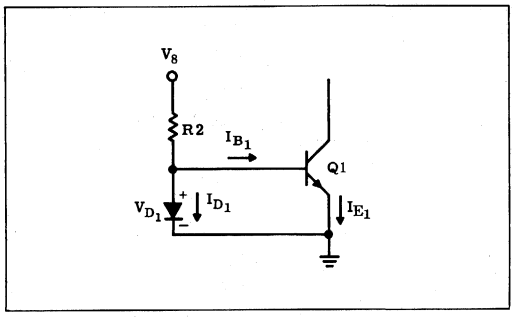


FIGURE 4 – BIASING OF INPUT TRANSISTOR

Substituting the value for V_8 from equation (1) into (7):

$$I_{E_1} = \frac{\left[V_{CC} + \left(\frac{R_1}{R_3}\right)V_{D_1}\right]\left[1 + \frac{R_4}{R_3}\right] + V_{AGC}\left[\frac{R_1}{R_3}\right]}{R_2\left[\left(1 + \frac{R_4}{R_3}\right)\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right) - \left(\frac{R_1}{R_3}\right)\left(\frac{R_4}{R_3}\right)\right]} - \frac{V_{D_1}}{R_2} \quad (8)$$

To obtain the variation of I_{E_1} with V_{AGC}, (8) is differentiated:

$$\frac{\partial I_{E_1}}{\partial V_{AGC}} = \frac{\frac{R_1}{R_3}}{R_2\left[\left(1 + \frac{R_4}{R_3}\right)\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right) - \left(\frac{R_1}{R_3}\right)\left(\frac{R_4}{R_3}\right)\right]} \quad (9)$$

For nominal values of $R_1 = R_2 = R_3 = 3k$, $R_4 = 18k$

$$\frac{\partial I_{E_1}}{\partial V_{AGC}} = 22\ \mu a/volt \quad (10)$$

For a supply voltage $V_{CC} = 6.0V$, $I_{E_1} \approx 0.88$ mA, thus for full AGC operation (0.86V), the change in I_{E_1} is $19\mu A$ or 2.16%. For larger supply voltages, the effect of AGC voltage on I_{E_1} is even less (1% for $V_{CC} = 12.0V$). Since I_{E_1} varies only slightly, the input impedance variation (which depends on $r_e = KT/qI_E$) is very small. This fact is shown by the measured 60 MHz data in Figure 5.

III. TEMPERATURE STABILITY

The ability of the diode current to closely track the emitter current in Q_1 will give a good indication of the circuit's gain stability with temperature. A curve of I_{D_1}/I_{E_1} vs temperature is shown in Figure 6. The absolute variation of I_{E_1} is also shown on the curve for $V_{CC} = 6.0V$. The variation of I_{E_1} produces a measured variation in power gain of ±1.5 dB over the temperature range -55°C to +125°C, which will be explained in more detail in following sections.

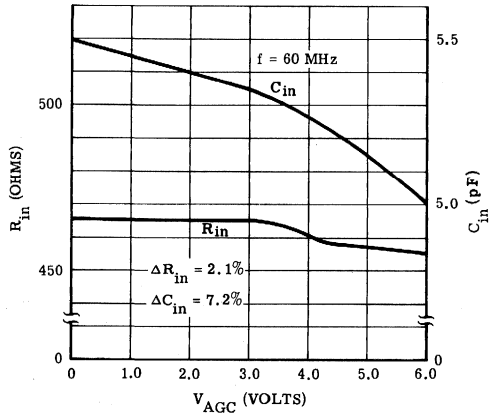


FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

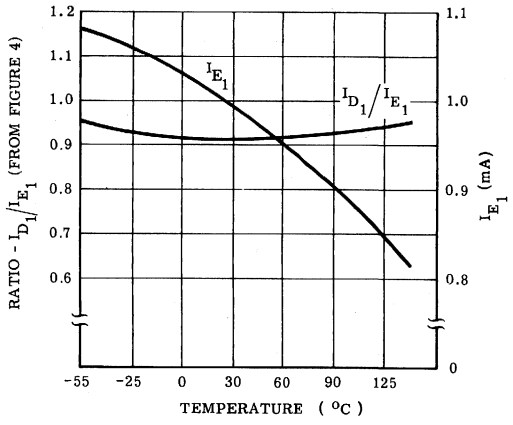


FIGURE 6 – DC CURRENTS versus TEMPERATURE

IV. CIRCUIT CHARACTERIZATION AND Y-PARAMETERS

There are two basic methods by which integrated circuits may be characterized. The first method is based on measurement or calculation of internal transistor parameters, forming of a suitable model for each, combining with other internal components and transistor models to form a overall model which will approximate the actual circuit. For integrated circuits which contain more than one or two active devices combined with distributed substrate capacitance and resistor parasitic capacitance, this method of analysis becomes difficult and the accuracy of results depends upon the accuracy of the model. This type of formulation has value in helping to relate specific circuit applications to device parameters. However, the accuracy of predicted performance is not quite as good as that obtainable when measured two-port parameters are used. The two-port method characterizes the linear active network as a black box, and is not limited by approximations but by the accuracy of measurement of the parameters. This method has the additional advantage of being amenable to well established design techniques. The MC1550 is characterized on the data sheet in terms of y-parameters which were measured on both the Boonton R-X meter and the General Radio 1607A Immittance bridge. The correlation between the two instruments was ±5% where frequencies overlapped. Therefore, the y-parameters will be used in later sections for circuit design, and predicted and measured performance are very close to each other. However, in order to better understand the reasons for some of the values of y-parameters obtained, a y-parameter discussion is in order.

To discuss the y-parameters of the MC1550, it is convenient to consider the circuit as a common-emitter, common-base cascode as shown in Figure 7. The circuit has been analyzed in reference 3, but the method is repeated here for clarity. To derive the y-parameters, the transmission matrix for a common-emitter and common-base stage may be used as in Figure 7. The overall transmission matrix then becomes:

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A_1 A_2 + B_1 C_2 & A_1 B_2 + B_1 D_2 \\ A_2 C_1 + C_2 D_1 & B_2 C_1 + D_1 D_2 \end{bmatrix} \begin{bmatrix} e_2 \\ i_2 \end{bmatrix} \quad (11a)$$

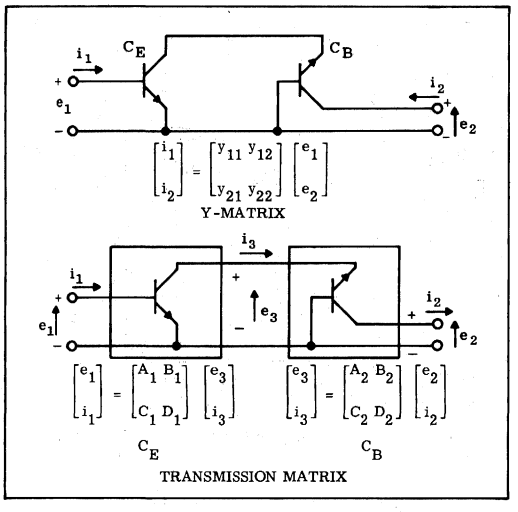


FIGURE 7 – CE-CB MATRIX PARAMETERS

The y-parameters of each stage in the cascode circuit are related to the above transmission factors as follows:

$$A_1 = -\frac{y_{oe}}{y_{fe}} \quad B_1 = -\frac{1}{y_{fe}} \quad A_2 = -\frac{y_{ob}}{y_{fb}} \quad B_2 = -\frac{1}{y_{fb}}$$

$$C_1 = -\frac{\Delta y}{y_{fe}} \quad D_1 = -\frac{y_{ie}}{y_{fe}} \quad C_2 = -\frac{\Delta y}{y_{fb}} \quad D_2 = -\frac{y_{ib}}{y_{ob}}$$

where $\Delta y = y_i y_o - y_f y_r$

and $y_{fe} = y_{21}$ common-emitter

$y_{fb} = y_{21}$ common-base, etc.

At this point, the y-parameters may be substituted for the transmission parameters in the overall matrix and then a conversion may be made from an overall transmission matrix to an overall y-parameter matrix by using the equations below:

$$Y_{11} = \frac{D}{B} \quad Y_{12} = -\frac{\Delta T}{B}$$

$$Y_{21} = -\frac{1}{B} \quad Y_{22} = \frac{A}{B}$$

where $\Delta T = AD - BC$

and $A = A_1A_2 + B_1C_2 \quad B = A_1B_2 + B_1D_2$

$C = A_2C_1 + C_2D_1 \quad D = B_2C_1 + D_1D_2$.

The above set of equations may be manipulated into several forms. However, with the use of the relationship between the common-emitter and common-base y-parameters, the overall y-parameters may be put into the useful form presented in reference 3.

$$Y_{ib} = y_{ie} + y_{re} + y_{fe} + y_{oe}$$

$$Y_{rb} = -(y_{re} + y_{oe})$$

$$Y_{fb} = -(y_{fe} + y_{oe})$$

$$Y_{ob} = y_{oe} \qquad (11b)$$

The results of these manipulations are listed in equations 12 through 15 below.

$$Y_{11} = \frac{y_{ie}(y_{oe} + y_{ib}) - y_{fe}y_{re}}{(y_{oe} + y_{ib})} \approx y_{ie} \qquad (12)$$

$$Y_{12} = -\frac{y_{re}y_{rb}}{y_{oe} + y_{ib}} \qquad (13)$$

$$Y_{21} = -\frac{y_{fe}y_{fb}}{(y_{oe} + y_{ib})} \approx -y_{fe} \qquad (14)$$

$$Y_{22} = \frac{y_{ob}(y_{oe} + y_{ib}) - y_{rb}y_{fb}}{(y_{oe} + y_{ib})} \approx y_{ob} \qquad (15)$$

Where Y_{11}, Y_{12}, etc. denote the y-parameters of the cascode circuit. At this point, either calculations or measurements on common-emitter and common-base parameters for the individual transistors may be used to verify and explain the overall y-parameters. For the MC1550, individual transistors were bonded into a TO-18 package for these purposes. The results of both measurements and calculations indicate that the conculsions below are correct:

1. The input admittance of the cascode circuit is within 5% of the input admittance of a common-emitter transistor.
2. The reverse transfer admittance is extremely low since, in terms of milli-mhos, it involves the product of two numbers less than unity, divided by a number greater than one. Hence, the fact that it is extremely difficult to measure is understandable.
3. The forward transfer admittance is primarily that of a common-emitter transistor.
4. The output admittance is essentially that of a common-base amplifier (very low real part and an imaginary part controlled by the parasitic capacitance of a monolithic transistor).

These conclusions will be used to some extent in each of the applications in later sections of this note. Typical measured values of y-parameters versus frequency and versus AGC voltage are shown in Figures 8 through 11, and will be used in the following sections for designing tuned amplifiers. The y_{12} parameter is not shown since it was found to be less than 0.001 m-mhos, therefore, it will be neglected in examples to follow.

V. NOISE CONSIDERATIONS

The noise performance of all possible cascoded integrated circuit pairs has been theoretically evaluated in reference 2. Two major points that are results of this analysis should be repeated here:

1. The noise figure of a small geometry monolithic transistor is very closely the same as that of a discrete bottom collector transistor which has the same geometry.

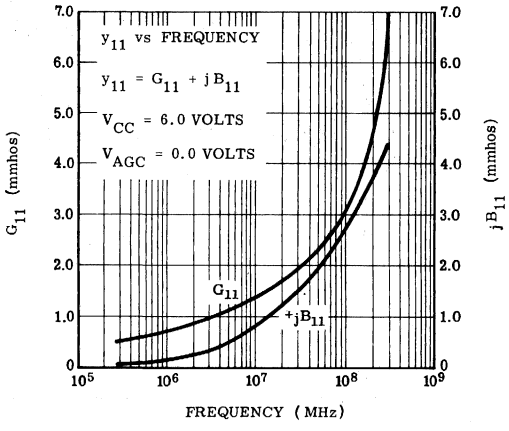


FIGURE 8 – INPUT ADMITTANCE versus FREQUENCY

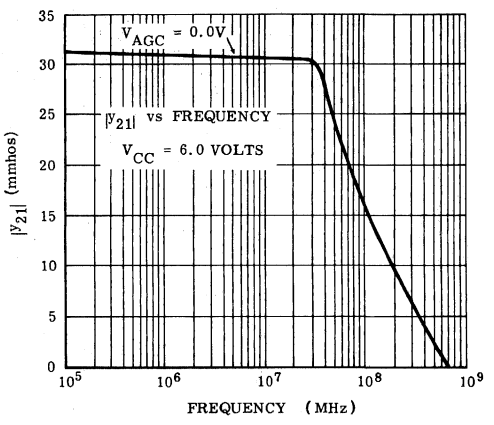


FIGURE 11 – MAGNITUDE OF FORWARD TRANSFER ADMITTANCE versus FREQUENCY

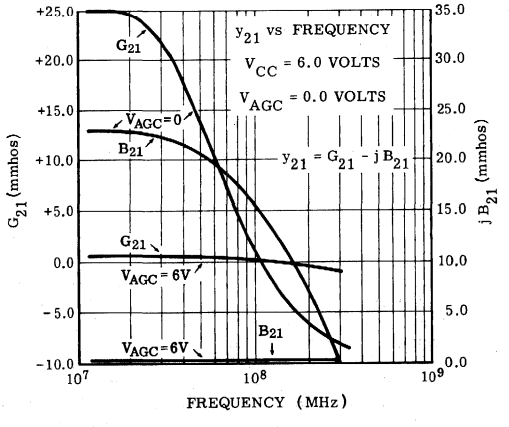


FIGURE 9 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

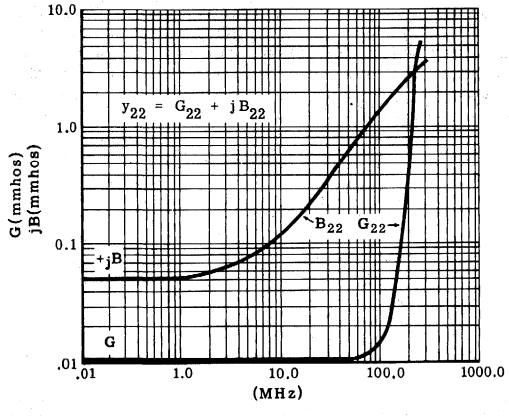


FIGURE 10 – OUTPUT ADMITTANCE versus FREQUENCY

2. Of all possible connections of two transistors, the best noise figure will be obtained when the input device is in the common-emitter connection. The second device will have little or no influence on noise figure.

The MC1550 amplifier, therefore, should follow closely that of it's discrete counterpart in the common-emitter connection. That this is true is seen in Figure 12 which shows a curve of optimum noise figure and optimum source resistance versus frequency.

VI. APPLICATIONS

NARROW BAND TUNED AMPLIFIER (CE-CB)

This section considers the design of a single stage, 60 MHz amplifier. A typical circuit for this application is shown in Figure 13. The following two-port y-parameters are obtained from the curves in figures 8 through 11 at 60 MHz, for V_{CC} = 6.0, and V_{AGC} = 0.0

$$y_{11} = 2.50 + j2.3 = 3.34 \angle 42.6^{o} \text{ mmhos}$$

$$y_{12} = \text{(negligible)}$$

$$y_{21} = 10.0 - j19.0 = 21.5 \angle -62.3^{o} \text{ mmhos}$$

$$y_{22} = 0.01 + j0.80 = 0.80 \angle 90^{o} \text{ mmhos}$$

Since y_{12} has been neglected, the maximum available gain (MAG) is assumed to exist and may be calculated from the equation (16) below:

$$MAG = \frac{\text{Power Available at Output}}{\text{Power Available from Source}} = \frac{|y_{21}|^2}{4\, R_e(y_{11})\, R_e(y_{22})} \quad (16)$$

MAG = 4620 and 10 log (MAG) = 36.7 dB

This is the theoretical maximum limit for this circuit at this frequency. Another important measure of power gain is transducer gain, G_T, defined by the equation

$$G_T = \frac{\text{Power Delivered to the Load}}{\text{Power Available from the Source}} = \frac{P_o}{P_{AVS}} \quad (17)$$

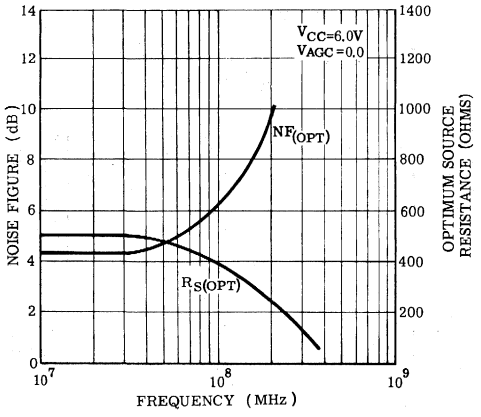


FIGURE 12 – NOISE FIGURE versus FREQUENCY OPTIMUM SOURCE RESISTANCE versus FREQUENCY

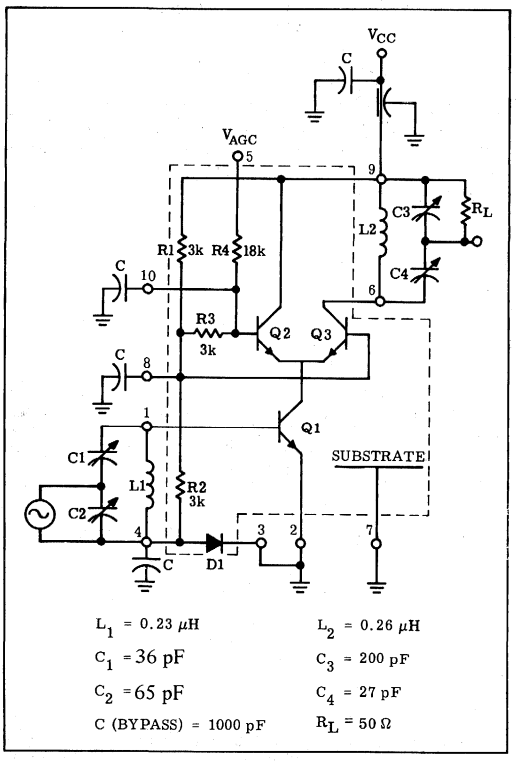


FIGURE 13 – 60 MHz TUNED AMPLIFIER

It can be shown* that maximum power gain through a linear two-port network occurs when the source admittance is the complex conjugate of the input admittance of the network and the load admittance is the complex conjugate of the output admittance of the network. From basic two-port analysis using y-parameters, the formulas for input and output admittances are:

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \tag{18}$$

$$Y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_S} \tag{19}$$

Since the assumption has been made that y_{12} is zero,

$$Y_{in} \approx y_{11}$$

$$Y_{out} \approx y_{22}$$

Therefore, the optimum source and load admittances are given by:

$$y_{S(opt)} = y_{11}^* = 2.50 - j2.30 \text{ mmhos}$$

$$y_{L(opt)} = y_{22}^* = 0.01 - j0.80 \text{ mmhos}$$

These values of Y_S and Y_L are not exact, but they do turn out to be very close to the final values obtained in the laboratory. Having calculated $y_{S(opt)}$ and $y_{L(opt)}$, G_T may be calculated:

$$G_T = \frac{4|y_{21}|^2 R_e(y_S) R_e(y_2)}{|(y_{11} + y_S)(y_{22} + y_L) - y_{12}y_{21}|^2} \tag{20}$$

Using values found above: G_T = 4620 or G_T = 36.7 dB.

The value for G_T is equal to the available power gain which also follows since $y_{12} \approx$ zero. In practice, it is difficult to achieve the calculated theoretical value of transducer power gain because of the losses in the inductors. The finite value of unloaded Q for a practical inductor results in an equivalent resistance which will load the output and restrict both the bandwidth and the power gain. As will be seen in the following section, the equivalent R_P can be used to modify y_{22} and then the calculation performed with the new y'_{22}.

Due to the low value of y_{12}, the assumption that the output load can be varied without affecting the input is valid and can be used to advantage in this design. Consider first the input tuned network and the input admittance as shown in the circuit of Figure 14(a). There are many ways to proceed with the design, and the method chosen here is to arbitrarily broad-band the input network and design the matching network to conjugate match y_{11}. The matching network[1] then transforms the 50 ohm source into y_{11}^*. Using techniques in reference 1 the calculated values of L_1, C_1, and C_2 are:

$$L_1 = 0.23 \ \mu H$$

$$C_1 = 36 \text{ pF}$$

$$C_2 = 65 \text{ pF}$$

*See Reference 1

[1]Chapter 13 of reference 1 details a design procedures for matching networks.

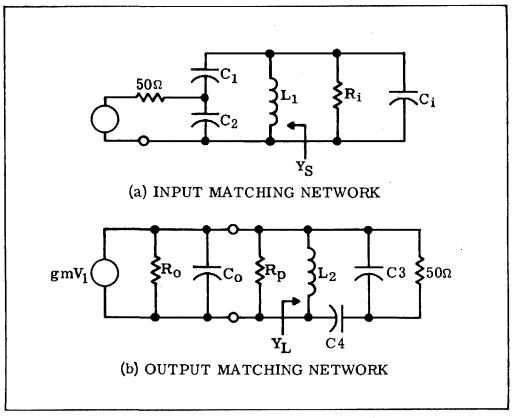


FIGURE 14 – INPUT AND OUTPUT MATCHING NETWORKS

Considering now the output matching network in Figure 14(b), the bandwidth should be considered first:

$$BW = \frac{1}{2\pi R_T C_T}$$

R_T = Total R at the output

C_T = Total C at the output

In Figure 14(b), resistor R_P is the equivalent resistance across the output caused by the finite unloaded Q of L_2. The measured value of R_P is 35k ohms at 60 MHz. This value may be placed in parallel with the value of R_O, and the resultant R used to calculate a new $y_{22} = y'_{22}$. The new value of y_{22} will be used to design the matching network so that the load admittance is the complex conjugate of y'_{22}. The total R and total C across the output may then be traded to achieve the required bandwidth and transducer power gain and L may be varied to maintain the desired center frequency. For R_P = 35k ohms, the new y_{22} is:

$$y'_{22} = 0.039 + j0.80 \quad \text{mmhos}$$

then

$$y_L = 0.039 - j0.80 \quad \text{mmhos}$$

The matching network values are then calculated:

$$L_2 = 0.26\ \mu H$$

$$C_3 = 630\ pF$$

$$C_4 = 27\ pF$$

The total R and C present across the output is:

$\frac{1}{R_T} = 2\,(0.039)\,10^{-3}$ $\qquad C_T = C_0 + C_{(\text{Matching network})}$

R_T = 12.5k ohms $\qquad C_T$ = 28 pF

These values may then be used with y-parameters to calculate the transducer power gain, center frequency, and bandwidth. The results are:

f_o = 60 MHz

G_T = 30.1 dB

BW = 0.5 MHz

Using the values of L and C previously calculated, the circuit of Figure 13 was constructed and tested in the laboratory. The results using 4 different MC1550's are:

Circuit No.	Center Frequency	Transducer Power Gain	Bandwidth
1	60 MHz	30.0 dB	0.6 MHz
2	60 MHz	30.0 dB	0.5 MHz
3	60 MHz	30.5 dB	0.6 MHz
4	60 MHz	30.4 dB	0.4 MHz

No retuning was done when the units were interchanged, which accounts for the slight differences in measured values. The AGC characteristics of the amplifier are shown in Figure 15. The center frequency and bandwidth are very constant over a 40 dB AGC range and the bandwidth varies ± 0.15MC for a 55 dB AGC range. This stability is due mostly to the fact that input impedance does not change with AGC, and because the input tuned circuitry is broad-banded. The design in the next section will show only small variations in center frequency and bandwidth (less than 3%) when the input tuning network is a narrow-band circuit.

The performance of the circuit over the temperature range -55°C to +125°C is shown in Figure 16. The worst variation was -2 dB over the complete range.

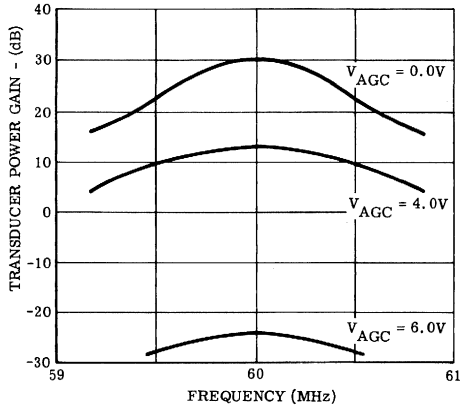


FIGURE 15 – 60 MHz SINGLE STAGE AMPLIFIER GAIN

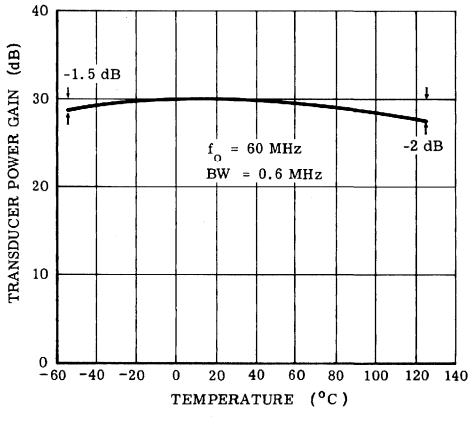


FIGURE 16 – 60 MHz POWER GAIN versus TEMPERATURE

WIDEBAND TUNED AMPLIFIER

The foregoing example demonstrates the high gain of the MC1550 at the expense of bandwidth. This narrow bandwidth is primarily due to the large value of resistance which is across the parallel tuned output circuit. Reducing this value of resistance will broaden the bandwidth and reduce the power gain so that more than one stage may be required to achieve the specified gain and bandwidth. This section is concerned with the design of a multi-stage amplifier to illustrate the above points. The amplifier specifications are:

Single Tuned
Center Frequency – 45 MHz
Bandwidth – 15 MHz
Transducer Power Gain – 30 dB

For this application, it will be necessary to use a two-stage amplifier. Because there will be three tuned circuits, there will be a bandwidth reduction according to the following equation:

$$BW_{OVERALL} = BW_{STAGE}\sqrt{2^{1/n} - 1}$$

where n is the number of tuned circuits.

Thus, for an overall bandwidth of 15 MHz, each stage should be designed for 30 MHz bandwidth. From the curves given in Figures 8 through 10, the y-parameters at 45 MHz, V_{CC} = 6.0V, V_{AGC} = 0.0V are as follows:

y_{11} = 2.5 + j2.0 mmhos

y_{12} = (negligible)

y_{21} = 16 - j21 mmhos

y_{22} = 0.01 + j0.55 mmhos

For the following calculations, the source and load impedance are 50 ohms.

The simplified circuit shown in Figure 17 will be used for this design. For this circuit, a new output resistance for each network can be found in order to simplify the calculations. By doing this, the two-port is extended as shown by the dashed lines in Figure 17. This value of R is the parallel combination of R_o and R_L. From the value of y_{22}, R_o is found to be 100k. Assuming that y_S can be accurately transformed into y_{11}* and $y_L = y_{22}$*, the value of R_L which will give the required gain of 15 dB for each stage can be found from the transducer power gain as shown in equation 21:

$$G_T = \frac{|y_{21}|^2}{4\,R_e(y'_{22})\,R_e(y_{11})} \quad . \qquad (21)$$

For the values given, $R_e(y'_{22})$ = 2.88 mmhos

Then,

$$\frac{R_o R_L}{R_o + R_L} = \frac{1}{R_e(y'_{22})}$$

Solving, $R_{L(min)}$ = 350 ohms

Let R_L = 500 ohms to realize the specified transducer power gain.

Inductors with an unloaded Q of 30 or more must be used so that the effect of their resistance on R_L can be neglected. Using the equations for center frequency and bandwidth of a tuned circuit,

$$F_o = \frac{1}{2\pi\sqrt{LC}} \qquad BW = \frac{1}{2\pi RC}$$

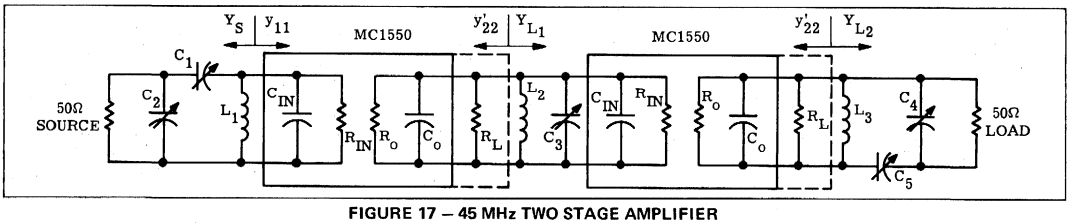


FIGURE 17 – 45 MHz TWO STAGE AMPLIFIER

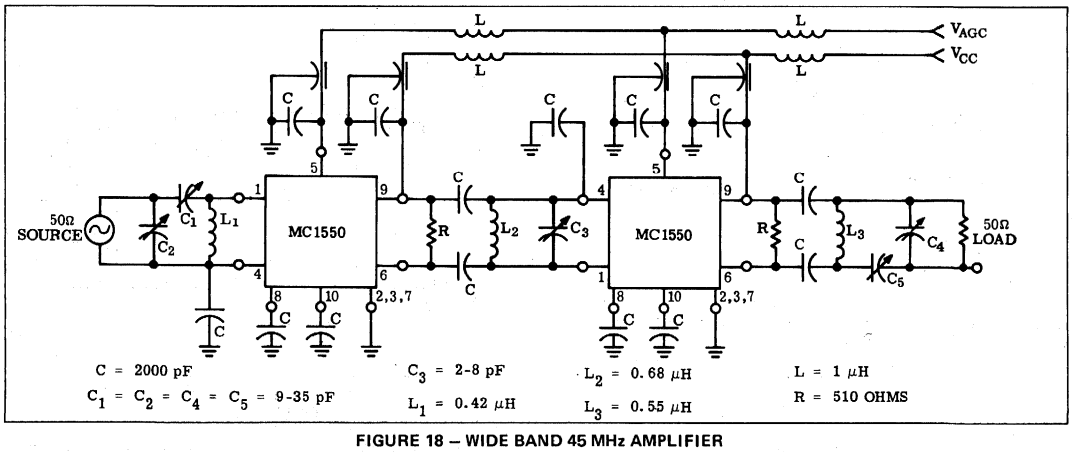


FIGURE 18 – WIDE BAND 45 MHz AMPLIFIER

the necessary value of L and C at each interstage may be found. These values are:

C_1 = 25 pF (9-35) L_1 = 0.42 μH R_L = 510Ω

C_2 = 20 pF (9-35) L_2 = 0.68 μH

C_3 = 5 pF (2-8) L_3 = 0.55 μH

C_4 = 20 pF (9-35)

C_5 = 25 pF (9-35)

The circuit of Figure 18 was built and the table below indicates the measured values of transducer power gain and bandwidth.

Unit	Center Frequency	Gain (dB)	Bandwidth
1	45 MHz	30.2	15.4 MHz
2	45 MHz	30.5	15.0 MHz
3	45 MHz	31.0	14.5 MHz
4	45 MHz	30.3	14.2 MHz

The practical circuits closely follow the predicted values previously calculated. The AGC characteristic is shown in Figure 19; and, as before, the bandpass characteristics are preserved over the entire AGC range.

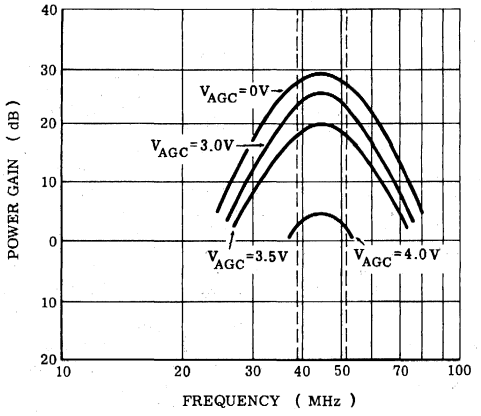


FIGURE 19 – AGC CHARACTERISTICS OF 45 MHz WIDE BAND AMPLIFIER

A STAGGER TUNED I-F STRIP

The term "stagger tuning" refers to an amplifier comprising several stages in cascade, in which the stages are not tuned to the same frequency but are "staggered" at frequencies above and below the desired center frequency. Not only are the tunings of the individual stages not identical, but often their bandwidths are also different. Although the advantages of this method were apparent to a few persons several years earlier, the credit for first exploiting the stagger tuning technique in detail belongs to Henry Wallman. [5] Since that time, many authors have extended Wallman's work and the technique is well documented.

The objectives of stagger tuning are twofold: (1) A gain-bandwidth product is achieved which is greater than that of synchronously tuned cascade stages, and (2) it is possible to achieve a selectivity curve of prescribed amplitude response. Thus it is possible to stagger tune n single stages as to achieve a flat bandpass, an equal ripple (Chebyshev) bandpass, or numerous other selectivity curves with very good gain. A design procedure for a maximally flat stagger tuned amplifier and laboratory results are given in the following section.

DESIGN PROCEDURE

Consider the following hypothetical design for an IF amplifier:

Center Frequency (fo)	45 MHz	Stagger Tuned	
Bandwidth (Δf)	6 MHz	Source Impedance	50Ω
Power Gain (G_T)	70 dB	Load Impedance	50Ω
AGC Control	>50 dB		

A typical circuit for this application using transformer interstage coupling is shown in Figure 20. The individual stage requirements of this flat staggered amplifier are as follows:

a. One stage tuned to f_0 with bandwidth Δf.
b. One stage tuned to $f_0 \alpha$ with $Q = 2.0/\delta$
c. One stage tuned to f_0/α with $Q = 2.0/\delta$

where $\delta = \Delta f/f_0$ and $\alpha = 1 + 0.433\delta$

For the amplifier specifications given above, the following results are obtained:

$\delta = 0.1333$ $\alpha = 1.0578$

a. One stage tuned to 45 MHz with a 6 MHz bandwidth.
b. One stage tuned to 47.60 MHz with a 3 MHz bandwidth.
c. One stage tuned to 42.50 MHz with a 3 MHz bandwidth.

There is nothing new or tricky involved in the interstage design. The most expedient procedure is to assume that the coupling transformers are ideal, form equivalent models with one side of the transformer referred to the other side, then compute the bandwidth and center frequency from the equations for the parallel tuned circuits:

$$\Delta f = \frac{1}{2\pi R_T C_T} \qquad f = \frac{1}{2\pi\sqrt{L_T C_T}}$$

where R_T = total parallel resistance
C_T = total parallel capacitance
L_T = total parallel inductance

However, due to the fact that there are two tuned circuits associated with each stage, there will be an overall bandwidth shrinkage of each stage. This is easily handled by broadbanding the output tuned circuit of Stage 1 while achieving the desired selectivity and bandwidth with the

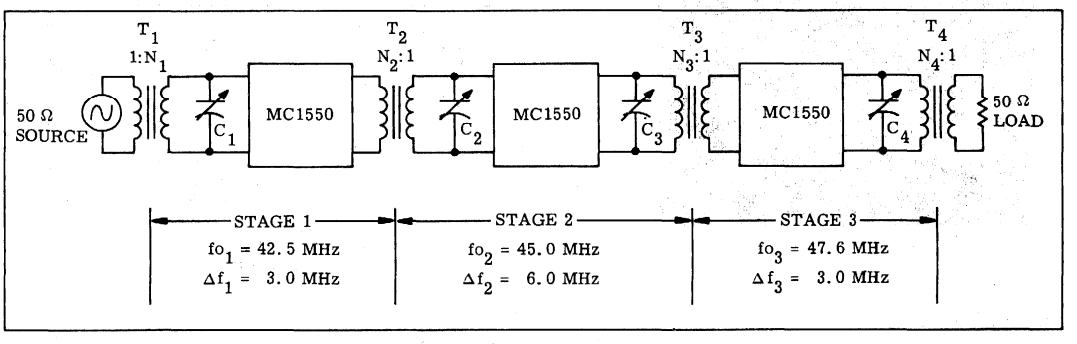


FIGURE 20

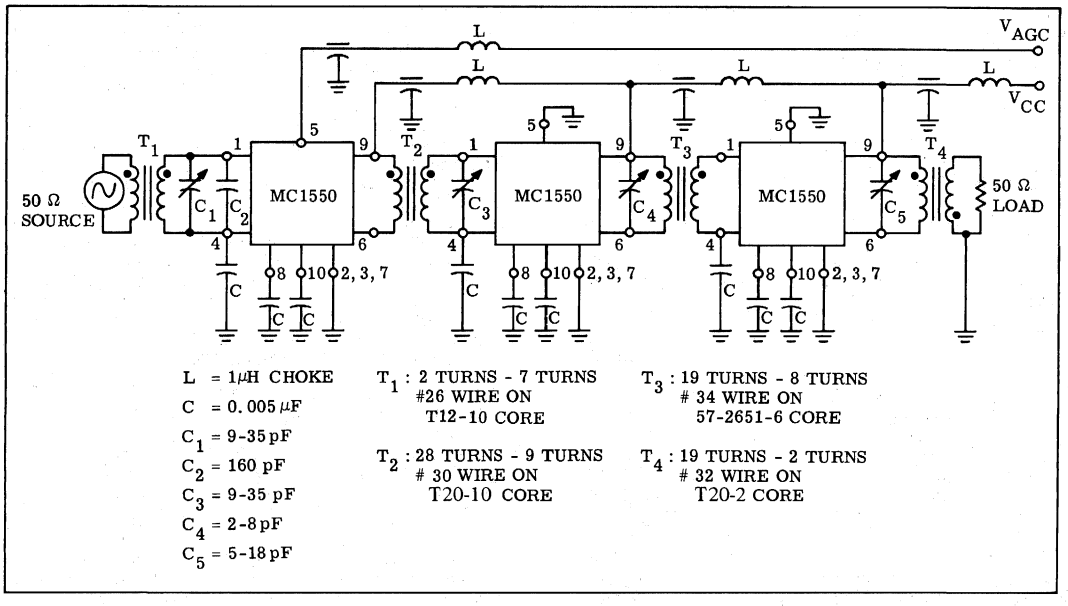


FIGURE 21 – 45 MHz STAGGER TUNED AMPLIFIER

input tuned circuit and visa versa with Stage 3. The same procedure could be followed in the design of Stage 2 by broadbanding the output tuned circuit while achieving the desired bandwidth and selectivity with the input tuned circuit. However, for this particular circuit, the procedure taken was to synchronously tune both the input and output circuits of Stage 2 and take into account the shrinkage factor. A schematic of the final design showing all pin connections is given in Figure 21.

TUNING

As was pointed out earlier, one very important characteristic of the MC1550 is the ease with which it is tuned. The first prototype circuit was tuned as follows: each stage was disconnected from the other stages and loading applied to each stage to simulate the actual circuitry in cascade. Each stage was then tuned to the desired center frequency with the correct bandwidth. Once each stage was tuned, the circuits were connected in cascade and final fine tuning adjustments made. With the experience gained in tuning the first prototype, the second prototype was tuned by merely sweeping the amplifier with a Jerrold 890 sweep generator and tuning while observing the output on an oscilloscope. A photograph of the sweep is shown in Figure 22. The final results were: Center frequency - 45 MHz, Bandwidth - 6 MHz, and Power Gain - 70.0 dB.

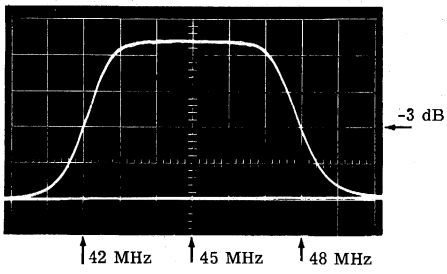


FIGURE 22

AGC CHARACTERISTICS

The choice of which stage or stages are to be AGC'd is more or less arbitrary. Various AGC combinations of the three stages were tried to study their effectiveness. With the AGC applied only to the first stage, 64 dB of AGC control was obtained with a maximum deviation from flatness in the passband of 0.7 dB. With the AGC applied to all three stages, 90 dB of AGC control was obtained, with a maximum deviation from flatness in the passband of 1 dB. These two conditions represent the minimum and maximum extremes. When the combinations of the three stages taken two at a time were tried, they all fell within the above range. Thus for the design specification, it was sufficient to AGC only the first stage. The variation of bandwidth and center frequency were measured and the results are shown in Figure 23. This data indicates a maximum of 5% bandwidth deviation occurring at the low gain (maximum AGC) condition, with full AGC occurring over a 2.5 volt range. With an input of 50μ volts rms, the output signal into 50 ohms is 156 mvolts with a noise level of 6.8 mvolts.

The results of this design strongly indicate that the MC1550 has tremendous potential for use in both the R-F and I-F stages of television, radio, radar, and communication gear where high gain, wide AGC control, and low cost are of prime importance.

AGC Voltage	Power Gain dB	Center Frequency MHz	Bandwidth MHz
0.0	70.0	45.0	6.0
0.5	70.0	45.0	6.0
1.0	70.0	45.0	6.0
1.5	70.2	45.0	6.0
2.0	70.2	45.0	6.0
2.5	63.5	45.0	5.9
3.0	58.4	45.0	5.8
3.5	46.1	45.0	5.8
4.0	28.7	45.0	5.8
4.5	6.2	45.0	5.7

FIGURE 23

OSCILLATOR

The MC1550 can conveniently be used as an oscillator in both the CE-CB and CC-CB configurations. In this section, the CE-CB configuration will be analyzed to determine the factors that will influence the frequency of oscillation, and a practical circuit given for a 5-10 MHz oscillator. Consider first the fundamentals of oscillator operation from Figure 24. The closed loop voltage gain of Figure 24 is given by:

$$A_{CL} = \frac{e_0}{e_1} = \frac{A_{OL}(\omega)}{1 - A_{OL}(\omega)\,\beta(\omega)} \qquad (22)$$

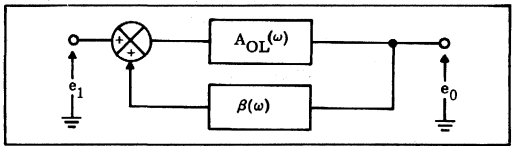


FIGURE 24 – BASIC FEEDBACK AMPLIFIER

Where A_{OL} represents the open-loop gain of the amplifier with the output of the amplifier loaded by the input impedance of the feedback network, $\beta(\omega)$. From equation 22, the closed-loop gain increases without bound when

$$A_{OL}(\omega)\,\beta(\omega) = 1 \qquad (23)$$

and self-sustained oscillations result. This equation indicates that the frequency of oscillation can be found by setting the imaginary component of $A_{OL}\,\beta(\omega)$ equal to zero. Once the frequency of oscillation, ω_0, has been determined, $\beta(\omega_0)$ can be found, and the threshold gain, A_T, below which oscillations will not be sustained may be determined from equation 24 below:

$$A_T(\omega_0) = \frac{1}{\beta(\omega_0)} \qquad (24)$$

This is the approach which will be used in analyzing the MC1550. With a signal applied to the base of transistor Q_1, the MC1550 acts as a common-emitter, common-base amplifier with high voltage gain and 180^o phase shift at low frequencies. Because of the internal 180^o phase shift, the $\beta(\omega)$ network must introduce an additional 180^o phase shift from the output terminal (pin 6) to the input terminal (pin 1) so that positive feedback will result.

Although this phase shift can be accomplished by a number of methods, perhaps the easiest method of achieving it is the use of an inverting transformer connection. This method is shown in Figure 25. A simplified analysis of this circuit is as follows: Assuming first an ideal transformer, the voltage appearing at the input terminal is:

$$e_1 = -\frac{1}{n}\,e_0 \qquad (25)$$

By definition,

$$\beta(\omega) = \frac{e_1}{e_0}$$

so that

$$\beta(\omega) = -\frac{1}{n} \qquad (26)$$

Substituting equation 26 into equation 2:

$$A_{OL}\left(-\frac{1}{n}\right) = 1$$

or

$$A_{OL} = -n \qquad (27)$$

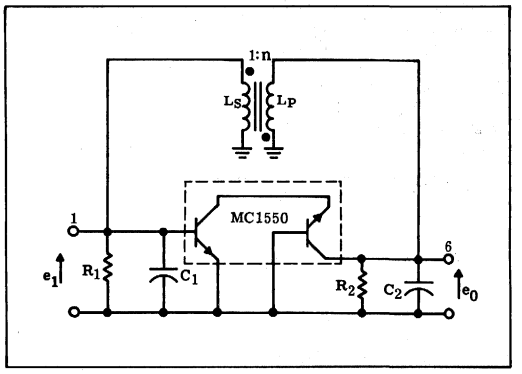


FIGURE 25 – TRANSFORMER COUPLED FEEDBACK AMPLIFIER

Hence, the open-loop gain must be equal to or greater than the turns ratio of the ideal transformer. From the discussion given in the video amplifier section of this application note, the expression for the low frequency voltage gain is:

$$A_V = -\frac{R_L}{r_{e_1}} \qquad (28)$$

Where R_L is the output load of the device and r_{e_1} is the dynamic emitter resistance of transistor Q_1 and is given by

$$r_{e_1} = \frac{26\ (mV)}{I_e\ (mA)}\ \text{(at room temperature.)}$$

From Figure 26, the equivalent load on the amplifier is:

$$R_L = R_o \parallel R_2 \parallel r_p \parallel n^2R_1 \qquad (29)$$

where

R_o = the output resistance of the MC1550

R_2 = external load resistor

r_p = resistance of the transformer coil

$r_p = (Q_{\text{unloaded of coil}}) \cdot (\omega L_p)$

n^2R_1 = resistance reflected into the primary from the secondary due to the transformer action

$\parallel$ denotes the parallel combination.

The expression of the open-loop gain now becomes

$$\left|A_{OL}\right| = \frac{R_o \parallel r_p \parallel R_2 \parallel n^2R_1}{r_{e_1}} \qquad (30)$$

Substituting equation 30 into equation 27, the condition for self-starting and sustained oscillation is

$$\frac{R_o \parallel r_p \parallel R_2 \parallel n^2R_1}{nr_{e_1}} \geq 1\ . \qquad (31)$$

The frequency of oscillation of the circuit is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_P\left(C_2 + \frac{C_1}{n^2}\right)}} \qquad (32)$$

Although the above equations were derived for an ideal transformer, the same method of analysis will be valid for the non-ideal transformer case. Using the model given in Figure 26, the same procedure used above may be repeated to solve for the minimum value of gain and the frequency of oscillation. This analysis is detailed in Appendix C, and the results are:

$$f_{osc} = \frac{1}{2\pi\sqrt{(1-K^2)\,L_P C_T}} \quad \text{For } K<1 \qquad (33)$$

$$A_T(\omega_0) = -\alpha \quad \text{Where } \alpha = K\sqrt{\frac{L_P}{L_S}} \qquad (34)$$

(See Appendix C for definition of terms).

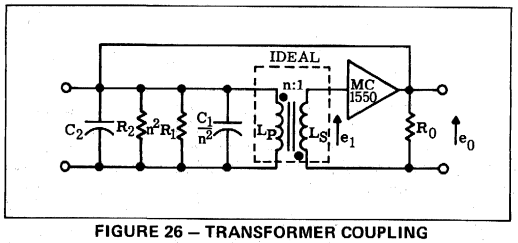


FIGURE 26 – TRANSFORMER COUPLING REFERRED TO PRIMARY

The circuit shown in Figure 27 was designed using the above equations, to obtain an output frequency that is variable from 5 to 10 MHz. The curve in Figure 28 shows the relationship between the value of C_2 and the frequency of oscillation for both measured and calculated values using equations 32 and 33.

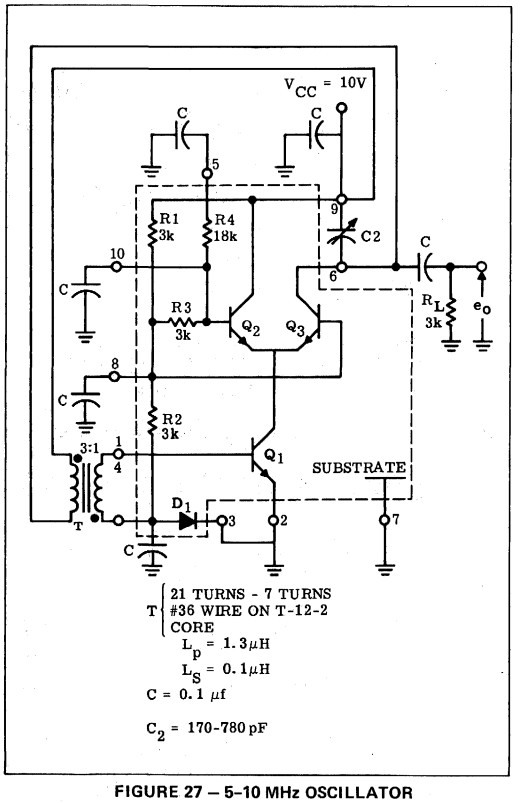


FIGURE 27 – 5-10 MHz OSCILLATOR

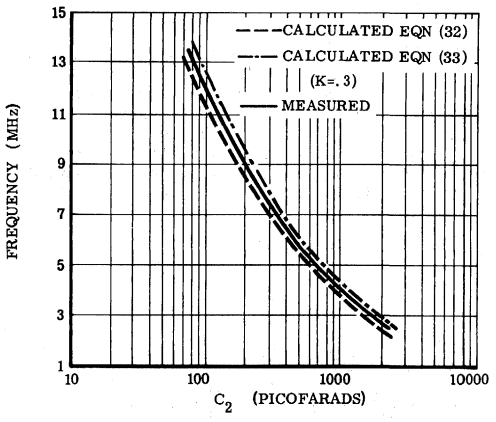


FIGURE 28 – FREQUENCY versus C_2

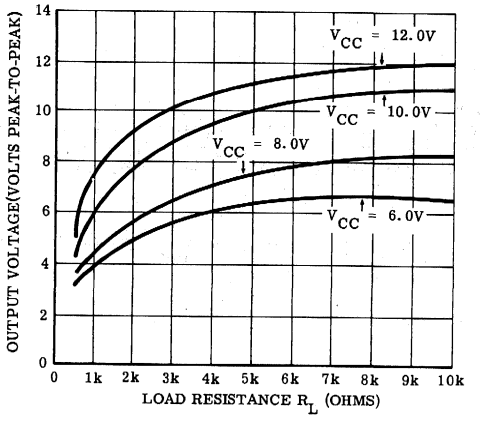


FIGURE 29 – OUTPUT VOLTAGE versus LOAD RESISTANCE

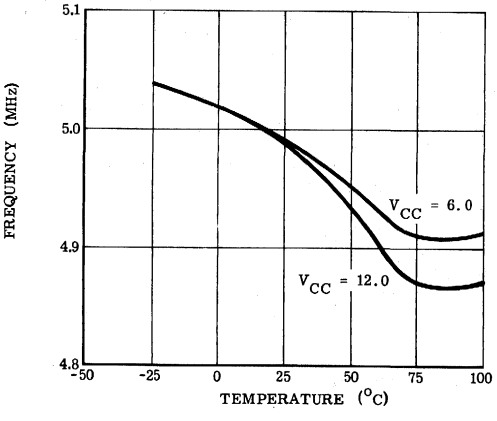


FIGURE 30 – FREQUENCY versus TEMPERATURE

The curves in Figure 29 shows the output voltage of the oscillator as a function of load resistance for various supply voltages. It is seen that for a load resistance greater than 10k ohms, the output voltage is essentially constant.

Figure 30 gives an indication of the frequency stability of this oscillator centered at 5.00 MHz at 25°C over a temperature range from -25°C to 100°C. Figure 31 is a photograph of the output waveform at 5.0 MHz.

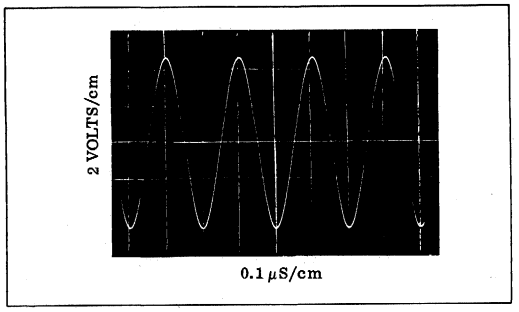


FIGURE 31 – OUTPUT WAVEFORM OF OSCILLATOR (FIGURE 27)

VIDEO AMPLIFIER

One of the many methods of using the MC1550 as a video amplifier as shown in Figure 32. The circuit may be analyzed for voltage gain using the equivalent circuit shown in Figure 33. Using model analysis, the equations from Figure 33 are:

$$\frac{e_S}{r_b' + R_S} = V_2\left(\frac{1}{\beta r_{e_1}} + \frac{1}{r_b' + R_S}\right) \tag{35}$$

$$0 = V_2\left(\frac{1}{r_{e_1}}\right) + V_3\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}} + SC_S\right) \tag{36}$$

$$0 = -V_3\left(\frac{\alpha}{r_{e_1}}\right) + e_0\left(\frac{1}{R_L} + SC_O\right) \tag{37}$$

Where

$$\frac{1}{\beta} = \frac{1}{\beta_o} + \frac{S}{\omega_T}$$

and

$$C_O = C_S + C_L$$

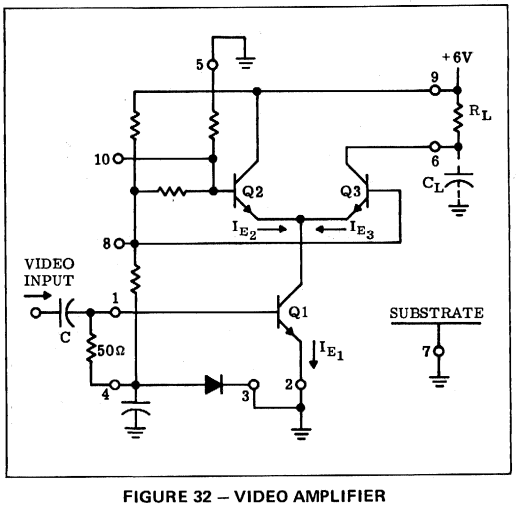


FIGURE 32 – VIDEO AMPLIFIER

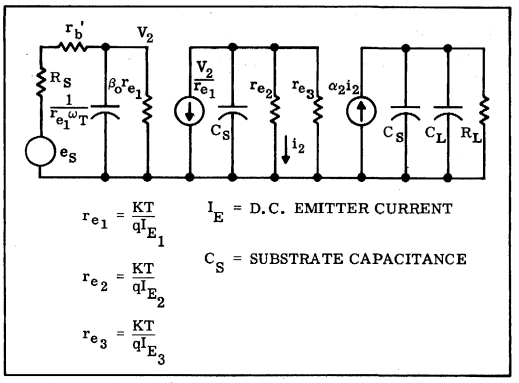


FIGURE 33 – MC1550 EQUIVALENT CIRCUIT

Using equations 35, 36, and 37 above, the equation for the voltage gain is

$$A_V(S) = \frac{e_o}{e_S} = -\frac{1}{r_b' + R_S}\left(\frac{\alpha}{r_{e_1} r_{e_2}}\right) \frac{1}{\left\{\left[\left(\frac{1}{r_{e_1}}\right)\left(\frac{1}{\beta_o} + \frac{S}{\omega_T}\right) + \frac{1}{r_b' + R_S}\right]\left[SC_S + \frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right]\left[SC_O + \frac{1}{R_L}\right]\right\}} \tag{38}$$

Equation 38 can be somewhat simplified if

$$\frac{1}{\beta_o r_{e_1}} \ll \frac{1}{r_b' + R_S} \quad \text{OR} \quad r_b' + R_S \ll \beta_o r_{e_1} \tag{39}$$

Using the simplification in Figure 5 and factoring, equation 40 results:

$$A_V(S) = -\frac{1}{r_b' + R_S}\left(\frac{\alpha}{r_{e_1} r_{e_2}}\right) \left[\frac{1}{\frac{C_S C_O}{r_{e_1}\omega_T}\left(S + \frac{r_{e_1}\omega_T}{r_b' + R_S}\right)\left(S + \frac{1}{C_S}\left[\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right]\right)\left(S + \frac{1}{R_L C_O}\right)}\right] \tag{40}$$

Using equation 40, the D.C. value of voltage gain is calculated by setting S = 0:

$$A_V(0) = -\frac{R_L}{r_{e_1} r_{e_2}\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right)} \text{ FOR } \alpha = 1 \tag{41}$$

Equation 41 clearly points out the effect that the AGC variations has on voltage gain. If V_{AGC} = 0 volts, then $I_{Q_3} \approx 0$ and $1/r_{e_3} \approx 0$. For this case, equation 41 becomes:

$$A_V(0) = -\frac{R_L}{r_{e_1}} \tag{41a}$$

If V_{AGC} = +6 volts, then $I_{Q_2} \approx 0$ and $1/r_{e_2} \approx 0$ or $r_{e_2} \to \infty$ so that equation 41 becomes

$$A_V(0) = -\frac{R_L}{r_{e_1}\left(1 + \frac{r_{e_2}}{r_{e_3}}\right)} \approx 0 \tag{42}$$

Equations 41a and 42 represent the extremes of the D.C. voltage gain, and equation 41 can be used to find the gain at any point between 0 and the maximum. Consider now the use of equation 40 in the design of a video amplifier to meet the following specifications:

$A_V(0) = 25$

$V_{CC} = 6$ volts

Bandwidth > 20 MHz

$R_S = 50$ ohms

The transistor parameters are

$r_b' = 50\Omega$

$\omega_T = 2\pi(9 \times 10^8)$ Hz

$C_S = 5$ pF

$r_{e_1} = 25\Omega$ For $V_{CC} = 6.0$ Volts

The load resistor, R_L required is:

$$R_L = A_V(0)\, r_{e_1}$$

$$R_L = 625\Omega.$$

The dominant pole will be created by the load capacitance and R_L. Since $C_S \approx 5$ pF, the value of C_L must be less than 8 pF for a bandwidth greater than 20 MHz. Therefore, assume that $C_O \approx 10$ pF, then the break frequencies are given by:

$$f_1 = \frac{1}{2\pi R_L C_O} = 25.4 \text{ MHz}$$

$$f_2 = \frac{r_{e_1} f_T}{r_b' + R_S} \approx \frac{f_T}{3} = 300 \text{ MHz}$$

$$f_3 = \frac{1}{C_S}\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right) > 1.2 \text{ gHz for } V_{AGC} = 0 \text{ or } 6 \text{ volts.}$$

The curve in Figure 34 shows a comparison between measured and calculated data for the circuit of Figure 32 when $R_L = 625\Omega$ and $C_L < 5$ pF. The data indicates that, although a simplified model was used to analyze the circuit, reasonably valid results are obtained in the laboratory.

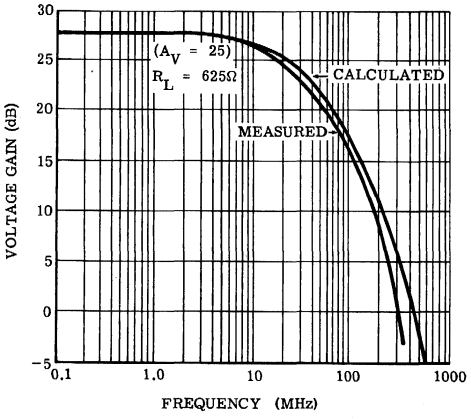


FIGURE 34 – MC1550 VIDEO AMPLIFIER GAIN versus FREQUENCY

AMPLITUDE MODULATOR

The AGC characteristics of the MC1550 make it very useful as an amplitude modulator as shown in Figure 35. If the voltage at the base of transistor Q_2 is time-varying, the gain of the amplifier will also be time-varying. By injecting an audio signal into the base of transistor Q_2, the RF carrier will be amplified as a function of the audio input. Considering the circuit in terms of y-parameters, the voltage gain is given by:

$$A_V = \frac{|y_{21}|\angle\phi}{y_{22} + Y_L} \qquad (43)$$

From this equation, it is seen that if $|y_{21}|$ is varied sinusoidally, the voltage gain varies sinusoidally, and the output will be an amplitude modulated wave. The amount of distortion will depend on how linear the gain varies with the input sinusoid. Figure 37 shows the manner in which $|y_{21}|$ varies with AGC voltage at 45 MHz ($V_{CC} = 6.0$V). The curve in Figure 37 shows that between $V_{AGC} = 2.75$ volts and $V_{AGC} = 4.25$ volts, $|y_{21}|$ is very linear with AGC voltage. By biasing the AGC line (pin 5) to 3.5 volts and impressing an audio signal on the base of Q_2 (pin 10), $|y_{21}|$ varies along the linear portion of the curve. Because of the linearity of this portion of the curve, very little distortion in the output results. Using the y-parameter curve of Figure 37, the up modulation and down modulation may be calculated. Referring to Figure 36, the up and down modulation factors are defined as:

$$M_u = \frac{E_{max} - E}{E} \quad \text{(UPWARD MODULATION)} \qquad (44)$$

$$M_d = \frac{E - E_{min}}{E} \quad \text{(DOWNWARD MODULATION)} \qquad (45)$$

Where:

E = peak amplitude of the unmodulated carrier

E_{max} = maximum amplitude attained by the modulated carrier envelope.

E_{min} = minimum amplitude of the modulated carrier envelope.

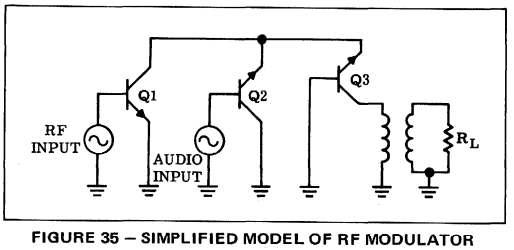


FIGURE 35 – SIMPLIFIED MODEL OF RF MODULATOR

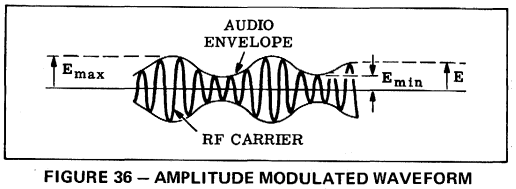


FIGURE 36 – AMPLITUDE MODULATED WAVEFORM

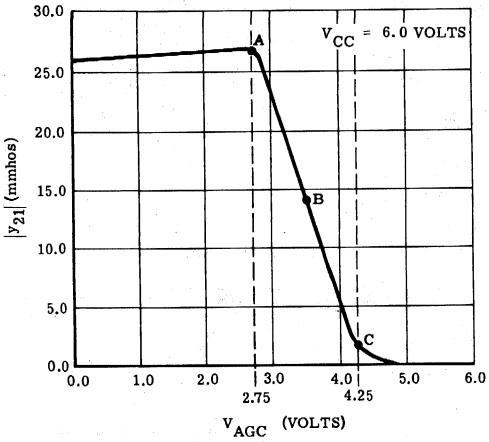


FIGURE 37 – $|y_{21}|$ versus V_{AGC} AT 45 MHz

Observe from Figure 37 that E_{max} occurs at point "A" where the audio signal is at minimum amplitude and E_{min} occurs at point "C" where the audio signal is at maximum amplitude. The nominal value of E occurs at point "B" when the audio signal crosses thru zero volts. If we let e_{in} be the input voltage, then the output voltage can be found from equation 43.

$$e_0 = \frac{e_{in}|y_{21}|}{y_{22} + Y_L} \tag{46}$$

Thus the values of E_{min}, E_{max}, and E can be found to be

$$E_{min} = \frac{e_{in}|y_{21}|_C}{y_{22} + Y_L} \tag{47}$$

$$E_{max} = \frac{e_{in}|y_{21}|_A}{y_{22} + Y_L} \tag{48}$$

$$E = \frac{e_{in}|y_{21}|_B}{y_{22} + Y_L} \tag{49}$$

$M\mu$ and M_d can now be found from equations 44 and 45:

$$M_u = \frac{|y_{21}|_A - |y_{21}|_B}{|y_{21}|_B} \tag{50}$$

and

$$M_d = \frac{|y_{21}|_B - |y_{21}|_C}{|y_{21}|_B} \tag{51}$$

Substituting the values of $|y_{21}|_A$, $|y_{21}|_B$ and $|y_{21}|_C$ found in Figure 37 into equations 51 and 52, we find,

$$M_u = 0.90$$
$$M_d = 0.91$$

These are the values of up modulation and down modulation which may be expected without distortion.

When the circuit shown in Figure 38 was designed and tested, the following results were achieved:

$$M_u = 0.89 \text{ and } M_d = 0.89$$

Two output waveforms of this modulator are shown in Figures 39(a) and 39(b). As one can see, very good modulation has been achieved with very little distortion.

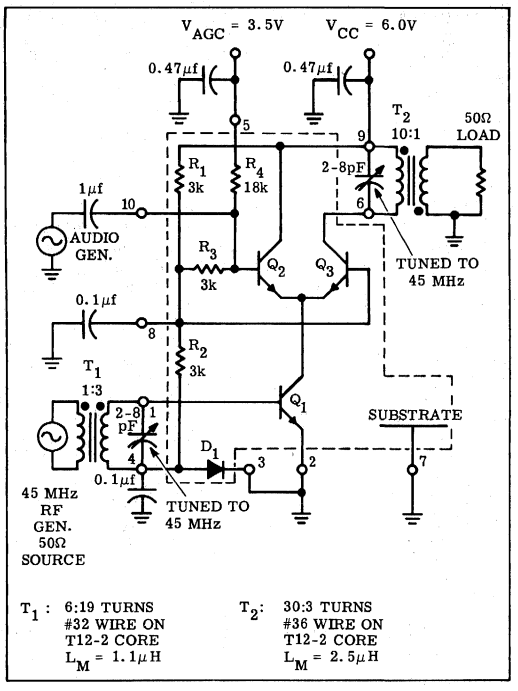
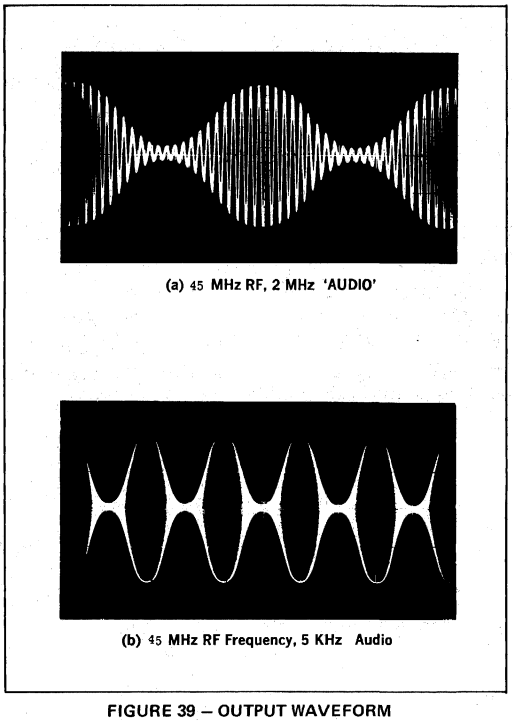


FIGURE 38 – RF MODULATOR



(a) 45 MHz RF, 2 MHz 'AUDIO'

(b) 45 MHz RF Frequency, 5 KHz Audio

FIGURE 39 – OUTPUT WAVEFORM OF RF MODULATOR (FIGURE 34)

APPENDIX A

For an ideal p-n junction, the current is related to the voltage by the equation

$$I = I_o\left(e^{\frac{V}{nV_T}} - 1\right) \tag{52}$$

where a positive value of V represents a forward biased junction, n is a parameter (≈2 for silicon) to account for recombination at the junction transition region, V_T is the electron-volt equivalent of temperature and is given by $V_T = KT/q$, and I_o is the reverse saturation current. Thus, for transistor Q_1 biasing

$$I_{D_1} = I_{o_{D_1}}\left(e^{\frac{V_{D_1}}{nV_T}} - 1\right) \text{and } I_{E_1} = I_{o_{E_1}}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right). \tag{53}$$

When the diode is forward biased, V_{D_1} is equal to the base-emitter voltage, V_{BE}, of transistor Q_1 and the -1 term in the parenthesis can be neglected. Thus; we may write

$$I_{D_1} = I_{o_{D_1}}\left(e^{\frac{V}{nV_T}}\right) \text{and } I_{E_1} = I_{o_{E_1}}\left(e^{\frac{V}{nV_T}}\right) \tag{54}$$

where

$$V = V_{BE} = V_{D_1} .$$

If the two p-n junctions are physically matched by being located very close together, the reverse saturation currents will be nearly equal. That is,

$$I_{o_{D_1}} = I_{o_{E_1}} \tag{55}$$

thus, $I_{D_1} = I_{E_1}$ as given in the text.

APPENDIX B – TRANSITION WIDTH OF EMITTER-COUPLED CIRCUIT

The MC1550 is partially re-drawn in Figure 40. In this figure, Q_1 is represented as a current source and current I_3 is to be related to voltages V_8 and V_{10}:

The currents I_2 and I_e may be related to the voltages ϕ_1 and ϕ_2 by equations 56 and 57:

$$I_2 \approx a_{11}\, e^{\frac{q\phi_1}{KT}} \tag{56}$$

$$I_3 = a_{11}\, e^{\frac{q\phi_2}{KT}} \tag{57}$$

Assuming I_2 and I_3 are approximately equal to the emitter currents, then:

$$I_2 + I_3 = I_{Q_1} . \tag{58}$$

Also,

$$V_8 - V_{10} = \phi_1 - \phi_2 . \tag{59}$$

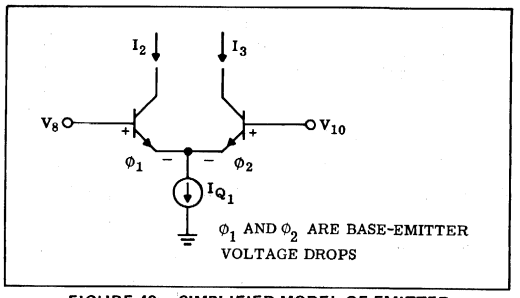


FIGURE 40 – SIMPLIFIED MODEL OF EMITTER COUPLED CIRCUIT

Using the above equations, the current I_3 may be found:

$$I_3 = \frac{I_{Q_1}}{1 + e^{\frac{q(V_8 - V_{10})}{KT}}} \tag{60}$$

Assuming V_{10} is held constant at some prescribed value, I_3 is plotted as a function of V_8 in Figure 41.

If $(V_8 - V_{10})$ is assumed to reach two values, one which causes $I_3 = 0.1\, I_{Q_1}$ (denote it as V_a) and one which causes $I_E = 0.9\, I_{Q_1}$ (denote it as V_b), then the difference between the two will give the transition width ΔV_B:

$$0.1\, I_{Q_1}\left(1 + e^{\frac{qV_a}{KT}}\right) = I_{Q_1} \tag{61}$$

$$0.9\, I_{Q_1}\left(1 + e^{\frac{qV_b}{KT}}\right) = I_{Q_1} \tag{62}$$

Solving for V_a and V_b we have

$$V_a = \left(\frac{KT}{q}\right) \ln 9 \tag{63}$$

$$V_b = \left(\frac{KT}{q}\right) \ln \frac{1}{9} . \tag{64}$$

Hence

$$\Delta V_8 = V_a - V_b \tag{65}$$

and

$$\Delta V_8 = \frac{KT}{q} \ln 9 + \frac{KT}{q} \ln 9 \tag{66}$$

or

$$\Delta V_8 = \frac{KT}{q} \ln 81 \approx 4.4\, \frac{KT}{q} . \tag{67}$$

At room temperature ($T \doteq 25^oC$)

$$\Delta V_8 = 114 \text{ mv} .$$

APPENDIX C – DERIVATION OF OSCILLATOR FREQUENCY AND THRESHOLD GAIN

The circuit shown in Figure 42 is an equivalent model of the transformer when the coefficient of coupling is not unity. The parameters for this model are as follows:

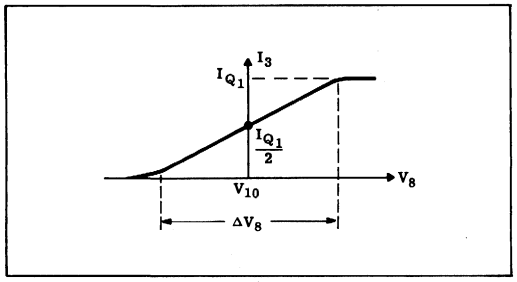


FIGURE 41 – TRANSITION WIDTH OF EMITTER COUPLED CIRCUIT

R_o = output resistance of the MC1550

R_L = external load resistance

R_1 = input resistance of the MC1550

C_o = output capacitance of the MC1550

C_L = external load capacitance

C_1 = input capacitance of the MC1550

L_e = leakage inductance of the transformer

$= (1 - K^2)\, L_p$

L_m = magnatizing inductance of the transformer

$= K^2 L_p$

L_p = primary inductance of transformer

L_s = secondary inductance of transformer

α = effective turns ratio $= K\sqrt{\frac{L_p}{L_s}}$

K = coefficient of coupling

In the circuit of Figure 43, the secondary impedance have been reflected into the primary and,

$$R_T = \frac{R_o R_L}{R_o + R_L},\quad R_X = \alpha^2 R_1,\quad C_T = C_o + C_L,\quad C_X = \frac{C_1}{\alpha^2}\ .$$

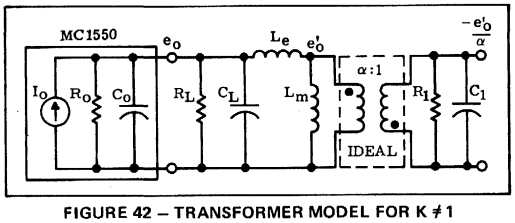


FIGURE 42 – TRANSFORMER MODEL FOR K ≠ 1

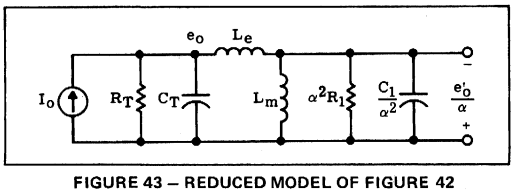


FIGURE 43 – REDUCED MODEL OF FIGURE 42

Consider next the output current of the MC1550 as an independent source and form a Thévenin equivalent for this source. This is shown in Figure 44. This is the figure which will be used for the following analysis. By definition,

$$\beta = \frac{e_1}{V_o} \tag{68}$$

or from Figure 40

$$\beta = \frac{-e'_o}{\alpha V_o}\ . \tag{69}$$

Solving for $\frac{e_o}{V_o}$ in Figure 25:

$$\frac{e'_o}{V_o} = \frac{S\left(S + \frac{1}{R_T C_T}\right)}{S^4(L_e C_X) + S^3\left(\frac{L_e}{R_X} + \frac{L_e C_X}{R_T C_T}\right) + S^2\left(1 + \frac{L_e}{L_m} + \frac{C_X}{C_T} + \frac{L_e}{R_T R_X C_T}\right)}$$

$$\frac{S\left(S + \frac{1}{R_T C_T}\right)}{+ S\left(\frac{1}{R_T C_T} + \frac{L_e}{L_m R_T C_T} + \frac{1}{R_X C_T}\right) + \frac{1}{L_m C_T}}\ . \tag{70}$$

Now letting $S = j\omega$

$$\frac{e'_o}{V_o} = \frac{-\omega^2 + j\omega\left(\frac{1}{R_T C_T}\right)}{\left[\omega^4\left(L_e C_X\right) - \omega^2\left(1 + \frac{L_e}{L_m} + \frac{C_X}{C_T} + \frac{L_e}{R_T R_X C_T}\right) + \frac{1}{L_m C_T}\right]}$$

$$\frac{-\omega^2 + j\omega\left(\frac{1}{R_T C_T}\right)}{- j\left[\omega^3\left(\frac{L_e}{R_X} + \frac{L_e C_X}{R_T C_T}\right) - \omega\left(\frac{1}{R_T C_T} + \frac{L_e}{L_m R_T C_T} + \frac{1}{R_X C_T}\right)\right]} \tag{71}$$

Multiplying both the numerator and denominator by the conjugate of the denominator, and setting the imaginary component equal to zero and combining like terms, we have

$$\omega^4 + \omega^2\left(\frac{R_X}{R_T}\right)\left(\frac{\frac{C_X}{C_T} - \frac{R_T}{R_X} + \frac{L_e}{R_T R_X C_T}}{L_e C_T}\right) - \frac{R_X}{R_T}\left(\frac{1}{L_m L_e C_T^2}\right) \tag{72}$$

The exact solution to this equation is quite complex and offers little insight to the analysis. However, with the following assumptions, this reduces to a very simple form.

Assume:

(A) $C_T \gg C_X$ (B) $\frac{L_e}{C_T} \ll R_T^2$ (C) $R_T \gg R_X$

For these assumptions,

$$\omega_o^2 = \frac{1}{L_e C_T} \tag{73}$$

or

$$f_o = \frac{1}{2\pi\sqrt{(1-K^2)\, L_p C_T}} \tag{74}$$

This is the approximate frequency of oscillation. To find the threshold gain of the amplifier, the value of ω_o found above must be substituted into the real component of β to solve for $\beta(\omega_o)$. With the same assumptions as above, this procedure results in equation 75:

$$\text{Real } \beta(\omega_o) = \frac{1 - \frac{L_e}{R_T C_T}\left[\frac{L_e}{L_m R_T} - \frac{1}{R_X}\right]}{-\alpha\left\{1 + \frac{L_e}{R_T C_T}\left[\frac{2}{R_X} + \frac{L_e}{R_T C_T R_X^2} - \frac{4R_T}{R_X^2}\right.\right.} \\ \left.\left. \frac{1 - \frac{L_e}{R_T C_T}\left[\frac{L_e}{L_m R_T} - \frac{1}{R_X}\right]}{- \frac{4}{R_X}\left(\frac{L_e}{L_m} - 1\right) + \frac{1}{R_T}\left(\frac{L_e}{L_m} - 1\right)^2}\right]\right\} \tag{75}$$

which reduces to the approximation,

$$\text{Real } \beta(\omega_o) = -\frac{1}{\alpha} \tag{76}$$

The threshold gain, A_T, is now found from the equation

$$A_T(\omega_o) = \frac{1}{\beta(\omega_o)}$$

or

$$A_T(\omega_o) = -\alpha \tag{77}$$

where α is the effective coefficient of coupling.

Equations 74 and 77 are those given in the text.

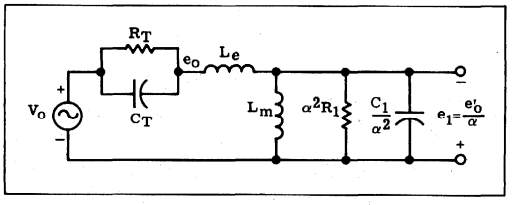


FIGURE 44 – THEVENIN EQUIVALENT OF FIGURE 43

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RF SMALL SIGNAL DESIGN USING ADMITTANCE PARAMETERS

INTRODUCTION

Design of the solid-state small-signal RF amplifier using two port parameters is a systematic, mathematical procedure, with an exact solution (free from approximation) available for the complete design problem. The only sources of error in the final design are parameter variations resulting from transistor parameter distributions and strays in the physical circuit. Parameter distributions result from limits in measurement and random variations among identically designed transistors.

The purpose of this paper is to provide, in a single working reference, the important relationships necessary for the complete solution of the RF small signal design problem using admittance parameters. Further, equations are given in the appendix for the conversion of other sets of two-port parameters to admittance parameters.

The paper is based on work by Linvill[1], Stern[2], and others. Those who may wish to consider the derivations of some of the expressions should refer to the original work presented in the references.

The report assumes that the reader is familiar with the two port parameter method of describing a linear active network. Several references are available on this subject.[1,2,6]

It has also been assumed that a suitable transistor for the task at hand has been selected, and that two-port parameters are available for the frequency and bias point which will be used. Device selection will not be covered as a separate topic in this report; rather, a thorough understanding of the material in the report should provide the designer with the tools he needs to select transistors for a particular small signal application.

The equations given in the text of the report are applicable to the common emitter, common base, or common collector configuration, if the applicable set of parameters (common emitter, common base, or common collector parameters) is used. Equations for the conversion of the admittance or hybrid parameters of any configuration to either of the other two configurations of the same parameter set are given in the appendix.

While directed primarily toward circuit design with conventional junction transistors, two port network theory has the advantage of being applicable to any linear active network. The same design approach and equations may therefore be used with field effect transistors[7], integrated circuits, or any other device which may be described as a linear active two-port network with measurable parameters.

Finally, various parameter interrelationships and other data are given in the Appendix.

GENERAL DESIGN CONSIDERATIONS

Design of the RF small signal tuned amplifier is usually based on a requirement for a specified power gain at a given frequency. Other design goals include bandwidth, stability, and input-output isolation. After a basic circuit type is selected, the applicable design equations can be solved.

Circuits may be categorized according to feedback (neutralization, unilateralization, or no feedback), and matching at transistor terminals (circuit admittances either matched or mismatched to transistor input and output admittances). Each of these circuit categories will be discussed, including the applicable design equations and the considerations leading to the selection of a particular configuration.

STABILITY

A major factor in the overall design is the potential stability of the transistor. This may be determined by computing the Linvill stability factor[1] C using the following expression: †

$$C = \frac{\left|y_{12}\, y_{21}\right|}{2g_{11}\, g_{22} - \mathrm{Re}\,(y_{12}y_{21})} \qquad (1)$$

When C is less than 1, the transistor is unconditionally stable. When C is greater than 1, the transistor is potentially unstable.

The C factor is a test for stability under a hypothetical worst case condition; that is, with both input and output transistor terminals open circuited. With no external feedback, an unconditionally stable transistor will not oscillate with any combination of source and load. If a transistor is potentially unstable, certain source and load combinations will produce oscillations.

Although the C factor may be used to determine the potential stability of a transistor, the conditions of open circuited source and load which are assumed in the C factor test are not applicable to a practical amplifier. Consequently it is also desirable to compute the relative stability of actual amplifier circuits, and Stern[2] has defined a stability factor k for this purpose. The k factor is similar to the C factor except that it also takes into account finite source and load admittances connected to the transistor. The expression for k is:

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{\left|y_{12}y_{21}\right| + \mathrm{Re}\,(y_{12}y_{21})} \qquad (2)$$

If k is greater than one, the circuit will be stable. If k is less than one, the circuit will be potentially unstable and will very likely oscillate at some frequency.

Note that the C factor simply predicts potential stability of a transistor with an open circuited source and load, while the k factor provides a stability computation for a specific circuit.

Stability considerations will be discussed further in the descriptions of each basic circuit type to follow.

GENERAL DESIGN EQUATIONS

There are a number of design equations which are applicable to most types of amplifiers. These equations will be discussed first. Descriptions of specific amplifier types will then follow, and each will contain additional design equations applicable to that particular amplifier.

POWER GAIN

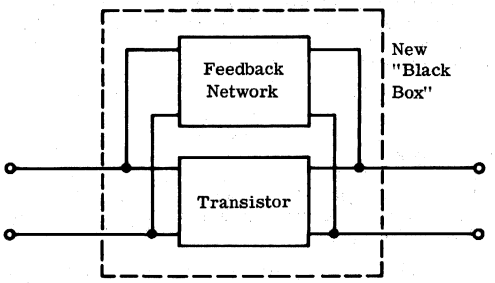
The general expression for power gain is:

$$G = \frac{\left|y_{21}\right|^2 \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22}\right|^2 \mathrm{Re}\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (3)$$

Equation 3 applies to circuits with no external feedback. It can also be used with circuits which have external feedback if the composite y parameters of both transistor and feedback network are substituted for the transistor y parameters in the equation. The composite y parameters

† $\mathrm{Re}\,(Y_{12}Y_{21})$ = Real part of $(Y_{12}Y_{21})$

are determined by considering the transistor and the feedback network to be two "black boxes" in parallel:



For example, the above combination of transistor and feedback network may be characterized as a single "black box" by the following equations:†

$$\begin{aligned} y_{11c} &= y_{11t} + y_{11f} \\ y_{12c} &= y_{12t} + y_{12f} \\ y_{21c} &= y_{21t} + y_{21f} \\ y_{22c} &= y_{22t} + y_{22f} \end{aligned} \qquad (4)$$

Where:

y_{11c}, y_{12c}, y_{21c}, y_{22c} are the composite y parameters of the parallel combination of transistor and feedback network.

y_{11t}, y_{12t}, y_{21t}, y_{22t} are the y parameters of the transistor.

y_{11f}, y_{12f}, y_{21f}, y_{22f} are the y parameters of the feedback network.

Note that, since this approach treats the transistor and feedback network combination as a single "black box" with y_{11c}, y_{12c}, y_{21c}, and y_{22c} as its y parameters, the composite y parameters may therefore be substituted in any of the design equations applicable to a linear, active, two port analysis.

The neutralized and unilateralized amplifiers are special cases of this general concept, and equations associated with those special cases will be given later.

Equation 3 provides a solution for power gain of the linear active network (transistor) only. Input and output networks are considered to be part of the source and load, respectively. Two important points should therefore be kept in mind:

(1) Power gain computed from equation 3 will not take into account network losses. Input network loss reduces power delivered to the transistor. Power lost in the output network is computed as useful power output, since the load admittance Y_L is the combination of the output network and its load.

(2) Power gain is independent of source admittance. An input mismatch results in less input power being delivered to the transistor. Accordingly, note that equation 3 does not contain the term Y_S.

†Refer to Seshu and Balabanian, "Linear Network Analysis, "John Wiley and Sons, 1959, P321

The power gain of a transistor together with its associated input and output networks may be computed by measuring the input and output network losses, and subtracting them from the power gain computed with equation 3 .

In some cases it may be desirable to include the effects of input matching in power gain computations. A convenient term is transducer gain G_T, defined as output power delivered to a load by the transistor, divided by the maximum input power available from the source.

The equation for transducer gain is:

$$G_T = \frac{4 \operatorname{Re}(Y_s) \operatorname{Re}(Y_L) |y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2} \qquad (5)$$

In this equation, Y_L is the composite transistor load admittance-composed of both output network and its load, and Y_S is the composite transistor source admittance-composed of both input network and its source. Therefore, transducer gain includes the effects of the degree of admittance match at the transistor input terminals but does not take into account input and output network losses.

As in equation 3 , the composite y parameters of a transistor feedback network combination may be substituted for the transistor y parameters when such a combination is used.

The Maximum Available Gain MAG is an often used transistor figure-of-merit. The MAG is the theoretical power gain of a transistor with its reverse transfer admittance y_{12} set equal to zero, and its source and load admittances conjugately matched to y_{11} and y_{22}, respectively.

If $y_{12} = 0$, the transistor exhibits an input admittance equal to y_{11} and an output admittance equal to y_{22}.† The equation for MAG is, therefore, obtained by solving the general power gain expression, equation 3 , with the conditions

$$y_{12} = 0$$

$$y_L = y_{22}^*$$

$$\text{and } y_s = y_{11}^*$$

which yields:

$$MAG = \frac{|y_{21}|^2}{4 \operatorname{Re}(y_{11}) \operatorname{Re}(y_{22})} \qquad (6)$$

MAG is a figure of merit only, since it is physically impossible to reduce y_{12} to zero without changing the other parameters of the transistor. An external feedback network may be used to achieve a composite y_{12} of zero, but then the other composite parameters will also be modifed according to the relationships given in the discussion of the composite transistor - feedback network "black box."

TRANSISTOR INPUT AND OUTPUT ADMITTANCES

The expression for the input admittance of a transistor is:

$$Y_{IN} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L} \qquad (7)$$

†Obtained by solving the equations for transistor Y_{IN} and Y_{OUT} with y_{12} equal to zero. These equations are given later in the report.

The expression for the output admittance of a transistor is:

$$Y_{OUT} = y_{22} - \frac{y_{12}\, y_{21}}{y_{11} + Y_s} \qquad (8)$$

When the feedback parameter y_{12} is not zero, Y_{IN} is dependent on load admittance and Y_{OUT} is dependent on source admittance.

AMPLIFIER STABILITY

One of the major considerations in RF amplifier design is stability. The stability of a final design can be assured by including stability computations and considering stability in all design decisions relating to feedback and transistor source and load admittances.

The potential stability of the transistor should first be computed using equation 1 .

The various alternatives concerning input - output matching and neutralization - unilateralization will now be discussed for both the unconditionally stable transistor and the potentially unstable transistor.

THE UNCONDITIONALLY STABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is less than one, the transistor is unconditionally stable. Oscillations will not occur using any combination of source and load admittances without external feedback. Stability is therefore eliminated as a factor in the remainder of the design, and complete freedom is possible with regard to matching and neutralization to optimize the amplifier for other performance requirements.

AMPLIFIERS WITHOUT FEEDBACK

The amplifier with no feedback is a logical choice for the unconditionally stable transistor in many applications since it may offer the advantages of fewer components and a simple tuning procedure.

Source and load admittances may be selected for maximum gain and/or any number of other requirements. Power gain and transducer gain may be computed using equations 3 and 5 , respectively; input and output admittances may be computed using equations 7 and 8, respectively.

The amplifier stability factor may be computed using equation 2 . While amplifier stability was assured from the beginning by the use of an unconditionally stable transistor, the designer may still wish to perform this computation to provide some insight into danger of instability under adverse environmental conditions, source and load variations, etc.

G_{max}

G_{max}, the highest transducer gain possible without external feedback, forms a special case of the no feedback amplifier.

The source and load admittances required to achieve G_{max} may be computed from the following:

$$G_s = \frac{1}{2\ \mathrm{Re}(y_{22})} \left\{ \left[2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \qquad (9)$$

$$B_s = -\mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{22})} \qquad (10)$$

$$G_L = \frac{1}{2\ \mathrm{Re}(y_{11})} \left\{ \left[2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \qquad (11)$$

$$B_L = -\mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{11})} \qquad (12)$$

Therefore, if the maximum possible power gain without feedback is desired for an amplifier, equations 9, 10, 11, and 12 are used to compute Y_S and Y_L.

The magnitude of G_{max} may be computed from the following expression:

$$G_{max} = \frac{\left| y_{21} \right|^2}{2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left\{ \left[2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}}} \qquad (13)$$

Equations 9, 10, 11, and 12 can be obtained by differentiating equation 5 with respect to G_S, B_S, G_L, and B_L, and setting the four derivatives equal to zero. The G_S, B_S, G_L, and B_L thus computed can then be substituted in equation 5 to obtain the expression for G_{max}, equation 13.

THE LINVILL METHOD

The amplifier without feedback design problem may also be solved graphically using a technique developed by J.G. Linvill.† Linvill's technique is very useful for a certain class of problems. Since it is so fully discussed in many good references we will not go into it further here. An advantage of the Linvill technique is that it provides a reasonably rapid graphic solution relating gain, bandwidth, and stability. A disadvantage is its scope of usefulness, since the standard Linvill solution applies only to an amplifier with no external feedback and with Y_S conjugately matched to the transistor input admittance, Y_{IN}.

THE UNILATERALIZED AMPLIFIER

Unilateralization consists of employing an external feedback network to achieve a composite y_{12} of zero.

While unilateralization is perhaps most often used to achieve stability with a potentially unstable transistor, other circuit considerations may also warrant the use of unilateralization with the unconditionally stable transistor. For example, the input-output isolation afforded by unilateralization may be desirable in a particular design.

Design equations for the unilateralized case are obtained by first computing the composite y parameters of the transistor - feedback network combination and then substituting the composite parameters in the general equations.

Referring to the discussion on composite y parameters and setting up the basic condition that y_{12c} must equal zero, the other composite y parameters can be computed. Assuming that a passive feedback network is being used, then

$$y_{11f} = y_{22f} = -y_{12f} = -y_{21f},$$

and since $y_{12c} = 0$, $y_{12t} + y_{12f} = 0$

then $y_{12t} = -y_{12f}$,

and $y_{12t} = -y_{12f} = y_{11f} = y_{22f} = -y_{21f}$

†Application Note AN166.
See also reference 5 in the bibliography.

Substituting the above results in equations 4 yields the following:

$$y_{11c} = y_{11t} + y_{12t}$$

$$y_{22c} = y_{22t} + y_{12t}$$

$$y_{12c} = y_{12t} - y_{12t} = 0$$

$$y_{21c} = y_{21t} - y_{12t}$$

Substituting these composite y parameters in equations 7, 8, 3, 16, and 5 respectively, yields equations 14, 15, 16, 17 and 18 for the unilateralized case:

Unilateralized input admittance

$$Y_{IN} = y_{11} + y_{12} \tag{14}$$

Unilateralized output admittance

$$Y_{OUT} = y_{22} + y_{12} \tag{15}$$

Unilateralized power gain, general expression:

$$G_{PU} = \frac{\left|y_{21} - y_{12}\right|^2 \, \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22} + y_{12}\right|^2 \, \mathrm{Re}(y_{11})} \tag{16}$$

Unilateralized power gain with Y_L conjugately matched to Y_{OUT}:

$$G_U = \frac{\left|y_{21} - y_{12}\right|^2}{4\,\mathrm{Re}(y_{11} + y_{12})\,\mathrm{Re}(y_{22} + y_{12})} \tag{17}$$

Unilateralized transducer gain:

$$G_{TU} = \frac{4\,\mathrm{Re}(Y_s)\,\mathrm{Re}(Y_L)\,\left|y_{21} - y_{12}\right|^2}{\left|(y_{11} + y_{12} + Y_s)\,(y_{22} + y_{12} + Y_L)\right|^2} \tag{18}$$

Note that equations 14, 15, 16, 17, and 18, are given entirely in terms of the transistor y parameters, not those of the feedback network or the composite.

Another benefit of unilateralization is input - output isolation. As can be seen in equations 14 and 15, Y_{IN} is completely independent of Y_L, and Y_{OUT} is similarly independent of Y_S. In a practical sense, this means that in a single or multi-stage amplifier using unilateralized stages, tuning of any one network will not affect tuning in other parts of the circuit. Thus, the troublesome task of having to re-peak an entire amplifier following a change in tuning at a single point can be eliminated.

NEUTRALIZATION

Neutralization consists of employing a feedback network to reduce y_{12} to some value other than zero. Neutralization is generally used for the same purposes as unilateralization, but provides something less than the ideal cancellation of the transistor feedback parameter which unilateralization achieves. A typical example of neutralization might be a feedback network which provides a composite b_{12} of zero while having only a negligible effect on the transistor g_{12}.

The equations for a particular neutralized case would be developed in the same manner as those for the unilateralized case. Since there are an infinite number of possibilities, no specific equations will be given here.

This completes the discussion of design with the unconditionally stable transistor. The potentially unstable transistor will now be considered.

THE POTENTIALLY UNSTABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is greater than one, the transistor is potentially unstable. Certain combinations of source and load admittances will cause oscillations if no feedback is used. In designing with the potentially unstable transistor, steps must be taken to insure that the amplifier will be stable.

Stability is usually achieved by one or both of two methods:

(1) Using a feedback network which reduces the composite y_{12} to a value which insures stability.

(2) Choosing a source and load admittance combination which provides stability.

A discussion of these basic methods is given below.

USING FEEDBACK TO ACHIEVE STABILITY

Either unilateralization or neutralization may be used to achieve stability. If unilateralization is used, the transistor-feedback network combination will be unconditionally stable. This may be verified by computing the Linvill stability factor of the combination. Since $y_{12c} = 0$, the numerator in equation 1 would be zero.

With stability thus assured, the remainder of the design may then be done to satisfy other requirements placed on the amplifier. After unilateralization has converted the potentially unstable transistor to an unconditionally stable combination, all other aspects of the design are identical to the unilateralized case with the unconditionally stable transistor. Power gains and input and output admittances may be computed using equations 14 through 18.

If neutralization is used to achieve stability, the Linvill stability factor can be used to compute the potential stability of any transistor - neutralization-network combination. Since in this case $y_{12c} \neq 0$, C will have a value other than zero.

After unconditional stability of the transistor-neutralization network combination has been achieved, the design may then be completed by treating the combination as an unconditionally stable transistor, and proceeding with the case of the unconditionally stable transistor in an amplifier without feedback. Power gains, input and output admittances, and the circuit stability factor may be computed by using the composite parameters of the combination in equations 2, 3, 5, 7, and 8.

STABILITY WITHOUT FEEDBACK

A stable design with the potentially unstable transistor is possible without external feedback by proper choice of source and load admittances. This can be seen by inspection of equation 2; G_S and/or G_L can be made large enough to yield a stable circuit regardless of the degree of potential instability of the transistor.

This suggests a relatively simple way to achieve a stable design with a potentially unstable transistor. A circuit stability factor k is selected, and equation 2 is used to arrive at values of G_S and G_L which will provide the desired k. In achieving a particular circuit stability factor, the designer may choose any of the following combinations of matching or mismatching of G_S and G_L to the transistor input and output conductances, respectively:

(1) G_S matched and G_L mismatched

(2) G_L matched and G_S mismatched

(3) Both G_S and G_L mismatched

Often a decision on which combination to use will be dictated by other performance requirements or practical considerations.

Once G_S and G_L have been chosen, the remainder of the design may be completed using the relationships which apply to the amplifier without feedback. Power gain and input and output admittances may be computed using equations 3, 5, 7, and 8.

Although the above procedure may be adequate in many cases, a more systematic method of source and load admittance determination is desirable for designs which demand maximum power gain per degree of circuit stability. Stern has analyzed this problem and developed equations for computing the conductance and susceptance of both Y_S and Y_L for maximum power gain for a particular circuit stability factor.[2,4] These equations are given here:

$$G_S = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{11}}{g_{22}}} - g_{11} \tag{19}$$

$$G_L = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22} \tag{20}$$

$$B_S = \frac{(G_S + g_{11})\ Z_0}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{11} \tag{21}$$

$$B_L = \frac{(G_L + g_{22})\ Z_0}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{22} \tag{22}$$

Where,

$$Z = \frac{(B_S + b_{11})(G_L + g_{22}) + (B_L + b_{22})\,k(L+M)/2(G_L + g_{22})}{\sqrt{k\ (L + M)}} \tag{23}$$

$$L = \left|y_{12}y_{21}\right| \tag{24}$$

$$M = \mathrm{Re}(y_{12}y_{21}) \tag{25}$$

Defining D as the denominator in equation 5 yields:

$$D = \frac{Z^4}{4} + \frac{\left[k(L + M) + 2M\right] Z^2}{2} - 2NZ\sqrt{k(L + M)} + A^2 + N^2 \tag{26}$$

where,

$$A = \frac{k(L + M)}{2} - M, \tag{27}$$

$$N = \mathrm{Im}(y_{12}y_{21}), \tag{28}$$

and,

Z_0 = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + \left[k(L + M) + 2M\right] Z - 2N\sqrt{k(L + M)}. \tag{29}$$

equal to zero.

Computation of Y_S and Y_L using equations 19 through 29 is a bit tedious to be done very frequently, and this may have discouraged wide usage of the complete Stern solution. However, examination of Stern's work suggests some interesting shortcuts:

(A) COMPUTATION OF G_S AND G_L ONLY, USING EQUATIONS 19 AND 20. If a value equal to $-b_{22}$ is then chosen for B_L, the resulting Y_L will be very close to the true Y_L for maximum gain. The transistor Y_{IN} can then be computed from Y_L using equation 7, and B_S can be set equal to $-I_m(Y_{IN})$.

Computation of B_S and B_L comprise by far the more complex portion of the Stern solution. This alternate method therefore permits the designer to closely approximate the exact Stern solution for Y_S and Y_L while avoiding that portion of the computations which are the most complex and time consuming. Further, the circuit can be designed with tuning adjustments for varying B_S and B_L, thereby creating the possibility of experimentally achieving the true B_S and B_L for maximum gain as accurately as if all the Stern equations had been solved.

(B) MISMATCHING G_S TO g_{11} AND G_L TO g_{22} BY AN EQUAL RATIO YIELDS A TRUE STERN SOLUTION FOR G_S AND G_L. This can be derived from equations 19 and 20, which lead to the following result:

$$\frac{G_L}{g_{22}} = \frac{G_S}{g_{11}} \tag{30}$$

If a mismatch ratio, R, is defined as follows,

$$R = \frac{G_L}{g_{22}} = \frac{G_S}{g_{11}} \tag{31}$$

then R may be computed for any particular circuit stability factor using the equation:

$$(1 + R)^2 = k\left[\frac{\left|y_{21}y_{12}\right| + \mathrm{Re}(y_{12}y_{21})}{2\ g_{11}\ g_{22}}\right] \tag{32}$$

Equation 32 was derived from equations 2 and 31. Having thus determined R, G_S and G_L can be quickly found using equation 31.

B_S and B_L can then be determined in the manner described above in alternate method (A).

This alternate method may be advantageous if source and load admittances and power gains for several different values of k are desired. Once the R for a particular k has been determined, the R for any other k may be quickly found from the equation

$$\frac{(1 + R_1)^2}{(1 + R_2)^2} = \frac{k_1}{k_2} \tag{33}$$

where R_1 and R_2 are values of R corresponding to k_1 and k_2, respectively.

(C) COMPUTER DESIGN. The complete Stern design problem may be programmed into a computer. Power gain, circuit stability factor, Y_S and Y_L can be obtained from the computer for any value of k. MAG, G_U, and the Linvill stability factor of the transistor may also be included in the program.

After employing either the complete Stern solution or an alternate method to obtain Y_S and Y_L for the potentially unstable transistor in an amplifier without feedback, power gains and input and output admittances may be obtained using equations 3, 5, 7, and 8.

SENSITIVITY

In all but the unilateralized amplifier, Y_{IN} is a function of load admittance. Thus Y_{IN} changes with output circuit tuning, and this can be troublesome. Consequently, it is sometimes desirable to compute the extent of variation of Y_{IN} with changes in Y_L. A term, sensitivity δ, has been defined to provide a measure of this characteristic, and is equal to per cent change in Y_{IN} divided by per cent change in Y_L. The equation for sensitivity is:

$$\delta = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}}\ K\ e^{j\theta}\right|} \tag{34}$$

where,

$$K = \left|\frac{y_{21}\ y_{12}}{g_{11}\ g_{22}}\right|$$

$$\theta = \arg\ (-y_{12}y_{21})^*$$

$$K\ e^{j\theta} = K\ (\cos\theta + j\ \sin\theta)$$

A more complete discussion of sensitivity is given in reference 6.

SUMMARY

The small signal amplifier performance of a transistor is completely described by two port admittance parameters. Based on these parameters, equations for computing the stability, gain, and optimum source and load admittances for the unilateralized, neutralized, and no-feedback amplifier cases have been discussed.

The unconditionally stable transistor will not oscillate with any combination of source and load admittances, and circuits using a stable transistor may be optimized for other performance requirements without fear of oscillations.

The potentially unstable transistor requires that steps be taken to guarantee a stable design. Stability is usually achieved by unilateralization, neutralization, or selection of source and load admittances which result in a stable amplifier.

Unilateralization and neutralization reduce the composite reverse transfer admittance. They may be used to achieve stability, input - output isolation, or both.

Maximum power gain per degree of circuit stability without feedback may be achieved using Stern's equations.

The degree of input - output isolation is described by the term sensitivity, which makes it possible to compute changes in input admittance for any change in load admittance.

The theory and design equations in this report are applicable to any linear active device which may be characterized as a two-port network. Therefore, the term "transistor" used herein refers generally to all such devices, including FETs and integrated circuits.

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GLOSSARY

C	=	Linvill's stability factor
k	=	Stern's stability factor
G_s	=	Real part of the source admittance
G_L	=	Real part of the load admittance
B_s	=	Imaginary part of the source admittance
B_L	=	Imaginary part of the load admittance
g_{11}	=	Real part of y_{11}
g_{22}	=	Real part of y_{22}
G	=	Generalized power gain
Y_L	=	Complex load admittance
Y_s	=	Complex source admittance
G_T	=	Transducer gain
MAG	=	Maximum available gain
*	=	Conjugate
Y_{IN}	=	Input admittance
Y_{OUT}	=	Output admittance
G_{max}	=	Maximum gain without feedback
G_U	=	Unilateralized gain
G_{TU}	=	Unilateralized transducer gain
δ	=	Sensitivity

APPENDIX I

A. Conversions among parameter types for y, z, h, and g parameters.

h to y

$$y_{11} = \frac{1}{h_{11}} \qquad y_{12} = \frac{-h_{12}}{h_{11}} \qquad y_{21} = \frac{h_{21}}{h_{11}} \qquad y_{22} = \frac{\Delta h}{h_{11}}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

y to h

$$h_{11} = \frac{1}{y_{11}} \qquad h_{12} = \frac{-y_{12}}{y_{11}} \qquad h_{21} = \frac{y_{21}}{y_{11}} \qquad h_{22} = \frac{\Delta y}{y_{11}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

h to z

$$z_{11} = \frac{\Delta h}{h_{22}} \qquad z_{12} = \frac{h_{12}}{h_{22}} \qquad z_{21} = \frac{-h_{21}}{h_{22}} \qquad z_{22} = \frac{1}{h_{22}}$$

z to h

$$h_{11} = \frac{\Delta z}{z_{22}} \qquad h_{12} = \frac{z_{12}}{z_{22}} \qquad h_{21} = \frac{-z_{21}}{z_{22}} \qquad h_{22} = \frac{1}{z_{22}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

h to g

$$g_{11} = \frac{h_{22}}{\Delta h} \qquad g_{12} = \frac{-h_{12}}{\Delta h} \qquad g_{21} = \frac{-h_{21}}{\Delta h} \qquad g_{22} = \frac{h_{11}}{\Delta h}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

g to h

$$h_{11} = \frac{g_{22}}{\Delta g} \qquad h_{12} = \frac{-g_{12}}{\Delta g} \qquad h_{21} = \frac{-g_{21}}{\Delta g} \qquad h_{22} = \frac{g_{11}}{\Delta g}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

z to y

$$y_{11} = \frac{z_{22}}{\Delta z} \qquad y_{12} = \frac{-z_{12}}{\Delta z} \qquad y_{21} = \frac{-z_{21}}{\Delta z} \qquad y_{22} = \frac{z_{11}}{\Delta z}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

y to z

$$z_{11} = \frac{y_{22}}{\Delta y} \qquad z_{12} = \frac{-y_{12}}{\Delta y} \qquad z_{21} = \frac{-y_{21}}{\Delta y} \qquad z_{22} = \frac{y_{11}}{\Delta y}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

z to g

$$g_{11} = \frac{1}{z_{11}} \qquad g_{12} = \frac{-z_{12}}{z_{11}} \qquad g_{21} = \frac{z_{21}}{z_{11}} \qquad g_{22} = \frac{\Delta z}{z_{11}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

g to z

$$z_{11} = \frac{1}{g_{11}} \qquad z_{12} = \frac{-g_{12}}{g_{11}} \qquad z_{21} = \frac{g_{21}}{g_{11}} \qquad z_{22} = \frac{\Delta g}{g_{11}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

g to y

$$y_{11} = \frac{\Delta g}{g_{22}} \qquad y_{12} = \frac{g_{12}}{g_{22}} \qquad y_{21} = \frac{-g_{21}}{g_{22}} \qquad y_{22} = \frac{1}{g_{22}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

y to g

$$g_{11} = \frac{\Delta y}{y_{22}} \qquad g_{12} = \frac{y_{12}}{y_{22}} \qquad g_{21} = \frac{-y_{21}}{y_{22}} \qquad g_{22} = \frac{1}{y_{22}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

B. Conversions among common emitter, common base, and common collector parameters of the same type for y, and h parameters.

Common emitter y parameters in terms of common base and common collector y parameters.

$$y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b} = y_{11c}$$

$$y_{12e} = -(y_{12b} + y_{22b}) = -(y_{11c} + y_{12c})$$

$$y_{21e} = -(y_{21b} + y_{22b}) = -(y_{11c} + y_{21c})$$

$$y_{22e} = y_{22b} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common base y parameters in terms of common emitter and common collector y parameters.

$$y_{11b} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{22c}$$

$$y_{12b} = -(y_{12e} + y_{22e}) = -(y_{21c} + y_{22c})$$

$$y_{21b} = -(y_{21e} + y_{22e}) = -(y_{12c} + y_{22c})$$

$$y_{22b} = y_{22e} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common collector y parameters in terms of common emitter and common base y parameters.

$$y_{11c} = y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b}$$

$$y_{12c} = -(y_{11e} + y_{12e}) = -(y_{11b} + y_{21b})$$

$$y_{21c} = -(y_{11e} + y_{21e}) = -(y_{11b} + y_{12b})$$

$$y_{22c} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{11b}$$

Common emitter h parameters in terms of common base and common collector h parameters.

$$h_{11e} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11c}$$

$$h_{12e} = \frac{h_{11b} h_{22b} - h_{12b}(1+h_{21b})}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b} h_{22b}}{1 + h_{21b}} - h_{12b} = 1-h_{12c}$$

$$h_{21e} = \frac{-h_{21b}(1-h_{12b}) - h_{22b} h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{-h_{21b}}{1 + h_{21b}} = -(1 + h_{21c})$$

$$h_{22e} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22c}$$

Common base h parameters in terms of common emitter and common collector h parameters.

$$h_{11b} = \frac{h_{11e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{11e}}{1 + h_{21e}}$$

$$= \frac{h_{11c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-h_{11c}}{h_{21c}}$$

$$h_{12b} = \frac{h_{11e} h_{22e} - h_{12e}(1 + h_{21e})}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{11e} h_{22e}}{1 + h_{21e}} - h_{12e}$$

$$= \frac{h_{21c}(1-h_{12c}) + h_{11c} h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx (h_{12c} - 1) - \frac{h_{11c} h_{22c}}{h_{21c}}$$

$$h_{21b} = \frac{-h_{21e}(1-h_{12e}) - h_{11e} h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{-h_{21e}}{1 + h_{21e}}$$

$$= \frac{h_{12c}(1 + h_{21c}) - h_{11c} h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-(1 + h_{21c})}{h_{21c}}$$

$$h_{22b} = \frac{h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{22e}}{1 + h_{21e}}$$

$$= \frac{h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{h_{22c}}{h_{21c}}$$

Common collector h parameters in terms of common base and common emitter h parameters.

$$h_{11c} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11e}$$

$$h_{12c} = \frac{1 + h_{21b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx 1 = 1-h_{12e}$$

$$h_{21c} = \frac{h_{12b} - 1}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{-1}{1 + h_{21b}} = -(1 + h_{21e})$$

$$h_{22c} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22e}$$

Expressions for voltage gain, current gain, input impedance, and output impedance in terms of y, z, h, and g parameters.

Voltage Gain

$$A_v = \frac{z_{21} Z_L}{\Delta z + z_{11} Z_L} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-h_{21} Z_L}{h_{11} + \Delta h Z_L} = \frac{g_{21} Z_L}{g_{22} + Z_L}$$

Current Gain

$$A_i = \frac{-z_{21}}{z_{22} + Z_L} = \frac{-y_{21} Y_L}{\Delta y + y_{11} Y_L} = \frac{-h_{21} Y_L}{h_{22} + Y_L} = \frac{-g_{21}}{\Delta g + g_{11} Z_L}$$

Input Impedance

$$Z_{IN} = \frac{\Delta z + z_{11} Z_L}{z_{22} + Z_L} = \frac{y_{22} + Y_L}{\Delta y + y_{11} Y_L} = \frac{\Delta h + h_{11} Y_L}{h_{22} + Y_L} = \frac{g_{22} + Z_L}{\Delta g + g_{11} Z_L}$$

Output Impedance

$$Z_{OUT} = \frac{\Delta z + z_{22} Z_s}{z_{11} + Z_s} = \frac{y_{11} + Y_s}{\Delta y + y_{22} Y_s} = \frac{h_{11} + Z_s}{\Delta h + h_{22} Z_s} = \frac{\Delta g + g_{22} Y_s}{g_{11} + Y_s}$$

Conversion between y parameters and s (scattering) parameters:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12} y_{21}}{(1+y_{11})(1+y_{22}) - y_{12} y_{21}} \dagger$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12} y_{21}} \dagger$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12} y_{21}} \dagger$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{21} y_{12}}{(1+y_{11})(1+y_{22}) - y_{12} y_{21}} \dagger$$

$$y_{11} = \left[\frac{(1+s_{22})(1-s_{11}) + s_{12} s_{21}}{(1+s_{11})(1+s_{22}) - s_{12} s_{21}}\right] \frac{1}{Z_o}$$

$$y_{12} = \left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12} s_{21}}\right] \frac{1}{Z_o}$$

$$y_{21} = \left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12} s_{21}}\right] \frac{1}{Z_o}$$

$$y_{22} = \left[\frac{(1+s_{11})(1-s_{22}) + s_{12} s_{21}}{(1+s_{22})(1+s_{11}) - s_{12} s_{21}}\right] \frac{1}{Z_o}$$

Where Z_O = the characteristic impedance of the transmission lines used in the scattering parameter system, usually 50 ohms.

Conversion between h parameters and s parameters:

$$s_{11} = \frac{(h_{11}-1)(h_{22}+1) - h_{12} h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12} h_{21}} \dagger\dagger$$

$$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1) - h_{12} h_{21}} \dagger\dagger$$

$$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12} h_{21}} \dagger\dagger$$

$$s_{22} = \frac{(1+h_{11})(1-h_{22}) + h_{12} h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12} h_{21}} \dagger\dagger$$

$$h_{11} = \left[\frac{(1+s_{11})(1+s_{22}) - s_{12} s_{21}}{(1-s_{11})(1+s_{22}) + s_{12} s_{21}}\right] Z_o$$

$$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22}) + s_{12} s_{21}}$$

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12} s_{21}}$$

$$h_{22} = \left[\frac{(1-s_{22})(1-s_{11}) - s_{12} s_{21}}{(1-s_{11})(1+s_{22}) + s_{12} s_{21}}\right] \frac{1}{Z_o}$$

† In converting from y to s parameters, the y parameters must first be multiplied by Z_O and then substituted in the equations for conversion to s parameters.

†† In converting from h to s parameters, the h parameters must first be normalized to Z_O in the following manner and then substituted in the equations for conversion to s parameters:

Parameter	To Normalize
h_{11}	divide by Z_o
h_{12}	use as is
h_{21}	use as is
h_{22}	multiply by Z_o

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MECL II MC1000/MC1200 Series

MHTL

MC660 Series

MTTL

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MTTL II MC2100/MC2000 Series
MTTL III MC3000 Series

MDTL

MDTL MC930/MC830 Series
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MRTL

MRTL MC900/MC800 Series
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COMPLEX ARRAYS

LINEAR

Application Selector Guide
Operational Amplifiers
High-Frequency Amplifiers
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APPLICATION NOTES